Using the TPS40192EVM-001, A 12-V Input, 1.8-V Output, 10-A Synchronous Buck Converter

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1 Introduction

The TPS40192EVM-001 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.8-V output at up to 10 A from a 12-V input bus. The EVM is designed to start up from a single supply; so, no additional bias voltage is required for start-up. The module uses the TPS40192 reduced pin count, mid-voltage, synchronous buck controller.

1.1 Description

TPS40192EVM-001 is designed to use a regulated 12-V (8-V to 14-V) bus to produce a regulated 1.8-V output at up to 10 A of load current. TPS40192EVM-001 is designed to demonstrate the TPS40192 in a typical 12-V bus to low-voltage applications while providing a number of test points to evaluate the performance of the TPS40192 in a given application. The EVM can be modified to support output voltages from 0.9 V to 3.3 V by changing a single set resistor.

1.2 Applications

- Non-isolated, medium-current point of load and low-voltage bus converters
- Networking equipment
- Telecommunications equipment
- Computer peripherals
- Digital set-top box

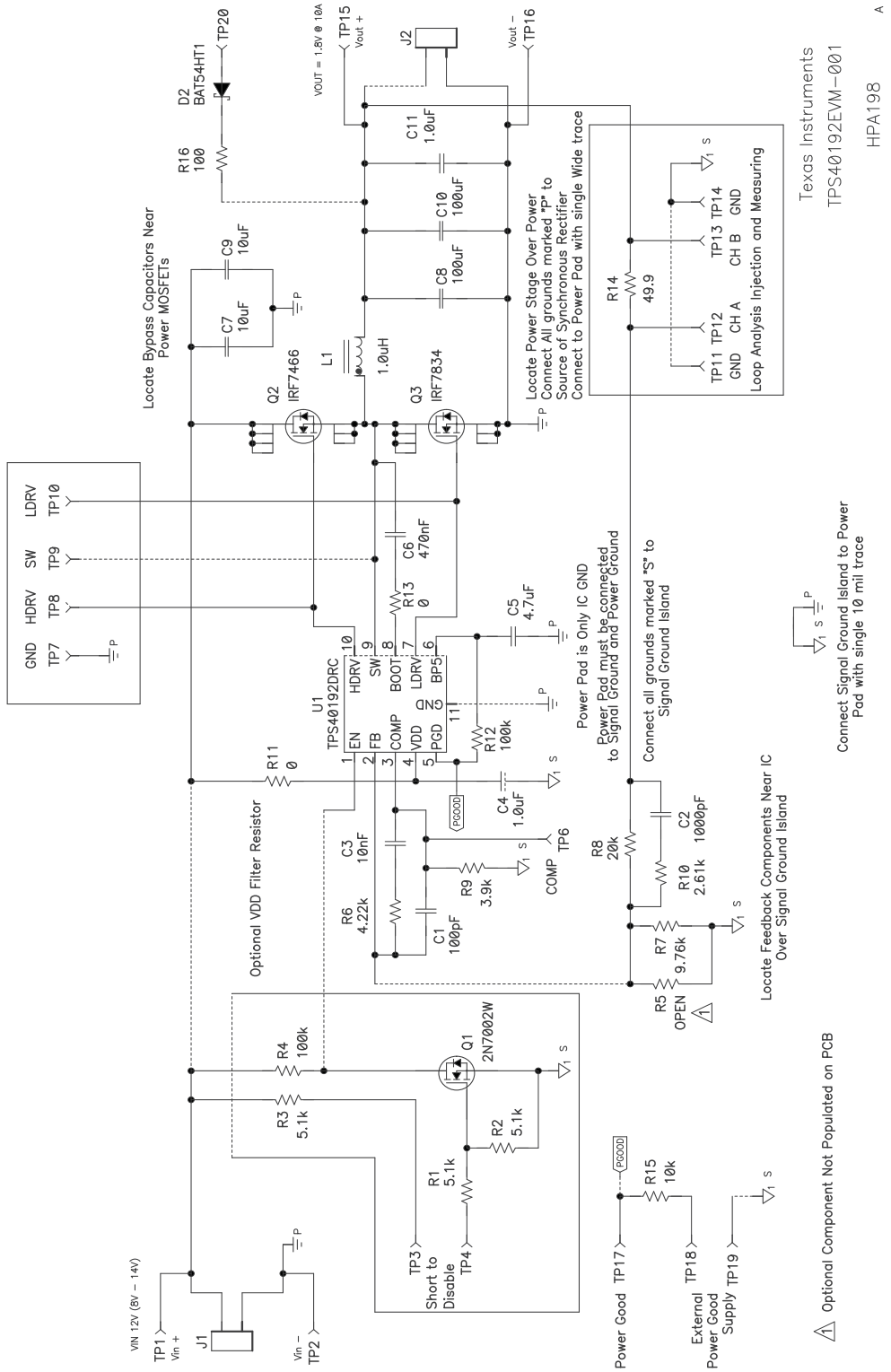
1.3 Features

- 8-V to 14-V input range
- 1.8-V fixed output, adjustable with single resistor
- 10-Adc steady-state output current
- 600-kHz switching frequency (fixed by TPS40192)
- Single SO-8 MOSFETs for both main switch and synchronous rectifier.
- Double-sided, two active layer PCB with all components on top side (test-point signals routed on internal layers)
- Active converter area of less than 1 square inch, 1.20-inch $\times$ 0.85-inch
- Convenient test points for probing switching waveforms and noninvasive loop-response testing

2 TPS40192EVM-001 Electrical Performance Specifications

Parameter		Notes and Conditions	Min	Nom	Max	Units
Input Characteristics						
VIN	Input voltage		8	12	14	V
IIN	Input current	VIN = Min, IOUT = Max		2.7	2.85	A
	No load input current	VIN = Min, IOUT = 0A		48	60	mA
VIN_UVLO	Input UVLO	IOUT = Min to Max	3.9	4.2	4.4	V
VIN_OV	Input OV	IOUT = Min to Max		NA		V
Output Characteristics						
VOUT	Output voltage	VIN = Nom, IOUT = NOM	1.86	1.8	1.84	V
	Line regulation	VIN = Min to Max, IOUT = Nom			0.5%	
	Load regulation	VIN = Nom, IOUT = Min to Max			0.5%	
VOUT_ripple	Output voltage ripple	VIN = Nom, IOUT = Max			40	mVpp
IOUT	Output current	VIN = Min to Max	0	6	10	A
IOCP	Output overcurrent inception point	VIN = Nom, VOUT = VOUT-5%		19		A
VOVP	Output OVP	IOUT = Min to Max		NA		V
Transient Response						
ΔI	Load step	0.75 x IOUT_Max to 0.25 × IOUT _Max		5		A
	Load slew rate			5		A/µsec
	Overshoot				50	mV
	Settling time					msec
Systems Characteristics						
FSW	Switching frequency		480	600	720	kHz
ηpk	Peak efficiency	VIN=Nom, IOUT = Min to Max		86%		
η	Full-load efficiency	VIN=Nom, IOUT = Max		82%		
T_{op}	Operating temperature range	VIN = Min to Max, IOUT = Min to Max	-40	25	60	°C
Mechanical Characteristics						
W	Dimensions (active area) width			1.2		ins
L	Length			0.85		ins

3 Schematic



NOTE: For reference only; see Table 4: Bill of Materials for specific values

3.1 Adjusting Output Voltage (R5)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R7). The output voltage is given by the formula

$$V_{VOUT} = V_{VREF} \times \frac{R8 + R7}{R7} \quad (1)$$

Where V_{VREF} = 0.591 V and R8 = 20 kΩ

Table 1 contains common values for R7 to generate popular output voltages. TPS40192EVM-001 is stable through these output voltages but the efficiency may suffer as the power stage is optimized for the 1.8-V output.

Table 1. Adjusting V_{OUT} with R7

V_{OUT} (V)	R7 (kΩ)
3.3	4.32
2.5	6.19
2.25	7.15
2	8.25
1.8	9.76
1.5	13
1.25	19.1
1	28.7
0.9	38.3

The values in Table 1 provide less than 1% nominal set-point error in the output voltage. If a tighter nominal value is required, R5 can be used in parallel with R7 to obtain a wider range of resistor values using commonly available E96 resistors.

3.2 Adjusting Short-Circuit Protection (R9)

The TPS40192 uses a selectable current limit for short-circuit protection. The current limit is selected from three levels by placing a resistor at R9. The TPS40192 compares the voltage drop across the high-side FET (VDD to SW) to an internal reference voltage selected during start-up. The voltage levels are shown in Table 2.

Table 2. Adjusting V_{SCP} With R9

$V_{SCP(min)}$ (V)	R9 (kΩ)
88	3.9
160	Open
228	12

The current before declaring short-circuit protection can be determined by dividing the V_{SCP} by the $R_{DS(ON)}$ of the high-side FET (Q2).

3.3 Test Point Descriptions

Test Point	Label	Use	Section
TP1	Vin+	Monitor input voltage to the module	3.3.1
TP2	Vin–	Monitor input voltage to the module	3.3.1
TP3	Disable	Vin connection for disable circuit	3.3.2
TP4	Disable	Gate connection for disable circuit	3.3.2
TP5	Not Used	Not present on PCB	NA

Test Point	Label	Use	Section
TP6	COMP	Monitor COMP voltage and monitor power stage frequency response	3.3.3 and 3.3.5
TP7	GND	Ground for SW, LDRV, and HDRV measurements	3.3.4
TP8	HDRV	Monitor high-side gate drive (Q2)	3.3.4
TP9	SW	Monitor switch-node waveforms	3.3.4
TP10	LDRV	Monitor low-side gate drive (Q3)	3.3.4
TP11	GND	Ground for loop-monitoring probe	3.3.5
TP12	CH1	Loop injection point and injection monitoring point	3.3.5
TP13	CH2	Loop injection point and output response monitoring point	3.3.5
TP14	GND	Ground for loop-monitoring probe	3.3.5
TP15	Vout+	Monitor output voltage from the module	3.3.6
TP16	Vout–	Monitor output voltage from the module	3.3.6
TP17	Power Good	Power-good output voltage	3.3.7
TP18	Ext Source	External source for power-good circuit	3.3.7
TP19	GND	Ground for external source for power good	3.3.7
TP20	Prebias	Injection point to test prebias load compliance	3.3.8

3.3.1 Input Voltage Monitoring (TP1 and TP2)

TPS40192EVM-001 provides two test points for measuring the voltage applied to the module. This allows the user to measure the actual module voltage without losses from input cables and connector losses. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive terminal to TP1 and the negative terminal to TP2.

3.3.2 Disable (TP3 and TP4)

TPS40192EVM-001 defaults to the Enabled state. Short TP4 to TP3 to disable the TPS40192 controller. TP4 also can be used as a Disable input driven by a 5-V logic input from an external circuit. The Enable test point uses two 5.1-kΩ pulldown resistors in series so that TPS40192 turns on if the Enable test point is left floating.

3.3.3 Compensation and Initialization (TP6)

TPS40192EVM-001 provides a test-point connection to the COMP pin of the TPS40192 controller. This test point can be used to monitor the COMP voltage during the controller's power-on initialization that sets the controller's short-circuit protection (SCP) threshold. The test point also can be used to monitor the PWM comparator input voltage (COMP) during operation or to measure the power-stage gain by following the loop-analysis procedure in section 4.5 .

3.3.4 Switching Waveforms (TP7, TP8, TP9, and TP10)

TPS40192EVM-001 provides three test points and a local ground connection (TP7) for the monitoring of the main switching waveforms. Connect an oscilloscope probe to TP8 to monitor the high-side gate drive applied to the gate of Q2. Connect an oscilloscope probe to TP9 to monitor the switch-node voltage. The gate-to-source voltage (VGS) of the high-side FET can be determined by a math function TP8–TP9 if both channels use the same scale. Connect an oscilloscope probe to TP9 to monitor the low-side gate drive applied to the gate of Q3. Because the source of Q3 is connected directly to ground, no math function is required to determine the gate-to-source voltage of the low-side FET.

3.3.5 Loop Analysis (TP11, TP12, TP13, and TP14)

TPS40192EVM-001 contains a 49.9-Ω series resistor in the feedback loop to allow for matched impedance signal injection into the feedback for loop-response analysis. An isolation transformer should be used to apply a small (30-mV or less) signal across R14 through TP12 and TP13. By monitoring the AC injection level at TP13 and the returned AC level at TP14, the power-supply loop response can be determined.

By moving channel A from TP12 to TP6 (COMP), the control-to-output response of the power stage (also referred to as the power-stage transfer function) can be directly measured. See Section 3.9 for a detailed procedure of loop-response measurements.

3.3.6 Output Voltage Monitoring (TP15 and TP16)

TPS40192EVM-001 provides two test points for measuring the voltage generated by the module. This allows the user to measure the actual module output voltage without losses from output cables and connector losses. All output voltage measurements should be made between TP15 and TP16. To use TP1 and TP2, connect a voltmeter positive terminal to TP15 and negative terminal to TP16. For output ripple measurements, TP15 and TP16 allow a user to limit the ground loop area by using the tip and barrel measurement technique shown in Figure 2. All output ripple measurements should be made using this technique.

3.3.7 Power Good (TP17, TP18, and TP19)

TPS40192EVM-001 has three test points to allow the user to evaluate the TPS40192 power-good function. TP18 provides access to the power-good output of the TPS40192. It has a 100-kΩ pullup to the TPS40192 5-V regulator and can be used as a logic signal with no additional requirements. TP17 provides a connection for an external power-good source for 3.3-V logic. TP17 is connected to the power-good circuit through a 10-kΩ pullup resistor. TP19 provides a local ground access to connect a remote disable circuit.

3.3.8 Prebias Input (TP20)

TPS40192EVM-001 contains a prebias injection circuit with a 100-Ω resistor and series diode to allow testing and evaluation of the TPS40192's prebias support compatibility. Apply a voltage less than the target output voltage to TP20. Monitoring the output voltage during start-up demonstrates the ability of the TPS40192 to power up without drawing current from a prebiased output. D2 prevents the output voltage from back-driving the prebias source.

4 Test Setup

4.1 Equipment

4.1.1 Voltage Source

The input voltage source (V_{IN}) should be a 0- to 15-V variable DC source capable of 5 Adc. Connect V_{IN} to J1 as shown in Figure 1.

4.1.2 Meters

A1: 0- to 5-Adc ammeter
V1: V_{IN}, 0- to 15-V voltmeter
V2: V_{OUT}, 0- to 5-V voltmeter

4.1.3 Loads

The output load (LOAD1) should be an electronic constant-current mode load capable of 0 to 10 Adc at 1.8 V.

4.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the ripple voltage on V_{OUT}. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, AC coupling, 1-µs/division horizontal resolution, 10-mV/division vertical resolution for taking output ripple measurements. TP15 and TP16 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP15 and holding the ground barrel to TP16 as shown in Figure 2. For a hands-free approach, the loop in TP16 can be cut and opened to cradle the probe barrel. Using a leaded ground connection may induce additional noise due to the large ground loop area.

4.1.5 Recommended Wire Gauge (V_{IN} to J1)

The connection between the source voltage, VIN and J1 of HPA198 can carry as much as 5 Adc. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet (2 feet input, 2 feet return). J2 to LOAD1 (power)

The power connection between J2 of HPA198 and LOAD1 can carry as much as 10 Adc. The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 2 feet (1 feet output, 1 feet return).

4.1.6 Other

This evaluation module includes components that can become hot to the touch; because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended if powered. The EVM should not be probed if the fan is not running.

4.2 Equipment Setup

Shown in Figure 1 is the basic test setup recommended to evaluate the TPS40192EVM-001. Note that although the return for J1 and J2 are the same, the connections should remain separate as shown in Figure 1.

4.2.1 Procedure

1. When working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses also should be worn.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from VIN to 5 A maximum. Ensure that V_{IN} is initially set to 0 V and connected as shown in Figure 1.
3. Connect the ammeter A1 (0- to 5-A range) between V_{IN} and J1 as shown in Figure 1.
4. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 1.
5. Connect LOAD1 to J2 as shown in Figure 1. Set LOAD1 to constant-current mode to sink 0 Adc before V_{IN} is applied.
6. Connect voltmeter, V2 across TP15 and TP16 as shown in Figure 1.
7. Place fan as shown in Figure 1 and turn on, ensuring that air is flowing across the EVM.

4.2.2 Diagrams

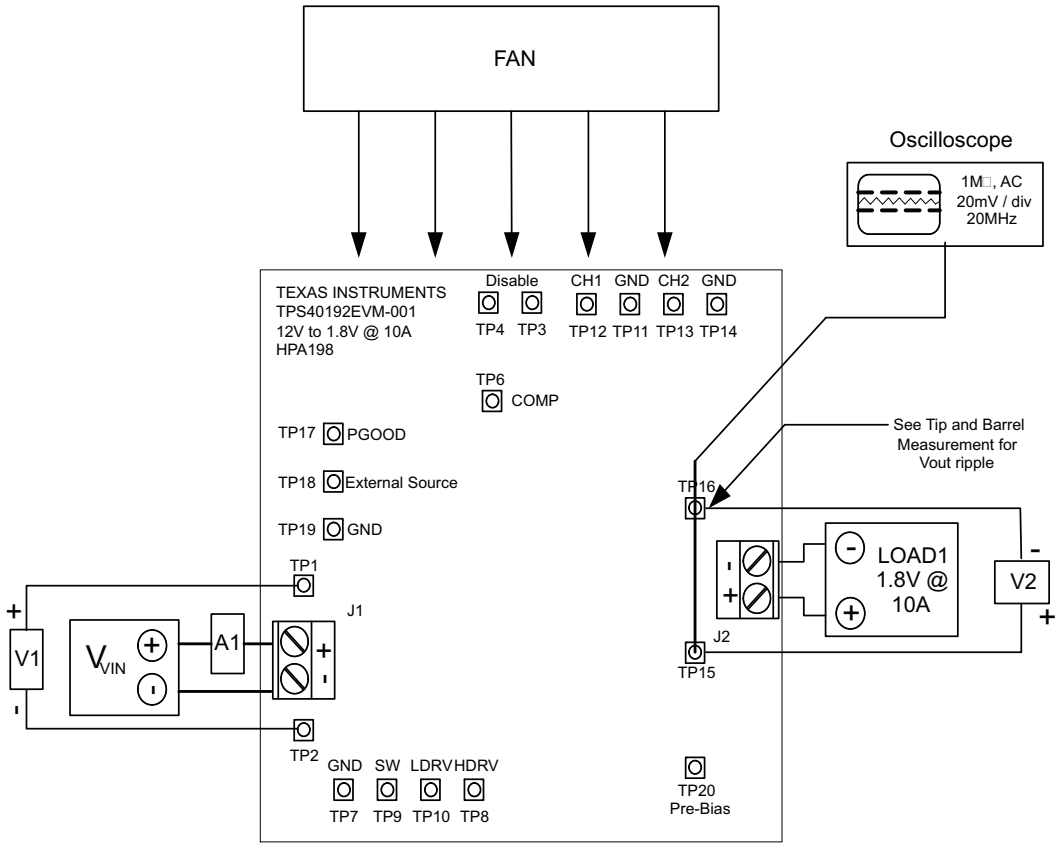


Figure 1. TPS40192EVM-001 Recommended Test Setup

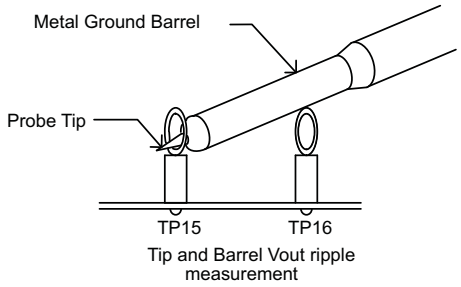


Figure 2. Output Ripple Measurement – Tip and Barrel Using TP9 and TP10

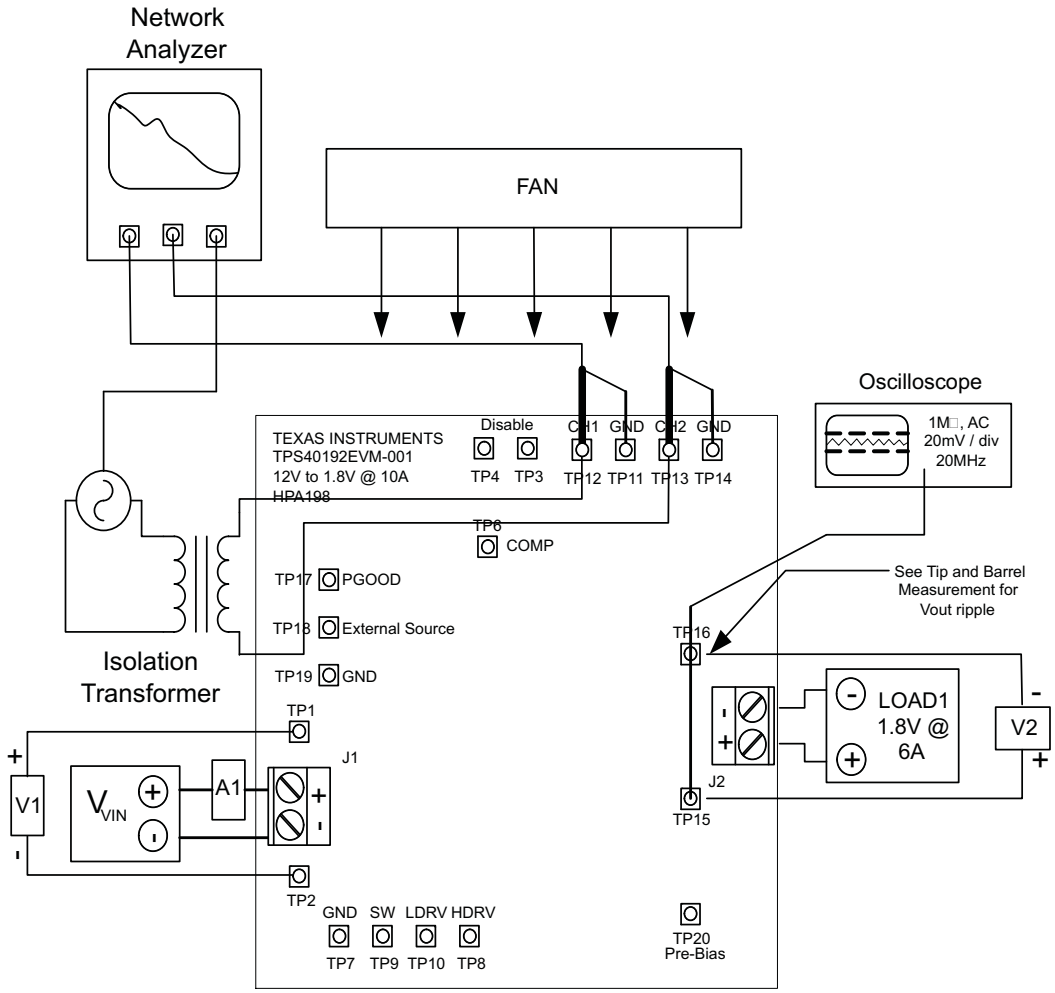


Figure 3. Control Loop Measurement Setup

4.3 Start-Up/Shutdown Procedure

1. Increase V_{IN} from 0 V to 12 Vdc.
2. Vary LOAD1 from 0 to10 Adc.
3. Vary V_{IN} from 8 Vdc to 14 Vdc.
4. Decrease LOAD1 to 0 A.
5. Decrease V_{IN} to 0 Vdc.

4.4 Output Ripple Voltage Measurement Procedure

1. Increase V_{IN} from 0 V to 12 Vdc.
2. Adjust LOAD1 to desired load between 0 Adc and 10 Adc.
3. Adjust VIN to desired load between 8 Vdc and 14 Vdc
4. Connect oscilloscope probe to TP15 and TP16 as shown in Figure 2.
5. Measure output ripple.
6. Decrease LOAD1 to 0 A.
7. Decrease V_{IN} to 0 Vdc.

4.5 Control Loop Gain and Phase Measurement Procedure

1. Connect a 1-kHz to 1-MHz isolation transformer to TP12 and TP13 as shown in Figure 3.
2. Connect the input signal amplitude measurement probe (channel A) to TP12 as shown in Figure 3.
3. Connect the output signal amplitude measurement probe (channel B) to TP13 as shown in Figure 3.
4. Connect the ground lead of channel A and channel B to TP11 and TP14 as shown in Figure 3.
5. Inject a 30-mV or less signal across R14 through the isolation transformer.
6. Sweep the frequency from 1 kHz to 1 MHz with a 10-Hz or lower post filter
7. The control loop gain can be measured by $20 \times \mathrm{LOG}\left(\frac{\mathrm{ChannelB}}{\mathrm{ChannelA}}\right)$
8. The control loop phase is measured by the phase difference between channel A and channel B.
9. The control-to-output response (power stage transfer function) can be measured by connecting the channel A probe to TP6 (COMP) and the channel B probe to TP13.
10. The output-to-control response (error amplifier transfer function) can be measured by connecting the channel B probe to TP6 (COMP) and the channel A probe to TP12.
11. Disconnect the isolation transformer from TP12 and TP13 before making other measurements. (The signal injection into feedback may interfere with the accuracy of other measurements.)

4.6 Equipment Shutdown

1. Shut down the oscilloscope.
2. Shut down LOAD1.
3. Shut down V_{IN}.
4. Shut down the fan.

5 TPS40192EVM Typical Performance Data and Characteristic Curves

5.1 Efficiency

Figure 4 through Figure 8 present typical performance curves for the TPS40192EVM-001. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference only and may differ from actual field measurements.

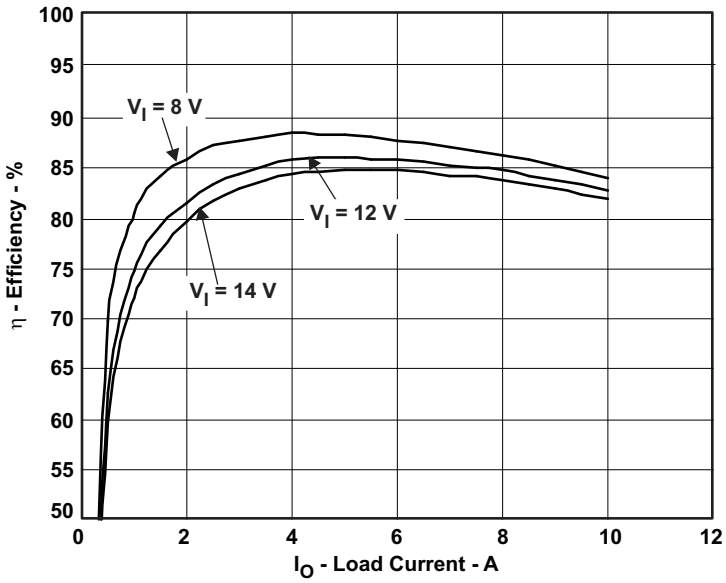


Figure 4. TPS40192EVM-001 Efficiency vs Load Current, Vin = 8 V - 14 V, Vout = 1.8 V, Iout = 0 A - 10 A

5.2 Line and Load Regulation

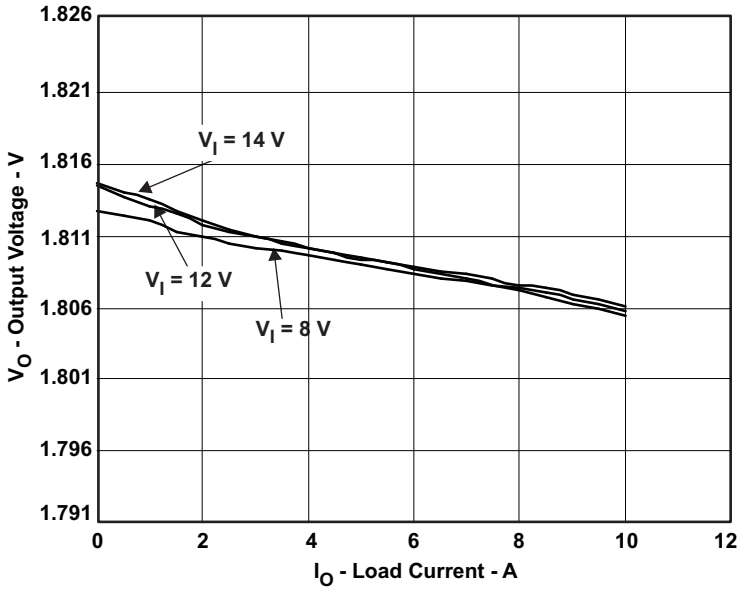


Figure 5. TPS40192EVM-001 Output Voltage vs Load Current, Vin = 8 V - 14 V, Vout = 1.8 V, Iout = 0 A - 10 A

5.3 Output Voltage Ripple

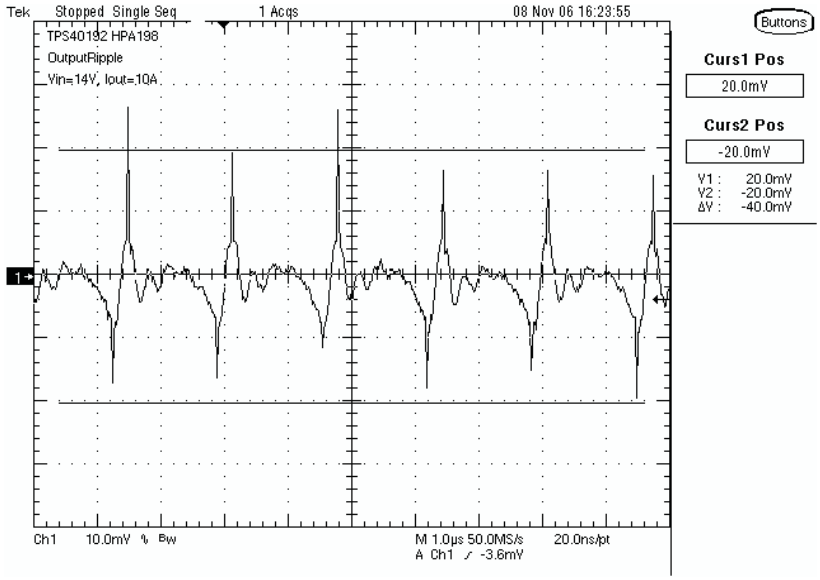


Figure 6. TPS40192EVM-001 Output Voltage Ripple, Vin = 14 V, Vout = 1.8 V, Iout = 10 A

5.4 Switch Node

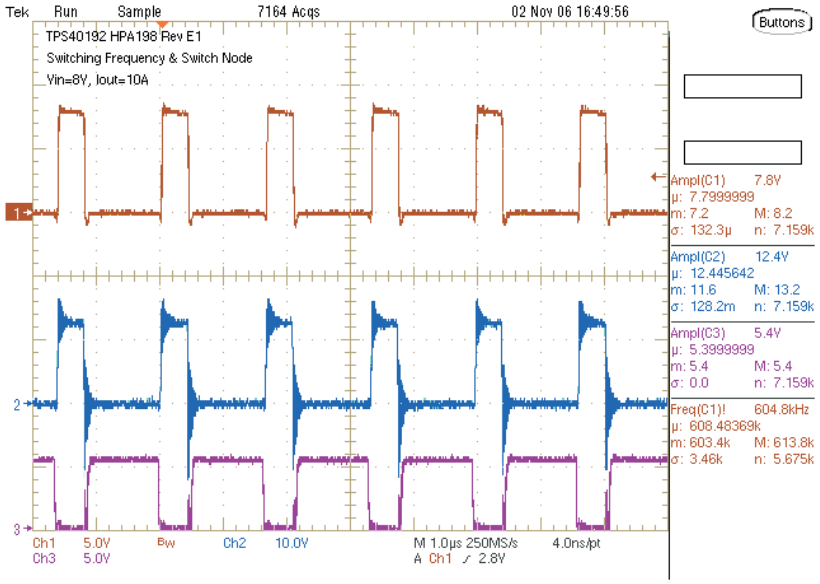


Figure 7. TPS40192EVM-001 Switching Waveforms, CH1: SW(TP), CH2: HDRV(TP), CH3: LDRV(TP); Vin = 8 V, Vout = 1.8 V, Iout = 10 A

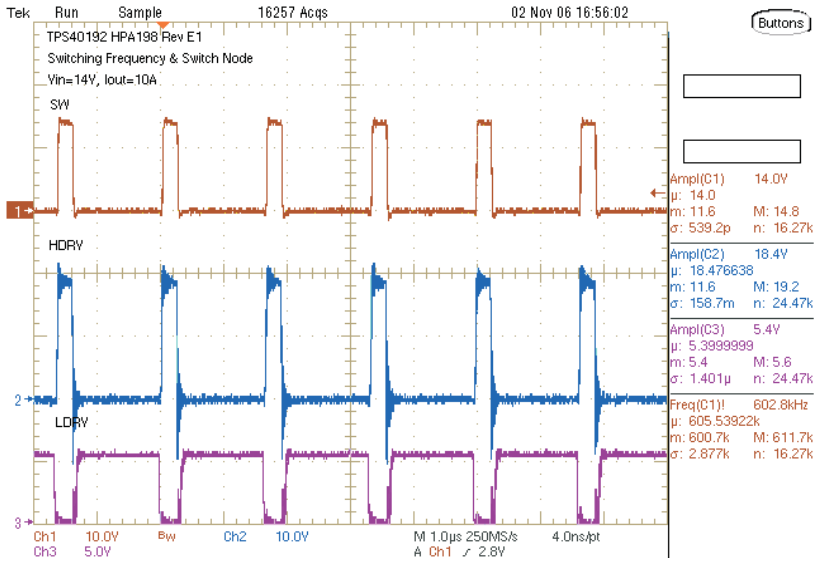


Figure 8. TPS40192EVM-001 Switching Waveforms, CH1: SW(TP), CH2: HDRV(TP), CH3: LDRV(TP); Vin = 14 V, Vout = 1.8 V, Iout = 10 A

6 EVM Assembly Drawings and Layout

The following figures (Figure 9 through Figure 14) show the design of the TPS40192EVM-001 printed-circuit board. The EVM has been designed using a 4-layer, 2-oz copper-clad circuit board 2.5-in. × 2.5-in. with all components in a 1.25-in. × 0.8-in. active area on the top side and all active traces to the top and bottom layers to allow the user to easily view, probe, and evaluate the TPS40192 control IC in a practical double-sided application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

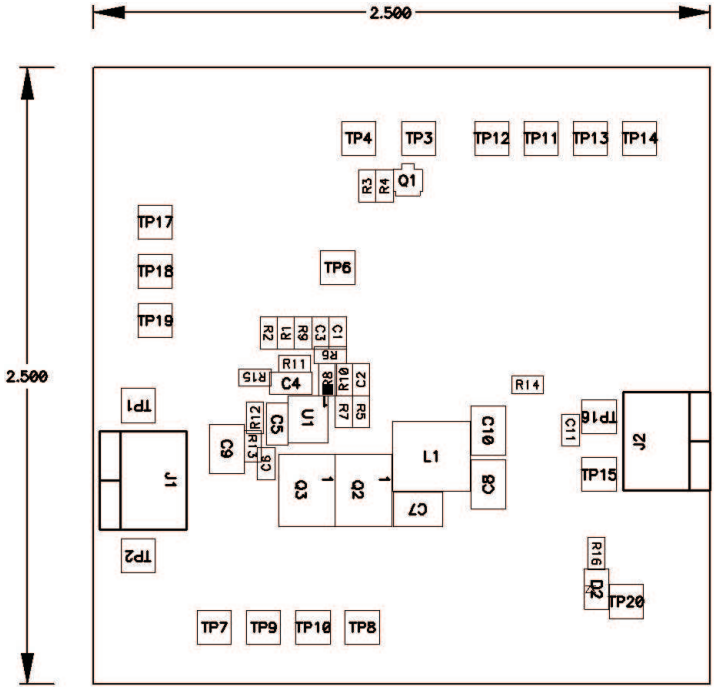


Figure 9. TPS40192EVM-001 Component Placement (Viewed From Top)

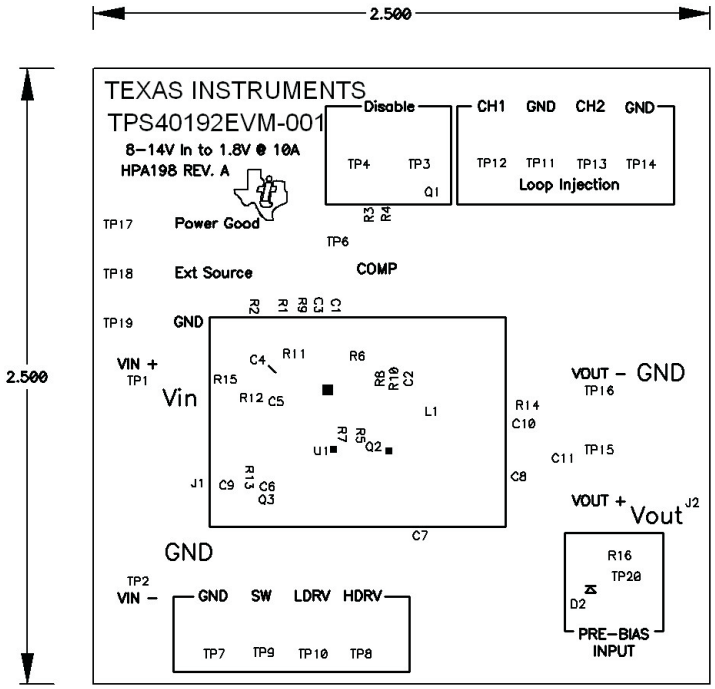


Figure 10. TPS40192EVM-001 Silkscreen (Viewed From Top)

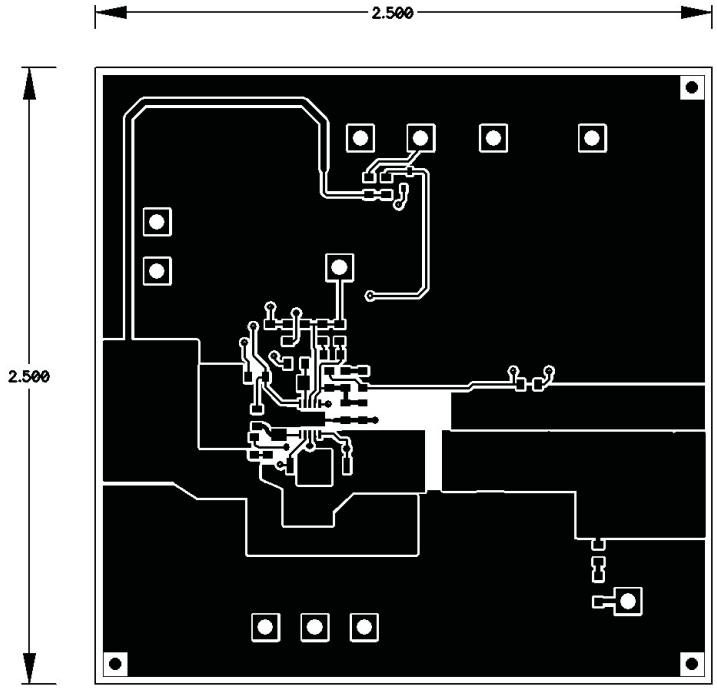


Figure 11. TPS40192EVM-001 Top Copper (Viewed From Top)

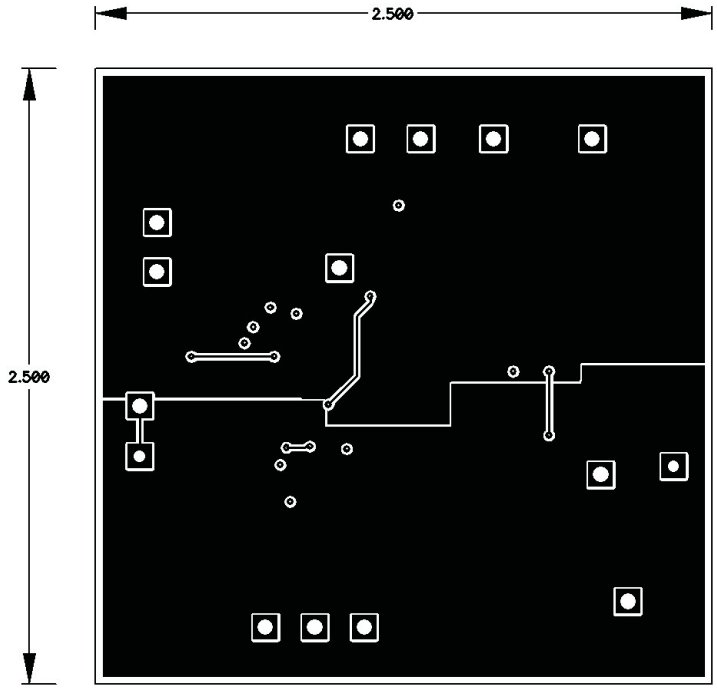


Figure 12. TPS40192EVM-001 Bottom Copper (X-Ray View From Top)

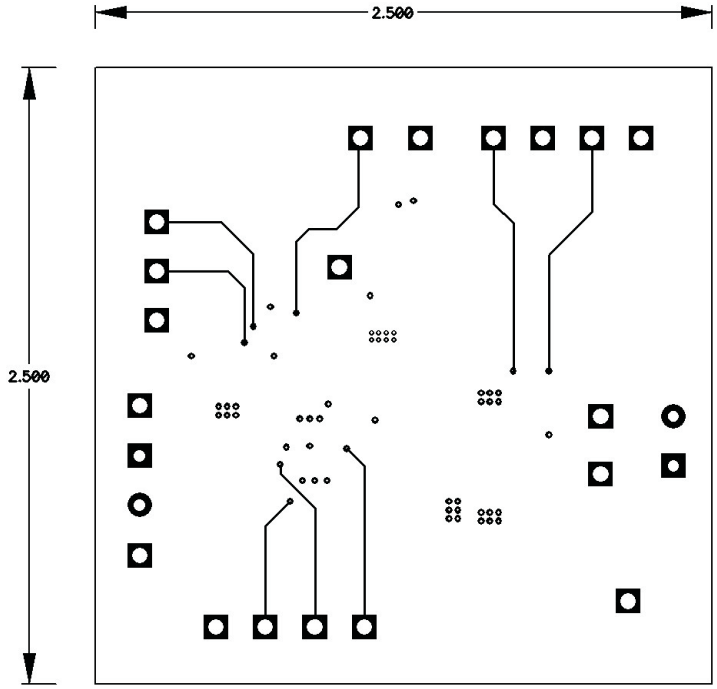


Figure 13. TPS40192EVM-001 Internal 1 (X-Ray View From Top)

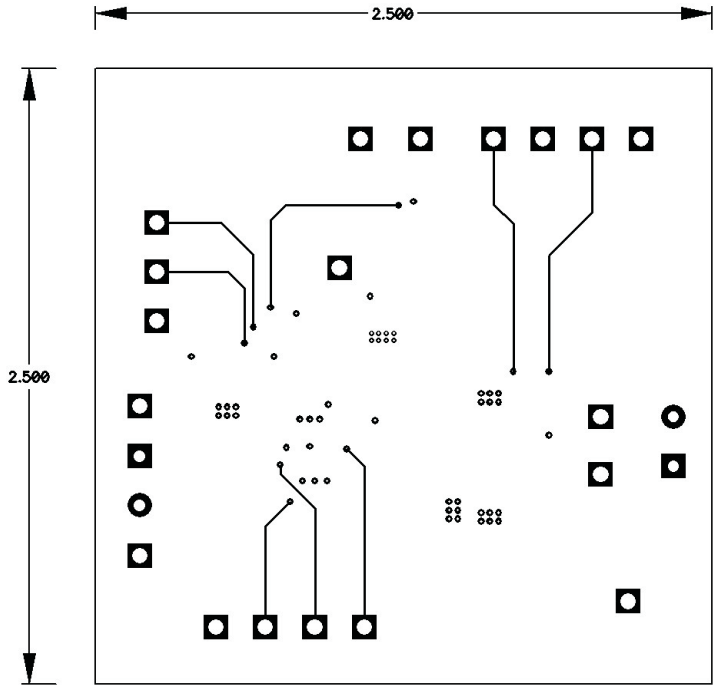


Figure 14. TPS40192EVM-001 Internal 2 (X-Ray View From Top)

7 List of Materials

Figure 14 lists the EVM components as configured according to the schematic shown in Section 3.

Table 3. TPS40192EVM-001 Bill of Materials

QTY	RefDes	Value	Description	Size	Part Number	MFR
1	C1	100pF	Capacitor, Ceramic, 10V, C0G, 10%	0603	STD	STD
1	C2	1000pF	Capacitor, Ceramic, 10V, C0G, 10%	0603	STD	STD
1	C3	10nF	Capacitor, Ceramic, 10V, C0G, 10%	0603	STD	STD
1	C4	1.0µF	Capacitor, Ceramic, 25V, X5R, 20%	0805	STD	STD
1	C5	4.7µF	Capacitor, Ceramic, 10V, X5R, 20%	0805	STD	STD
1	C6	470nF	Capacitor, Ceramic, 10V, X5R, 20%	0603	STD	STD
2	C7, C9	10µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	C3225X7R1E106M	TDK
2	C8, C10	100µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	C3225X5R0J107M	TDK
1	C11	1.0µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	STD	STD
1	D2		Diode, Schottky, 200-mA, 30-V	SOD323	BAT54HT1	On Semi
2	J1, J2		Terminal Block, 2-pin, 15-A, 5,1mm	0.40 × 0.35 in	ED1609	OST
1	L1	1.0µH	Inductor, SMT, 12A, 6.6 mΩ	0.268 × 0.268 in	PG0083.102	Pulse
1	Q1		MOSFET, N-Ch, VDS 60v, RDS 2 Ω, ID 115 mA	SOT-323 (SC-70)	2N7002W-7	Diodes Inc
1	Q2*		Transistor, MOSFET, N-Chan, 30V, Rds 17 mΩ, 9A	SO8	IRF7466	IR
1	Q3*		Transistor, MOSFET, N-Chan, 30V, Rds 5.5 mΩ, 9A	SO8	IRF7834	IR
3	R1, R2, R3	5.1k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R4	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R5	OPEN	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	4.22k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	9.76k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	20k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	3.9k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R10	2.61k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R11, R13	0	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R12	100k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R14	49.9	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R15	10k	Resistor, Chip, 1/16W, 5%	0603	Std	Std
1	R16		100 Resistor, Chip, 1/16W, 5%	0603	Std	Std
5	TP1, TP3, TP15, TP18, TP20		5010 Test Point, Red, Thru Hole	0.125 × 0.125 in	5010	Keystone
6	TP2, TP7, TP11, TP14, TP16, TP19		5011 Test Point, Black, Thru Hole	0.125× 0.125 in	5011	Keystone
8	TP4, TP6, TP8, TP9, TP10, TP12, TP13, TP17		5012 Test Point, White, Thru Hole	0.125 × 0.125 in	5012	Keystone
1	U1*		IC, Cost Optimized Mid Vin High Freq. Sync. Buck controller	DRC10	TPS40192DRC	TI

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 0.6 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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