Texas Instruments

TPS40007-Based Converter Delivers 10-A Output

User's Guide

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TPS40007-Based Converter Delivers 10-A Output

Mark Dennis *DC to DC Controller Products*

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1 Introduction

The TPS40007 is a voltage-mode, synchronous buck PWM controller that uses TI's proprietary Predictive Gate Drive™ technology to wring maximum efficiency from step-down converters. This controller provides a bootstrap circuit to allow the use of an N-channel MOSFET as the topside buck switch to reduce conduction losses and increase silicon device utilization. Predictive Gate Drive™ technology controls the delay from main switch turn-off to synchronous rectifier turn-on and also the delay from rectifier turn-off to main switch turn-on. This allows minimization of the losses in the MOSFET body diodes, both conduction and reverse recovery. This design note provides details on a buck converter that converts an input of 3 V to 5 V down to a 2.5-V output level using the TPS40007 controller.

A schematic for the board is shown in Figure 1. The list of material is provided in section 7 of this User's Guide.

2 Features

The specification for this board is as follows:

- V_{IN} = 3.3 V to 5 V
- V_{OUT} = 2.5 V +/−3%
- I_{OUT} = 0 A to 10 A
- Efficiency = > 95% with V_{IN} = 3.3 V, I_{LOAD} = 4 A
- Output voltage ripple < 2% V_{OUT}
- Power semiconductor devices: Each MOSFET is a single SO-8 package

3 Schematic

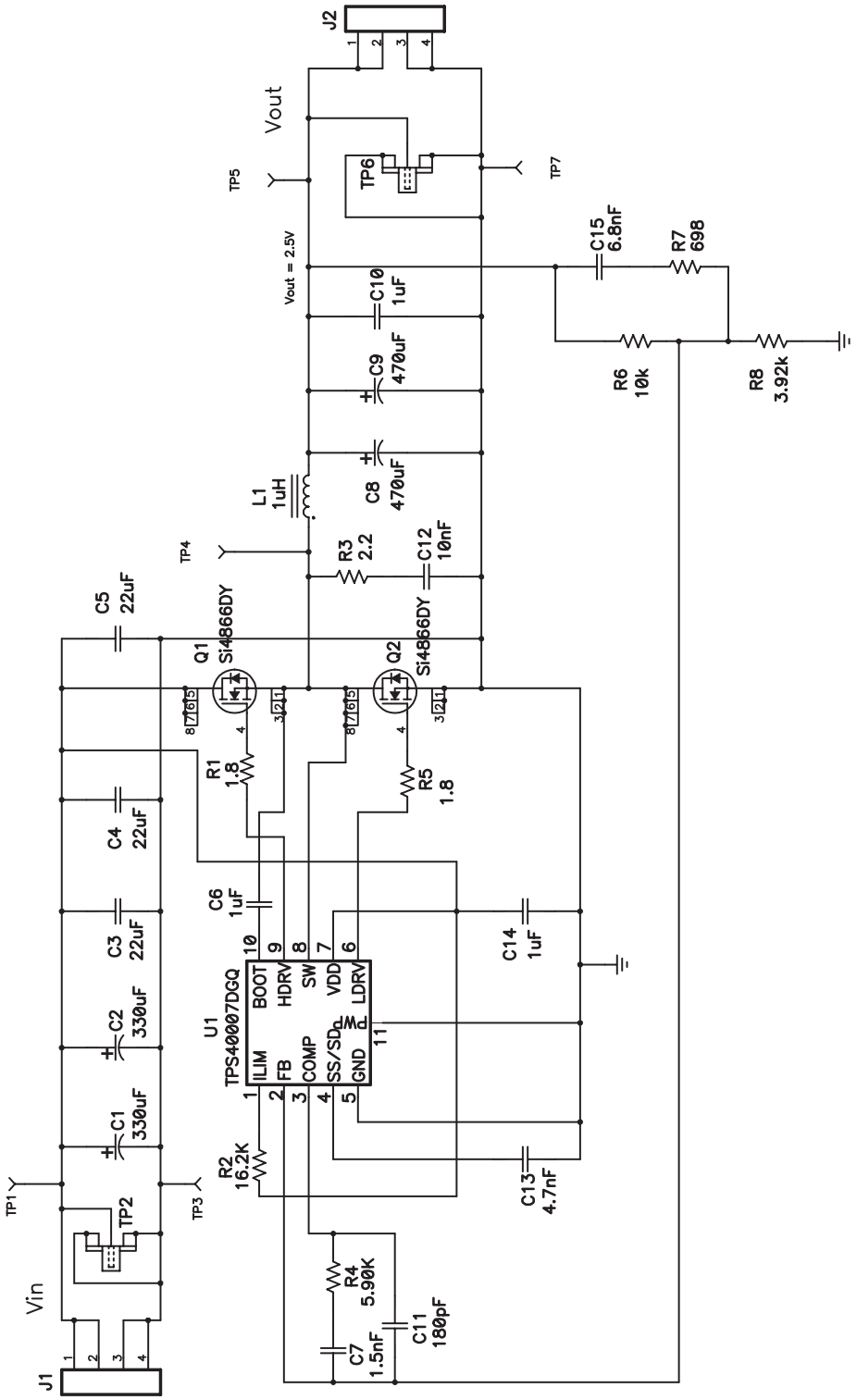


Figure 1. Application Diagram for the TPS40007EVM−001

4 Design Procedure

4.1 Controller Selection

The TPS40007 synchronous buck controller is selected for this high-current application because the 300-kHz switching frequency enables higher efficiency. The TPS40009 is available for applications needing 600-kHz operation for reducing component size. However, at higher frequency the efficiency is generally reduced, leading to more on-board power dissipation.

4.2 Inductance Value

The output inductor value is selected to set the ripple current to a value most suited to overall circuit functionality. An inductor selection that is too small leads to larger ripple current that increases RMS current losses in the inductor and MOSFETs, and also leads to more ripple voltage on the output. The inductor value is calculated by equation (1),

$$L_{MIN} = \frac{V_{OUT}}{f \times I_{RIPPLE}} \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) = \frac{2.5\ V}{300\ kHz \times 4\ A} \times \left(1 - \frac{2.5\ V}{5\ V}\right) = 1.0\ \mu H \quad (1)$$

in which I_{RIPPLE} is chosen to be 40% of I_{OUT}, or 4 A at max V_{IN}. This high value of ripple current is selected to keep the inductor small to minimize the $R_{DS(on)}$ losses due to the high output current. A synchronous rectifier controller that maintains continuous inductor current down to no load eliminates concerns arising from crossing the DCM boundary. A standard value of 1 μH with a resistance of 3.5 mΩ is selected. At full load the power loss is only 0.35 W, which is only 1.4% of the 25-W output power.

4.3 Input Capacitor Selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this standalone supply, onboard capacitance is added to handle input voltage ripple and RMS current considerations. For this power level, input voltage ripple of 150 mV is reasonable, and a conservative minimum value of capacitance is calculated as

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{10\ A \times 2.5\ \mu s}{0.15\ V} = 167\ \mu F \quad (2)$$

In addition to this minimum capacitance requirement, the RMS current stresses must be considered. In this converter, the large duty cycle causes the input RMS current to be nearly as large as the output current. This simplified formula calculates the RMS current for a trapazoidal current waveform, shown in equation (3).

$$I_{RMS} = I \times \sqrt{D} = I \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}}} = 10\ A \times \sqrt{\frac{2.5\ V}{3.0\ V}} = 9.1\ A \quad (3)$$

Additional terms for the ripple component of the current add only a small amount to the total RMS current, and can be neglected. To meet this initial requirement with small size and cost, a combination of capacitors is considered. To carry the high frequency ripple current, three 22-μF, X5R ceramic capacitors are placed close to the power circuitry. Although these capacitors have an extremely small resistance, the datasheet indicates that the part undergoes a 30°C temperature rise with 2 A_{RMS} current at 500 kHz, so more current capability is needed. Two 330-μF POSCAPs with an RMS current capability of 4.4 A each is selected. In typical embedded converters, these POSCAPs is not required if the upstream converter feeding this buck has sufficient current handling capability.

4.4 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. First, the minimum allowable output capacitance should be determined by the amount of inductor ripple current and one-half the allowable output ripple, as given in equation (4).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} = \frac{4\ A}{8 \times 300\ kHz \times 25\ mV} = 67\ \mu F \quad (4)$$

This only affects the capacitive component of the ripple voltage. In addition, the voltage component due to the capacitor ESR must be considered, shown in equation (5).

$$ESR_{Cout} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{25\ mV}{4\ A} = 6.25\ m\Omega \quad (5)$$

To minimize capacitor size while maintaining good transient response, two 470-μF POSCAPs (with an ESR of 10 mΩ each) are fitted in paralleled with a 1-μF ceramic capacitor.

4.5 MOSFET Selection

One constraint of this design is the use of one SO-8 MOSFET in the upper switch device and one SO-8 in the lower synchronous rectifier location in the buck converter power stage. The upper device loss is usually dominated by switching loss, so a device with lower gate charge and switching times was selected. Since this application has a relatively high output voltage, the upper device runs at a high duty cycle and needs to have a low $R_{DS(on)}$ to keep conduction losses low, and an 8-mΩ device with a maximum gate charge of 30 nC is selected. The same device is fitted in the bottom switch location to achieve high efficiency.

4.6 Short Circuit Protection

The TPS40003 implements short circuit protection by comparing the voltage across the topside MOSFET while it is on to a voltage dropped from VDD by R_{LIM} due to an internal current source of 15 μA inside pin 1. Due to tolerances in the current source and variations in the power MOSFET on-voltage versus temperature, the short circuit level can protect against gross overcurrent conditions only, and should be set much higher than rated load. In this particular case, R_{LIM} is selected as shown in equation (6).

$$R_{LIM} = R2 = \frac{3 \times I_{OUT} \times R_{DS(on)}}{15\ \mu A} = \frac{3 \times 10\ A \times 0.008\ \Omega}{15\ \mu A} = 15\ k\Omega \quad (6)$$

For this design, a standard value of 16.2 kΩ is selected for R2. The factor of 3 in the equation accounts for the variations in component tolerances (both initial and over temperature) and output current ripple. The component tolerances include MOSFET $R_{DS(on)}$, I_{LIM} sink current, and the V_{OS} offset voltage of SW vs I_{LIM}.

4.7 Compensation Design

The TPS40007 uses voltage mode control in conjunction with a high frequency error amplifier. The power circuit L-C double pole corner frequency f_C is located in equation (7).

$$Freq_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = 5.1\ kHz \quad (7)$$

The output capacitor ESR zero is calculated by equation (8),

$$F_{Z(esr)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = 33.8\ kHz \quad (8)$$

where the two POSCAPs ESR of 5 mΩ is used in the calculation because the 1 μF is effectively out of the picture at these relatively low frequencies.

The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed near the origin to improve dc regulation.

The first zero is placed below f_C at 2.2 kHz in equation (9).

$$f_{z1} = \frac{1}{2 \times \pi \times \left(R_6 + R_7\right) \times C_{15}} \quad (9)$$

The second zero is placed at 18 kHz shown in equation (10).

$$f_{z2} = \frac{1}{2 \times \pi \times R_4 \times C_7} \quad (10)$$

The first pole is placed near the ESR zero frequency in equation (11),

$$f_{p1} = \frac{1}{2 \times \pi \times R_7 \times C_{15}} \quad (11)$$

and the second pole is placed at one-half the switching frequency at 150 kHz to allow a high-speed transient response, shown in equation (12).

$$f_{p2} = \frac{1}{2 \times \pi \times R_4 \times \left(\frac{C_7 \times C_{11}}{C_7 + C_{11}}\right)} \quad (12)$$

Figure 2 is presents the measured loop gain and phase characteristics. At the loop crossover frequency of 20 kHz the phase margin is approximately 50 degrees.

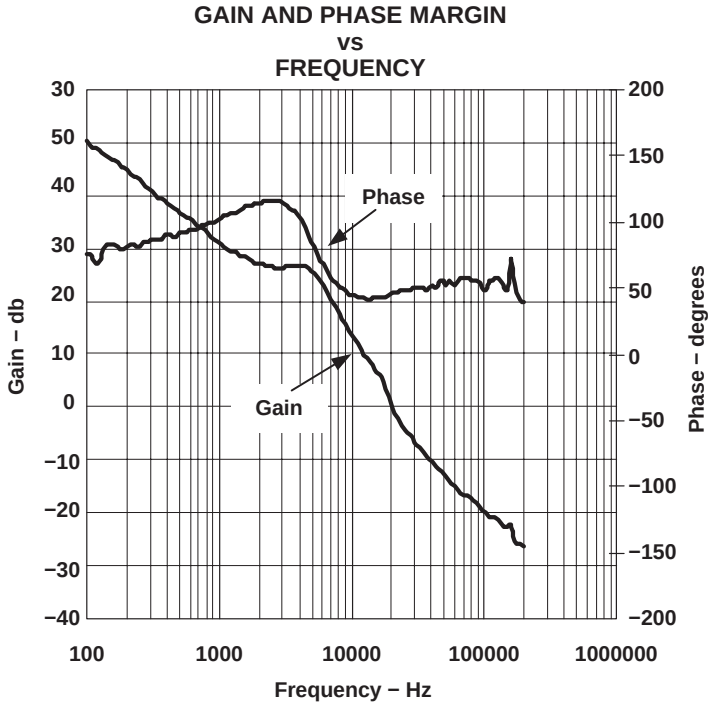


Figure 2.

4.8 Snubber Component Selection

The switch node where Q1 and L1 come together is very noisy. An R-C network fitted between this node and ground can help reduce ringing and voltage overshoot on Q2. This ringing noise should be minimized to prevent it from confusing the control circuitry which is monitoring this node for current limit, Predictive Gate Drive™, and DCM control functions.

As a starting point, the snubber capacitor, C12, is generally chosen to be 5 to 8 times larger than the parasitic capacitance at the node, which is primarily C_{OS} of Q2. Since C_{OS} is around 1600 pF for Q2 at 5 V, C12 is chosen to be 10 nF. R3 is empirically determined to be 2.2 Ω, which minimizes the ringing and overshoot at the switch node. With the relatively low input voltage of 5 V, the power loss, $\frac{1}{2} CV^2f$, is relatively small at 37 mW.

5 PowerPAD™ Packaging

The TPS4000X family is available in the DGQ version of TI's PowerPAD™ thermally enhanced package. In the PowerPAD™, a thermally conductive epoxy is utilized to attach the integrated circuit die to the leadframe die pad, which is exposed on the bottom of the completed package. The leadframe die pad can be soldered to the PCB using standard solder flow techniques when maximum heat dissipation is required. However, depending on power dissipation requirements, the PowerPAD™ may not need to soldered to the PCB.

The thermally conductive epoxy bonding the circuit die to the leadframe die pad causes a high resistance from the leadframe die pad to the device ground pin 5. When the PowerPad™ package is soldered to the PCB, the leadframe die pad can be connected to ground (pin 5), but this is not required. The leadframe die pad should not be connected to other potentials in the circuit.

The PowerPAD™ package helps to keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

To effectively remove heat from the PowerPAD™ package, a thermal land should be provided directly underneath the package. This thermal land usually has vias that help to spread heat to internal copper layers and/or the opposite side of the PCB. The vias should not have thermal reliefs that are often used on ground planes, because this reduces the copper area to transfer heat. Additionally, the vias should be small enough so that the holes are effectively plugged when plated. This prevents the solder from wicking away from the connection between the PCB surface and the bottom of the part. A typical footprint pattern is shown in Figure 2, but does not include the additional copper plane which includes the vias above and below the device.

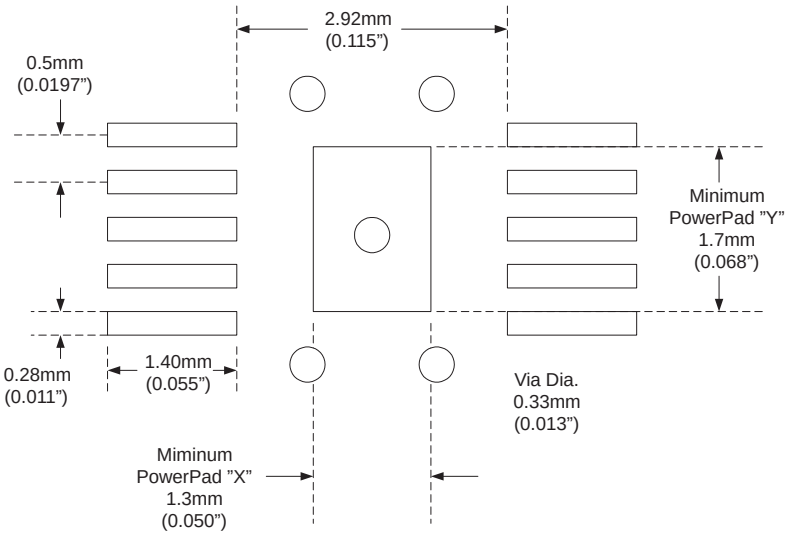


Figure 3. PowerPAD™ PCB Layout Guidelines

The Texas Instrument document, PowerPAD™ Thermally Enhanced Package Application Report (Texas Instrument Literature Number SLMA002) should be consulted for more information on the PowerPAD™ package. This report offers in-depth information on the package, assembly and rework techniques, and illustrative examples of the thermal performance of the PowerPAD™ package.

6 Test Results/Performance Data

6.1 Test Setup

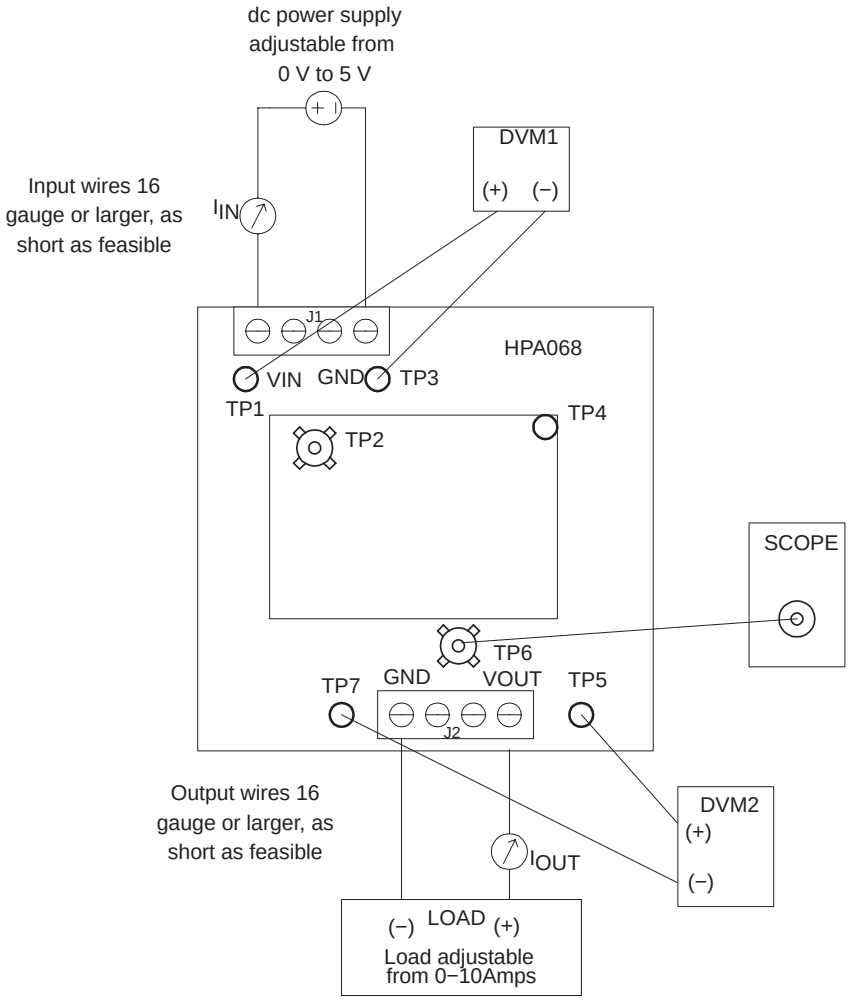


Figure 4. Test Setup

Typical efficiency curves are shown in Figure 5 for 3.3-V input. It should be stressed that measuring high efficiencies requires the utmost care in instrumentation. The power losses are so low that small errors can lead to large variations in measured efficiency. The input and output voltages are measured on the PCB as shown in the test diagram to avoid the losses associated with the input and output connectors.

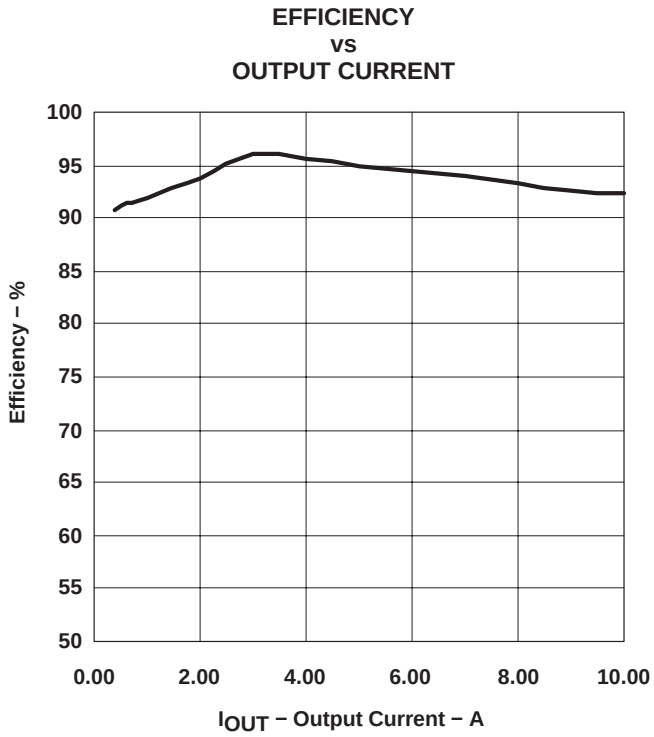


Figure 5.

Figure 6 shows the switch node at V_{IN} = 5 V and I_{OUT} =10 A. As the picture indicates, there is almost negligible body diode conduction using the Predictive Gate Drive™ technique.

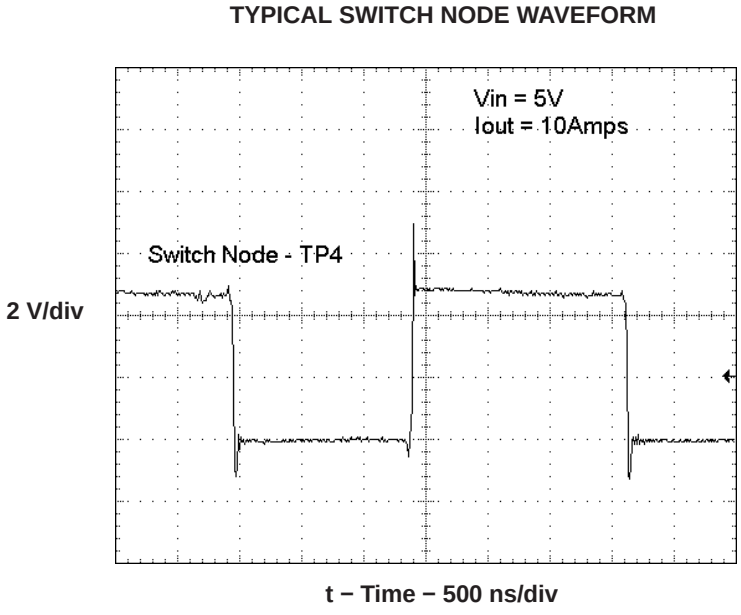


Figure 6.

Figure 7 shows the output voltage ripple at high V_{IN} and full load, which is the worst case condition for output voltage ripple.

OUTPUT VOLTAGE RIPPLE

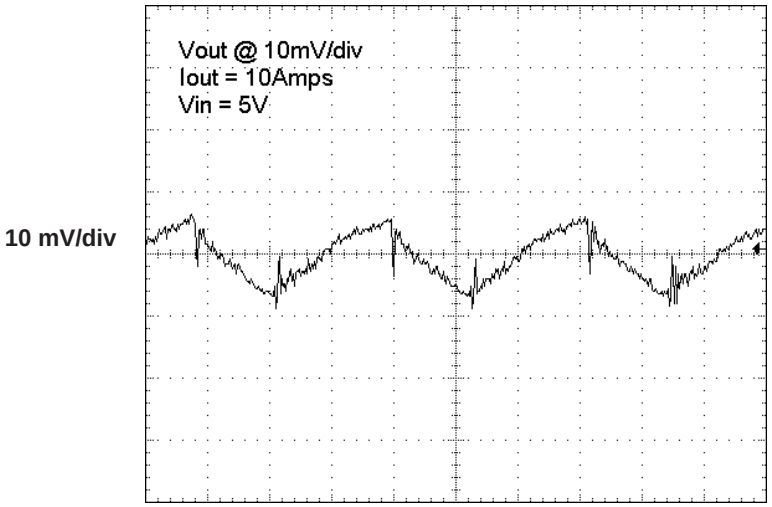


Figure 7.

Figure 8 shows the transient response with a 50% load step from 2.5 A to 7.5 A.

TRANSIENT RESPONSE

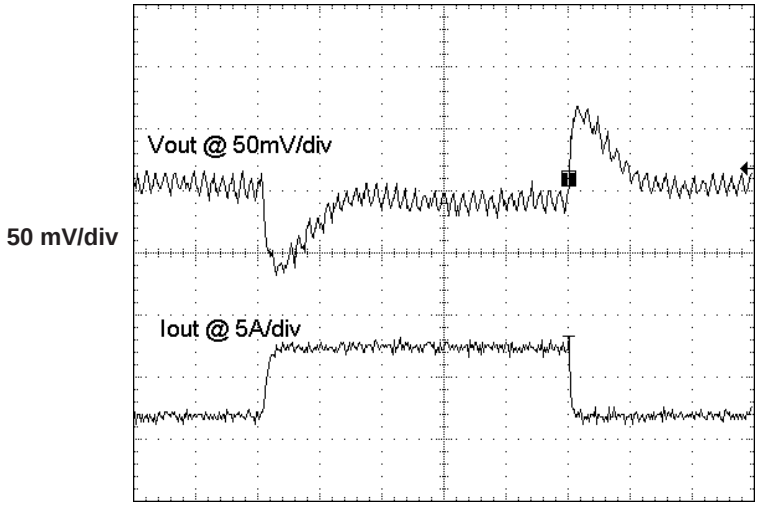


Figure 8.

7 PCB Layout

The PCB top assembly and copper layers are shown in Figures 9 through 11.

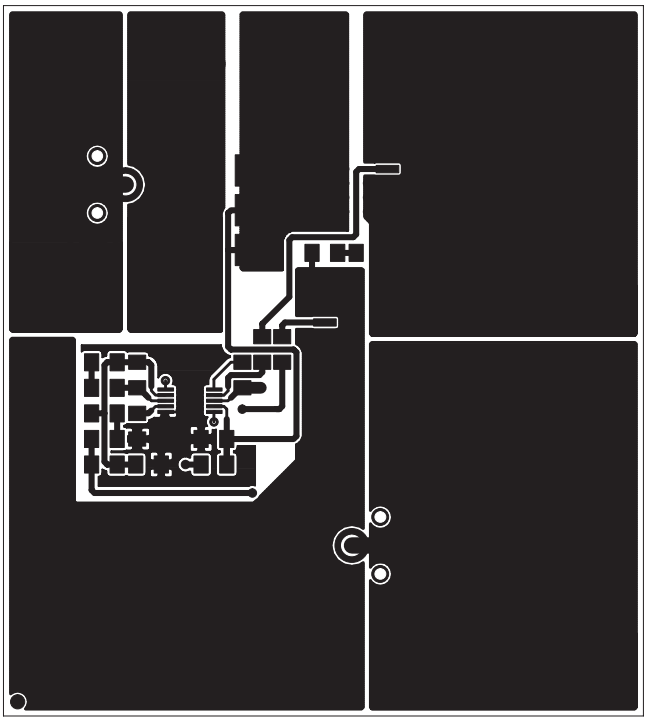


Figure 9

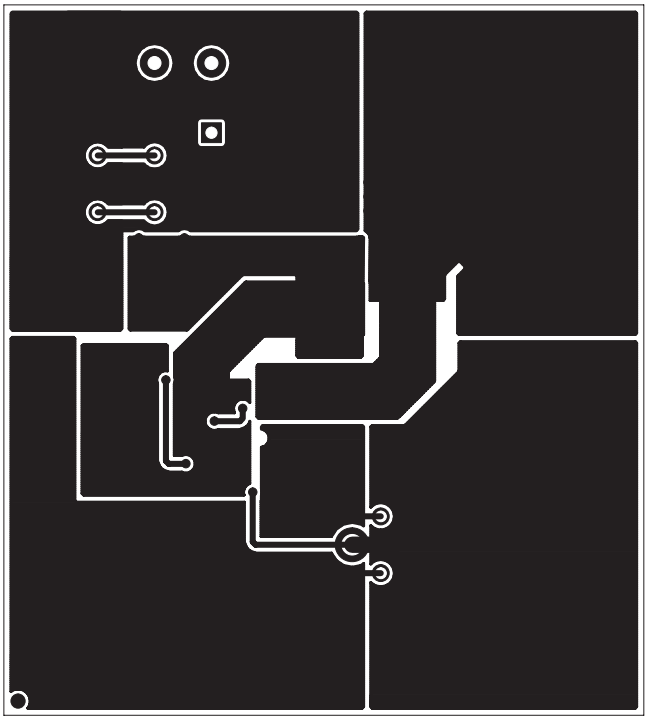


Figure 10

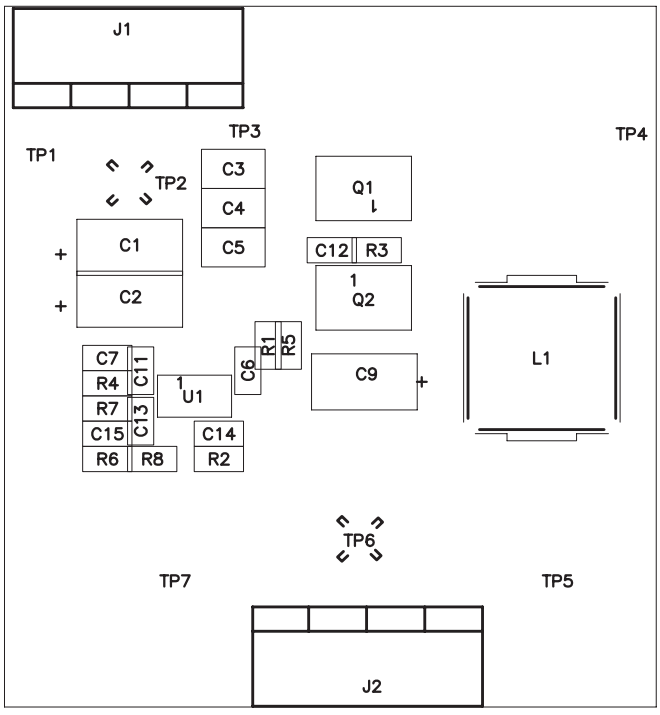


Figure 11

8 List of Material

Table 1 lists the components used in this design. With minor component tweaks this design could be modified to meet a wide range of applications.

	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C1, C2	2	POSCAP, 330 µF, 6.3 V, 10 milliohm, 20%, 7343 (D)	Sanyo	6TPD330M
	C11	1	Ceramic, 180 pF, 50 V, NPO, 10%, 805	Vishay	VJ0805A181KXAAT
	C12	1	Ceramic, 0.01µF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y103KXAAT
	C13	1	Ceramic, 0.0047 µF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y472KXAAT
	C15	1	Ceramic, 6.8 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y682KXAAT
	C3, C4, C5	3	Ceramic, 22 µF, 6.3 V, X5R, 20%, 1210	Panasonic	ECJ−4YB0J226M
	C6, C10, C14	3	Ceramic, 1 µF, 10 V, X5R, 10%, 805	Panasonic	ECJ−2YB1A105K
	C7	1	Ceramic, 1.5 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y152KXAAT
	C8, C9	2	POSCAP, 470 µF, 4 V, 10 mΩ, 20%, 7343 (D)	Sanyo	4TPD470M
Terminal Block	J1, J2	2	4-pin, 15 A, 5.1 mm, 291126	OST	ED2227
Inductor	L1	1	Inductor, SMT, 1 µH, 15 A, 3.5 mΩ, 0.51 x 0.51	Vishay	IHLP−5050CE−01
MOSFET	Q1, Q2	2	MOSFET, N-channel, 12 V, 17 A, 5.5 mΩ, SO8	Siliconix	Si4866DY
Resistor	R1, R5	1	Chip, 1.8 Ω, 1/10 W, 5%, 805	Std	Std
	R2	1	Chip, 16.2 kΩ, 1/10 W, 1%, 805	Std	Std
	R3	1	Chip, 2.2 Ω, 1/10 W, 5%, 805	Std	Std
	R4	1	Chip, 5.90 kΩ, 1/10 W, 1%, 805	Std	Std
	R6	1	Chip, 10 kΩ, 1/10 W, 1%, 805	Std	Std
	R7	1	Chip, 698 Ω, 1/10 W, 1%, 805	Std	Std
	R8	1	Chip, 3.92 Ω, 1/10 W, 1%, 805	Std	Std
JACK	TP1, TP4, TP5,	3	Red, 1 mm, 0.038”, 6400”	Farnell	240−345
Adapter	TP2, TP6	2	3.5-mm probe clip (or 131−5031−00), 72900	Tektronix	131−4244−00
JACK	TP3, TP7	1	Black, 1mm, 0.038”,6400”	Farnell	240−333
Device	U1	1	Low Input Voltage Mode, Syncronous Buck Controller DGQ10	TI	TPS40007DGQ

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