TPS2663x 60-V, 6-A Power Limiting, Surge Protection Industrial eFuse

1 Features

- 4.5 V to 60 V Operating Voltage, 62-V Absolute Maximum
- Integrated 60-V Hot-Swap FET with 31-mΩ R_{ON}
- Reverse Polarity Protection and Reverse Current Blocking Support with an External N-channel FET
- 0.6 A to 6 A Adjustable Current Limit (± 8% Accuracy at 6 A)
- Electrical Fast Transients (IEC61000-4-4) Immunity and Load Protection During Surge (IEC 61000-4-5) with Class-A System Performance
- Fast Reverse Current Blocking (0.12 µs)
- Variants with Adjustable Output Power Limiting
- Fast Turn ON of the FETs (140 µs) During Transient Recovery
- Adjustable UVLO, OVP Cut Off, Output Slew Rate Control for Inrush Current limiting
- Power Up in Thermal Regulation (dVdT = Open) Enables Charging of Large Capacitors
- Variants with 35-V and 40-V Over Voltage Clamp
- Power Good Output (PGOOD) with Adjustable Detection Threshold (PGTH)
- Selectable Over Current Fault Response Options Between Auto-Retry and Latch Off (MODE)
- Variants with 2x Pulse Over Current Support
- Analog Current Monitor (IMON) Output
- UL 2367 Recognition Pending

2 Applications

- Factory Automation and Control – PLC, DCS, HMI, I/O Modules, Sensor Hubs
- Motor Drives – CNC, Encoder Supply
- Electronic Circuit Breakers

3 Description

The TPS2663x devices are easy to use, positive 60 V and 6 A eFuse with a 31 mΩ integrated FET. It features a B-FET driver to control an external N-channel FET in the system designs that require protection from input reverse polarity faults and reverse current blocking. The device incorporates robust protection features that simplify system designs requiring class-A performance (no supply interrupts) during system tests like IEC61000-4-5 Surge tests as well as input supply brown-out tests. The TPS26632, TPS26633 and TPS26635 devices integrate adjustable output power limiting (PLIM) functionality that simplifies the system design requiring compliance in accordance to the standards like IEC61010-1.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS26630 TPS26631 TPS26632 TPS26633 TPS26635	VQFN (24)	4.00 mm × 4.00 mm
TPS26631 TPS26632 TPS26633	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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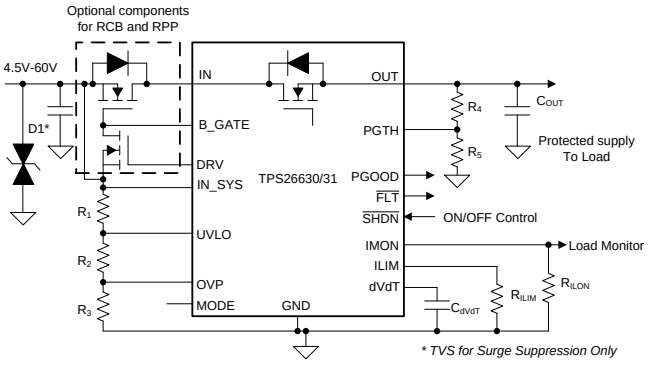
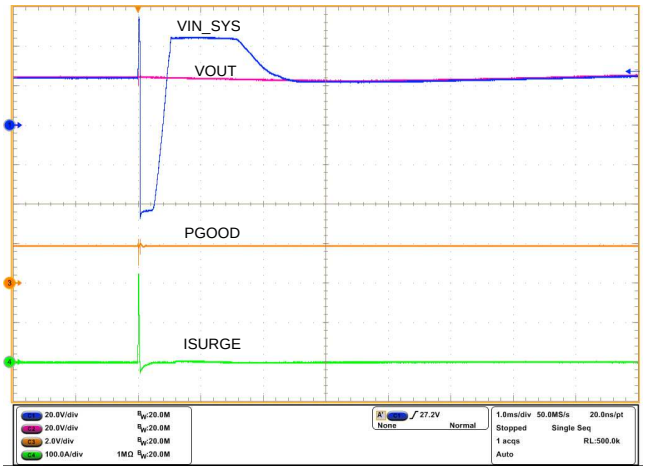
Simplified Schematic



IEC61000-4-5 Surge Performance at 24-V Supply



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4 Revision History

DATE	REVISION	NOTES
September 2018	*	Initial release.

5 Description (Continued)

Inrush current control during hot-plug operation can be achieved with the help of dVdT feature. The TPS26630 and TPS26631 devices feature adjustable over voltage cut-off functionality whereas the TPS26632 and TPS26633 feature a fixed 35 V output voltage clamp whereas TPS26635 feature 40 V clamp. The devices also feature adjustable over current functionality. The TPS26631 and TPS26633 features pulse over current support up to 2x. Analog current monitor can be used to sense the real time load current. The device features fault indicator output. PGOOD with adjustable detection threshold (PGTH) and can be used for enable/disable control of the downstream DC-DC converters.

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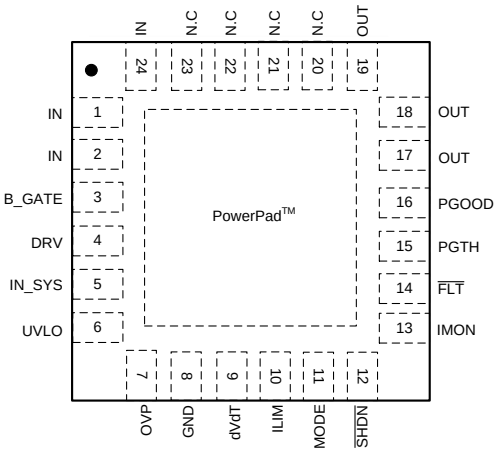
6 Device Comparison Table

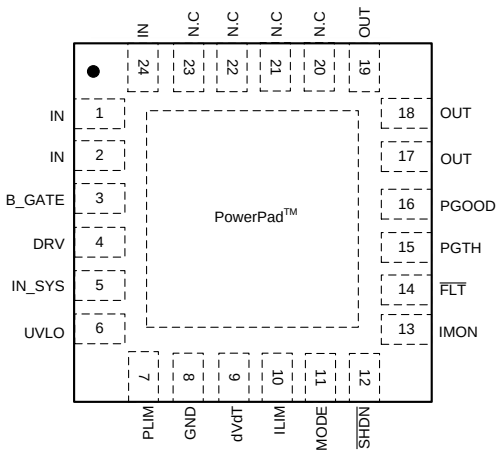
PART NUMBER	OVERVOLTAGE PROTECTION	OVERLOAD FAULT RESPONSE	ADJUSTABLE OUTPUT POWER LIMITING
TPS26630	Overvoltage cut-off, adjustable	Active Current Limiting (1x)	No
TPS26631	Overvoltage cut-off, adjustable	Active Current Limiting with Pulse current support (2x)	No
TPS26632	Overvoltage clamp, fixed (35 V)	Active Current Limiting (1x)	Yes
TPS26633	Overvoltage clamp, fixed (35 V)	Active Current Limiting with Pulse current support (2x)	Yes
TPS26635	Overvoltage clamp, fixed (40 V)	Active Current Limiting with Pulse current support (2x)	Yes

7 Pin Configuration and Functions

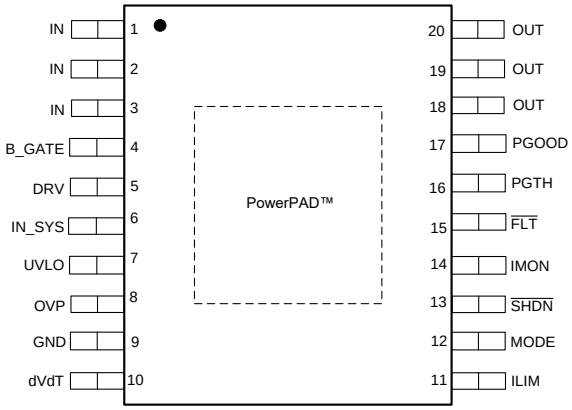
TPS26630, TPS26631 RGE Package
24-Pin VQFN
Top View



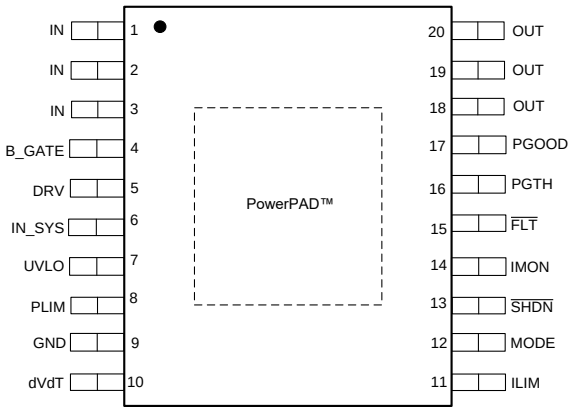
TPS26632, TPS26633, TPS26635 RGE Package
24-Pin VQFN
Top View



TPS26630, TPS26631 PWP Package
20-Pin HTSSOP
Top View



TPS26632, TPS26633, TPS26635 PWP Package
20-Pin HTSSOP
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	TPS26630, TPS26631, TPS26632, TPS26633, TPS26635			
	VQFN	HTSSOP		
IN	1	1	P	Power input. Connects to the DRAIN of the internal FET
	2	2		
	24	3		
B_GATE	3	4	O	Blocking FET gate driver output. Connect B_GATE to GATE of the external NFET. If external FET is not used then leave B_GATE pin floating
DRV	4	5	O	Blocking FET fast pull down switch drive. Connect DRV to the GATE of external pull down switch. Leave this pin floating if external N-FET is not used.
IN_SYS	5	6	P	Power input and supply voltage of the device. When an external Blocking FET is used then connect IN_SYS to source of the FET. Short IN_SYS to IN in case blocking FET is not used
UVLO	6	7	I	Input for setting the programmable undervoltage lockout threshold. An undervoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the power-failure. Connect UVLO pin to GND pin to select the internal default threshold
OVP	7	8	I	Input for setting the programmable overvoltage protection threshold (For TPS26630 and TPS26631 Only). An overvoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the overvoltage fault. Connect OVP pin to GND pin externally to select the internal default threshold.
PLIM	7	8	I	Input for setting the programmable output power limiting threshold (For TPS26632, TPS26633 and TPS26635 Only). Connect a resistor across PLIM to GND to set the output power limit. Connect PLIM to GND if PLIM feature is not used. See the *Output Power Limiting, PLIM (TPS26632, TPS26633 and TPS26635 Only)* section
GND	8	9	—	Connect GND to system ground
dVdT	9	10	I/O	A capacitor from this pin to GND sets output voltage slew rate. Leaving this pin floating enables device power up in thermal regulation resulting in fast output charge. See the *Hot Plug-In and In-Rush Current Control* section
ILIM	10	11	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit. See the *Overload and Short Circuit Protection* section
MODE	11	12	I	Mode selection pin for over load fault response. See the *Device Functional Modes* section
$\overline{SHDN}$	12	13	I	Shutdown pin. Pulling $\overline{SHDN}$ low makes the device to enter into low power shutdown mode. Cycling $\overline{SHDN}$ pin voltage resets the device that has latched off due to a fault condition
IMON	13	14	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage. If unused, leave it floating
$\overline{FLT}$	14	15	O	Fault event indicator. It is an open drain output. If unused, leave floating or connect to GND
PGTH	15	16	I	PGOOD comparator input.
PGOOD	16	17	O	Active High. A high indicates PGTH has crossed the $V_{(PGTHR)}$ threshold and the internal FET is enhanced. PGOOD goes low when $V_{(PGTH)}$ hits $V_{(PGTHF)}$ threshold. If PGOOD is unused then connect to GND or leave it floating
OUT	17	18	P	Power output of the device
	18	19		
	19	20		
N. C	20	—	—	No Connect
	21			
	22			
	23			
PowerPad™	—	—	—	Connect PowerPad to GND plane for heat sinking. Do not use PowerPad as the only electrical connection to GND

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN_SYS		–60	62	V
IN_SYS (10ms transient)		–60	75	V
IN, OUT, UVLO, $\overline{FLT}$, PGOOD, PGTH		–0.3	62	
IN_SYS – OUT (10ms transient), with a Blocking FET		–85	75	
IN (10ms transient)		–0.3	75	
BGATE		–60	76	
BGATE – IN_SYS		–0.3	14	
DRV		–60	67	
DRV – IN_SYS		–0.3	5	
OVP, dVdT, IMON, MODE, $\overline{SHDN}$, ILIM		–0.3	5	V
$I_{\overline{FLT}}$, I_{dVdT}, PGOOD	Sink current		10	mA
IdVdT, IILIM	Source current			Internally limited
T_J	Operating Junction temperature	–40	150	°C
	Transient junction temperature	–65	$T_{(TSD)}$	
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN_SYS, IN	Input Voltage	4.5		60	V
$\overline{OUT}$,UVLO, PGTH, PGOOD, $\overline{FLT}$		0		60	V
$\overline{OVP}$, dVdT, IMON, MODE, $\overline{SHDN}$		0		4	V
ILIM	Resistance	3		30	kΩ
IMON		1			kΩ
IN, IN_SYS, OUT	External Capacitance	0.1			µF
T_J	Operating Junction temperature	–40	25	125	°C

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8.4 Thermal Information

THERMAL METRIC(1)		TPS2663		UNIT
		RGE (VSON)	PWP (HTSSOP)	
		24 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.2	23.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	10	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.2	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN\_SYS)}$	Operating input voltage		4.5		60	V
$IQ_{(ON)}$	Supply current	Enabled: $V_{(\overline{SHDN})}$ = 2 V		1.42	1.6	mA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})}$ = 0 V		22	53	µA
$I_{(GND)}$	Ground current during reverse polarity	$V_{(IN\_SYS)}$ = –24V, $V_{(IN)}$ = Floating, $V_{(OUT)}$ = 0V			200	µA
$V_{(OVC)}$	Over voltage clamp	TPS26632, TPS26633 Only, $V_{(IN\_SYS)}$ > 35V, $I_{(OUT)}$ = 1mA	32.7		35	V
		TPS26635 Only, $V_{(IN\_SYS)}$ > 40V, $I_{(OUT)}$ = 1mA	36		40	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(INSYS\_UVLO)}$	Factory set $V_{(IN\_SYS)}$ undervoltage trip level trip level	$V_{(IN\_SYS)}$ rising, $V_{(UVLO)}$ = 0 V	15.1	15.6	15.9	V
		$V_{(IN\_SYS)}$ falling, $V_{(UVLO)}$ = 0 V		14.8		V
$V_{(SEL\_UVLO)}$	Internal UVLO select threshold		180		240	mV
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.176	1.2	1.224	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling			1.14		V
$I_{(UVLO)}$	UVLO Input leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 60 V	–100	0	100	nA
OVERVOLTAGE PROTECTION (OVP) INPUT						
$V_{(IN\_SYS\_OVP)}$	Factory set $V_{(IN\_SYS)}$ overvoltage trip level trip level	$V_{(IN\_SYS)}$ rising, $V_{(OVP)}$ = 0 V	32.8	34.2	35.8	V
		$V_{(IN\_SYS)}$ falling, $V_{(OVP)}$ = 0 V	32.4	33.7	35.4	V
$V_{(SEL\_OVP)}$	Internal OVP select threshold		180		240	mV
$V_{(OVPR)}$	over-voltage threshold voltage, rising		1.176	1.2	1.224	V
$V_{(OVPF)}$	over-voltage threshold voltage, falling			1.14		V
$I_{(OVP)}$	OVP Input leakage current	0 V ≤ $V_{(OVP)}$ ≤ 4 V	–100	0	100	nA
POWER LIMITING CONTROL (PLIM) INPUT – TPS26632, 33, 35 ONLY						
$V_{(SEL\_PLIM)}$	Power Limit Feature select threshold				240	mV
$I_{(PLIM)}$	PLIM sourcing current	$V_{(PLIM)}$ = 0 V		5		µA
$P_{(PLIM)}$	Max Output power	$R_{(PLIM)}$ = 100 kΩ		100		W
		$R_{(PLIM)}$ = 150 kΩ		150		W
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Open circuit voltage	$I_{(\overline{SHDN})}$ = 0.1 µA	2.48		3.4	V
$V_{(SHUTF)}$	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling				0.8	V
$V_{(SHUTR)}$	$\overline{SHDN}$ threshold rising		2			V

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Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(\overline{SHDN})}$	Leakage current	$V_{(\overline{SHDN})}$ = 0.4 V	–10			µA
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0 V	1.9	2	2.1	µA
$GAIN_{(dVdT)}$	dVdT to OUT gain	$V_{(OUT)}$ /$V_{(dVdT)}$		24		V/V
V_dVdTmax	dVdT maximum capacitor voltage				4.75	V
$R_{(dVdT)}$	dVdT discharging resistance	$V_{(\overline{SHDN})}$ = 0 V, with $I_{(dVdT)}$ = 10 mA sinking		14		Ω
CURRENT LIMIT PROGRAMMING (ILIM)						
$I_{(OL)}$	Over Load current limit	$R_{(ILIM)}$ = 30 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.51	0.6	0.69	A
		$R_{(ILIM)}$ = 9 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V		2		A
		$R_{(ILIM)}$ = 4.02 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V		4.5		A
		$R_{(ILIM)}$ = 3 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V		6		A
$I_{(OL\_Pulse)}$	Transient Pulse Over current limit	3 kΩ < $R_{(ILIM)}$ < 30 kΩ, TPS26631, TPS26633 and TPS26635 Only		2x$I_{(OL)}$		A
$I_{(FASTRIP)}$	Fast-trip comparator threshold			2x$I_{(OL)}$		A
$I_{(SCP)}$	Short Circuit Protect current			40		A
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain factor $I_{(IMON)}$:$I_{(OUT)}$	0.6 A ≤ $I_{(OUT)}$ ≤ 6 A		27.7		µA/A
BFET (BLOCKING FET GATE DRIVER)						
V_{BGATE}	B_GATE clamp voltage	$V_{(BGATE)}$ – $V_{(IN\_SYS)}$	8.6	12	14	V
I_{BFET}	Blocking FET Gate drive current	$V_{(BGATE)}$ – $V_{(IN\_SYS)}$ = 1 V	17	20	23	µA
Rpd_BGATE	B_GATE Pull down resistance			1000		kΩ
$V_{(DRV\_OH)}$	DRV logic high level	$V_{(DRV)}$ – $V_{(IN\_SYS)}$, $C_{(DRV)}$ <= 50 pF		3.6		V
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 6 A, –40°C ≤ T_J ≤ +125°C		31	53	mΩ
$I_{lkg(OUT)}$	OUT leakage during input supply brownout	$V_{(IN\_SYS)}$ = 0V, $V_{(OUT)}$ = 24V, $V_{(IN)}$ = Floating, $V_{(\overline{SHDN})}$ = 2V, Sinking			500	µA
$V_{(REVTH)}$	$V_{(IN\_SYS)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, rising			–15		mV
$V_{(FWDTH)}$	$V_{(IN\_SYS)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, falling		49	57	63	mV
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5 mA sinking	36	70	130	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 60 V	–100		100	nA
POWER GOOD (PGOOD)						
$R_{(PGOOD)}$	PGOOD Pull-down resistance	$V_{(dVdT)}$ = 0 V, $I_{(PGOOD)}$ = 5 mA sinking	36	70	130	Ω
$I_{(PGOOD)}$	PGOOD Input leakage current	0 V ≤ $V_{(PGOOD)}$ ≤ 60 V	–100		100	nA
POSITIVE INPUT FOR POWER GOOD COMPARATOR (PGTH)						
$V_{(PGTHR)}$	PGTH threshold voltage, rising		1.176	1.2	1.224	
$V_{(PGTHF)}$	PGTH threshold voltage, falling			1.14		
$I_{(PGOOD)}$	PGTH input leakage current	0 V ≤ $V_{(PGTH)}$ ≤ 60 V	–100		100	nA
THERMAL SHUT DOWN (TSD)						
$T_{(J\_REG)}$	Thermal regulation set point		147	150	154	ºC
$T_{(TSD)}$	TSD threshold, rising			164		ºC
$T_{(TSDhyst)}$	TSD hysteresis			11		ºC
MODE						

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Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MODE_SEL	Mode selection	MODE = Open		Latch		
		MODE = Short to GND		Auto–Retry		

8.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO INPUT (UVLO)						
$UVLO\_t_{on(dly)}$	UVLO switch turnon delay	UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV with $V_{(PGTH}$ < $V_{(PGTHF)}$		669 + 49564 x $C_{(dVdT)}$		µs
$UVLO\_t_{on(fast\_dly)}$	UVLO switch turnon delay (fast)	UVLO↑ (100 mV above $V_{(UVLOR)}$) to FET ON with $V_{(PGTH)}$ > $V_{(PGTHF)}$		162	250	µs
$UVLO\_t_{off(dly)}$	UVLO switch turnoff delay	UVLO↓(20 mV below $V_{(UVLOF)}$) to $\overline{FLT}$↓		12		µs
OVER VOLTAGE PROTECTION INPUT (OVP)						
$t_{OVP(dly)}$	OVP switch turnOFF delay	OVP↑ (20 mV above $V_{(OVPR)}$) to $\overline{FLT}$↓		10		µs
$t_{OVP(fast\_dly)}$	OVP switch turnOFF delay (fast)	OVP↓ (100 mV below $V_{(OVPF)}$) to FET ON with $V_{(PGTH\ )}$ > $V_{(PGTHF)}$	58	141	225	µs
$t_{OVP(dly)}$	OVP switch disable delay	OVP↓ (100 mV below $V_{(OVPF)}$) to FET ON with $V_{(PGTH\ )}$ < $V_{(PGTHF)}$		150 + 49564 x $C_{(dVdT)}$		µs
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
$t_{SD(dly)}$	SHUTDOWN entry delay	$\overline{SHDN}$↓ (below $V_{(SHUTF)}$) to FET OFF		0.9		µs
CURRENT LIMIT						
$t_{RCB\_FLT(dly)}$	Hot-short response time	$I_{(OUT)}$ > $I_{(SCP)}$		0.3		µs
	Soft short response	$I_{(FASTTRIP)}$ < $I_{(OUT)}$ < $I_{(SCP)}$		3.3	4.2	µs
$t_{CL\_PLIM(dly)}$	Maximum duration in current & (power limiting: TPS26632, TPS26633 and TPS26635 Only)			162		ms
$t_{CB(dly)}$	Maximum duration in 2x current limiting	$I_{(OL)}$ < $I_{(OUT)}$ ≤ $I_{(2xOL)}$		25.5		ms
$t_{CBRetry(dly)}$	Retry delay in Pulse over current limiting	MODE = GND, TPS26631, TPS26633 and TPS26635 Only		648		ms
$t_{CL\_PLIM\_FLT(dly)}$	$\overline{FLT}$ delay in current & (power limiting: TPS26632, TPS26633 and TPS26635 Only)			1.3		ms
REVERSE CURRENT BLOCKING (RCB) COMPARATOR						
$t_{RCB(fast\_dly)}$	Reverse protection comparator dectection delay (reverse)	($V_{(IN\_SYS)}$ – $V_{(OUT)}$)↓ (1 V overdrive below $V_{(REVTH)}$) to $V_{(DRV)}$ – $V_{(IN\_SYS)}$ = $V_{(DRV\_OH)}$		0.12	0.37	µs
$t_{RCB(dly)}$		($V_{(IN\_SYS)}$ – $V_{(OUT)}$)↓ (10 mV overdrive below $V_{(REVTH)}$) to $V_{(DRV)}$ – $V_{(IN\_SYS)}$ = $V_{(DRV\_OH)}$			30	µs
$t_{RCB(flt\_dly)}$	Fault assertion Delay	($V_{(IN\_SYS)}$ – $V_{(OUT)}$)↓ (10 mV overdrive below $V_{(REVTH)}$) to $\overline{FLT}$↓		650		µs
$t_{FWD\_FLT(dly)}$	Reverse protection comparator dectection delay (forward)	($V_{(IN\_SYS)}$ – $V_{(OUT)}$)↑ (10 mV overdrive above $V_{(FWDTH)}$) to $V_{(BGATE)}$ – $V_{(IN\_SYS)}$ = 5 V, $C_{(BFET\text{-}IN\_SYS)}$ = 4.7 nF		1.6		ms
	Fault de-assertion Delay	($V_{(IN\_SYS)}$ – $V_{(OUT)}$)↑ (10 mV overdrive above $V_{(FWDTH)}$) to $\overline{FLT}$↑		650		µs
OUTPUT RAMP CONTROL (dVdT)						

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Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN\_SYS)}$ = $V_{(IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(FASTCHARGE)}$	Output ramp time in fast charging	$C_{(dVdT)}$ = Open, 10% to 90% $V_{(OUT)}$, $C_{(OUT)}$ = 1 µF;		240		µs
$t_{(dVdT)}$	Output ramp time	$C_{(dVdT)}$ = 22 nF, 10% to 90% $V_{(OUT)}$		8.35		ms
POWER GOOD (PGOOD)						
t_{PGOODR}	PGOOD delay (deglitch) time	Rising edge		1.3		ms
t_{PGOODF}	PGOOD delay (deglitch) time	Falling edge, PGTH↓ (10mV below $V_{(PGTHF)}$)		1.6		µs
FAULT FLAG ($\overline{FLT}$)						
$t_{CB\_FLT(dly)}$	$\overline{FLT}$ assertion delay in Pulse over current limiting	Delay from $I_{(OUT)}$ > $I_{(OL)}$ to $\overline{FLT}$↓. TPS26631, TPS26633 and TPS26635 Only		25.5		ms
THERMAL SHUTDOWN (TSD)						
$t_{(TSD\_retry)}$	Retry delay in TSD	MODE = GND		648		ms
$t_{(Treg\_timeout)}$	Thermal Regulation Timeout			2.5		s

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9 Detailed Description

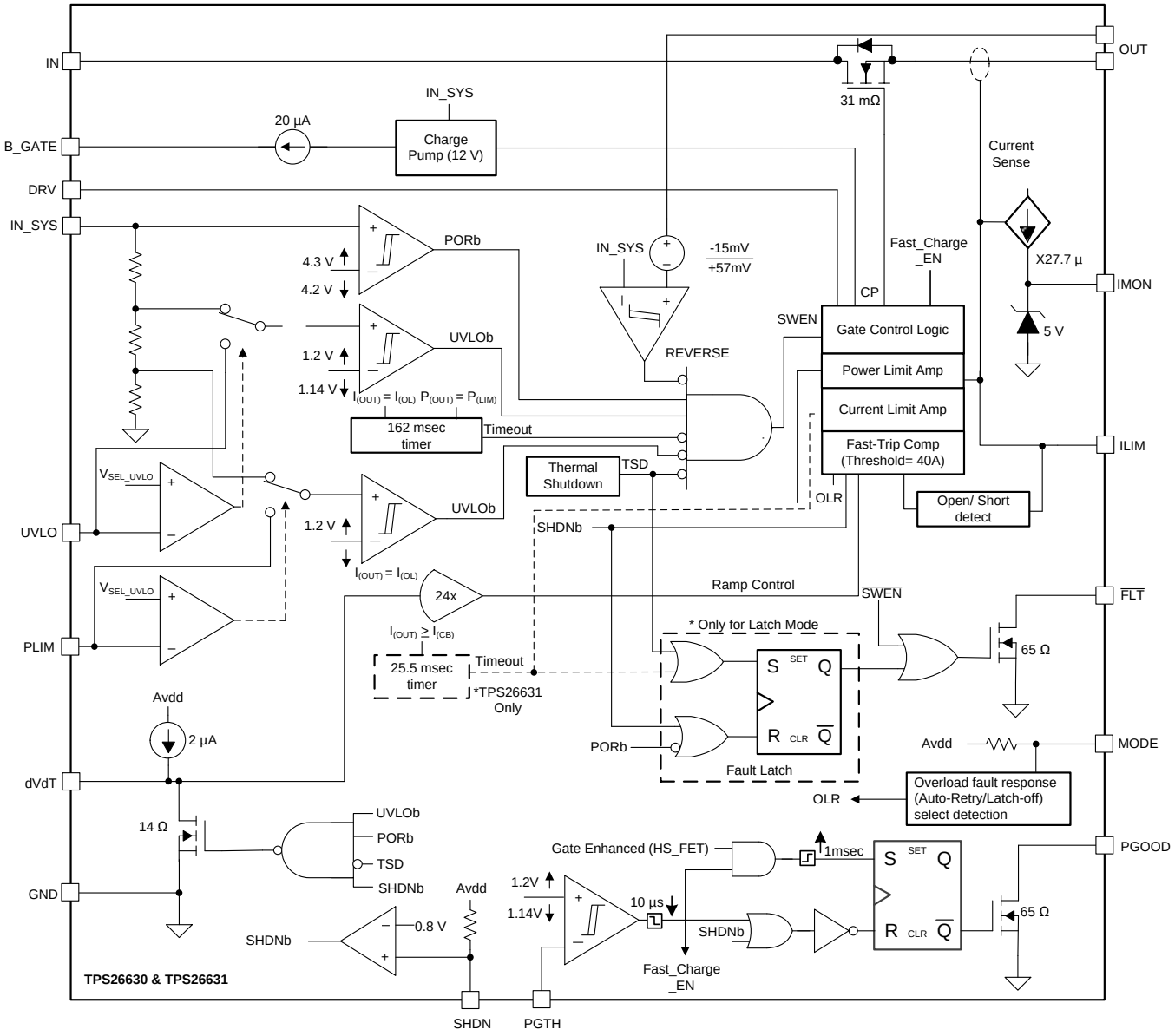
9.1 Overview

The TPS2663x devices are a family of high voltage industrial eFuses. The devices provides robust protection for all systems and applications powered from 4.5 V to 60 V. With an external N-channel FET the devices can be used to protect the loads from negative supply voltages down to – 60 V. For hot-pluggable boards, the devices provides hot-swap power management with in-rush current control and programmable output voltage slew rate features using the dVdT pin. Load, source and device protections are provided with many programmable features including overcurrent, overvoltage, undervoltage. The precision overcurrent limit (±8% at 6 A) helps to minimize over design of the input power supply, while the fast response short circuit protection 300 ns (typical) immediately isolates the faulty load from the input supply when a short circuit is detected. The device features fast reverse current blocking response (0.12 µs). The internal robust protection control blocks of the TPS2663x along with its ±60 V rating helps to simplify the system designs for the industrial surge compliance ensuring complete protection of the load and the device. By monitoring the output voltage through the PGTH pin, the device distinguishes between real system faults and system transients and the turn ON delay is controlled accordingly. This scheme ensures fast recovery during system tests like voltage interruption and brown-out tests, EMC testing like Electrical Fast Transients (IEC61000-4-4) and Surge (IEC61000-4-5). The TPS26632, TPS26633 and TPS26635 devices integrate adjustable output power limiting (PLIM) functionality that simplifies the system design requiring compliance in accordance to standards like IEC61010-1 *Output Power Limiting, PLIM (TPS26632, TPS26633 and TPS26635 Only)*. The devices provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault signal for the downstream system. The TPS2663x devices monitor functions threshold accuracy of ±3% ensures tight supervision of the supply bus, eliminating the need for a separate supply voltage supervisor chip. The devices monitors $V_{(IN\_SYS)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected.

Additional features of the TPS2663x devices include:

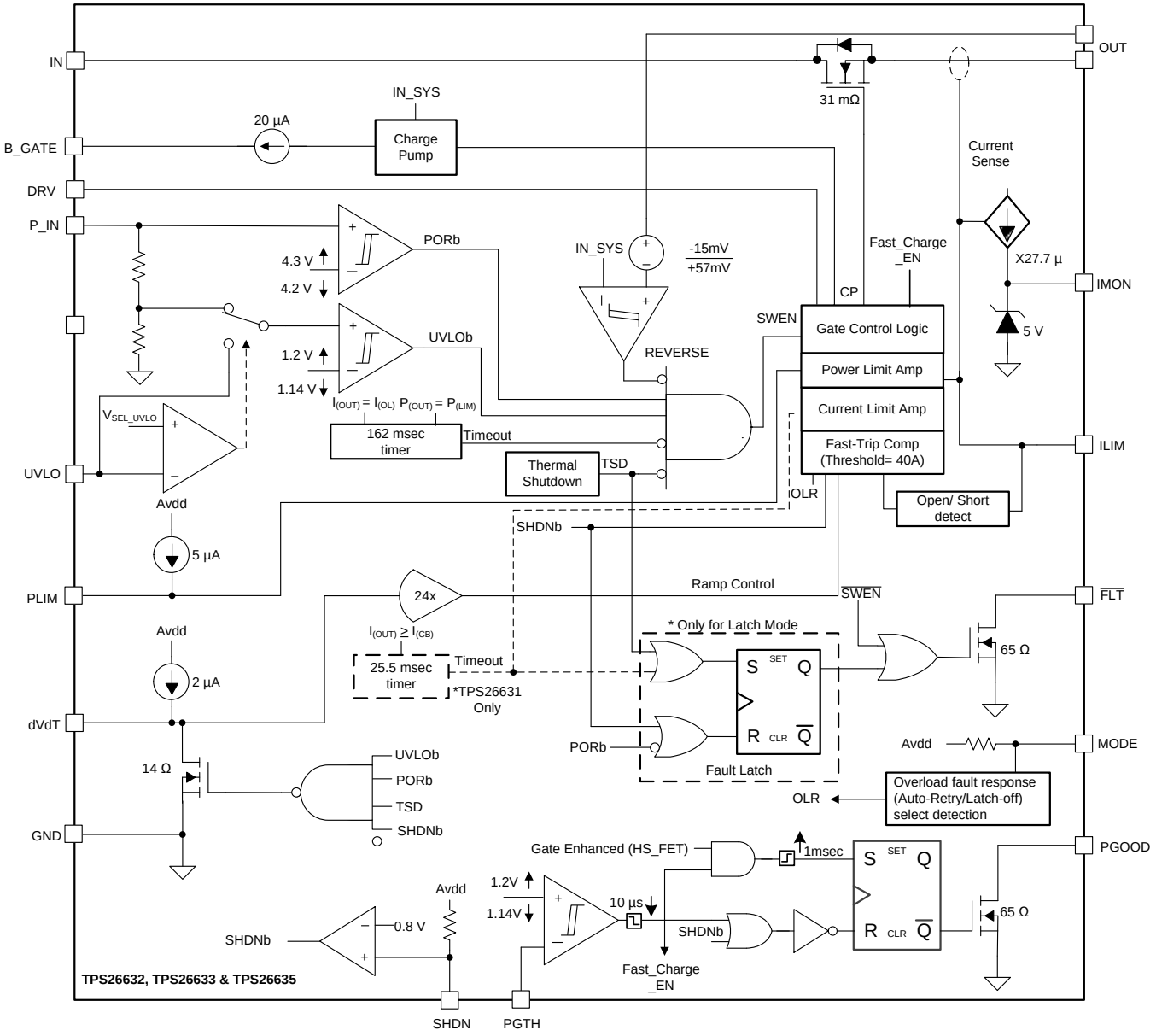
- Current monitor output (IMON) for health monitoring of the system
- A choice of latch off or automatic restart mode response during current limit, Power Limit and thermal fault using MODE pin
- PGOOD indicator output with adjustable detection threshold (PGTH)
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for supply brown-out and overvoltage faults
- Enable and Disable control from an MCU using $\overline{SHDN}$ pin

9.2 Functional Block Diagram



ADVANCE INFORMATION

Functional Block Diagram (continued)



9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

The undervoltage comparator input is when the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 60 mV. To set the input UVLO threshold, connect a resistor divider network from IN_SYS supply to UVLO terminal to GND as shown in the Typical Application circuit. The TPS2663x devices also features a factory set 15.6-V input supply undervoltage lockout $V_{(IN\_SYS\_UVLO)}$ threshold with 800 mV hysteresis. This feature can be enabled by connecting the UVLO terminal directly to the GND terminal. If the Undervoltage Lock-Out function is not needed, the UVLO terminal must be connected to the IN_SYS terminal. UVLO terminal must not be left floating. In the applications where reverse polarity protection is required connect a minimum of 300 kΩ resistor between UVLO and IN_SYS.

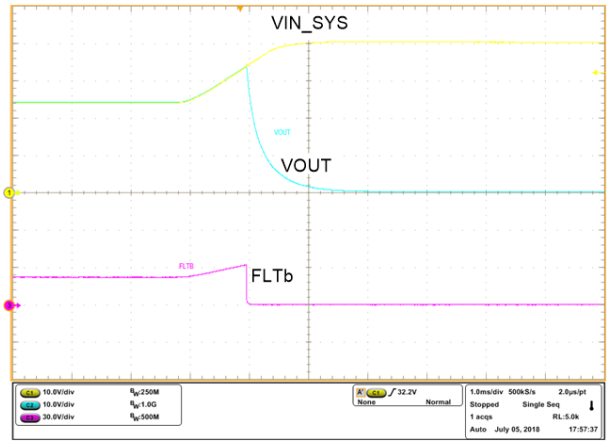
ADVANCE INFORMATION

Feature Description (continued)

9.3.2 Overvoltage Protection (OVP)

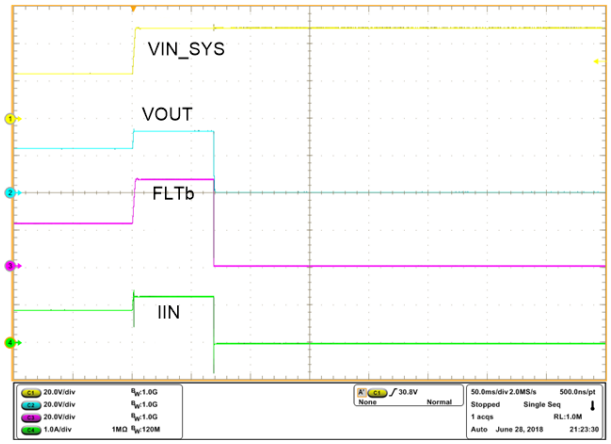
The TPS2663x devices incorporate circuitry to protect the system during overvoltage conditions. The TPS26630 and TPS26631 feature overvoltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN_SYS supply to OVP terminal to GND as shown in the Typical Application circuit. The TPS26630 and TPS26631 also feature a factory set 34.2-V input overvoltage cut off $V_{(IN\_SYS\_OVP)}$ threshold with a 500 mV hysteresis. This feature can be enabled by connecting the OVP terminal directly to the GND terminal. The TPS26632 and TPS26633 feature an internally fixed 35 V max overvoltage clamp $V_{(OVC)}$ functionality. The TPS26632 and TPS26633 clamps the output voltage to $V_{(OVC)}$, when the input voltage exceeds 35 V. TPS26635 features a fixed 40 V max over voltage clamp level. During the output voltage clamp operation, the power dissipation in the internal MOSFET is PD = $(V_{(IN\_SYS)} – V_{(OVC)}) \times I_{(OUT)}$. Excess power dissipation for prolonged period can make the device to enter into thermal shutdown.

Figure 1 illustrates the overvoltage cut-off functionality and Figure 2 illustrates the over voltage clamp functionality .



TPS26630 and TPS26631

Figure 1. Over Voltage Cut-off Response at 33-V Level



TPS26632 and TPS26633

Figure 2. Over Voltage Clamp Response

ADVANCE INFORMATION

9.3.3 Hot Plug-In and In-Rush Current Control

The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on. The fastest output slew rate of 24/240 µs can be achieved by leaving dVdT pin floating. The inrush current can be calculated using Equation 1.

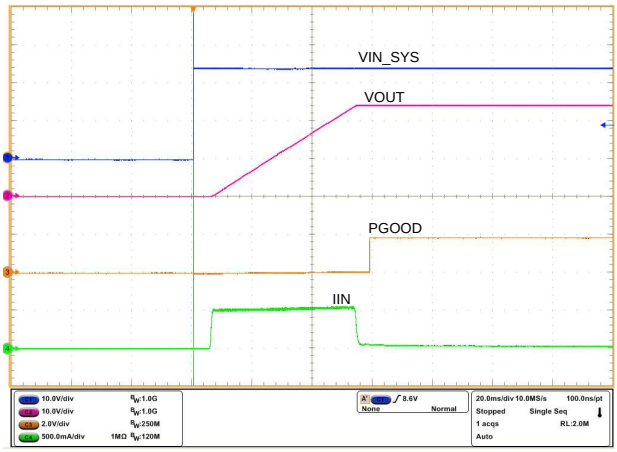
$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN\_SYS)}}{t_{dVdT}} \quad (1)$$

where

$$t_{dVdT} = 20.8 \times 10^3 \times V_{(IN\_SYS)} \times C_{(dVdT)} \quad (2)$$

Figure 3 illustrates in-rush current control performance of the device during Hot Plug-In.

Feature Description (continued)



C_{dVdT} = 100 nF C_{OUT} = 1000 µF R_{ILIM} = 4.02 kΩ

Figure 3. Hot Plug In and Inrush Current Control at 24-V Input

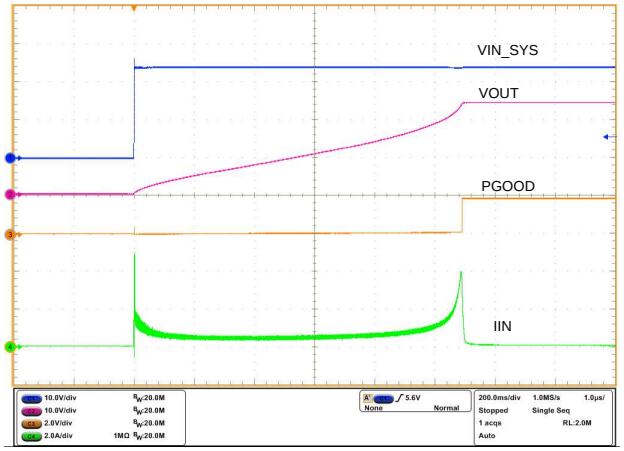
9.3.3.1 Thermal Regulation Loop

The power dissipation during power up can be calculated using Equation 3.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (3)$$

System designs requiring to charge large output capacitors rapidly or powering up an off board load may result in a higher $PD_{(INRUSH)}$ within the device causing the junction temperature to rise. Once the junction temperature rises to $T_{(J\_REG)}$ level, the device starts regulating the junction temperature at $T_{(J\_REG)}$ by controlling the inrush current profile through the device for a maximum duration of $t_{(Treg\_timeout)}$. If the output does not charge up within this time then the internal FET is turned OFF. Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF). This scheme ensures fast and reliable power up operation. Figure 4 illustrates performance of the device operating in thermal regulation loop during charging of a large output capacitor.

The Thermal regulation loop gets disabled internally after the power up when the internal FET gets fully enhanced or when the $t_{(Treg\_timeout)}$ time is elapsed.



C_{dVdT} = Open C_{OUT} = 30 mF R_{ILIM} = 4.02 kΩ

Figure 4. Thermal Regulation Loop Response During Power up With Large Capacitive Load

ADVANCE INFORMATION

Feature Description (continued)

9.3.4 PGOOD and PGTH

The devices feature an open drain Power good (PGOOD) indicator output. PGOOD can be used for enable and disable of the downstream loads like DC-DC converters. Connect a resistor ladder network from VOUT, PGTH and GND to set the PGOOD threshold level. PGOOD goes high when the internal FET's gate is enhanced and $V_{(PGTH)}$ is above $V_{(PGTHR)}$. PGOOD goes low when $V_{(PGTH)}$ goes below $V_{(PGTHF)}$. There is a deglitch of t_{PGOODR}, 1.6 msec (typical) at the rising edge and t_{PGOODR}, 1.6 µs (typical) deglitch on the falling edge of PGOOD indication. PGOOD is a rated for 60 V and can be pulled to IN_SYS or OUT through a resistor. PGTH can be used for setting downstream's supply UVLO levels and PGOOD as enable and disable control.

9.3.4.1 PGTH as VOUT sensing input

The devices use PGTH as the output voltage monitor input. Use PGTH to set the down stream loads UVLO threshold. During a system fault recovery (example: OVP high to low or UVLO low to high) when the internal FET gate control is enabled, the device samples the PGTH information and decides whether to turn ON the FET with fast slew rate or dVdT mode based on the sampled $V_{(PGTH)}$ information. During the fault recovery instance if the $V_{(PGTH)}$ level is above $_{(PGTHF)}$ then the internal FET turns ON within a delay of $t_{OVP(dly\_fast)}$ with fast slew rate (ignores the capacitance connected at dVdT pin) with thermal regulation loop enabled for a duration of $t_{CL(dly)}$. Maximum current through the device during this operation will be limited at $I_{(OL)}$. During the fault recovery instance if the $V_{(PGTH)}$ level is below $V_{(PGTHF)}$ then the device turns ON the internal FET in dVdT mode and the slew rate will depend on the dVdT capacitor value. This way the device distinguishes between real system faults and system transients and the turn ON delay is controlled accordingly. This scheme ensures fast recovery during system tests like voltage interruption and brown-out tests, EMC testing like Electrical Fast Transients (IEC61000-4-4) and Surge (IEC61000-4-5). The fast turn ON during transient recovery feature can be disabled by connecting PGTH to GND. In this case PGOOD will be pulled low.

9.3.5 Input Reverse Polarity Protection (B_GATE, DRV)

The TPS2663x devices support the reverse input polarity protection feature. Connect an N-channel power FET (Q1) with the source to IN_SYS, drain to IN and GATE to B-GATE as shown in Figure 5. This forms a back to back FET topology in power path that is required to protect the load from input reverse polarity faults. Connect an external signal FET (Q2) across BGATE, DRV and IN_SYS. Q2 acts as a pull down gate switch for Q1. In the applications where reverse polarity protection and reverse current blocking is not required then connect IN_SYS and IN together. Leave BGATE and DRV open as shown in Figure 6. Figure 7 illustrates the reverse input polarity protection functionality.

The TPS2663x devices support a maximum differential voltage across $V_{(IN\_SYS)} - V_{(OUT)}$ upto – 90 V. This high voltage transients generally appear during the IEC61000-4-5 surge testing at the $V_{(IN\_SYS)}$. This voltage stress appears across the external N-channel FET. The TPS2663x provides a gate drive (B_GATE) of 12 V (typical). The fast pull down gate switch Q2 pulls down the GATE of the Q1 during reverse current and reverse polarity fault events. Q2 should be atleast 15 V VDS rated FET with a maximum VGS rating of 20 V , Ciss <= 50 pF and VGTH(min) ≤ 3 V.

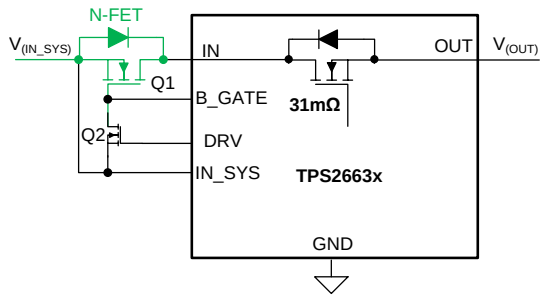


Figure 5. Configuration for Input Reverse Polarity Protection and Reverse Current Blocking

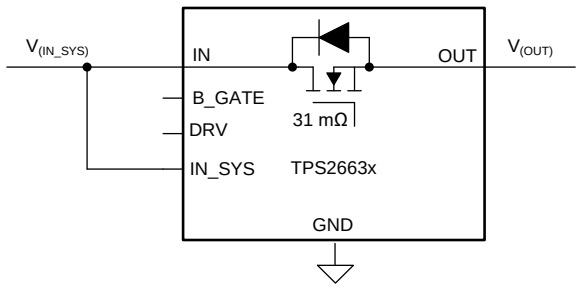


Figure 6. Configuration for Applications Without Input Reverse Polarity Protection and Reverse Current Blocking Requirement

ADVANCE INFORMATION

Feature Description (continued)

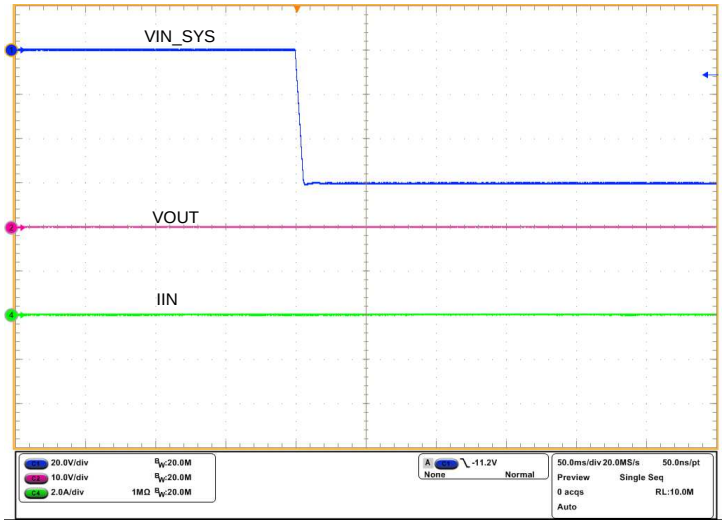


Figure 7. Input Reverse Polarity Response at – 60 V Input

9.3.6 Output Power Limiting, PLIM (TPS26632, TPS26633 and TPS26635 Only)

With a fixed over current limit threshold the power limit profile increases linearly with supply input. Electrical Industrial process control equipment such as PLC CPU needs to comply with standards like IEC61010-1 for fire safety, which require limited energy and power circuits. Limiting the output power becomes a challenge in such high power applications where the operating supply voltage range is wide. The TPS26632, TPS26633 and TPS26635 devices integrate adjustable output power limiting functionality that simplifies the system design requiring compliance in accordance to this standard.

Connect a resistor from PLIM to GND as shown in Figure 8 to program the output power limiting value. If PLIM is connected to GND then PLIM feature is not activated and the device works normally with current limiting set by the external RLIM resistor.

During an over power load event the TPS26632 limits the output power at the programmed value set by PLIM resistor. This indirectly results in the device operation in current limiting mode with steady state output voltage and current set by the load characteristics and $P_{LIM} = V_{OUT} \times I_{OUT}$. The maximum duration for the device to be in power limiting mode is $t_{CL(dly)}$. Post that the device operates either in auto-retry or latch off mode based on MODE pin configuration.

During an over power load event the TPS26633 and TPS26635 allows the extra power for a max duration of $t_{CB(dly)}$. The maximum power during this time is limited to V_{OUT} x2 x I_{OL} where I_{OL} is the over load current limit set by the $R_{(ILIM)}$ resistor. After the $t_{CB(dly)}$ time, the output power gets limited to the value programmed by the PLIM resistor. Set the power limit using Equation 4.

$$P_{(PLIM)} = 1 \times R_{(PLIM)} \quad (4)$$

Here $P_{(PLIM)}$ is output power limit in watts, $R_{(PLIM)}$ is the power limit setting resistor in kΩ. Figure 9 and Figure 10 illustrate output power limiting performance of TPS26632 and TPS26633 devices respectively.

ADVANCE INFORMATION

Feature Description (continued)

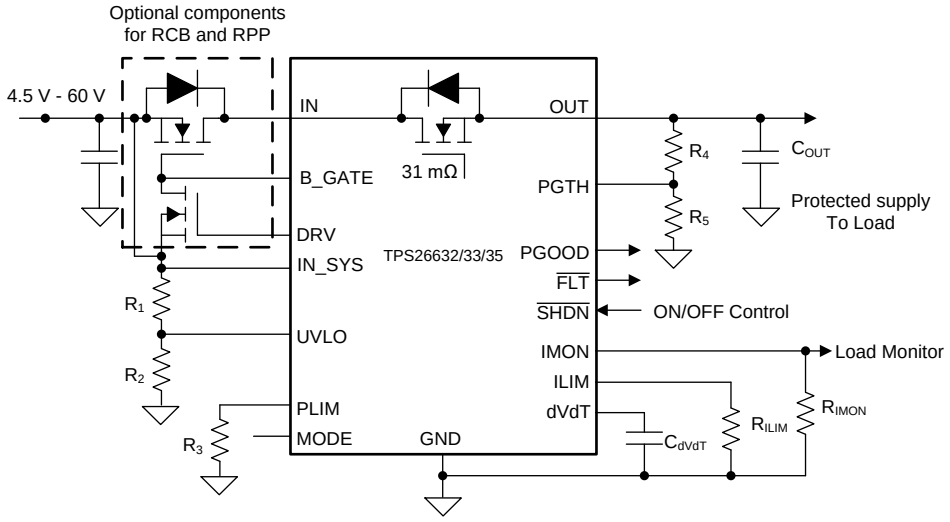
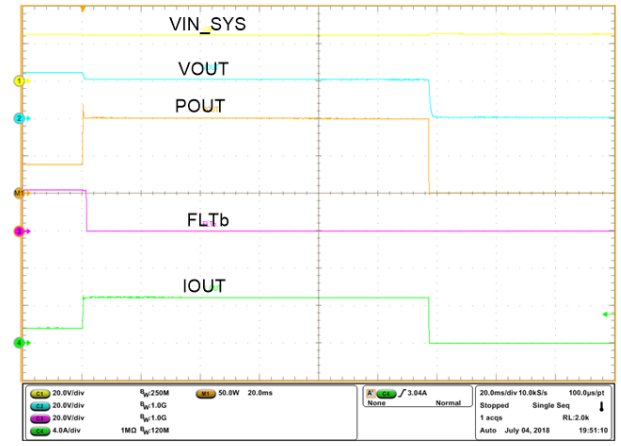
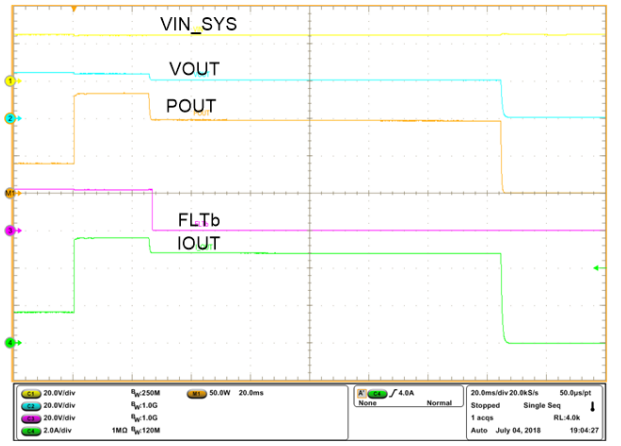


Figure 8. TPS26632, TPS26633 and TPS26635 Typical Application Schematic



R_{PLIM} = 100 kΩ R_{ILIM} = 3 kΩ

Figure 9. Output Power Limiting Response of TPS26630



R_{PLIM} = 100 kΩ R_{ILIM} = 3 kΩ

Figure 10. Output Power Limiting Response of TPS26633

9.3.7 Reverse Current Protection

The device monitors $V_{(IN\_SYS)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected. The reverse comparator turns OFF the external blocking FET Q1 quickly as soon as $V_{(IN\_SYS)} - V_{(OUT)}$ falls below –1 V. The total time taken to turn OFF the FET Q1 in this condition is $t_{RCB(fast\_dly)} + t_{(Driver)}$. The delay due to the driver stage $t_{(Driver)}$ can be calculated using Equation 5.

$$t_{(Driver)} = -RDSON_{(Q2)} \times Ciss_{(Q1)} \times \ln\left(\frac{VGTH_{(Q1)}}{V_{BGATE}}\right) \quad (5)$$

where

- $RDSON_{(Q2)}$ is the on resistance of the fast pull down switch Q2
- $Ciss_{(Q1)}$ is the input capacitance of the blocking FET Q1
- $VGTH_{(Q1)}$ is the GATE threshold voltage of the blocking FET Q1
- V_{BGATE} = 12 V (typical)

ADVANCE INFORMATION

Feature Description (continued)

In a typical system design, $t_{(Driver)}$ is generally 10% to 20% of $t_{RCB(fast\_dly)}$ of 120 nsec (typical).

Figure 11 and Figure 12 illustrates the behavior of the system during input hot short circuit condition. The blocking FET Q1 is turned ON within 1.6 ms (typical) once the differential forward voltage $V_{(IN\_SYS)} - V_{(OUT)}$ exceeds 67 mV (typical).

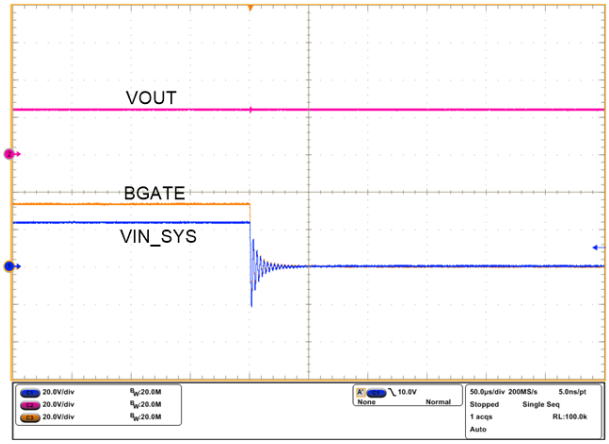


Figure 11. Input Hot Short Functionality at 24-V Supply

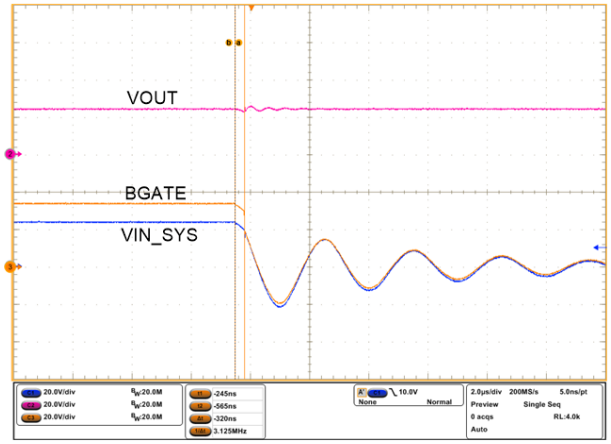


Figure 12. Hot-Short: Fast Trip Response (Zoomed)

The reverse comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the over-drive differential voltage $V_{(IN\_SYS)} - V_{(OUT)}$ over $V_{(REVTH)}$. Higher the over-drive, faster the turn OFF time, $t_{RCB(dly)}$.

9.3.8 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

9.3.8.1 Overload Protection

The TPS2663x devices feature accurate over load current limiting and fast short circuit protection feature. With TPS26630 and TPS26632 if the load current exceeds the programmed current limit I_{OL}, the device regulates the current through it at I_{OL} eventually reducing the output voltage. The power dissipation across the device during this operation will be (V_{IN} –V_{OUT}) x I_{OL} and this could heat up the device and eventually enter into thermal shutdown. The maximum duration for the over current through the FET $t_{CL(dly)}$. If the thermal shutdown occurs before this time the internal FET turns OFF and the subsequent operation (auto-retry or latch OFF) will depend on the MODE pin configuration. Set the current limit using Equation 6

$$I_{OL} = \frac{18}{R_{(ILIM)}} \quad (6)$$

where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ

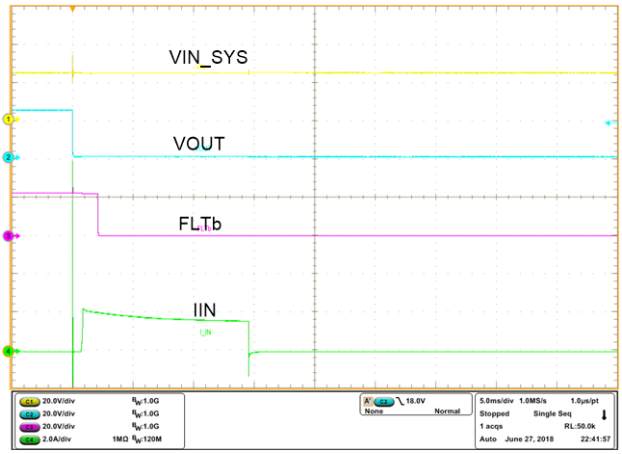
With TPS26631,TPS26633 and TPS26635 if the load current exceeds I_{OL}, then an internal fixed $t_{CB(dly)}$ timer starts. During this time the device will pass through the over current demanded by the load not more than 2 x I_{OL} above which the device will regulate at 2 x I_{OL}. Post $t_{CB(dly)}$ time, the device regulates the current at I_{OL}. The power dissipation across the device during this operation will be (V_{IN}–V_{OUT}) x I_{OL} and this could heat up the device and eventually enter into thermal shutdown. The max duration for the internal FET in current regulation is $t_{CL(dly)}$. The subsequent operation will be based on the MODE setting (either auto-retry or latch OFF).

ADVANCE INFORMATION

Feature Description (continued)

9.3.8.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF $t_{FASTTRIP(dly)}$ = 300 ns (typical) with $I_{(SCP)}$ = 40 A of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{(FASTTRIP)}$. The fasttrip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition. Figure 13 illustrates output hot-short performance of the device.



V_{IN_SYS} = 24 V R_{ILIM} = 9.09 kΩ

Figure 13. Output Hot-Short Response

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the over current level, $I_{(FASTTRIP)}$ through the device. Higher the over current faster the turn OFF time, $t_{FASTTRIP(dly)}$.

9.3.9 Current Monitoring

The current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND.;[terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage range ($V_{(IMONmax)}$) for monitoring the current is limited to minimum of to ensure linear output. This puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by Equation 7.

$$V(IMON) = \left[I(OUT) \times GAIN(IMON)\right] \times R(IMON) \quad (7)$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 27.7 µA/A (Typical)
- $I_{(OUT)}$ is the load current

This pin must not have a bypass capacitor to avoid delay in the current monitoring information.

ADVANCE INFORMATION

Feature Description (continued)

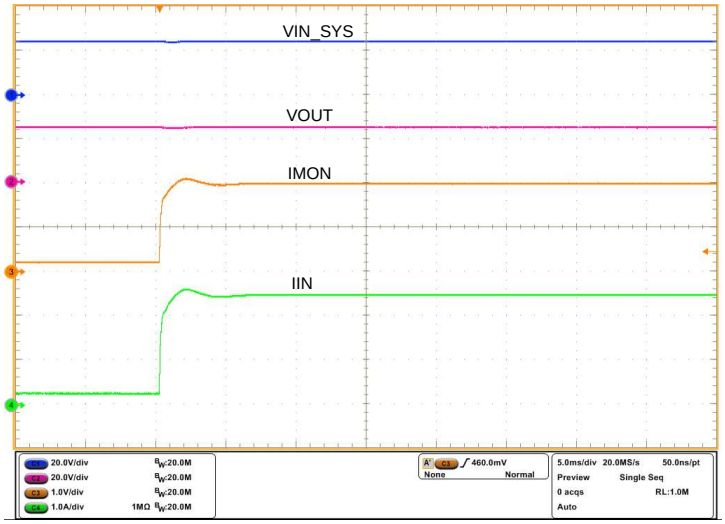


Figure 14. IMON Response During a Load Step

9.3.10 FAULT Response ($\overline{FLT}$)

The $\overline{FLT}$ open-drain output asserts (active low) under the faults events such as undervoltage, overvoltage, over load, power limiting, reverse current and thermal shutdown conditions. The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry. $\overline{FLT}$ can be left open or connected to GND when not used.

9.3.11 IN_SYS, IN, OUT and GND Pins

Connect a minimum of 0.1uF capacitor across IN_SYS and GND. For systems and applications where reverse polarity protection and/or reverse current blocking feature is required

- Connect a N-channel FET between IN_SYS and IN with source of the FET connected to IN_SYS, Drain at IN and GATE to B_GATE.
- Connect a N-channel signal FET with GATE to DRV, Drain to B_GATE, Source to IN_SYS

If the external N-channel FET is not used then connect IN_SYS and IN together and leave B_GATE and DRV pins floating as shown in Figure 7. Do not leave any of the IN and OUT pins un-connected.

9.3.12 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FET, if the junction temperature exceeds $T_{(TSD)}$. After the thermal shutdown event, depending upon the mode of fault response, the device either latches off or commences an auto-retry cycle $t_{(TSD\_retry)}$ after $T_J < [T_{(TSD)} – 11°C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

9.3.13 Low Current Shutdown Control ($\overline{SHDN}$)

The internal and the external FET and hence the load current can be switched off by pulling the $\overline{SHDN}$ pin below 0.8 V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device. The device quiescent current reduces to 22 µA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must sink at least 10 µA at 400 mV. To enable the device, $\overline{SHDN}$ must be pulled up to at least 2 V. Once the device is enabled, the internal FET turns on with dVdT mode.

9.4 Device Functional Modes

The TPS2663x devices respond differently to overload with MODE pin configurations. The operational differences are explained in Table 1.

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Device Functional Modes (continued)

Table 1. Device Operational Differences Under Different MODE Configurations

MODE Pin Configuration	Overload Protection Operation	Device
Open	Active Current limiting at 1x for a maximum duration of $t_{CL\_PLIM(dly)}$. There after Latches OFF. Latch reset by toggling $\overline{SHDN}$ low to high or power cycling IN_SYS	TPS26630, TPS26632
	Active Current limiting at 2x for $t_{CB(dly)}$ duration followed with 1x current limiting for a maximum duration of $t_{CL\_PLIM(dly)}$. There after Latches OFF. Latch reset by toggling $\overline{SHDN}$ low to high or power cycling IN_SYS	TPS26631, TPS26633, TPS26635
Shorted to GND	Active Current limiting at 1x for a maximum duration of $t_{CL\_PLIM(dly)}$. There after auto-retries after a delay of $t_{(TSD\_retry)}$.	TPS26630, TPS26632
	Active Current limiting at 2x for $t_{CB(dly)}$ duration followed with 1x current limiting for a maximum duration of $t_{CL\_PLIM(dly)}$. There after auto-retries after a delay of $t_{(TSD\_retry)}$.	TPS26631, TPS26633, TPS26635

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information: Power Path Protection in a PLC System

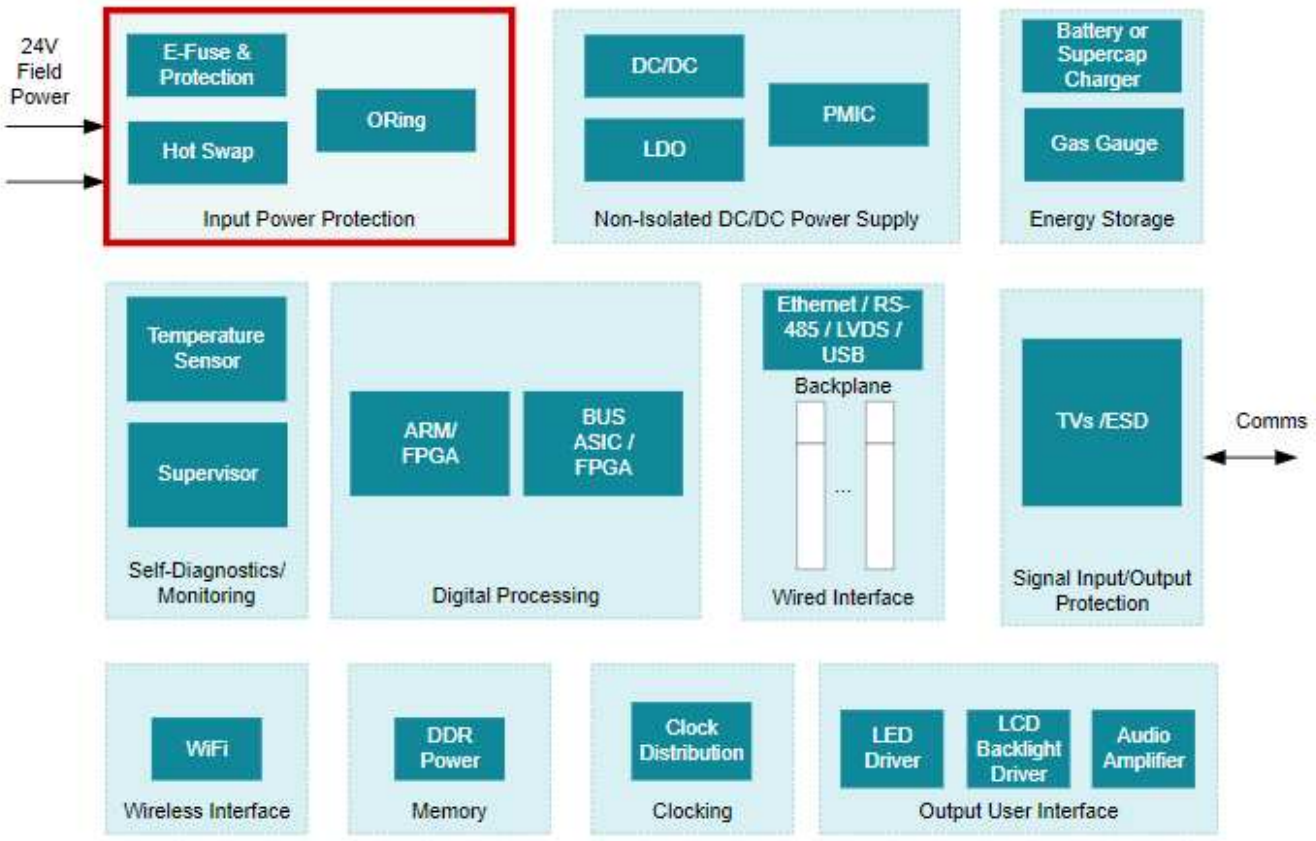

Figure 15. A Typical CPU (PLC Controller) System Block Diagram

The PLC system is usually connected to an external 24-V DC power supply to provide power to the controller unit, backplane, and I/O modules. Input protection circuits are required to protect the PLC from faults such as overvoltage, undervoltage, and overload. Because input supply connectors are screw type, there can always be a possibility of reverse supply connections. Protection circuits should block the reverse polarity to protect the PLC from possible negative voltages. At the same time, every PLC is tested for electrostatic discharge (ESD) according to IEC 61000-4-2, burst pulses (EFT) according to IEC 61000- 4-4, energy single pulse (surge) according to IEC 61000-4-5, and voltage drops and interruptions. Figure 15 shows a system block diagram of PLC controller unit along with the input protection socket. The TPS2663x devices offer a plug and play input protection solution for such applications. For more information about this end equipment refer to the TI application site on *Programmable Logic Controller (PLC), DCS & PAC: CPU (PLC Controller)*.

10.2 Typical Application

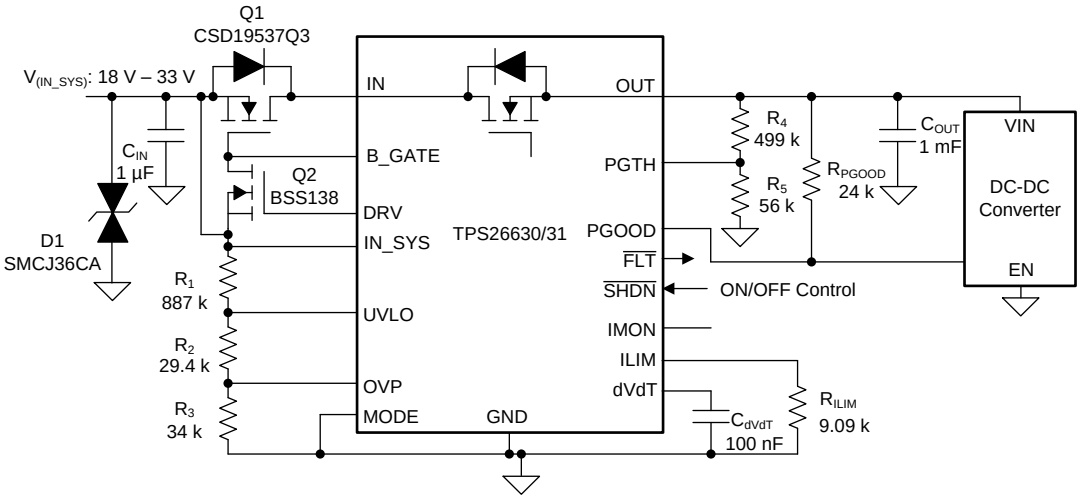

Figure 16. 24-V, 2-A eFuse Input Protection Circuit for Industrial PLC, CNC CPU

10.2.1 Design Requirements

Table 2 shows the Design Requirements for TPS2663x.

Table 2. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Typical input voltage	24 V
$V_{(UV)}$	Undervoltage lockout set point	18 V
$V_{(OV)}$	Overvoltage cutoff set point	33 V
$I_{(LIM)}$	Over load Current limit	2 A
$I_{(INRUSH)}$	Inrush Current limit	500 mA
$P_{(OUT)}$	Output Load	15 W (DC-DC) with 15 V $VINmin_{DC-DC}$
$T_{(FAIL\_TR)}$	Power Interruption time	10 msec
$P_{(Surge)}$	IEC61000-4-5 Surge test level	± 500 V, 2 Ω generator impedance

10.2.2 Detailed Design Procedure

10.2.2.1 Programming the Current-Limit Threshold—$R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using Equation 8.

$$R_{(ILIM)} = \frac{18}{I_{OL}} = 9k\Omega \quad (8)$$

where

- I_{LIM} = 2 A

Choose the closest standard 1% resistor value : $R_{(ILIM)}$ = 9.09 kΩ

10.2.2.2 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between IN_SYS, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 9 and Equation 10.

$$V_{(OVPR)} = \frac{R3}{R1 + R2 + R3} \times V_{(OV)} \quad (9)$$

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$$V_{(UVLOR)} = \frac{R2 + R3}{R1 + R2 + R3} \times V_{(UV)} \quad (10)$$

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)} / (R_1 + R_2 + R_3)$}, it is recommended to use higher value resistance for R_1, R_2 and R_3.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20x greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)}$ = 1.2 V and $V_{(UVLOR)}$ = 1.2 V. From the design requirements, $V_{(OV)}$ is 33 V and $V_{(UV)}$ is 18 V. To solve the equation, first choose the value of R_3 = 34 kΩ and use Equation 9 to solve for (R_1 + R_2) = 916 kΩ. Use Equation 10 and value of (R_1 + R_2) to solve for R_2 = 29.4 kΩ and finally R_1= 887 kΩ.

Choose the closest standard 1% resistor values: R_1 = 887 kΩ, R_2 = 29.4 kΩ, and R_3 = 34 kΩ.

The UVLO and the OVP pins can also be connected to the GND pin to enable the internal default $V_{(OV)}$ = 34.2 V and $V_{(UV)}$ = 15.6 V.

10.2.2.3 Output Buffer Capacitor – C_{OUT}

During the power interruption time T_{FAIL_TR} the output capacitor C_{OUT} of the TPS26630 provides energy to the 15W DC-DC converter load. Use Equation 11 to compute the required buffer capacitor C_{OUT}

$$C_{OUT} = \frac{2 \times P_{(DC-DC)} \times T_{FAIL\_TR}}{V_{(IN\_SYS)}^2 - V_{(UV\_DC-DC)}^2} \quad (11)$$

where

- $P_{(DC-DC)}$ = 15 W/η. Assuming efficiency of 95%, $P_{(DC-DC)}$ = 15.8 W
- T_{FAIL_TR} = 10 msec
- $V_{(IN\_SYS)}$ = 24 V
- $V_{(UV\_DC-DC)}$ = 15 V

C_{OUT} = 0.9 mF. Choose a capacitor with ±10% tolerance, C_{OUT} = 1 mF/35 V electrolytic capacitor. Figure 18 and Figure 19 illustrate the performance during the power interruption tests on TPS26630. Figure 21 illustrate the performance on TPS26631.

10.2.2.4 PGTH Set Point

Set the V_{PGTHF} threshold at the down-stream DC-DC converter UVLO falling threshold. VINmin operating voltage of the DC-DC converter is at 15 V. Assuming UVLO to be at 20% lower level, V_{UVLO_DC-DC} = 12 V. Use Equation 12 to calculate R_4 and R_5.

$$V_{(PGTHF)} = \frac{R_5}{R_4 + R_5} \times V_{UVLO\_DC-DC} \quad (12)$$

$V_{(PGTHF)}$ = 1.14 V. Assuming R_5 = 56 kΩ, R_4 comes out to be approximately 499 kΩ.

10.2.2.5 Setting Output Voltage Ramp Time—(t_{dVdT})

Use Equation 1 and Equation 2 to calculate required $C_{(dVdT)}$ for achieving an inrush current of 500 mA. $C_{(dVdT)}$ = 0.1 µF. Figure 17 illustrates the inrush current limiting performance during 24 V hot-plug in condition.

10.2.2.5.1 Support Component Selections— R_{PGOOD} and $C_{(IN)}$

The R_{PGOOD} serves as pull-up for the open-drain output. The current sink by this pin must not exceed 10 mA (see the *Absolute Maximum Ratings* table). Typical resistance value in the range of 10 kΩ to 100 kΩ is recommended for R_{PGOOD}. Connect PGOOD directly to the EN pin of the DC-DC converter. Figure 20 and Figure 22 illustrate the power up and power down performance of the system respectively. The C_{IN} is a local bypass capacitor to suppress noise at the input. A minimum of 1 µF is recommended for $C_{(IN)}$ for limit the slew rates during the surge test.

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10.2.2.6 Selecting Q1, Q2 and TVS Clamp for Surge Protection

For ± 500 V, 2 Ω surge, typically a SMC sized TVS like SMCJ36CA clamps the voltage around ±55 V. During the negative surge strike, the input voltage V_{IN_SYS}spikes to –55 V. This results in a voltage stress of –(55 V + 24 V) = –79 V across the external blocking FET Q1. Choose at least a 80 V rated N-channel FET. B_GATE drive is in the range of 10 V – 14 V. Select a suitable FET with the target RDSON specified at this gate drive voltage. The fast pull down gate switch Q2 pulls down the GATE of the Q1 during the reverse current event appearing during the surge test. Q2 should be atleast 15 V VDS rated FET with a maximum VGS rating of 20 V , Ciss <= 50 pF and VGTH(min) ≤ 3V. CSD19537Q3 and BSS138 are selected for Q1 and Q2 respectively. Figure 23 and Figure 24 illustrate the performance of the system during the surge testing.

10.2.3 Application Curves

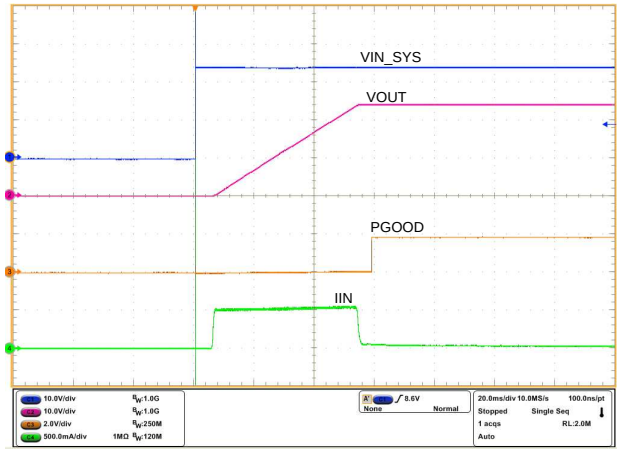

Figure 17. Hot-Plug In at 24 V Supply

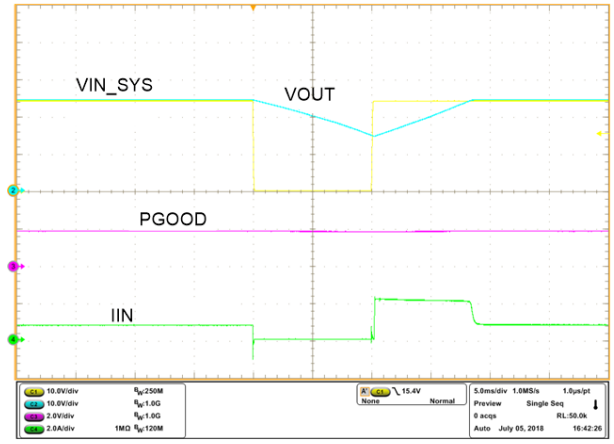

Figure 18. Voltage Interruption Response With TPS26630

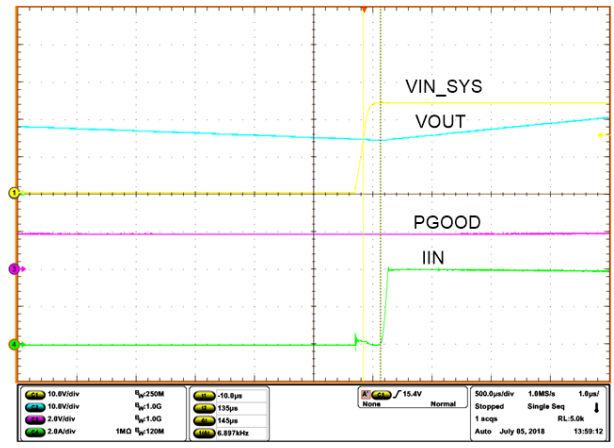

Figure 19. Voltage Interruption Response With TPS26630 (Zoomed)

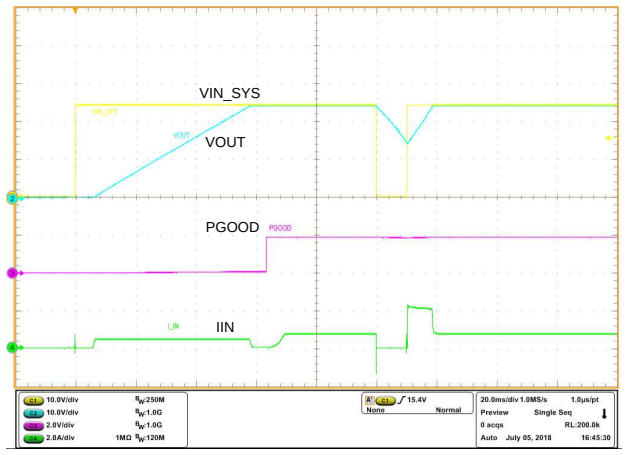

Figure 20. Power Up Followed With Voltage Interruption With TPS26630

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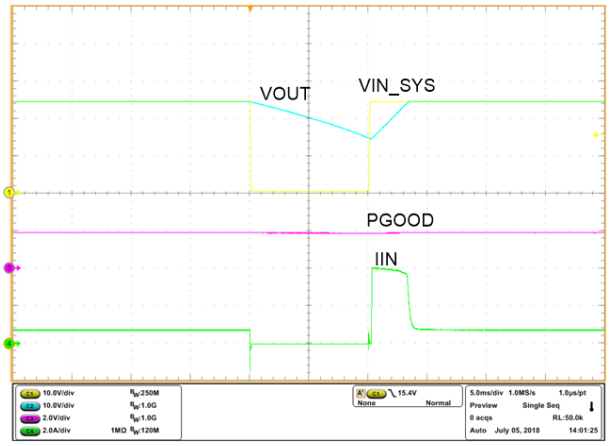

Figure 21. Voltage Interruption Performance With TPS26631

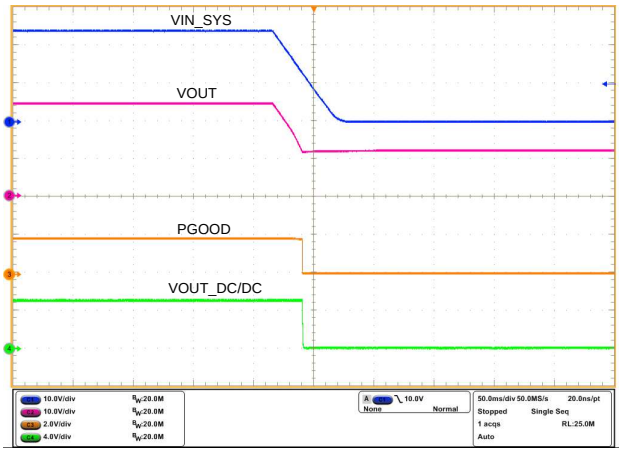

Figure 22. Power Down Response

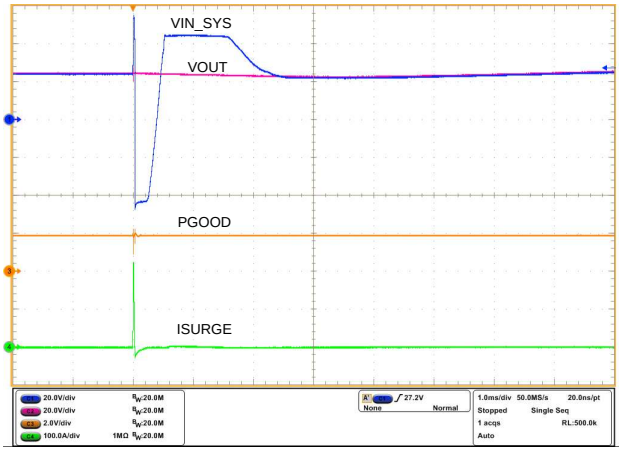

Figure 23. 500 V, 2 Ω Surge Response

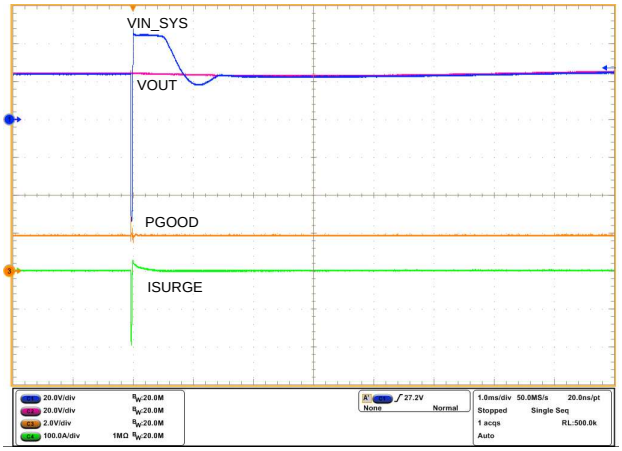

Figure 24. – 500 V, 2 Ω Surge Response

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10.3 System Examples

10.3.1 Simple 24-V Power Supply Path Protection

With the TPS2663x devices, a simple 24-V power supply path protection can be realized using a minimum of five external components as shown in the schematic diagram in Figure 25. The external components required are: a N–Channel Power FET Q_1, a N–Channel signal FET Q_2 and a $R_{(ILIM)}$ resistor to program the current limit, $C_{(IN)}$ and $C_{(OUT)}$ capacitors.

System Examples (continued)

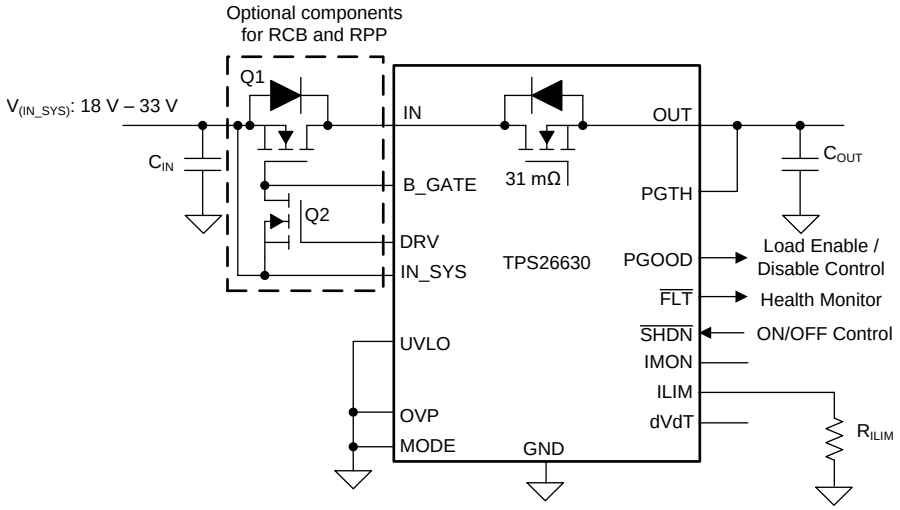

Figure 25. TPS26630 Configured for a Simple 24-V Supply Path Protection

Protection features with this configuration include:

- Load and device protection from reverse input polarity fault down to –60 V (with a 60 V rated Q_1)
- Over Voltage Protection at 34 V
- Inrush current control with 24 V/240 µs output voltage slew rate
- Reverse Current Blocking
- Accurate current limiting with Auto-Retry

10.3.2 Priority Power MUX Operation

Applications having two energy sources such as Portable battery powered equipment require preference of one source to another. For example, mains power (wall-adapter) has the priority over the internal back-up power or auxiliary power. These applications demand for switch over from mains power to backup power only when main input voltage falls below a user defined threshold. The TPS2663x devices provide a simple solution for priority power multiplexing needs.

Figure 26 shows a typical priority power multiplexing implementation using devices. When the MAIN power is present, the device in VIN_MAIN path powers the OUT bus irrespective of whether auxiliary power VIN_AUX is greater than or less than VIN_MAIN. Once the voltage on the VIN_MAIN rail falls below the user-defined threshold, the device VIN_MAIN issues a signal to switch over to auxiliary power VIN_AUX. The transition happens seamlessly in $t_{OVP(dly\_fast)}$), with minimal voltage droop on the output. The voltage droop during transition is a function of load current and output capacitance. See Equation 13.

$$V_{(DROOP)} = \frac{I_{(LOAD)} \times t_{OVP(fast\_dly)}}{C_{(OUT)}} \quad (13)$$

where

- $V_{(DROOP)}$ is in volts, $I_{(LOAD)}$ is load current in Ampere, $C_{(OUT)}$ is output capacitance in µF, $t_{OVP(fast\_dly)}$ = 140 µs (typical)

Figure 27, Figure 28, Figure 29 and Figure 30 show typical switch-over waveforms of Priority Muxing implementation using the TPS26630 or TPS26631 for 20 V Primary and 24 V Auxiliary Bus.

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System Examples (continued)

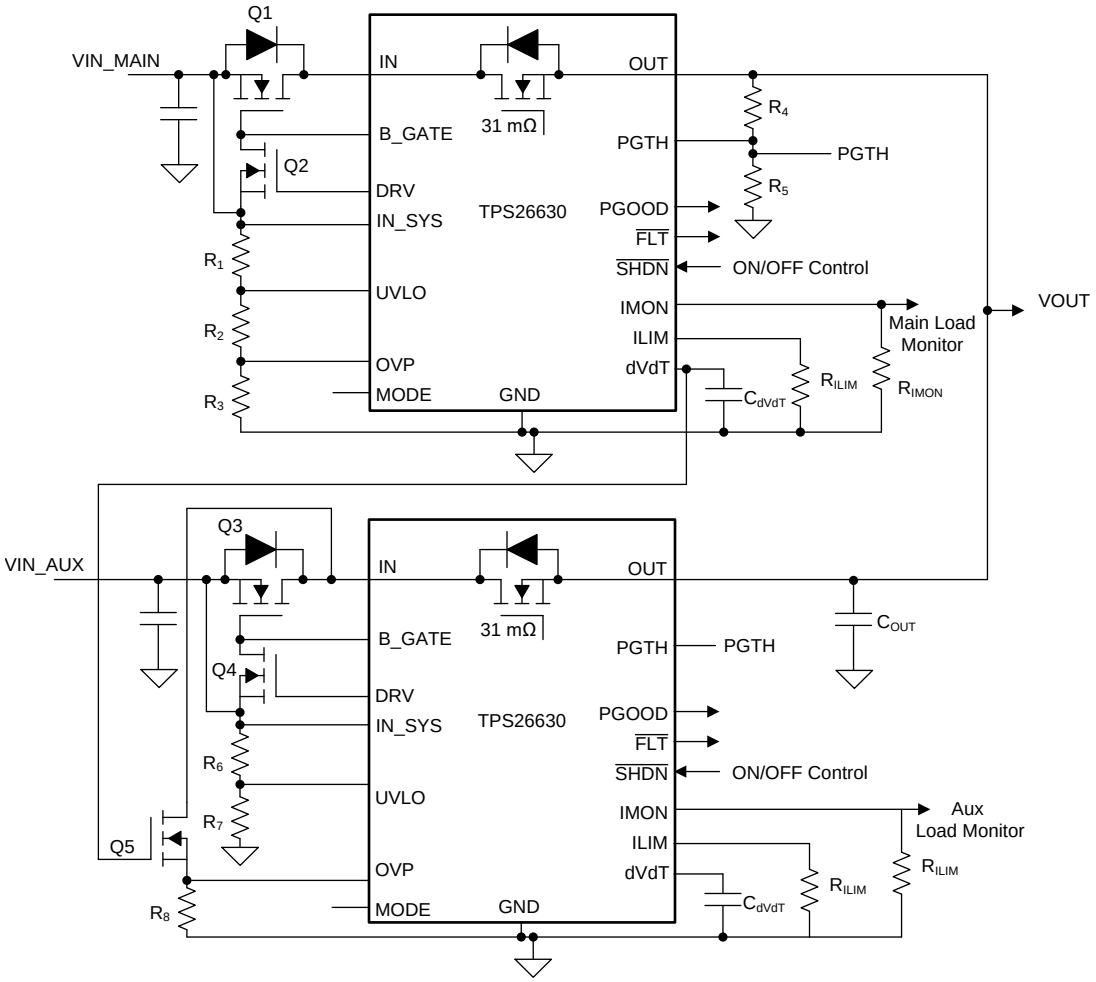

Figure 26. Priority Power Mux Implementation

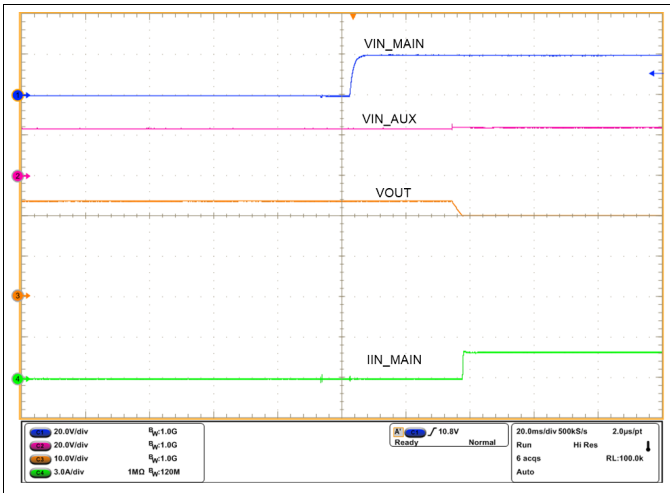

Figure 27. VIN_MAIN Power Recovery: Change Over from Auxiliary VIN_AUX to Primary Power VIN_MAIN

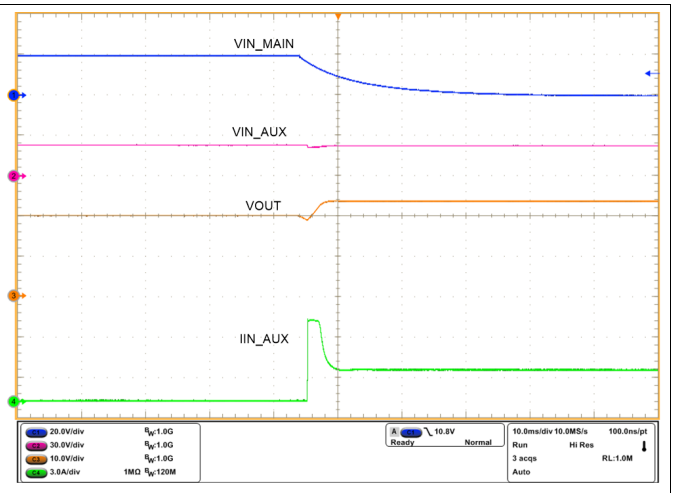

Figure 28. VIN_MAIN Brownout Condition: Change Over from Main VIN_MAIN to Auxiliary Power VIN_AUX

ADVANCE INFORMATION

System Examples (continued)

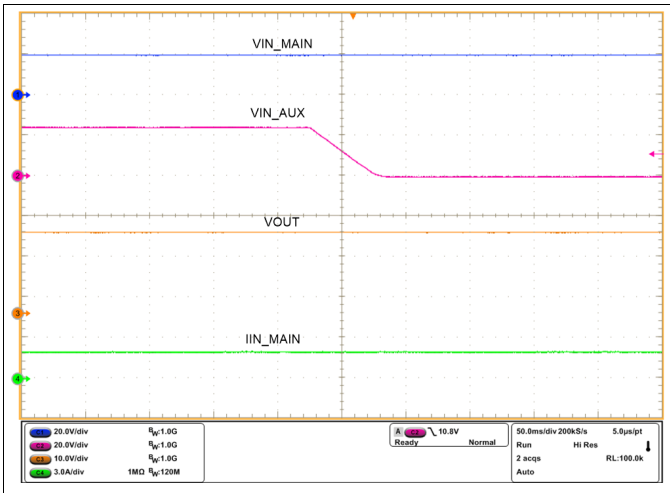

Figure 29. VIN_AUX Brownout Condition

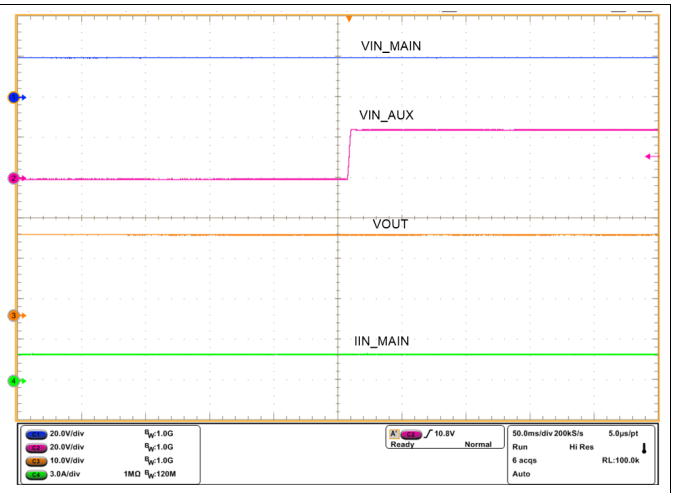

Figure 30. VIN_AUX Power Recovery

10.4 Do's and Don'ts

- In the applications where reverse polarity protection is required do use external FETs Q1 and Q2.
- Connect at least a 300 kΩ resistor across UVLO and IN_SYS in the applications where reverse polarity protection is required.

11 Power Supply Recommendations

The TPS2663x eFuse is designed for the supply voltage range of 4.5 V ≤ V_{IN} ≤ 60 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 14.

$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}}$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source

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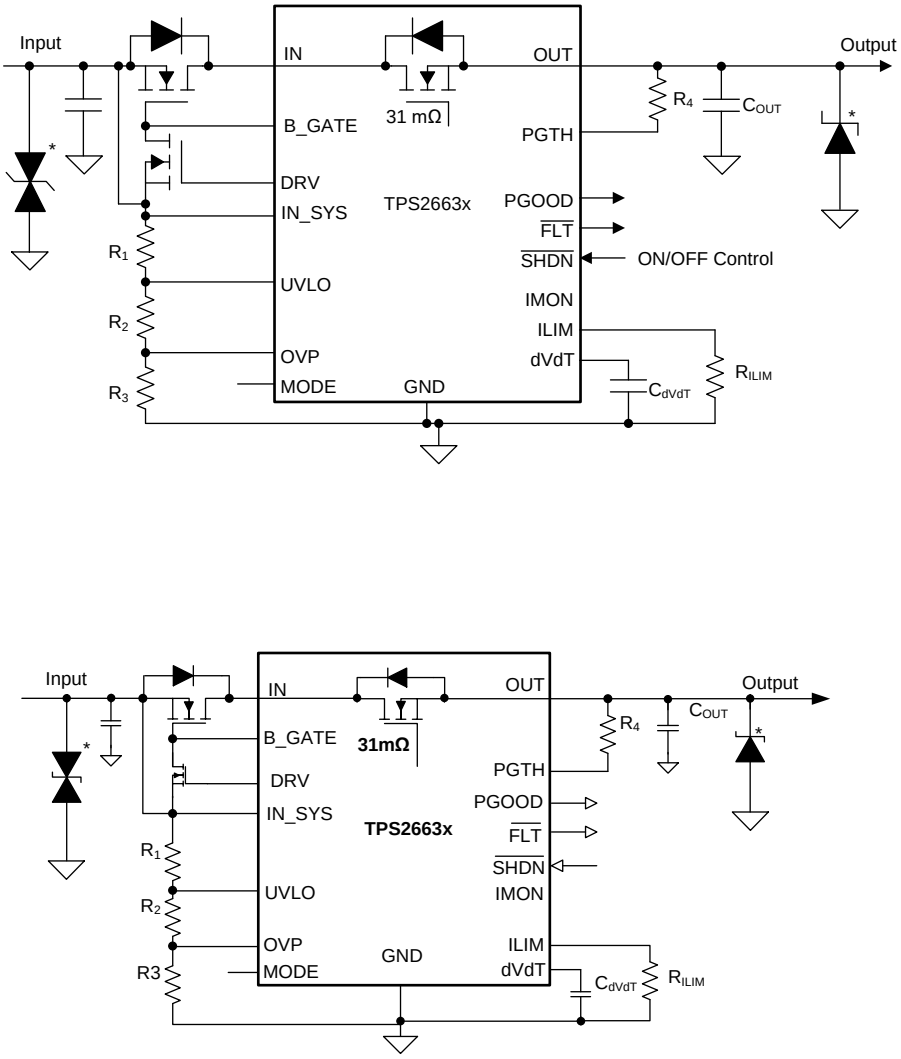
Transient Protection (continued)

- $C_{(IN)}$ is the capacitance present at the input

(14)

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications it is recommended to place at least 1 µF of input capacitor.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 31



* Optional components needed for suppression of transients

Figure 31. Circuit Implementation With Optional Protection Components for TPS2663x

11.2 Application Limitations

This section highlights some limitations in the application which were identified during bench evaluation of the existing TPS2663 silicon on the evaluation module (EVM).

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Application Limitations (continued)

11.2.1 Performance During Start Up With Short on Output

The device does not turn off the internal FET after the thermal regulation max timeout of $t_{(Treg\_timeout)}$, 2.5 sec (typical). The device regulates the junction temperature at $T_{(J\_REG)}$,150 °C (typical) and keeps the internal FET ON.

- Devices affected: All the variants of the TPS2663 Family (TPS26630, TPS26631, TPS26632, TPS26633, TPS26635)

A design fix will be included in the final release of the IC.

11.2.2 Performance of TPS26631, TPS26633 and TPS26635 During Over Load testing

With overload at > 1.5 x I_{OL}, for > 25.5 msec $t_{CB(dly)}$, the device limits the current at 2 x I_{OL} instead of at 1 x I_{OL} for a maximum duration of $t_{CL\_PLIM(dly)}$.

- Devices affected: All the variants of TPS2663 Family (TPS26630, TPS26631 and TPS26635 Only)

A design fix will be included in the final release of the IC.

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12 Layout

12.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN_SYS terminal and GND.
- The external FET Q1 should be placed with DRAIN close to the V_{IN} pins of the IC and connected through a plane. The fast pull down switch Q2 DRAIN and SOURCE should be placed very close to the GATE and SOURCE terminals of Q1 with very short loop. See Figure 32 and Figure 33 for a typical PCB layout example.
- The optimum placement of decoupling capacitor is closest to the IN_SYS and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN_SYS terminal, and the GND terminal of the IC.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- Locate all the TPS2663x family support components $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, UVLO, OVP, PGTH resistors close to their connection pin. Connect the other end of the component to the GND with shortest trace length.
- The trace routing for the R_{ILIM} component to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications.

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12.2 Layout Example

Top Layer

Bottom layer GND plane

Top Layer GND Plane

Via to Bottom Layer

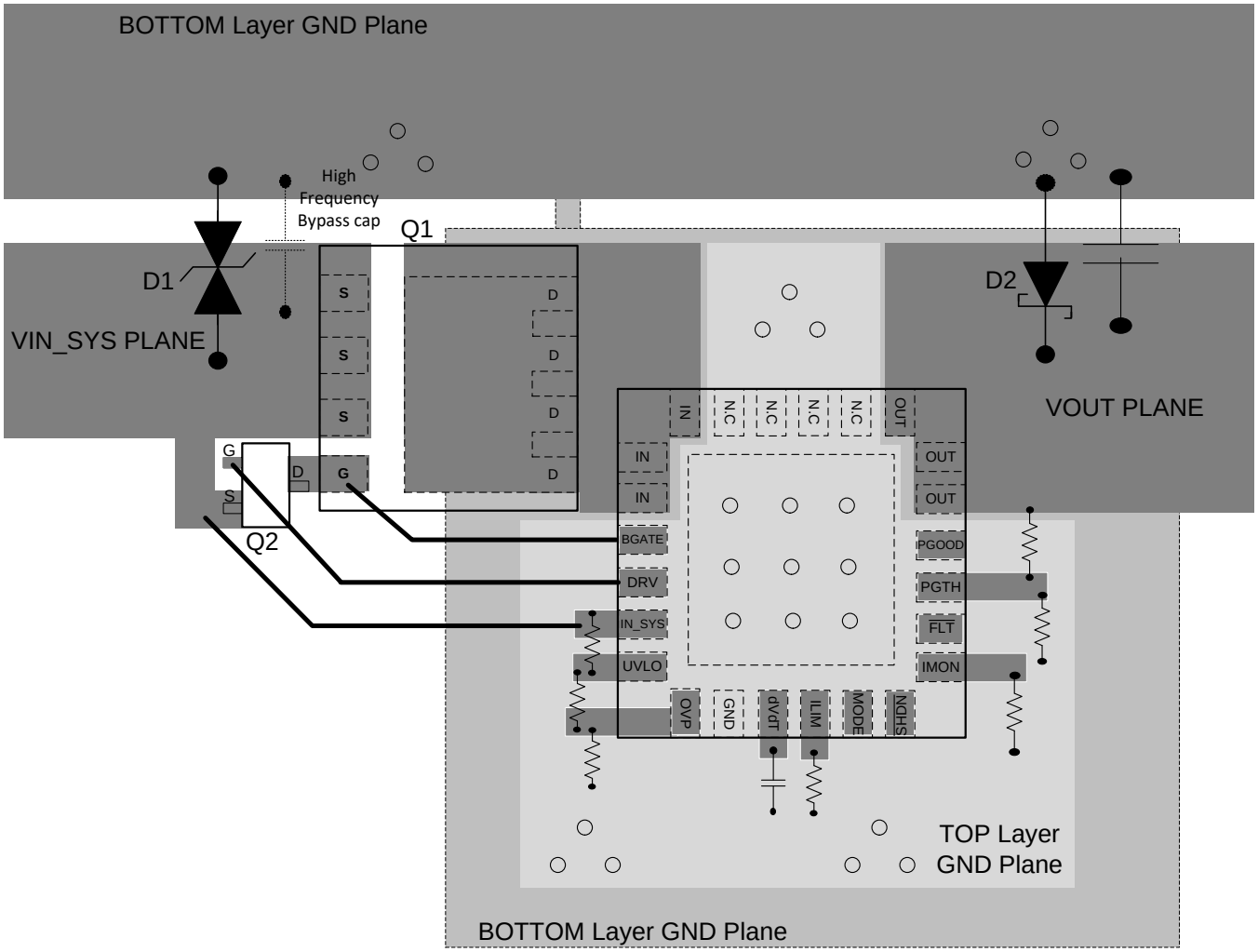

Figure 32. Typical PCB Layout Example With QFN Package With a 2 Layer PCB

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Layout Example (continued)

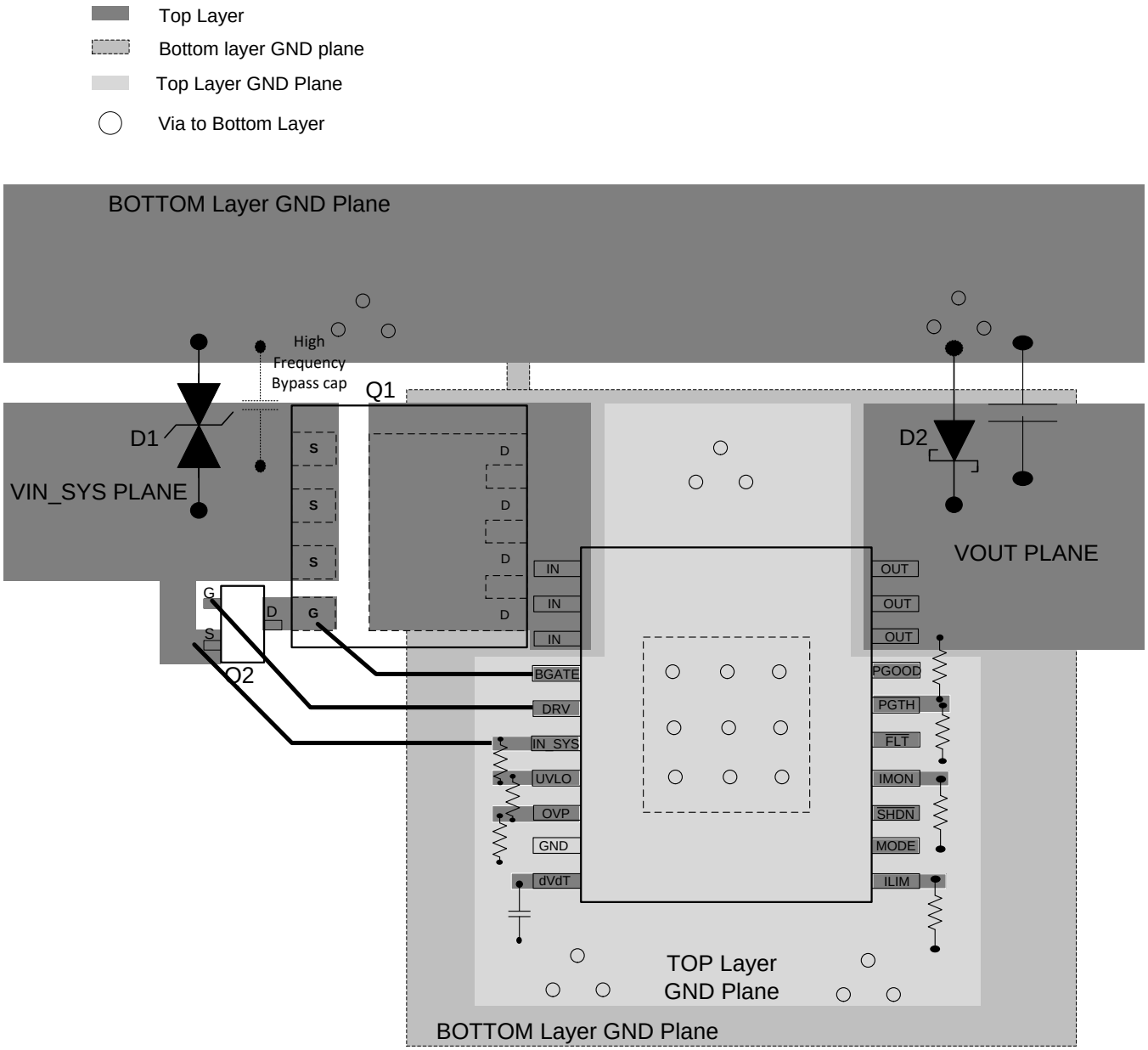


Figure 33. Typical PCB Layout Example With HTSSOP Package With a 2 Layer PCB

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS26630RGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS26631RGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS26632RGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS26633RGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS26635RGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		Samples
TPS26630RGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		
TPS26631RGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		
TPS26632RGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		
TPS26633RGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		
TPS26635RGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

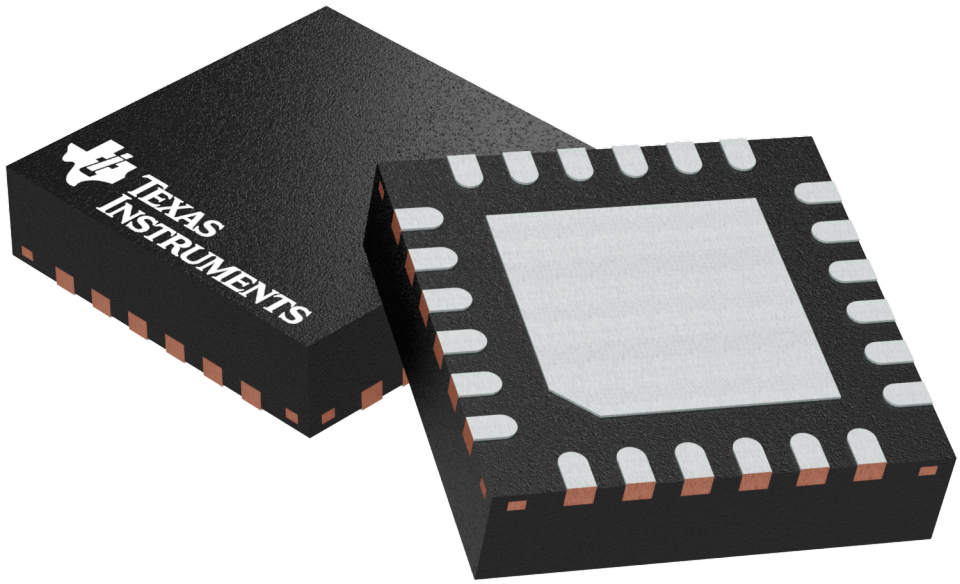
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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