TPS22993 Quad Channel Load Switch with GPIO and I²C Control

1 Features

- Input Voltage: 1.0V to 3.6V
- Low ON-State Resistance (V_{BIAS} = 7.2V)
  - R_{ON} = 15mΩ at V_{IN} = 3.3V
  - R_{ON} = 15mΩ at V_{IN} = 1.8V
  - R_{ON} = 15mΩ at V_{IN} = 1.5V
  - R_{ON} = 15mΩ at V_{IN} = 1.05V
- VBIAS voltage range: 4.5V to 17.2V
  - Suitable for 2S/3S/4S Li-ion Battery Topologies
- 1.2A Max Continuous Current per Channel
- Quiescent Current
  - Single Channel < 9µA
  - All Four Channels < 17µA
- Shutdown Current (all four channels) < 6µA
- Four 1.2V Compatible GPIO Control Inputs
- I²C Configuration (per channel)
  - On/Off Control
  - Programmable Slew Rate Control (5 options)
  - Programmable ON-delay (4 options)
  - Programmable Output Discharge (4 options)
- I²C SwitchALL™ Command for Multi-channel/Multi-chip Control
- QFN-20 package, 3mm x 3mm, 0.75mm height

2 Applications

- Ultrabook™
- Ultrathin PC
- Notebook PC
- Tablets
- Servers
- All-In-One PC

3 Description

The TPS22993 is a multi-channel, low R_{ON} load switch with user programmable features. The device contains four N-channel MOSFETs that can operate over an input voltage range of 1.0V to 3.6V. The switch can be controlled by I²C making it ideal for usage with processors that have limited GPIO available. The rise time of the TPS22993 device is internally controlled in order to avoid inrush current. The TPS22993 has five programmable slew rate options, four ON-delay options, and four quick output discharge (QOD) resistance options.

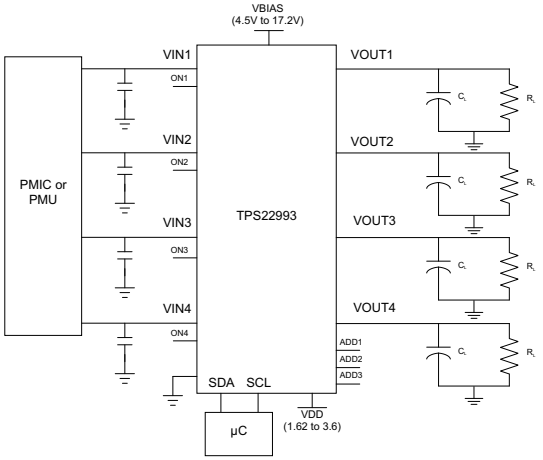
The channels of the device can be controlled via either GPIO or I²C. The default mode of operation is GPIO control through the ONx terminals. The I²C slave address terminals can be tied high or low to assign seven unique device addresses.

The TPS22993 is available in a space-saving RLW package (0.4mm pitch) and is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS22993PRLWR	WQFN (20)	3mm x 3mm

4 Simplified Schematic



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5 Revision History

Changes from Original (November 2013) to Revision A	Page
• Revised document to full version.	1

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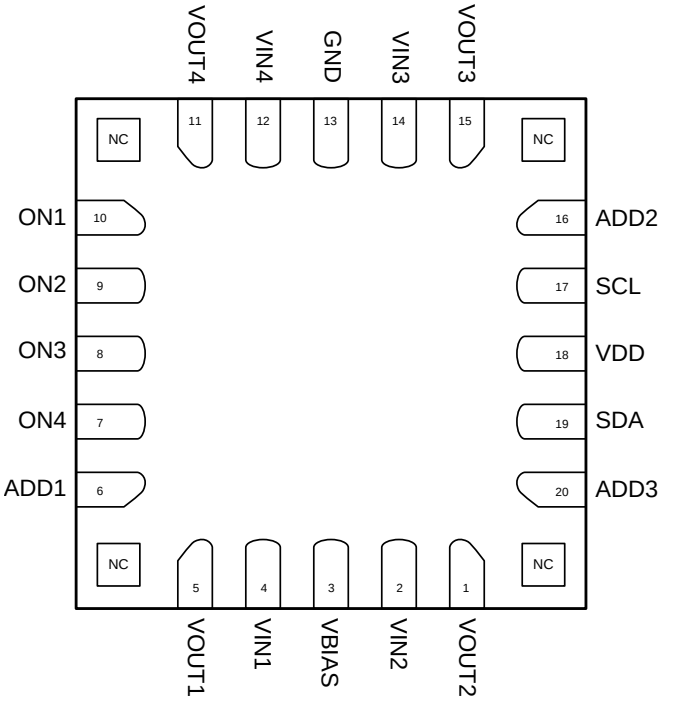
Device Comparison Table

TPS22993	
R_{ON} TYPICAL AT 3.3 V (V_{BIAS} = 7.2V)	15 mΩ
RISE TIME(1)	Programmable
ON DELAY (1)	Programmable
QUICK OUTPUT DISCHARGE(1)(2)	Programmable
MAXIMUM OUTPUT CURRENT (per channel)	1.2 A
GPIO ENABLE	Active High
OPERATING TEMP	–40°C to 85°C

(1) See Application Information section.
(2) This feature discharges output of the switch to GND through an internal resistor, preventing the output from floating. See Application information section.

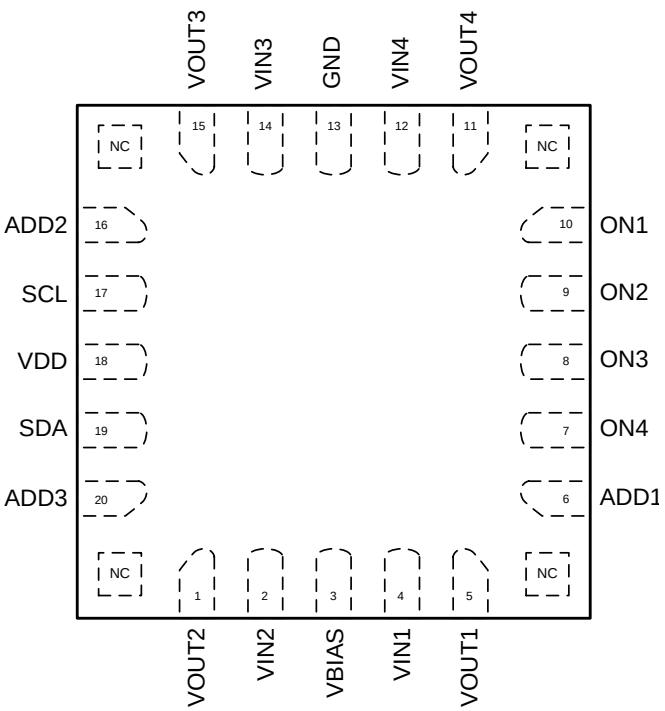
6 Terminal Configuration and Functions

Bottom View



20-RLW (3mm x 3mm x 0.75mm)

Top View



20-RLW (3mm x 3mm x 0.75mm)

Terminal Functions

Terminal		I/O	DESCRIPTION
NO.	NAME		
NC	NO CONNECT	-	Attached terminal to PCB. Leave the terminals floating or tie to GND.
1	VOUT2	O	Channel 2 output.
2	VIN2	I	Channel 2 input.
3	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this terminal is 5.2V to 14V. See Application Information section.
4	VIN1	I	Channel 1 input.
5	VOUT1	O	Channel 1 output.
6	ADD1	I	Device address terminal. Tie high or low. See Application Information section.
7	ON4	I	Active high channel 4 control input. Do not leave floating.
8	ON3	I	Active high channel 3 control input. Do not leave floating.
9	ON2	I	Active high channel 2 control input. Do not leave floating.
10	ON1	I	Active high channel 1 control input. Do not leave floating.
11	VOUT4	O	Channel 4 output.
12	VIN4	I	Channel 4 input.
13	GND	-	Device ground.
14	VIN3	I	Channel 3 input.
15	VOUT3	O	Channel 3 output.
16	ADD2	I	Device address terminal. Tie high or low. See Application Information section.
17	SCL	I	Serial clock input.
18	VDD	I	I^2C device supply input. Tie this terminal to the I^2C SCL/SDA pull-up voltage. See Application Information section.
19	SDA	I/O	Serial data input/output.
20	ADD3	I	Device address terminal. Tie high or low. See Application Information section.

7 Specifications

7.1 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{INx}	Input voltage for VIN1, VIN2, VIN3, VIN4	1.0	3.6	V
V_{BIAS}	Supply voltage for VBIAS	4.5	17.2	V
V_{DD}	Supply voltage for VDD	1.62	3.6	V
V_{ADDx}	Input voltage for ADD1, ADD2, ADD3	0	3.6	V
V_{ONx}	Input voltage for ON1, ON2, ON3, ON4	0	5	V
V_{OUTx}	Output voltage for VOUT1, VOUT2, VOUT3, VOUT4	0	V_{INx}	V
C_{INx}	Input capacitor on VIN1, VIN2, VIN3, VIN4	1 (1)		µF

(1) Refer to application section.

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7.2 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT[2]
		MIN	MAX	
V_{INx}	Input voltage for VIN1, VIN2, VIN3, VIN4	–0.3	4	V
V_{BIAS}	Supply voltage for VBIAS	–0.3	20	V
V_{OUTx}	Output voltage for VOUT1, VOUT2, VOUT3, VOUT4	–0.3	4	V
V_{DD}, V_{SCL}, V_{SDA}, V_{ADDx}	Input voltage for VDD, SCL, SDA, ADD1, ADD2, ADD3	–0.3	4	V
V_{ONx}	Input voltage for ON1, ON2, ON3, ON4	–0.3	6	V
I_{MAX}	Maximum continuous switch current per channel		1.2	A
T_A	Operating free-air temperature[3]	–40	85	°C
T_J	Maximum junction temperature	125	125	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [TA(max)] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [PD(max)], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

7.3 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature		–65	150	°C
ESD[1]	Electrostatic discharge protection	Human-Body Model (HBM)[2]		2000	V
		Charged-Device Model (CDM)[3]		500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

THERMAL METRIC[1][2]		TPS22993 RLW (20 TERMINALS)	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance	58	°C/W
$\Theta_{JC(top)}$	Junction-to-case(top) thermal resistance	24	
Θ_{JB}	Junction-to-board thermal resistance	10	
Ψ_{JT}	Junction-to-top characterization parameter	0.7	
Ψ_{JB}	Junction-to-board characterization parameter	10	
$\Theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

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7.5 Electrical Characteristics

The specification applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (Full) (unless otherwise noted). Typical values are for T_A = 25°C. V_{BIAS} = 7.2V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES CURRENTS AND LEAKAGES								
$I_{Q, VBIAS}$	Quiescent current for VBIAS (all four channels)	$I_{OUT1,2,3,4}$ = 0 A, $V_{IN1,2,3,4}$ = 3.6 V, $V_{ON1,2,3,4}$ = 3.6 V, V_{DD} = 0 V	V_{BIAS} = 4.5V	Full		14.8	26	µA
			V_{BIAS} = 5.2V			14.9	26	
			V_{BIAS} = 7.2V			16.2	28	
			V_{BIAS} = 10.8V			16.6	30	
			V_{BIAS} = 12.6V			16.7	30	
			V_{BIAS} = 17.2V			16.8	30	
	Quiescent current for VBIAS (single channel)	$I_{OUT1,2,3,4}$ = 0A, V_{IN1} = V_{ON1} = 3.6V, $V_{IN2,3,4}$ = $V_{ON2,3,4}$ = 0V, V_{DD} = 0V	V_{BIAS} = 4.5V	Full		7.7	15	µA
			V_{BIAS} = 5.2V			7.8	15	
			V_{BIAS} = 7.2V			8.5	16	
			V_{BIAS} = 10.8V			8.7	16	
			V_{BIAS} = 12.6V			8.8	16	
			V_{BIAS} = 17.2V			8.9	16	
$I_{Q, VDD}$	Quiescent current for VDD	$I_{OUT1,2,3,4}$ = 0A, $V_{IN1,2,3,4}$ = $V_{ON1,2,3,4}$ = 3.6V, f_{SCL} = 0Hz	V_{DD} = 1.8V	Full		0.6	2	µA
			V_{DD} = 3.6V			1.2	2	
$I_{DYN, VDD}$	Average dynamic current for VDD during I^2C communication	$I_{OUT1,2,3,4}$ = 0A, $V_{IN1,2,3,4}$ = $V_{ON1,2,3,4}$ = 3.6V, f_{SCL} = 1MHz	V_{DD} = 1.8V	Full			20	µA
			V_{DD} = 3.6V				35	
$I_{DYN, VBIAS}$	Average dynamic current for VBIAS (all four channels) during I^2C communication	$I_{OUT1,2,3,4}$ = 0A, $V_{IN1,2,3,4}$ = $V_{ON1,2,3,4}$ = 3.6V, f_{SCL}=1MHz	V_{BIAS} = 5.2V	Full			85	µA
			V_{BIAS} = 7.2V				85	
			V_{BIAS} = 10.8V				85	
			V_{BIAS} = 12.6V				85	
	Average dynamic current for VBIAS (single channel) during I^2C communication	$I_{OUT1,2,3,4}$ = 0A, V_{IN1} = V_{ON1} = 3.6V, $V_{IN2,3,4}$ = $V_{ON2,3,4}$ = 0V, f_{SCL}=1MHz	V_{BIAS} = 5.2V	Full			75	µA
			V_{BIAS} = 7.2V				75	
			V_{BIAS} = 10.8V				75	
			V_{BIAS} = 12.6V				75	
$I_{SD, VBIAS}$	Shutdown current for VBIAS (all four channels)	$V_{ON1,2,3,4}$ = 0V, $V_{OUT1,2,3,4}$ = 0V, V_{DD} = 3.6V, V_{BIAS} = 17.2V		Full		5.7	13	µA
$I_{SD, VDD}$	Shutdown current for VDD	$V_{ON1,2,3,4}$ = 0V, $V_{OUT1,2,3,4}$ = 0V, V_{DD} = 3.6V		Full		1.2	2	µA
$I_{SD, VINx}$	Shutdown current for VINx	V_{ONx} = 0V, V_{OUTx} = 0V, V_{DD} = 3.6V	V_{INx} = 3.3V	Full		0.009	4	µA
			V_{INx} = 1.8V			0.006	3	
			V_{INx} = 1.5V			0.006	3	
			V_{INx} = 1.05V			0.006	2.5	
I_{ONx}	Leakage current for ONx	V_{ONx} = 5V		Full		0.01	0.1	µA
I_{ADDx}	Leakage current for ADDx	V_{ADDx} = 3.6V		Full		0.01	0.2	µA
I_{SCL}	Leakage current for SCL	V_{SCL} = 3.6V		Full		0.01	0.2	µA
I_{SDA}	Leakage current for SDA	V_{SDA} = 3.6V		Full		0.01	0.2	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	On-state resistance	V_{BIAS} = 7.2V, I_{OUT} = –200mA	V_{IN} = 3.3V	25°C		15	20	mΩ
				Full			22	
			V_{IN} = 2.5V	25°C		15	20	mΩ
				Full			22	
			V_{IN} = 1.8V	25°C		15	20	mΩ
				Full			22	
			V_{IN} = 1.5V	25°C		15	20	mΩ
				Full			22	
			V_{IN} = 1.05V	25°C		15	20	mΩ
				Full			22	

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Electrical Characteristics (continued)

The specification applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (Full) (unless otherwise noted). Typical values are for T_A = 25°C. V_{BIAS} = 7.2V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
R_{ON}	On-state resistance	V_{BIAS} = 5.2V, I_{OUT} = –200mA	V_{IN} = 3.3V	25°C		18	25	mΩ
				Full			28	
			$_{VIN}$ = 2.5V	25°C		16	22	mΩ
				Full			24	
			V_{IN} = 1.8V	25°C		15	20	mΩ
				Full			23	
			V_{IN} = 1.5V	25°C		15	20	mΩ
				Full			22	
			V_{IN} = 1.05V	25°C		15	20	mΩ
				Full			22	
R_{PD}	Output pulldown resistance	V_{IN} = 3.3V, V_{ON} = 0V, I_{OUT} = 1mA, QOD[1:0] = 00		25°C		110		Ω
		V_{IN} = 3.3V, V_{ON} = 0V, I_{OUT} = 1mA, QOD[1:0] = 01		25°C		483		
		V_{IN} = 3.3V, V_{ON} = 0V, I_{OUT} = 1mA, QOD[1:0] = 10		25°C		949		
		V_{IN} = 3.3V, V_{ON} = 0V, I_{OUT} = 1mA, QOD[1:0] = 11				No QOD		
THRESHOLD CHARACTERISTICS								
$V_{IH,\ ADDx}$	High-level input voltage for ADDx			Full	0.7×V_{DD}		V_{DD}	V
$V_{IL,\ ADDx}$	Low-level input voltage for ADDx			Full	0		0.3×V_{DD}	V
$V_{IH,\ ONx}$	High-level input voltage for ONx			Full	1.05		5	V
$V_{IL,\ ONx}$	Low-level input voltage for ONx			Full	0		0.4	V
$V_{HYS,\ ONx}$	Hysteresis for ONx	V_{BIAS} = 5.2V		Full		130		mV
		V_{BIAS} = 7.2V				130		
		V_{BIAS} = 10.8V				130		
		V_{BIAS} = 12.6V				130		
I²C CHARACTERISTICS								
f_{SCL} (1)	Clock frequency			Full			1	MHz
$t_{SU,\ SDA}$ (1)	Setup time for SDA	f_{SCL} = 1MHz (fast mode plus)		Full	50			ns
$t_{HD,\ SDA}$ (1)	Hold time for SDA			Full	0			ns
$I_{OL,\ SDA}$	SDA output low current	$V_{OL,SDA}$ = 0.4V		25°C		8		mA
$V_{IH,\ SDA}$	High-level input voltage for SDA			Full	0.7×V_{DD}		V_{DD}	V
$V_{IH,\ SCL}$	High-level input voltage for SCL			Full	0.7×V_{DD}		V_{DD}	V
$V_{IL,\ SDA}$	Low-level input voltage for SDA			Full	0		0.3×V_{DD}	V
$V_{IL,\ SCL}$	Low-level input voltage for SCL			Full	0		0.3×V_{DD}	V

(1) Parameter verified by design.

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7.6 Switching Characteristics

Values below are typical values at T_A = 25°C. V_{BIAS} = 7.2V (unless otherwise noted).

PARAMETER		TEST CONDITION		VIN VOLTAGE				UNIT
				3.3V	1.8V	1.5V	1.05V	
t_{ON}	VOUTx turn-on time	V_{BIAS} = 7.2V, R_L=10Ω, C_L=0.1µF, QOD[1:0] = 10, ON-delay[6:5] = 00	Slew rate[4:2] = 000	11	11	11	11	µs
			Slew rate[4:2] = 001	247	181	167	146	
			Slew rate[4:2] = 010	416	302	279	243	
			Slew rate[4:2] = 011	761	549	505	438	
			Slew rate[4:2] = 100	1481	1066	980	848	
t_{OFF}	VOUTx turn-off time	V_{BIAS} = 7.2V, R_L=10Ω, C_L=0.1µF, QOD[1:0] = 10, ON-delay[6:5] = 00		2	2	2	2	µs
t_R	VOUTx rise time	V_{BIAS} = 7.2V, R_L=10Ω, C_L=0.1µF, QOD[1:0] = 10, ON-delay[6:5] = 00	Slew rate[4:2] = 000	2	1.1	1	0.8	µs
			Slew rate[4:2] = 001	307	203	180	147	
			Slew rate[4:2] = 010	527	346	307	248	
			Slew rate[4:2] = 011	970	638	566	459	
			Slew rate[4:2] = 100	1898	1245	1105	888	
t_F	VOUTx fall time	V_{BIAS} = 7.2V, R_L=10Ω, C_L=0.1µF, QOD[1:0] = 10, ON-delay[6:5] = 00		2	2	2	2	µs
t_D	VOUTx ON delay time	V_{BIAS} = 7.2V, R_L=10Ω, C_L=0.1µF, QOD[1:0] = 10, Slew rate[6:5] = 000	ON delay[4:2] = 00	11	11	11	11	µs
			ON delay[4:2] = 01	102	104	105	106	
			ON delay[4:2] = 10	324	332	334	338	
			ON delay[4:2] = 11	923	946	953	965	

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7.7 Typical Characteristics

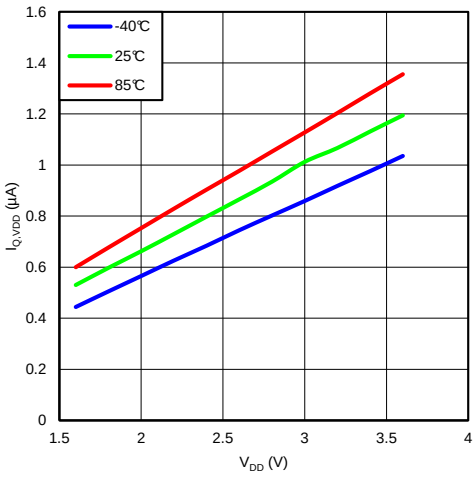

Figure 1. $I_{Q,VDD}$ vs. V_{DD}

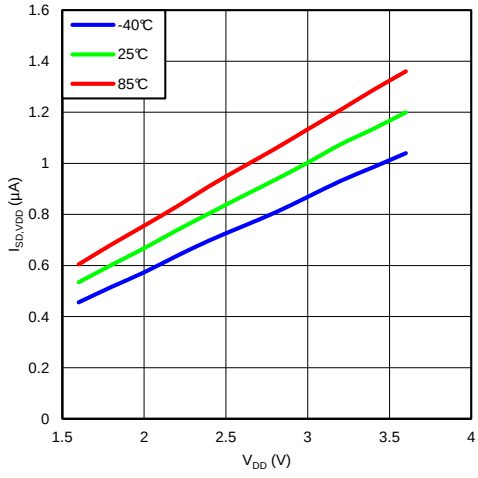

Figure 2. $I_{SD,VDD}$ vs. V_{DD}

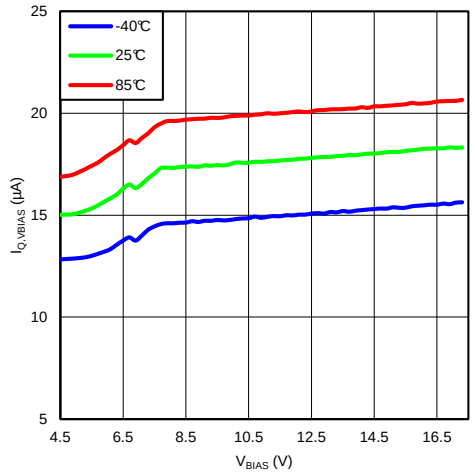

Figure 3. $I_{Q,VBIAS}$ vs. V_{BIAS} (all channels)

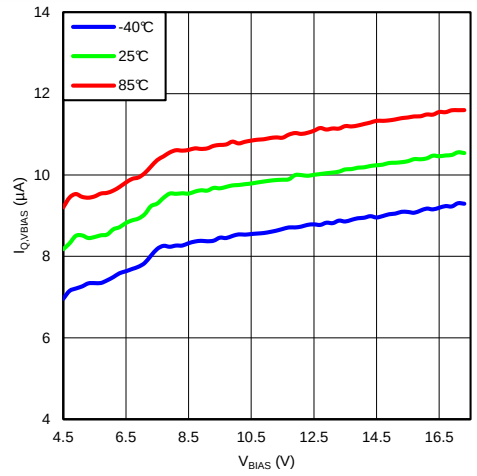

Figure 4. $I_{Q,VBIAS}$ vs. V_{BIAS} (single channel)

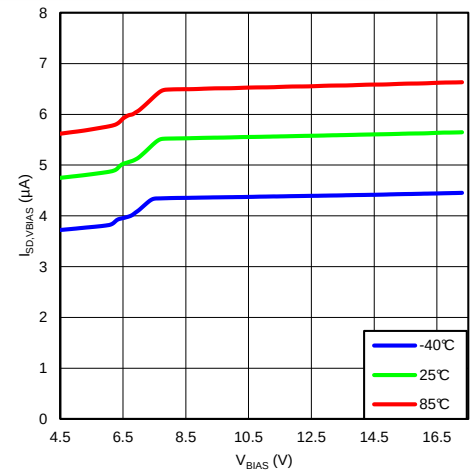

Figure 5. $I_{SD,VBIAS}$ vs. V_{DD}

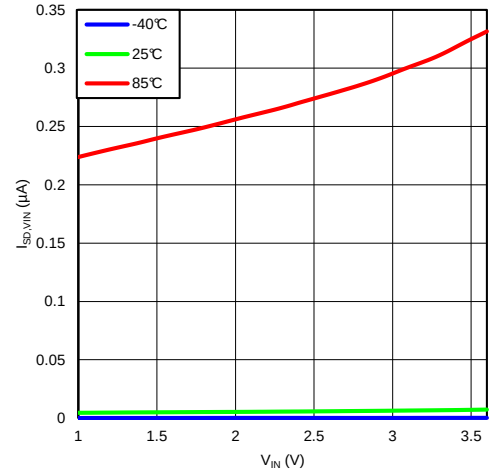

Figure 6. $I_{SD,VIN}$ vs. V_{IN}

Typical Characteristics (continued)

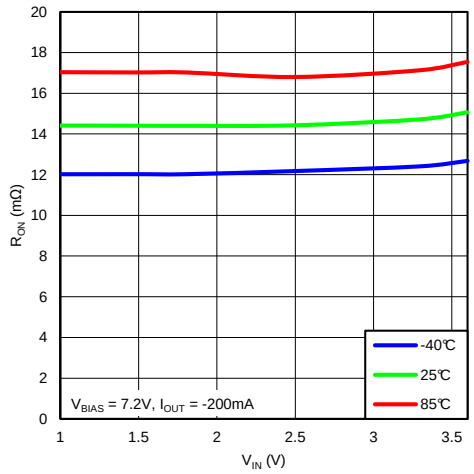

Figure 7. R_{ON} vs. V_{IN} (V_{BIAS} = 7.2V)

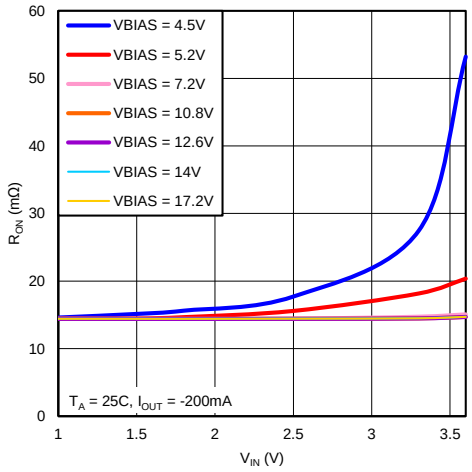

Figure 8. R_{ON} vs. V_{IN} vs. V_{BIAS} (T_A = 25°C)

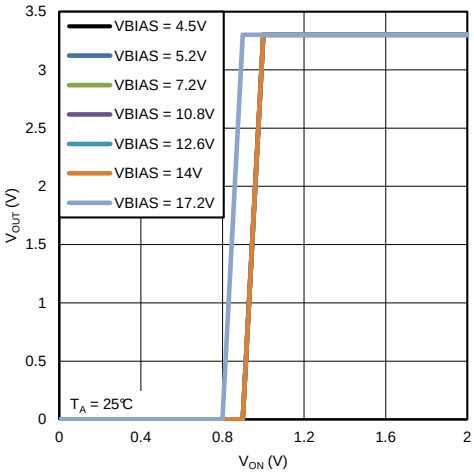

Figure 9. Output voltage vs. VOUT rising

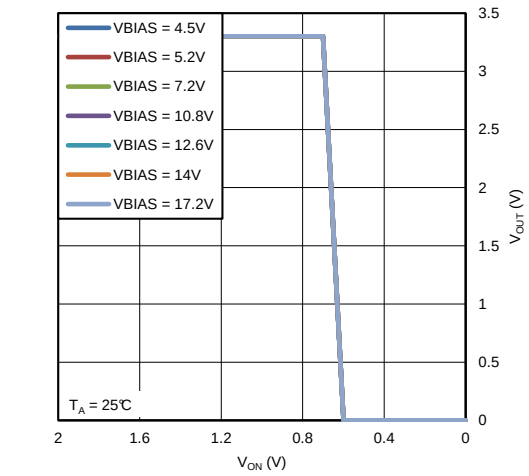

Figure 10. Output voltage vs. VOUT falling

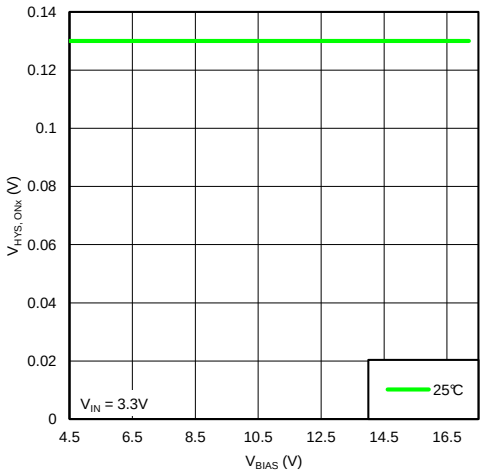

Figure 11. $V_{HYS, ONx}$ vs. V_{BIAS}

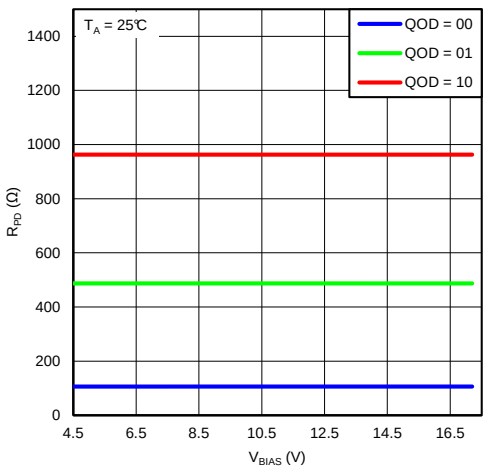

Figure 12. R_{PD} vs. V_{BIAS}

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Typical Characteristics (continued)

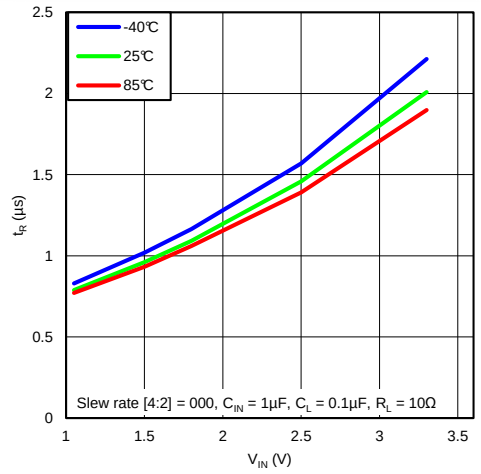

Figure 13. t_R vs. V_{IN} (Slew rate [4:2] = 000)

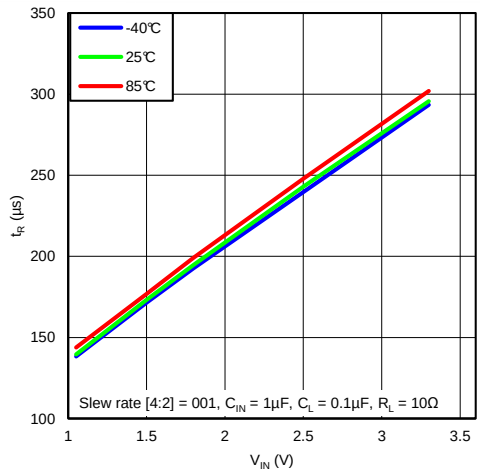

Figure 14. t_R vs. V_{IN} (Slew rate [4:2] = 001)

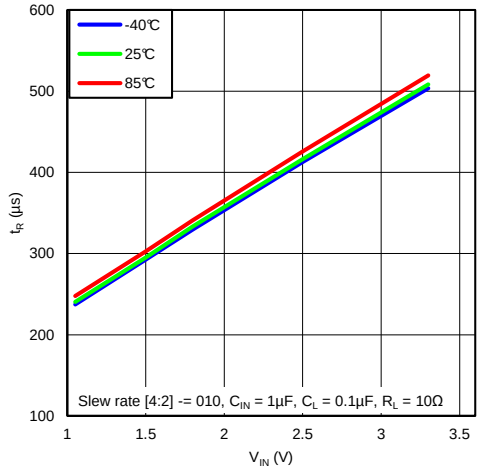

Figure 15. t_R vs. V_{IN} (Slew rate [4:2] = 010)

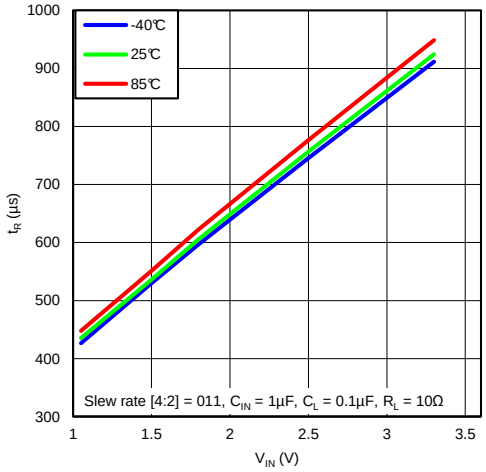

Figure 16. t_R vs. V_{IN} (Slew rate [4:2] = 011)

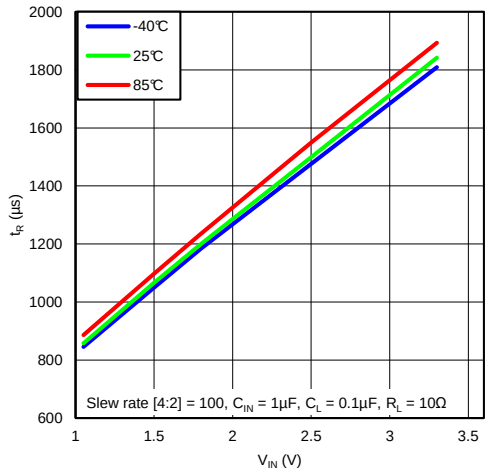

Figure 17. t_R vs. V_{IN} (Slew rate [4:2] = 100)

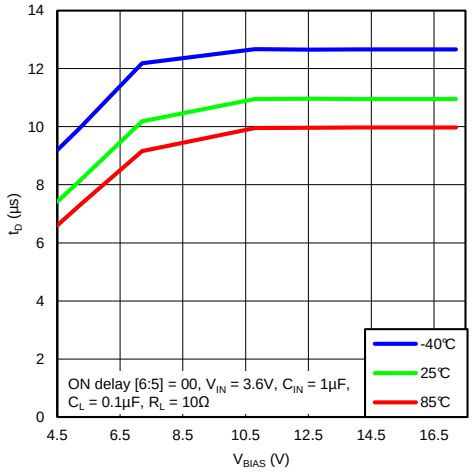

Figure 18. t_D vs. V_{BIAS} (ON delay [6:5] = 00)

Typical Characteristics (continued)

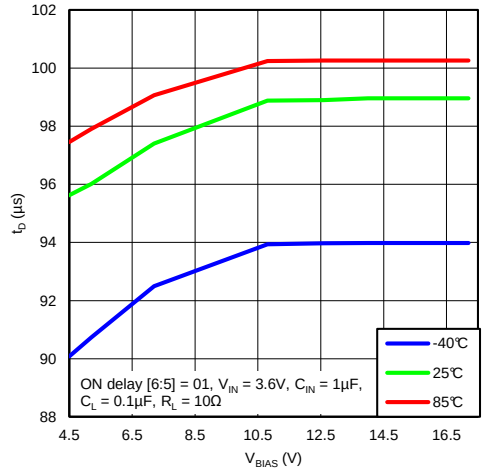

Figure 19. t_D vs. V_{BIAS} (ON delay [6:5] = 01)

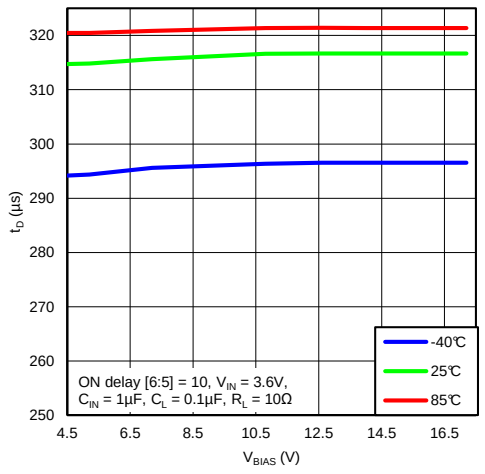

Figure 20. t_D vs. V_{BIAS} (ON delay [6:5] = 10)

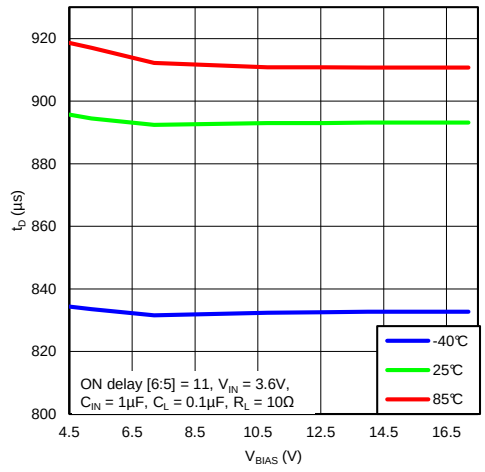

Figure 21. t_D vs. V_{BIAS} (ON delay [6:5] = 11)

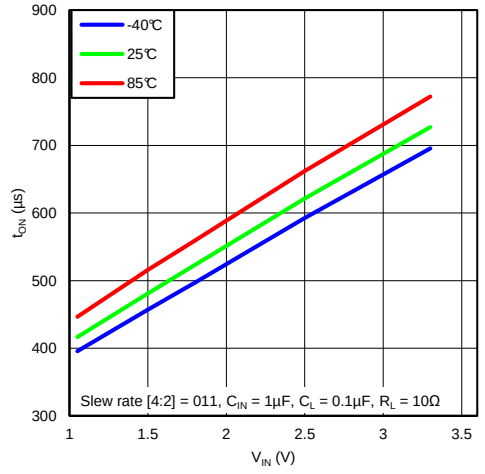

Figure 22. t_{ON} vs. V_{IN} (V_{BIAS} = 7.2V)

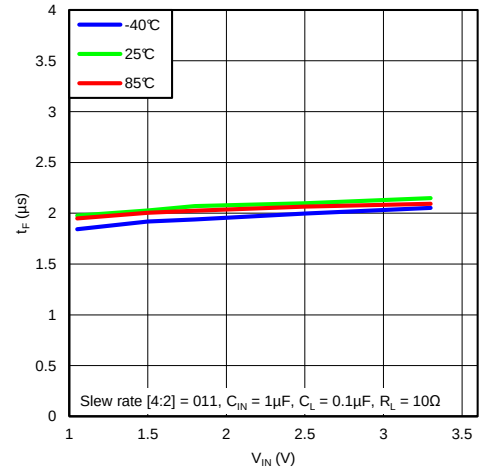

Figure 23. t_F vs. V_{IN} (V_{BIAS} = 7.2V)

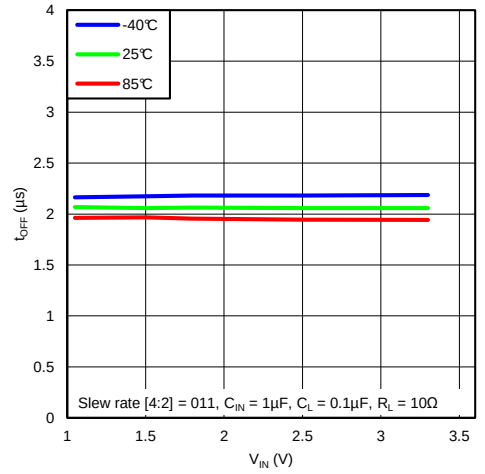

Figure 24. t_{OFF} vs. V_{IN} (V_{BIAS} = 7.2V)

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Typical Characteristics (continued)



Figure 25. +Power up with different slew rate settings

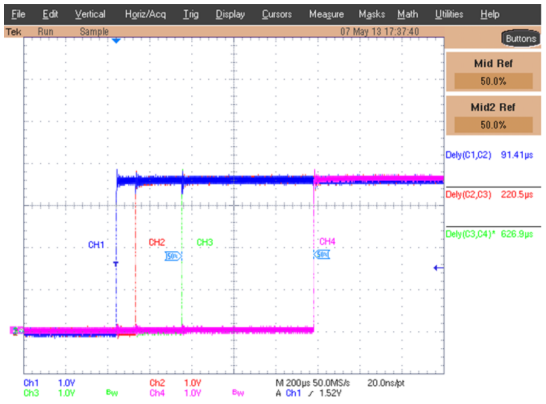


Figure 26. Power up with different tD settings

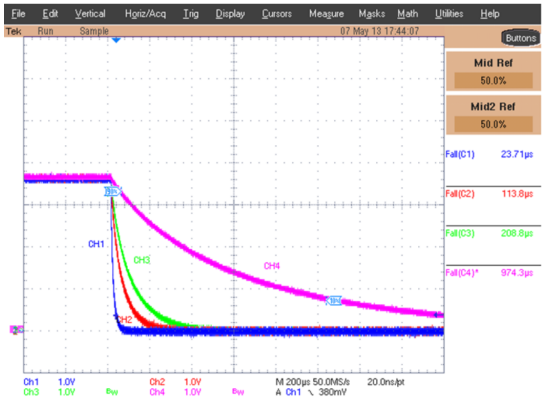


Figure 27. Power down with different QOD settings

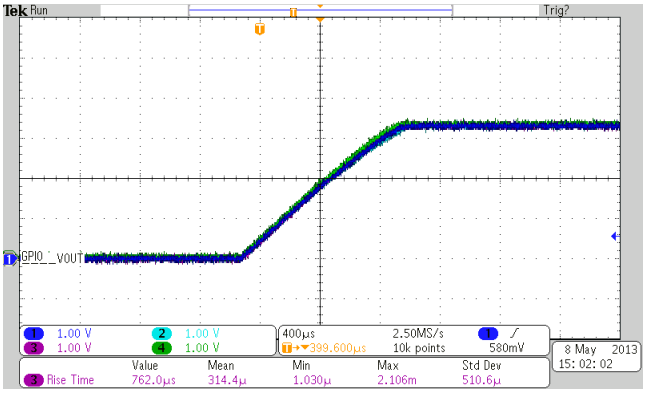


Figure 28. Power up with default settings

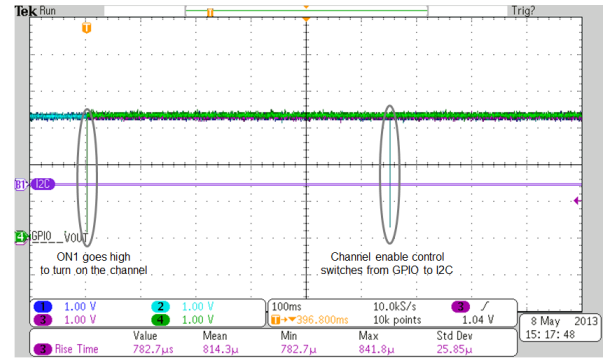


Figure 29. Channel 1 powered up via GPIO control, and control is switched over to I²C control without any glitches on VOUT.

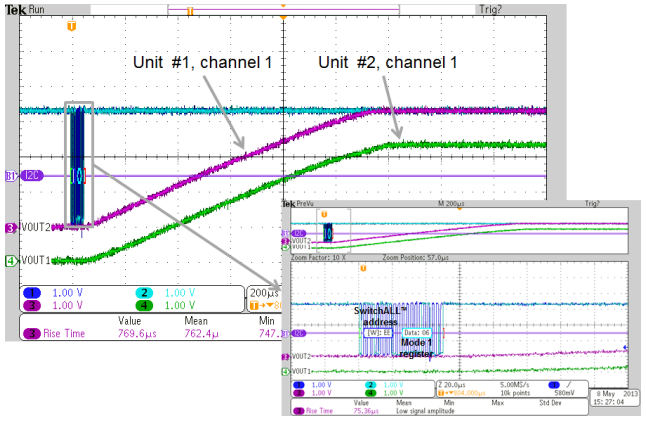
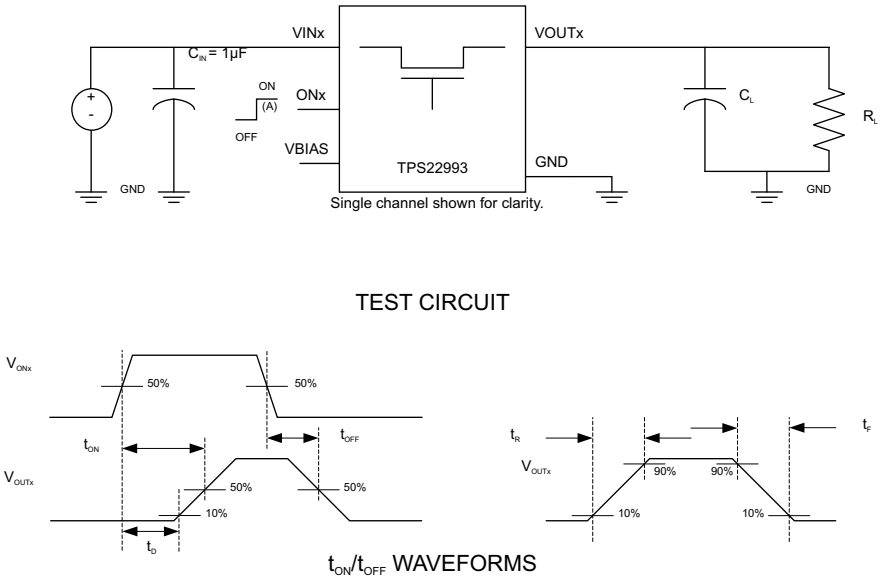


Figure 30. Enabling channel 1 across two TPS22993 devices with the SwitchALL™ command.

8 Parametric Measurement Information



(A) Rise and fall times of the control signal is 100ns.
(B) All switching measurements are done using GPIO control only.

Figure 31. Test Circuit and t_{ON}/t_{OFF} Waveforms

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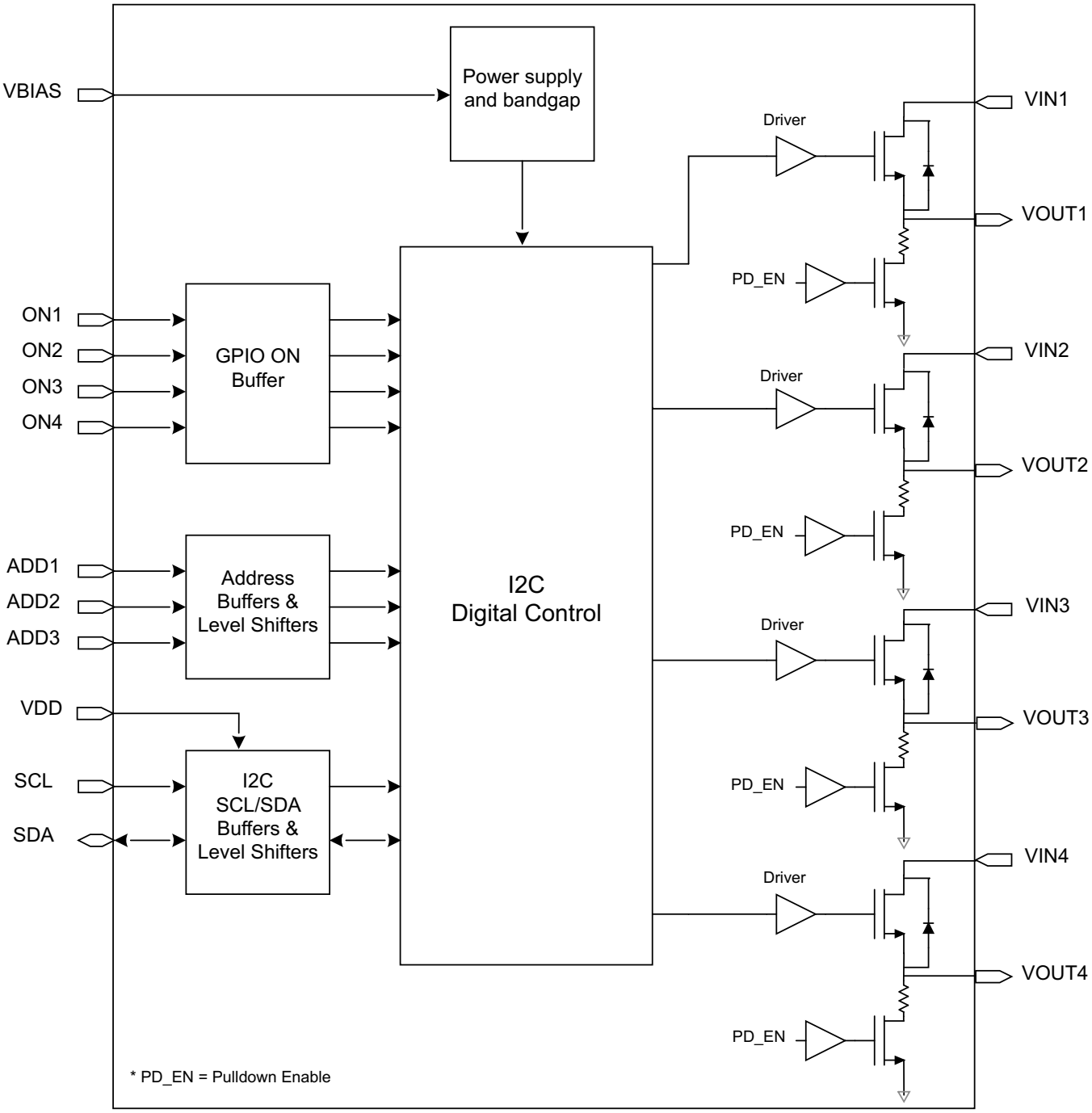
9 Detailed Description

9.1 Block Diagram



9.2 Register Map

Configuration registers (default register values shown below)

Channel 1 configuration register (Address: **01h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Channel 2 configuration register (Address: **02h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Channel 3 configuration register (Address: **03h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Channel 4 configuration register (Address: **04h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	1	1	0

Control register (default register values shown below)

Control register (Address: **05h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO/I^2C ch 4	GPIO/I^2C ch 3	GPIO/I^2C ch 2	GPIO/I^2C ch 1	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	0	0	0	0	0	0	0	0

Mode registers (default register values shown below)

Mode1 (Address: **06h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode2 (Address: **07h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode3 (Address: **08h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

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Mode4 (Address: **09h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode5 (Address: **0Ah**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode6 (Address: **0Bh**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode7 (Address: **0Ch**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode8 (Address: **0Dh**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode9 (Address: **0Eh**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode10 (Address: **0Fh**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode11 (Address: **10h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Mode12 (Address: **11h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

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10 Application and Implementation

10.1 Application Information

10.1.1 I²C Control

When power is applied to VBIAS, the device comes up in its default mode of GPIO operation where the channel outputs can be controlled solely via the ON terminals. At any time, if SDA and SCL are present and valid, the device can be configured to be controlled via I²C (if in GPIO control) or GPIO (if in I²C control).

The control register (address **05h**) can be configured for GPIO or I²C enable on a per channel basis.

10.1.1.1 Operating Frequency

The TPS22993 is designed to be compatible with fast-mode plus and operate up to 1MHz clock frequency for bus communication. The device is also compatible with standard-mode (100kHz) and fast-mode (400kHz). This device can reside on the same bus as high-speed mode (3.4MHz) devices, but the device is not designed to respond to I²C commands for frequencies greater than 1MHz. See table below for characteristics of the fast-mode plus, fast-mode, and standard-mode bus speeds.

Table 1. I²C Interface Timing Requirements(1)

PARAMETER		STANDARD MODE I²C BUS		FAST MODE I²C BUS		FAST MODE PLUS (FM+) I²C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	0	1000	kHz
t_{sch}	I²C clock high time	4		0.6		0.26		µs
t_{scl}	I²C clock low time	4.7		1.3		0.5		µs
t_{sp}	I²C spike time		50		50		50	ns
t_{sds}	I²C serial data setup time	250		100		50		ns
t_{sdh}	I²C serial data hold time	0		0		0		ns
t_{icr}	I2C input rise time		1000	20	300		120	ns
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		0.5		µs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		0.6		0.26		µs
t_{sth}	I²C Start or repeater Start condition hold time	4		0.6		0.26		µs
t_{sps}	I²C Stop condition setup time	4		0.6		0.26		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		3.45	0.3	0.9		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		3.45	0.3	0.9		0.45	µs

(1) over operating free-air temperature range (unless otherwise noted)

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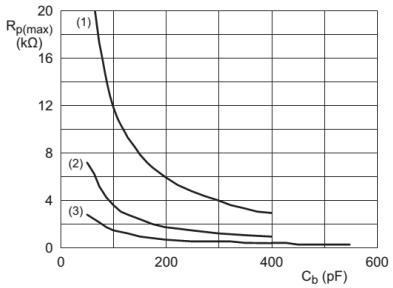
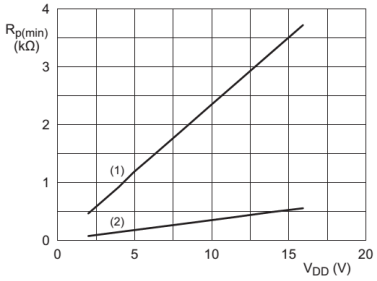
10.1.1.2 SDA/SCL Terminal Configuration

The SDA and SCL terminals of the device operate use an open-drain configuration, and therefore, need pull up resistors to communicate on the I^2C bus. The graph below shows recommended values for max pullup resistors (R_P) and bus capacitances (C_b) to ensure proper bus communications. The SDA and SCL terminals should be pulled up to VDD through an appropriately sized R_P based on the graphs below.



(1) Standard-mode
(2) Fast-mode
(3) Fast-mode Plus



(1) Fast-mode and Standard-mode
(2) Fast-mode Plus

10.1.1.3 Address (ADDx) Terminal Configuration

The TPS22993 can be configured with an unique I^2C slave addresses by using the ADDx terminals. There are 3 ADDx terminals that can be tied high to VDD or low to GND (independent of each other) to get up to 7 different slave addresses. The ADDx terminals should be tied to GND if the I^2C functionality of the device is not to be used. External pull-up resistors for the ADDx are optional as the ADDx inputs are high impedance. The following table shows the ADDx terminal tie-offs with their associated slave addresses (assuming an eight bit word, where the LSB is the read/write bit and the device address bits are the 7 MSB bits) :

Hex Address	ADD3	ADD2	ADD1
E0/E1	GND	GND	GND
E2/E3	GND	GND	VDD
E4/E5	GND	VDD	GND
E6/E7	GND	VDD	VDD
E8/E9	VDD	GND	GND
EA/EB	VDD	GND	VDD
EC/ED	VDD	VDD	GND
EE	Invalid unique device address. This address is the SwitchALL™ address.		

10.1.2 GPIO Control

There are four ON terminals to enable/disable the four channels. Each ON terminal controls the state of the switch by default upon power up. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON terminal is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V or higher voltage GPIO.

10.1.3 On-Delay Control

Using the I^2C interface, the configuration register for each channel can be set for different ON delays for power sequencing. The options for delay are as follows:

00 = 11µs delay (default register value)
01 = 105µs delay
10 = 330µs delay
11 = 950µs delay

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10.1.4 Slew Rate Control

Using the I^2C interface, the configuration register for each channel can be set for different slew rates for inrush current control and power sequencing. The options for slew rate are as follows:

000 = 1µs/V
001 = 150µs/V
010 = 250µs/V
011 = 460µs/V (default register value)
100 = 890µs/V
101 = invalid slew rate
110 = invalid slew rate
111 = reserved

10.1.5 Quick Output Discharge (QOD) Control

Using the I^2C interface, the configuration register for each channel can be set for different output discharge resistors. The options for QOD are as follows:

00 = 110Ω
01 = 490Ω
10 = 951Ω (default register value)
11 = No QOD (high impedance)

10.1.6 Mode Registers

Using the I^2C interface, the mode registers can be programmed to the desired on/off status for each channel. The contents of these registers are copied over to the control registers when a SwitchALL™ command is issued, allowing all channels of the device to transition to their desired output states synchronously. See the I^2C Protocol section and the Application Scenario section for more information on how to use the mode registers in conjunction with the SwitchALL™ command.

10.1.7 SwitchALL™ Command

I^2C controlled channels can respond to a common slave address. This feature allows multiple load switches on the same I^2C bus to respond simultaneously. The SwitchALL™ address is **EEh**. During a SwitchALL™ command, the lower four bits (bits 0 through 3) of the mode register is copied to the lower four bits (bits 0 through 3) of the control register. The mode register to be invoked is referenced in the body of the SwitchALL™ command. The structure of the SwitchALL™ command is as follows (as shown in Figure 32): <start><SwitchALL™ addr><mode addr><stop>. See the I^2C Protocol section and the Application Scenario section for more information on how to use the SwitchALL™ command in conjunction with the mode registers.

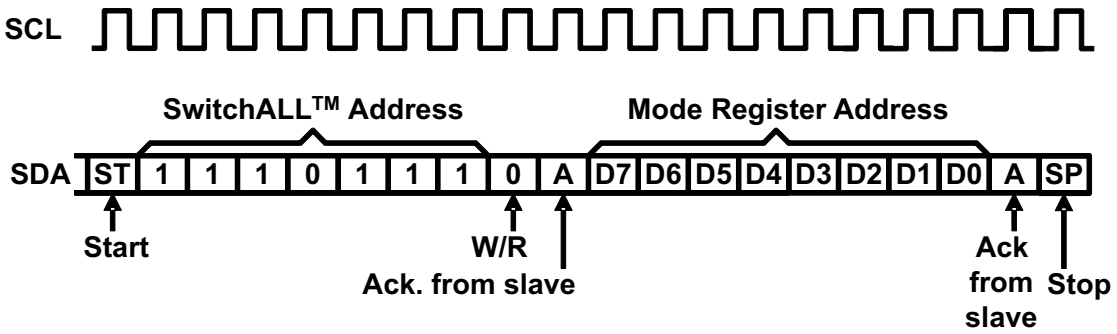

Figure 32. Composition of SwitchALL™ Command

10.1.8 V_{DD} Supply For I^2C Operation

The SDA and SCL terminals of the device must be pulled up to the VDD voltage of the device for proper I^2C bus communication.

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10.1.9 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the terminals, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop. For the fastest slew rate setting of the device, a CIN to CL ratio of at least 100 to 1 is recommended to avoid excessive voltage drop.

10.1.10 Output Capacitor (Optional)

Due to the integrated body diode of the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of at least 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup. For the fastest slew rate setting of the device, a CIN to CL ratio of at least 100 to 1 is recommended to minimize V_{IN} dip caused by inrush currents during startup.

10.1.11 I^2C Protocol

The following section will cover the standard I^2C protocol used in the TPS22993. In the I^2C protocol, the following basic blocks are present in every command (except for the SwitchALL™ command):

- Start/stop bit – marks the beginning and end of each command.
- Slave address – the unique address of the slave device.
- Sub address – this includes the register address and the auto-increment bit.
- Data byte – data being written to the register. Eight bits must always be transferred even if a single bit is being written or read.
- Auto-increment bit – setting this bit to ‘1’ turns on the auto-increment functionality; setting this bit to ‘0’ turns off the auto-increment functionality.
- Write/read bit – this bit signifies if the command being sent will result in reading from a register or writing to a register. Setting this bit to ‘0’ signifies a write, and setting this bit to ‘1’ signifies a read.
- Acknowledge bit – this bit signifies if the master or slave has received the preceding data byte.

10.1.11.1 Start and Stop Bit

In the I^2C protocol, all commands contain a START bit and a STOP bit. A START bit, defined by high to low transition on the SDA line while SCL is high, marks the beginning of a command. A STOP bit, defined by low to high transition on the SDA line while SCL is high, marks the end of a command. The START and STOP bits are generated by the master device on the I^2C bus. The START bit indicates to other devices that the bus is busy, and some time after the STOP bit the bus is assumed to be free.

10.1.11.2 Auto-increment Bit

The auto-increment feature in the I^2C protocol allows users to read from and write to consecutive registers in fewer clock cycles. Since the register addresses are consecutive, this eliminates the need to resend the register address. The I^2C core of the device automatically increments the register address pointer by one when the auto-increment bit is set to ‘1’. When this bit is set to ‘0’, the auto-increment functionality is disabled.

10.1.11.3 Write Command

During the write command, the write/read bit is set to ‘0’, signifying that the register in question will be written to. Figure 33 the composition of the write protocol to a *single* register:

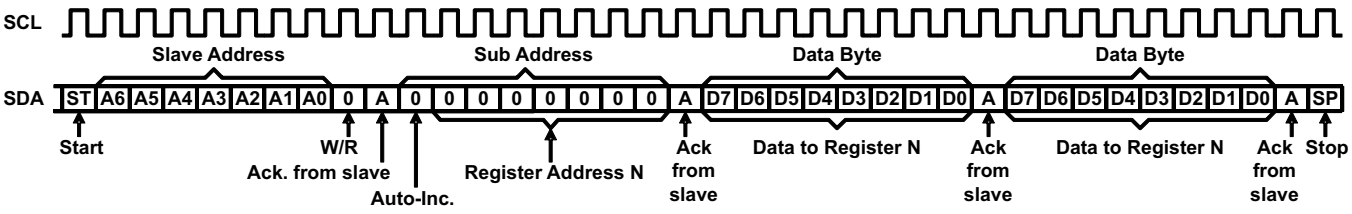

Figure 33. Data Write to a Single Register

Number of clock cycles for single register write: 29

If multiple consecutive registers must be written to, a short-hand version of the write command can be used. Using the auto-increment functionality of I^2C, the device will increment the register address after each byte. Figure 34 shows the composition of the write protocol to multiple *consecutive* registers:

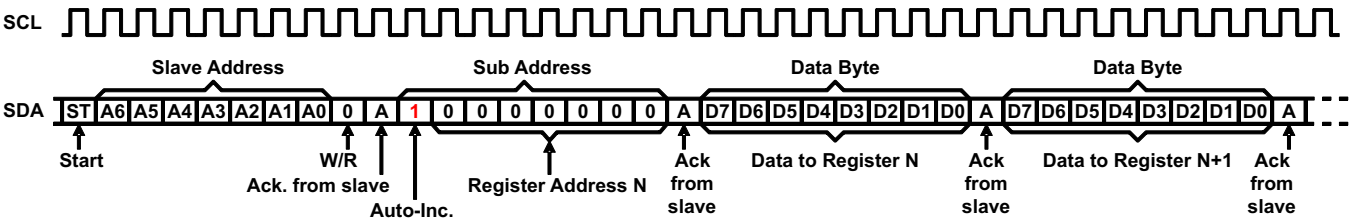

Figure 34. Data Write to Consecutive Registers

Number of clock cycles for consecutive register write: 20 + (Number of registers) x 9

The write command is always ended with a STOP bit after the desired registers have been written to. If multiple non-consecutive registers must be written to, then the format in Figure 33 must be followed.

10.1.11.4 Read Command

During the read command, the write/read bit is set to '1', signifying that the register in question will be read from. However, a read protocol includes a "dummy" write sequence to ensure that the memory pointer in the device is pointing to the correct register that will be read. Failure to precede the read command with a write command may result in a read from a random register. Figure 35 shows the composition of the read protocol to a single register:

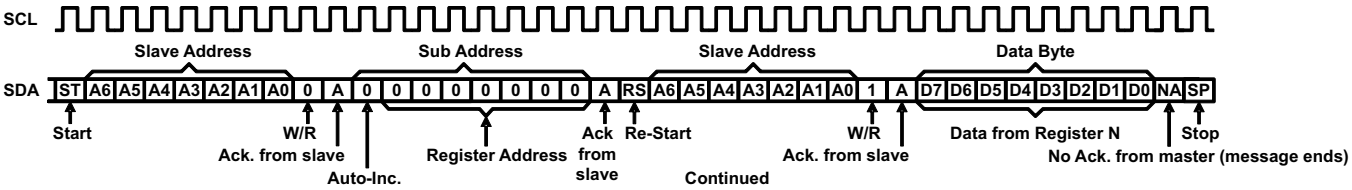

Figure 35. Data Read to a Single Register

Number of clock cycles for single register read: 39

If multiple registers must be read from, a short-hand version of the read command can be used. Using the auto-increment functionality of I^2C, the device will increment the register address after each byte. Figure 36 shows the composition of the read protocol to multiple consecutive registers:

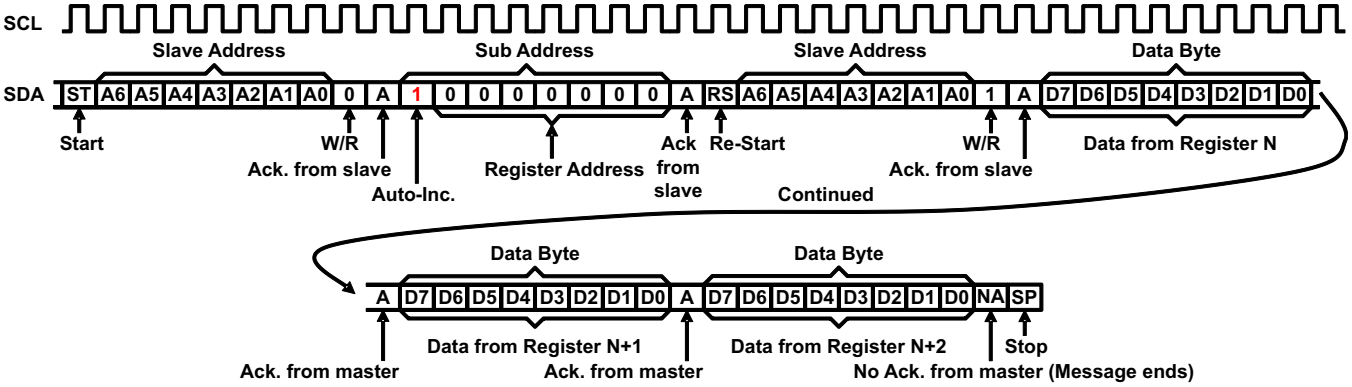

Figure 36. Data Read to Consecutive Registers

Number of clock cycles for consecutive register write: 30 + (Number of registers) x 9

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The read command is always ended with a STOP bit after the desired registers have been read from. If multiple non-consecutive registers must be read from, then the format in Figure 35 must be followed.

10.1.11.5 SwitchALL™ Command

The SwitchALL™ command allows multiple devices in the same I²C bus to respond synchronously to the same command from the master. Every TPS22993 device has a shared address which allows for multiple devices to respond or execute a pre-determined action with a single command. Figure 37 shows the composition of the SwitchALL™ command:

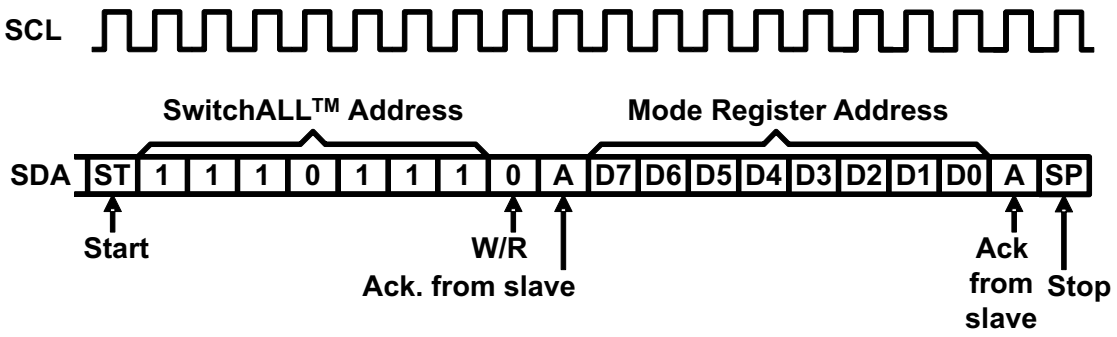

Figure 37. SwitchALL™ Command Structure

Number of clock cycles for a SwitchALL™ command: 20

10.2 Typical Applications

This section will cover applications of I²C in the TPS22993. Registers discussed here are specific to the TPS22993.

10.2.1 Switch from GPIO Control to I²C Control (and vice versa)

The TPS22993 can be switched from GPIO control to I²C (and vice versa) mode by writing to the control register of the device. Each device has a single control register and is located at register address 05h. The register's composition is as follows:

Control register (Address: **05h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO/I²C CH 4	GPIO/I²C CH 3	GPIO/I²C CH 2	GPIO/I²C CH 1	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	0	0	0	0	0	0	0	0

Figure 38. Control Register Composition

The higher four bits of the control register dictates if the device is in GPIO control (bit set to '0') or I²C control (bit set to '1'). The transition from GPIO control to I²C control can be made with a single write command to the control register. See Figure 33 for the composition of a single write command. It is recommended that the channel of interest is transitioned from GPIO control to I²C control with the first write command and followed by a second write command to enable the channel via I²C control. This will ensure a smooth transition from GPIO control to I²C control.

10.2.2 Configuration of Configuration Registers

The TPS22993 contains four configuration registers (one for each channel) and are located at register addresses **01h** through **04h**. The register's composition is as follows (single channel shown for clarity):

Channel 1 configuration register (Address: **01h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	ON-DELAY		SLEW RATE			QUICK OUTPUT DISCHARGE	
DEFAULT	X	0	0	0	1	0	1	0

Figure 39. Configuration Register Composition

10.2.2.1 Single Register Configuration

A single configuration register can be written to using the write command sequence shown in Figure 33.

Multiple register writes to non-consecutive registers is treated as multiple single register writes and follows the same write command as that of a single register write as shown in Figure 33.

10.2.2.2 Multi-register Configuration (Consecutive Registers)

Multiple consecutive configuration registers can be written to using the write command sequence shown in Figure 34.

10.2.3 Configuration of Mode Registers

The TPS22993 contains twelve mode registers located at register addresses **06h** through **11h**. These mode registers allow the user to turn-on or turn-off multiple channels in a single TPS22993 or multiple channels spanning multiple TPS22993 devices with a single SwitchALL™ command.

For example, an application may have multiple power states (e.g. sleep, active, idle, etc.) as shown in Figure 40.

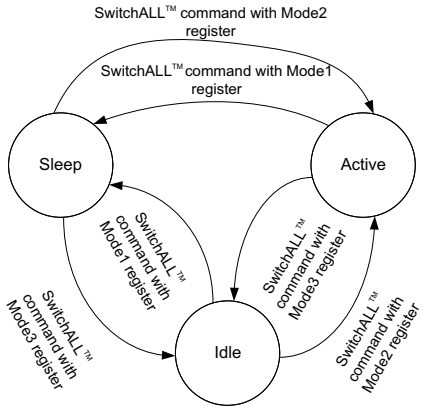

Figure 40. Application Example of Power States

In each of the different power states, different combinations of channels may be on or off. Each power state may be associated with a single mode register (Mode1, Mode2, etc.) across multiple TPS22993 as shown in Table 2. For example, with 7 quad-channel devices, up to 28 rails can be enabled/disabled with a single SwitchALL™ command.

Table 2. Application Example of State of Each Channel in Multiple TPS22993 in Different Power States

Mode Register	Power State	Load Switch #1				Load Switch #2				Load Switch #N			
		Ch. 1	Ch. 2	Ch. 3	Ch. 4	Ch. 1	Ch. 2	Ch. 3	Ch. 4	Ch. 1	Ch. 2	Ch. 3	Ch. 4
Mode1	Sleep	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
Mode2	Active	On	On	On	On	On	Off	On	Off	On	Off	On	Off
Mode3	Idle	On	Off	On	Off	On	On	On	On	On	On	On	On

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The contents of the lower four bits of the mode register is copied into the lower four bits of the control register during an SwitchALL™ command. The address of the mode register to be copied is specified in the SwitchALL™ command (see Figure 37 for the structure of the SwitchALL™ command). By executing a SwitchALL™ command, the application will apply the different on/off combinations for the various power states with a single command rather than having to turn on/off each channel individually by re-configuring the control register. This reduces the latency and allows the application to control multiple channels synchronously. The example above shows the application using three mode registers, but the TPS22993 contains twelve mode registers, allowing for up to twelve power states.

The mode register's composition is as follows (single mode register shown for clarity):

Mode1 (Address: **06h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	X	X	X	X	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	X	X	X	X	0	0	0	0

Figure 41. Mode Register Composition

The lower four bits of the mode registers are copied into the lower four bits of the control register during an all-call command.

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10.2.4 Turn-on/Turn-off of Channels

By default upon power up VBIAS, all the channels of the TPS22993 are controlled via the ONx terminals. Using the I^2C interface, each channel be controlled via I^2C control as well. The channels of the TPS22993 can also be switched on or off by writing to the control register of the device. Each device has a single control register and is located at register address **05h**. The register's composition is as follows:

Control Register (Address: **05h**)

BIT	B7	B6	B5	B4	B3	B2	B1	B0
DESCRIPTION	GPIO/I^2C CH 4	GPIO/I^2C CH 3	GPIO/I^2C CH 2	GPIO/I^2C CH 1	ENABLE CH 4	ENABLE CH 3	ENABLE CH 2	ENABLE CH 1
DEFAULT	0	0	0	0	0	0	0	0

Figure 42. Control Register Composition

The lower four bits of the control register dictate if the channels of the device are off (bit set to '0') or on (bit set to '1') during I^2C control. The transition from off to on can be made with a single write command to the control register. See Figure 33 for the composition of a single write command.

10.2.5 Tying Multiple Channels in Parallel

Two or more channels of the device can be tied in parallel for applications that require lower R_{ON} and/or more continous current. Tying two channels in parallel will result in half of the R_{ON} and two times the I_{MAX} capability. Tying three channels in parallel will result in one-third of the R_{ON} and three times the I_{MAX} capability. Tying four channels in parallel will result in one-fourth of the R_{ON} and four times the I_{MAX} capability. For the channels that are tied in parallel, it is recommended that the ONx terminals be tied together for synchronous control of the channels when in GPIO control. In I^2C control, all four channels can be enabaled or disabled synchronously by writing to the control register of the device. Figure 43 shows an application example of tying all four channels in parallel.

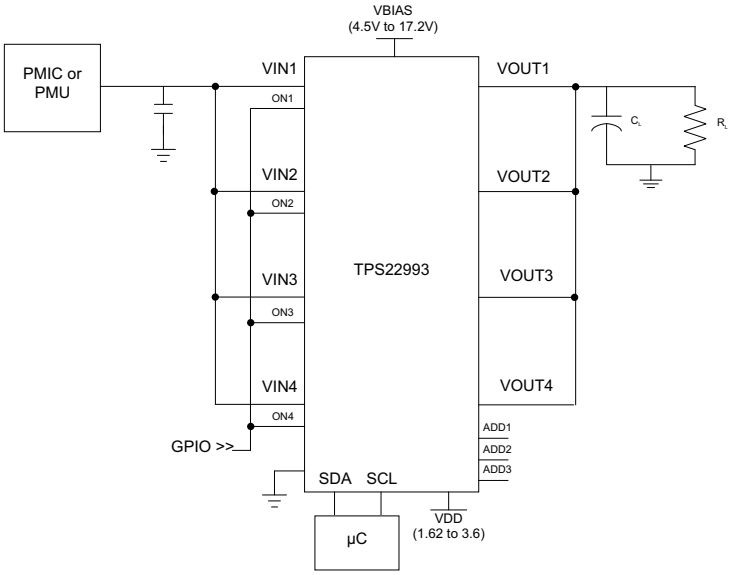

Figure 43. Parallel Channels

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10.2.6 Cold Boot Programming of all Registers

Since the TPS22993 has a digital core with volatile memory, upon power cycle of the VBIAS terminal, the registers will revert back to their default values (see register map for default values). Therefore, the application must reprogram the configuration registers, control register, and mode registers if non-default values are desired. The TPS22993 contains 17 programmable registers (4 configuration registers, 1 control register, 12 mode registers) in total.

During cold boot when the microcontroller and the I^2C bus is not yet up and running, the channels of the TPS22993 can still be enabled via GPIO control. One method to achieve this is to tie the ONx terminal to the respective VINx terminal for the channels that need to turn on by default during cold boot. With this method, when VINx is applied to the TPS22993, the channel will be enabled as well. Once the I^2C bus is active, the channel can be switched over to I^2C control to be disabled. See Figure 44 for an example of how the ONx terminals can be tied to VINx for default enable during cold boot.

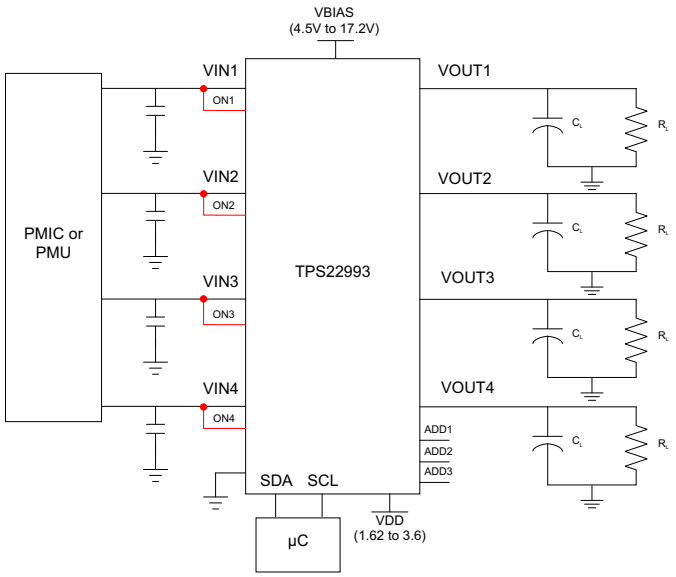

Figure 44. Cold Boot Programming

It is also possible to power sequence the channels of the device during a cold boot when there is no I^2C bus present for control. One method to accomplish this it to tie the VOUT of one channel to the ON terminal of the next channel in the sequence. For example, if the desired power up sequence is VOUT3, VOUT1, VOUT2, and VOUT4 (in that order), then the device can be configured for GPIO control as shown in Figure 45. The device will power up with default slew rate, ON-delay, and QOD values as specified in the register map.

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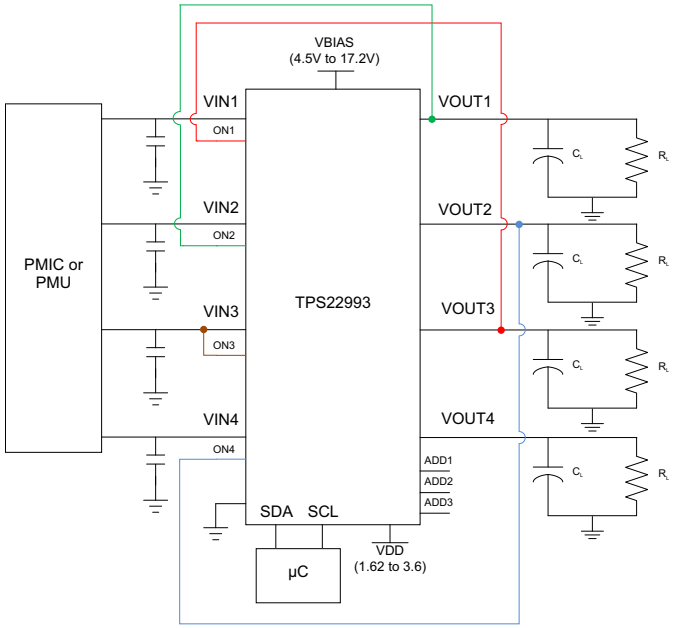

Figure 45. Power Sequencing Without I²C

10.2.7 Reading From the Registers

Reading any register from the TPS22993 follows the same standard I²C read protocol as outlined in the I²C Protocol section of this datasheet.

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11 Layout

11.1 Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\Theta_{JA}} \quad (1)$$

Where:

$P_{D(max)}$ = maximum allowable power dissipation
$T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22993)
T_A = ambient temperature of the device
Θ_{JA} = junction to air thermal impedance. See Thermal Information section. This parameter is highly dependent upon board layout.

The figure below shows an example of a layout.

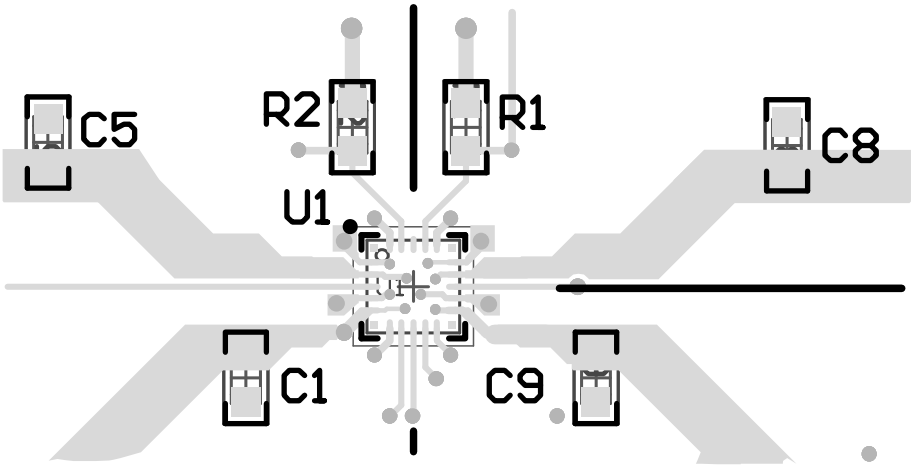

Figure 46. Top View of the TPS22993 EVM

Board Layout (continued)

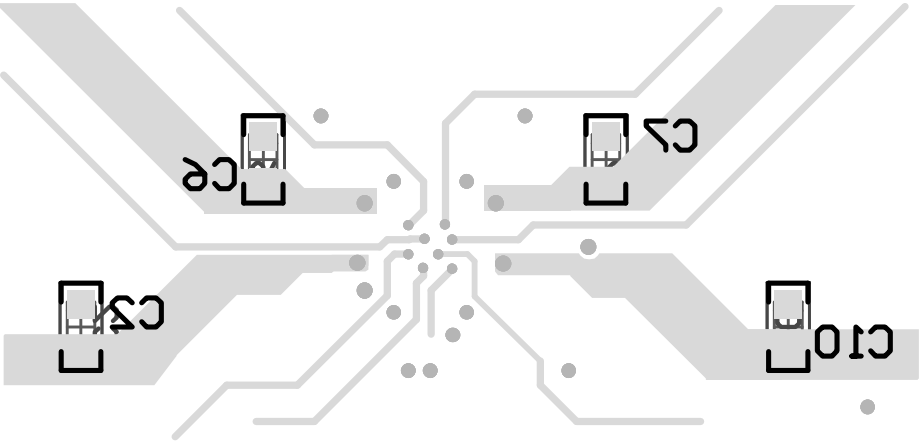

Figure 47. Bottom View of the TPS22993 EVM.

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12 Device and Documentation Support

12.1 Trademarks

SwitchALL is a trademark of Texas Instruments.
Ultrabook is a trademark of Intel.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22993PRLWR	OBSOLETE	WQFN-HR	RLW	20		Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	22993P	
TPS22993PRLWT	NRND	WQFN-HR	RLW	20	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	22993P	
TPS22993RLWR	ACTIVE	WQFN-HR	RLW	20	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	22993P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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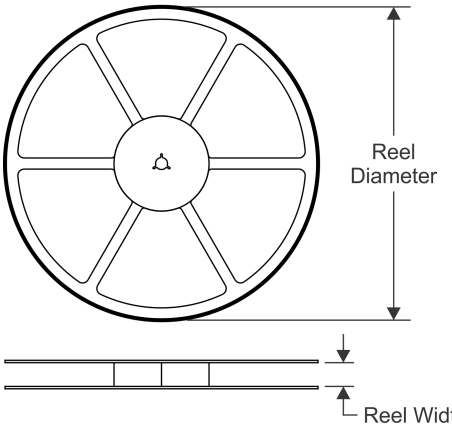
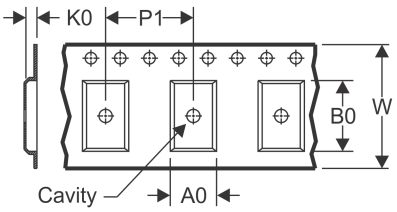
TAPE AND REEL INFORMATION

REEL DIMENSIONS

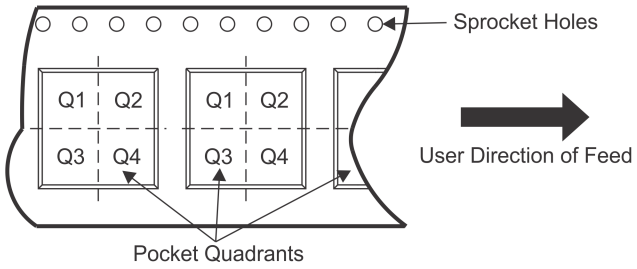


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

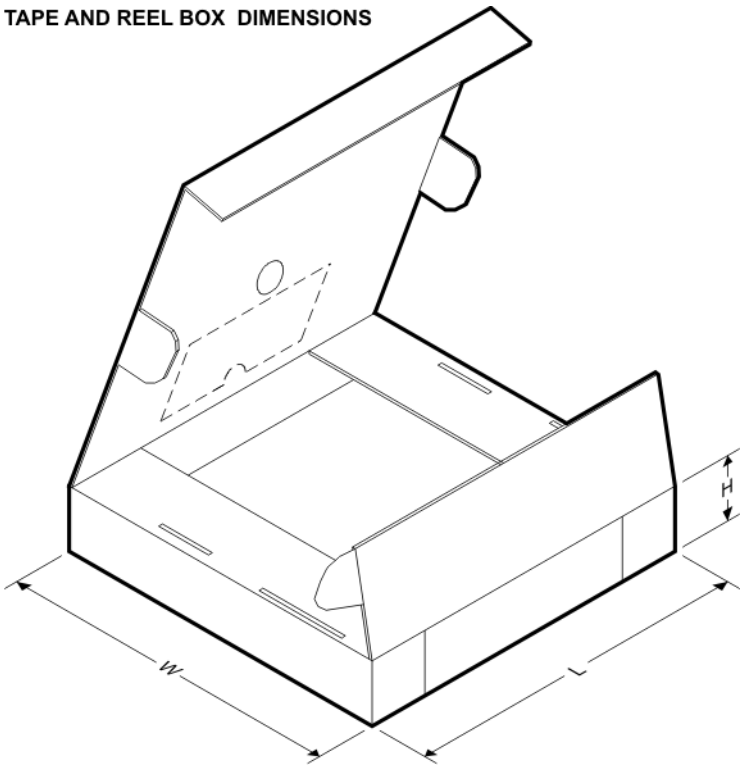
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22993PRLWR	WQFN-HR	RLW	20	0	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS22993PRLWT	WQFN-HR	RLW	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS22993RLWR	WQFN-HR	RLW	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

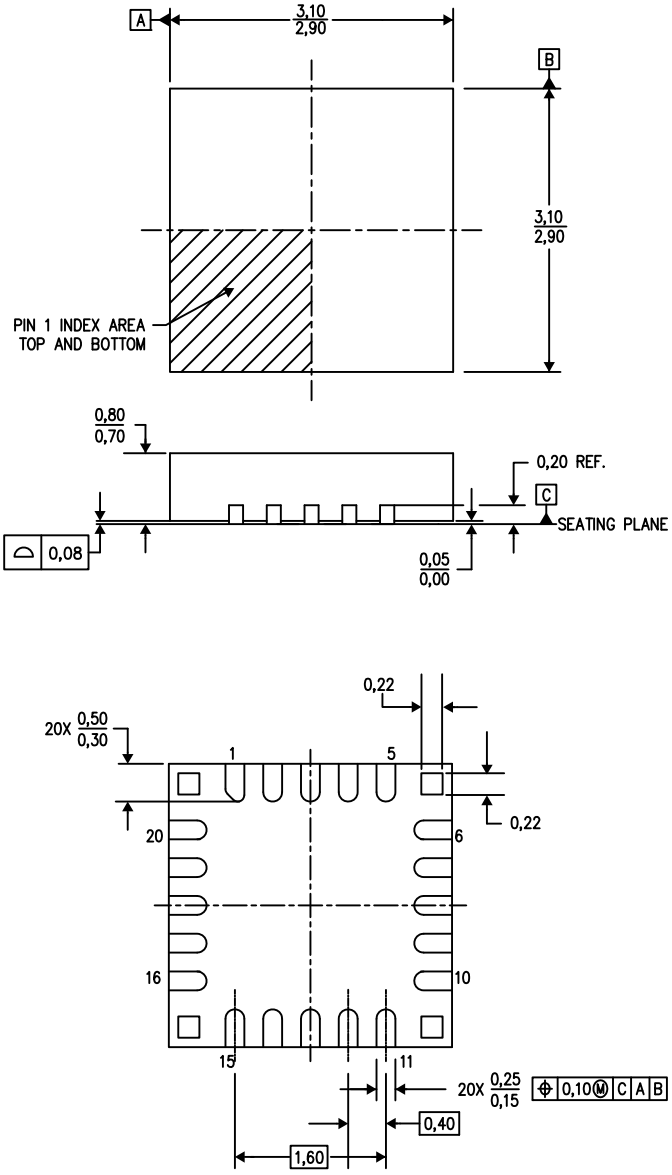
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22993PRLWR	WQFN-HR	RLW	20	0	367.0	367.0	35.0
TPS22993PRLWT	WQFN-HR	RLW	20	250	210.0	185.0	35.0
TPS22993RLWR	WQFN-HR	RLW	20	3000	367.0	367.0	35.0

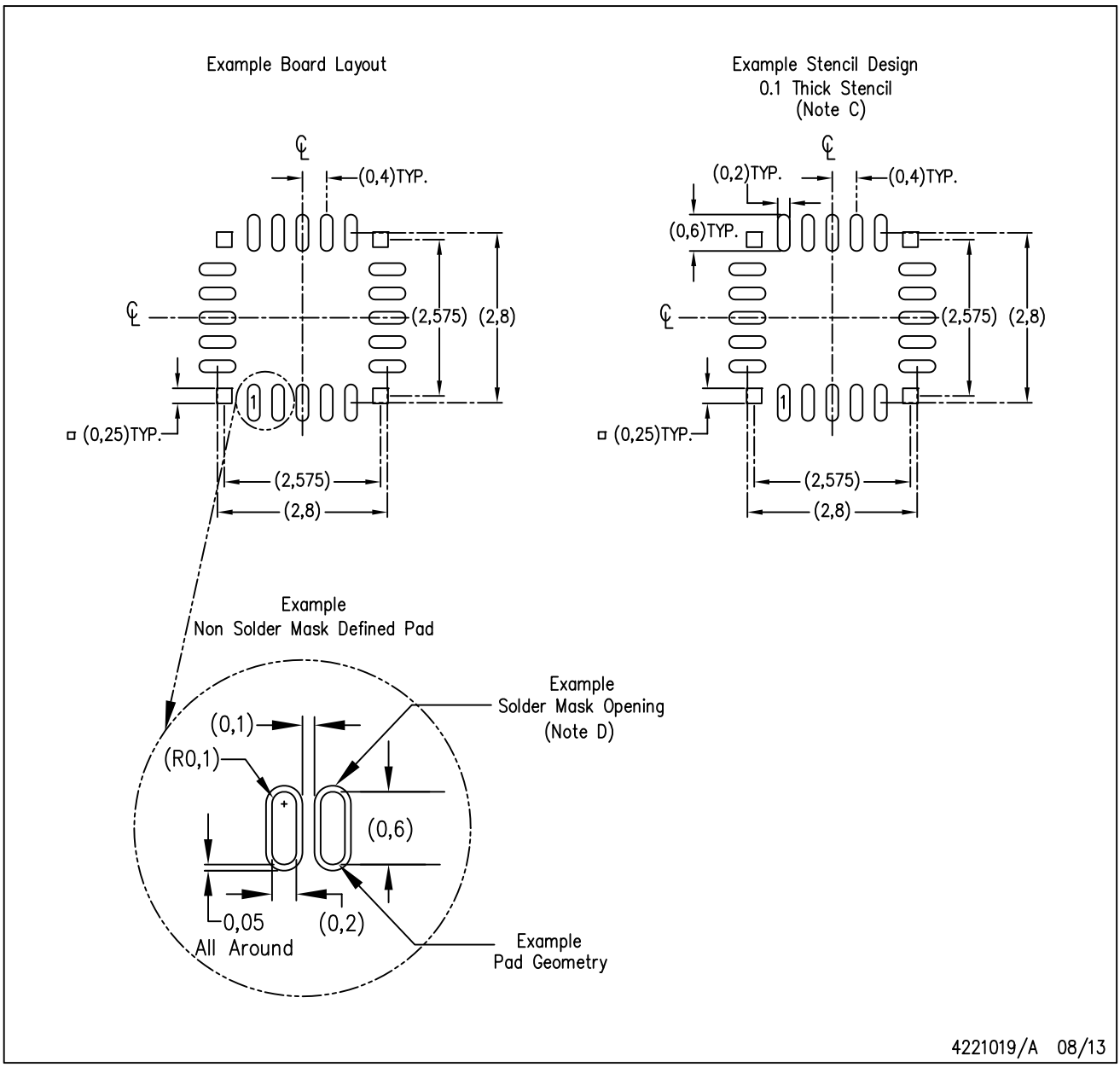
RLW (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



4218218/B 06/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. See the Product Data Sheet for details regarding the exposed power buss dimensions.
E. RoHS exempt flip chip application. Internal solder joints may contain Pb.
F. Exposed terminals are Pb–free

RLW (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
D. Customers should contact their board fabrication site for recommended solder mask tolerances.

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