TPS1663x 60-V, 6-A Power Limiting eFuse

ADVANCE INFORMATION

1 Features

- 4.5 V to 60 V Operating Voltage, 62-V Absolute Maximum
- Integrated 60-V Hot-Swap FET with 31-mΩ R_{ON}
- 0.6 A to 6 A Adjustable Current Limit (± 8% accuracy at 6 A)
- Low Quiescent Current, 22- µA in Shutdown
- Variant with Adjustable Output Power Limiting (TPS16632 only)
- Adjustable UVLO, OVP Cut Off, Output Slew Rate Control for Inrush Current Limiting
- Power Up in Thermal Regulation (dVdT = Open) Enables Charging of Large and Unknown Capacitive Loads
- Fixed 40-V Overvoltage Clamp (TPS16632 only)
- Power Good Output (PGOOD)
- Selectable Over Current Fault Response Options Between Auto-Retry and Latch Off (MODE)
- Analog Current Monitor (IMON) Output
- UL 2367 Recognition Pending
- Available in Easy-to-Use 24- Pin VQFN and 20-Pin HTSSOP Packages

2 Applications

- Factory Automation and Control – PLC, DCS, HMI, I/O Modules, Sensor Hubs
- Motor Drives – CNC, Encoder Supply
- Electronic Circuit Breakers
- Telecom Radios
- Industrial Printers

3 Description

The TPS1663x is an easy to use, positive 60 V, 6 A eFuse with a 31 mΩ integrated FET. Protection for the load, source and eFuse itself are provided along with adjustable features such as overcurrent protection, output slew rate control, overvoltage protection and undervoltage lockout. The TPS16630 device features an adjustable over voltage cut-off functionality whereas the TPS16632 features a fixed a 40 V output voltage clamp. The TPS16332 device integrates adjustable output power limiting (PLIM) functionality that simplifies and enables compliance to standards such as IEC61010-1. The device also includes adjustable over current functionality. PGOOD can be used for enable and disable control of the downstream DC-DC converters.

A shutdown pin provides external control for enabling and disabling the internal FET as well as placing the device in a low current shutdown mode. For system status monitoring and downstream load control, the device provides fault and a precise current monitor output. The MODE pin allows flexibility to configure the device between the two current-limiting fault responses (latch off and auto-retry).

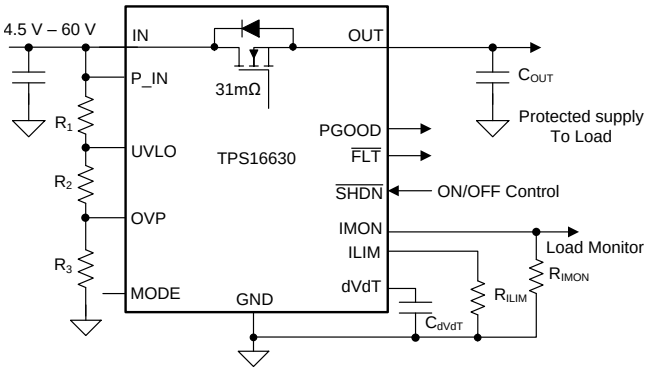
The devices are available in a 4-mm × 4-mm 24-pin VQFN as well as a 6.5-mm x 4.4-mm 20-pin HTSSOP package and are specified over a –40°C to +125°C temperature range.

Device Information(1)

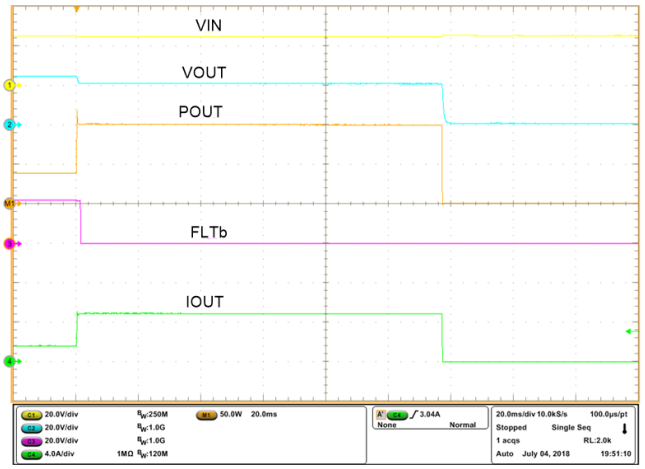
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS16630 TPS16632	VQFN (24)	4.00 mm × 4.00 mm
TPS16630	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Output Power Limiting Performance of TPS16632



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Device Comparison Table ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 5
7.5 Electrical Characteristics ... 6
7.6 Timing Requirements ... 7
8 Detailed Description ... 8
8.1 Overview ... 8
8.2 Functional Block Diagram ... 9
8.3 Feature Description ... 10
8.4 Device Functional Modes ... 16
9 Application and Implementation ... 17
9.1 Application Information ... 17
9.2 Typical Application ... 17
9.3 System Examples ... 20
10 Power Supply Recommendations ... 20
10.1 Transient Protection ... 21
10.2 Application Limitations ... 21
11 Layout ... 23
11.1 Layout Guidelines ... 23
11.2 Layout Example ... 24
12 Device and Documentation Support ... 26
12.1 Receiving Notification of Documentation Updates 26
12.2 Community Resources ... 26
12.3 Trademarks ... 26
12.4 Electrostatic Discharge Caution ... 26
12.5 Glossary ... 26
13 Mechanical, Packaging, and Orderable Information ... 26

ADVANCE INFORMATION

4 Revision History

Changes from Original (September 2018) to Revision A **Page**

- Changed Package Information ... 1

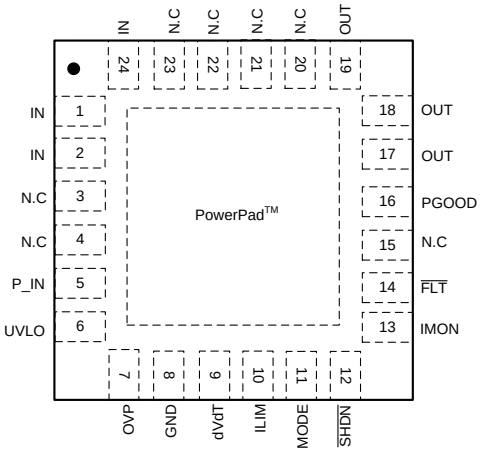
Copyright © 2018, Texas Instruments Incorporated

5 Device Comparison Table

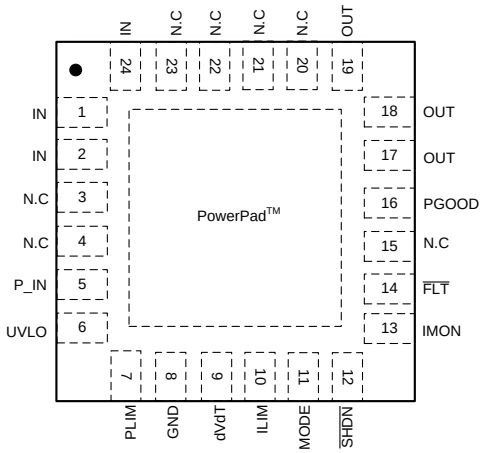
PART NUMBER	OVERVOLTAGE PROTECTION	ADJUSTABLE OUTPUT POWER LIMITING
TPS16630	Overvoltage cut-off, adjustable	No
TPS16632	Overvoltage clamp, fixed (40 V)	Yes

6 Pin Configuration and Functions

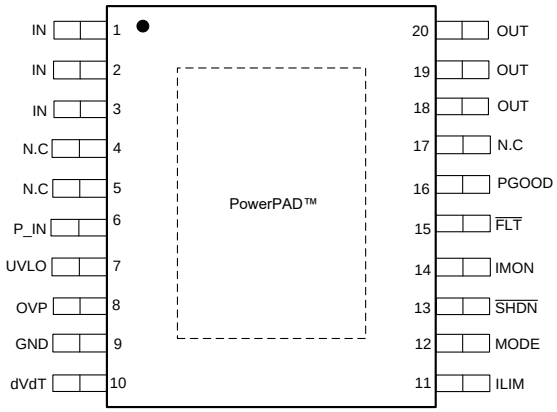
TPS16630 RGE Package
24-Pin VQFN
Top View



TPS16632 RGE Package
24-Pin VQFN
Top View



TPS16630 PWP Package
20-Pin HTSSOP
Top View



ADVANCE INFORMATION

ADVANCE INFORMATION

Pin Functions

PIN				TYPE	DESCRIPTION
NAME	TPS16630		TPS16632		
	VQFN	HTSSOP	VQFN		
dVdT	9	10	9	I/O	A capacitor from this pin to GND sets output voltage slew rate. Leaving this pin floating enables device power up in thermal regulation resulting in fast output charge. See the *Hot Plug-In and In-Rush Current Control* section
$\overline{FLT}$	14	15	14	O	Fault event indicator. It is an open drain output. If unused, leave floating or connect to GND
GND	8	9	8	—	Connect GND to system ground
ILIM	10	11	10	I/O	A resistor from this pin to GND sets the overload and short-circuit current limit. See the Overload and Short Circuit Protection section
IN	1	1	1	P	Power input. Connects to the DRAIN of the internal FET
	2	2	2		
	24	3	24		
IMON	13	14	13	O	Analog current monitor output. This pin sources a scaled down ratio of current through the internal FET. A resistor from this pin to GND converts current to proportional voltage. If unused, leave it floating
MODE	11	12	11	I	Mode selection pin for over load fault response. See the *Device Functional Modes* section
N.C	3	4	3	—	No Connect
	4	5	4		
	15	17	15		
	20	—	20		
	21	—	21		
	22	—	22		
	23	—	23		
OUT	17	18	17	P	Power output of the device
	18	19	18		
	19	20	19		
OVP	7	8	—	I	Input for setting the programmable overvoltage protection threshold (For TPS16630 Only). An overvoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the overvoltage fault.
PGOOD	16	16	16	O	Active High. A high that the internal FET is enhanced. PGOOD goes low when the internal FET is turned OFF during a fault or when $\overline{SHDN}$ is pulled low. If PGOOD is unused then connect to GND or leave it floating
P_IN	5	6	5	P	Supply voltage of the device. Connect P_IN to IN directly
PLIM	—	—	7	I	Input for setting the programmable output power limiting threshold (TPS16632 Only). Connect a resistor across PLIM to GND to set the output power limit. Connect PLIM to GND if PLIM feature is not used. See the *Output Power Limiting, PLIM (TPS16632 Only)* section.
$\overline{SHDN}$	12	13	12	I	Shutdown pin. Pulling $\overline{SHDN}$ low makes the device to enter into low power shutdown mode. Cycling $\overline{SHDN}$ pin voltage resets the device that has latched off due to a fault condition
UVLO	6	7	6	I	Input for setting the programmable undervoltage lockout threshold. An undervoltage event turns off the internal FET and asserts $\overline{FLT}$ to indicate the power-failure.
PowerPad™				—	Connect PowerPad to GND plane for heat sinking. Do not use PowerPad as the only electrical connection to GND

Copyright © 2018, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IN, P_IN, OUT, UVLO, $\overline{FLT}$, PGOOD		–0.3	62	V
IN, P_IN (10ms transient)		–0.3	75	V
OVP, dVdT, IMON, MODE, $\overline{SHDN}$, ILIM		–0.3	5	V
$I_{\overline{FLT}}$, I_{dVdT}, $I_{\overline{SHDN}}$	Sink current		10	mA
IdVdT, IILIM	Source current			Internally limited
T_J	Operating Junction temperature	–40	150	°C
	Transient junction temperature	–65	$T_{(TSD)}$	
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN, P_IN	Input Voltage	4.5		60	V
OUT,UVLO, PGOOD, $\overline{FLT}$		0		60	V
OVP, dVdT, IMON, MODE, $\overline{SHDN}$		0		4	V
ILIM	Resistance	3		30	kΩ
IMON		1			kΩ
IN, P_IN, OUT	External Capacitance	0.1			µF
T_J	Operating Junction temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS1663		UNIT
		RGE (VSON)	PWP (HTSSOP)	
		24 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.2	23.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	10	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.2	9.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

7.5 Electrical Characteristics

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN)}$ = $V_{(P_IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN)}$, $V_{(P_IN)}$	Operating input voltage		4.5		60	V
$IQ_{(ON)}$	Supply current	Enabled: $V_{(\overline{SHDN})}$ = 2 V		1.42	1.6	mA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})}$ = 0 V		22	53	µA
$V_{(OVC)}$	Over voltage clamp	TPS16632 Only, $V_{(IN)}$ > 40V, $I_{(OUT)}$ = 1mA	36		40	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.176	1.2	1.224	V
$V_{(UVLOF)}$	UVLO threshold voltage, falling			1.14		V
$I_{(UVLO)}$	UVLO Input leakage current	0 V ≤ $V_{(UVLO)}$ ≤ 60 V	–100	0	100	nA
OVERVOLTAGE PROTECTION (OVP) INPUT						
$V_{(OVPR)}$	over-voltage threshold voltage, rising		1.176	1.2	1.224	V
$V_{(OVPF)}$	over-voltage threshold voltage, falling			1.14		V
$I_{(OVP)}$	OVP Input leakage current	0 V ≤ $V_{(OVP)}$ ≤ 4 V	–100	0	100	nA
POWER LIMITING CONTROL (PLIM) INPUT – TPS16632 ONLY						
$V_{(SEL_PLIM)}$	Power Limit Feature select threshold				240	mV
$I_{(PLIM)}$	PLIM sourcing current	$V_{(PLIM)}$ = 0 V		5		µA
$P_{(PLIM)}$	Max Output power	$R_{(PLIM)}$ = 100 kΩ		100		W
		$R_{(PLIM)}$ = 150 kΩ		150		W
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Open circuit voltage	$I_{(\overline{SHDN})}$ = 0.1 µA	2.48		3.4	V
$V_{(SHUTF)}$	$\overline{SHDN}$ threshold voltage for low IQ shutdown, falling				0.8	V
$V_{(SHUTR)}$	$\overline{SHDN}$ threshold rising		2			V
$I_{(\overline{SHDN})}$	Leakage current	$V_{(\overline{SHDN})}$ = 0.4 V	–10			µA
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT charging current	$V_{(dVdT)}$ = 0 V	1.9	2	2.1	µA
$GAIN_{(dVdT)}$	dVdT to OUT gain	$V_{(OUT)}$ /$V_{(dVdT)}$		24		V/V
V_dVdTmax	dVdT maximum capacitor voltage				4.75	V
$R_{(dVdT)}$	dVdT discharging resistance	$V_{(\overline{SHDN})}$ = 0 V, with $I_{(dVdT)}$ = 10 mA sinking		14		Ω
CURRENT LIMIT PROGRAMMING (ILIM)						
$I_{(OL)}$	Over Load current limit	$R_{(ILIM)}$ = 30 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.51	0.6	0.69	A
		$R_{(ILIM)}$ = 9 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V		2		A
		$R_{(ILIM)}$ = 4.02 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V		4.5		A
		$R_{(ILIM)}$ = 3 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V		6		A
$I_{(FASTRIP)}$	Fast-trip comparator threshold			2x$I_{(OL)}$		A
$I_{(SCP)}$	Short Circuit Protect current			40		A
CURRENT MONITOR OUTPUT (IMON)						
$GAIN_{(IMON)}$	Gain factor $I_{(IMON)}$:$I_{(OUT)}$	0.6 A ≤ $I_{(OUT)}$ ≤ 6 A		27.7		µA/A
PASS FET OUTPUT (OUT)						
R_{ON}	IN to OUT total ON resistance	0.6 A ≤ $I_{(OUT)}$ ≤ 6 A, –40°C ≤ T_J ≤ +125°C		31	53	mΩ
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-down resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5 mA sinking	36	70	130	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input leakage current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 60 V	–100		100	nA
POWER GOOD (PGOOD)						

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN)}$ = $V_{(P_IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(PGOOD)}$	PGOOD Pull-down resistance	$V_{(dVdT)}$ = 0 V, $I_{(PGOOD)}$ = 5 mA sinking	36	70	130	Ω
$I_{(PGOOD)}$	PGOOD Input leakage current	0 V ≤ $V_{(PGOOD)}$ ≤ 60 V	–100		100	nA
THERMAL SHUT DOWN (TSD)						
$T_{(J_REG)}$	Thermal regulation set point		147	150	154	ºC
$T_{(TSD)}$	TSD threshold, rising			164		ºC
$T_{(TSDhyst)}$	TSD hysteresis			11		ºC
MODE						
MODE_SEL	Mode selection	MODE = Open		Latch		
		MODE = Short to GND		Auto–Retry		

7.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, 4.5 V < $V_{(IN)}$ = $V_{(P_IN)}$ < 60 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 30 kΩ, IMON = PGOOD = $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO INPUT (UVLO)						
UVLO_$t_{on(dly)}$	UVLO switch turnon delay	UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV		669 + 49564 x $C_{(dVdT)}$		µs
UVLO_$t_{off(dly)}$	UVLO switch turnoff delay	UVLO↓(20 mV below $V_{(UVLOF)}$) to $\overline{FLT}$↓		12		µs
OVER VOLTAGE PROTECTION INPUT (OVP)						
$t_{OVP(dly)}$	OVP switch turnOFF delay	OVP↑ (20 mV above $V_{(OVPR)}$) to $\overline{FLT}$↓		10		µs
$t_{OVP(dly)}$	OVP switch disable delay	OVP↓ (100 mV below $V_{(OVPF)}$) to FET ON		150 + 49564 x $C_{(dVdT)}$		µs
SHUTDOWN CONTROL INPUT ($\overline{SHDN}$)						
$t_{SD(dly)}$	SHUTDOWN entry delay	$\overline{SHDN}$↓ (below $V_{(SHUTF)}$) to FET OFF		0.9		µs
CURRENT LIMIT						
$t_{RCB_FLT(dly)}$	Hot-short response time	$I_{(OUT)}$ > $I_{(SCP)}$		0.3		µs
	Soft short response	$I_{(FASTTRIP)}$ < $I_{(OUT)}$ < $I_{(SCP)}$		3.3	4.2	µs
$t_{CL_PLIM(dly)}$	Maximum duration in current & (power limiting: TPS16632 Only)			162		ms
$t_{CL_PLIM_FLT(dly)}$	$\overline{FLT}$ delay in current & (power limiting: TPS16632 Only)			1.3		ms
OUTPUT RAMP CONTROL (dVdT)						
$t_{(FASTCHARGE)}$	Output ramp time in fast charging	$C_{(dVdT)}$ = Open, 10% to 90% $V_{(OUT)}$, $C_{(OUT)}$ = 1 µF;		240		µs
$t_{(dVdT)}$	Output ramp time	$C_{(dVdT)}$ = 22 nF, 10% to 90% $V_{(OUT)}$		8.35		ms
POWER GOOD (PGOOD)						
t_{PGOOD}	PGOOD delay (deglitch)	Rising and falling edges		11.5		ms
THERMAL SHUTDOWN (TSD)						
$t_{(TSD_retry)}$	Retry delay in TSD	MODE = GND		648		ms
$t_{(Treg_timeout)}$	Thermal Regulation Timeout			1.3		s

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The TPS1663x is a family of high voltage industrial eFuses. It provides robust protection for all systems and applications powered from 4.5 V to 60 V. For hot-pluggable boards, the device provides hot-swap power management with in-rush current control and programmable output voltage slew rate features using the dVdT pin. Load, source and device protections are provided with many programmable features including overcurrent, overvoltage, undervoltage. The precision overcurrent limit (±10% at 6 A) helps to minimize over design of the input power supply, while the fast response short circuit protection 300 ns (typical) immediately isolates the faulty load from the input supply when a short circuit is detected. The TPS16632 device integrate adjustable output power limiting (PLIM) functionality that simplifies the system design requiring compliance in accordance to standards like IEC61010-1. The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault signal for the downstream system. The TPS1663x monitor functions threshold accuracy of ±3% ensures tight supervision of the supply bus, eliminating the need for a separate supply voltage supervisor chip.

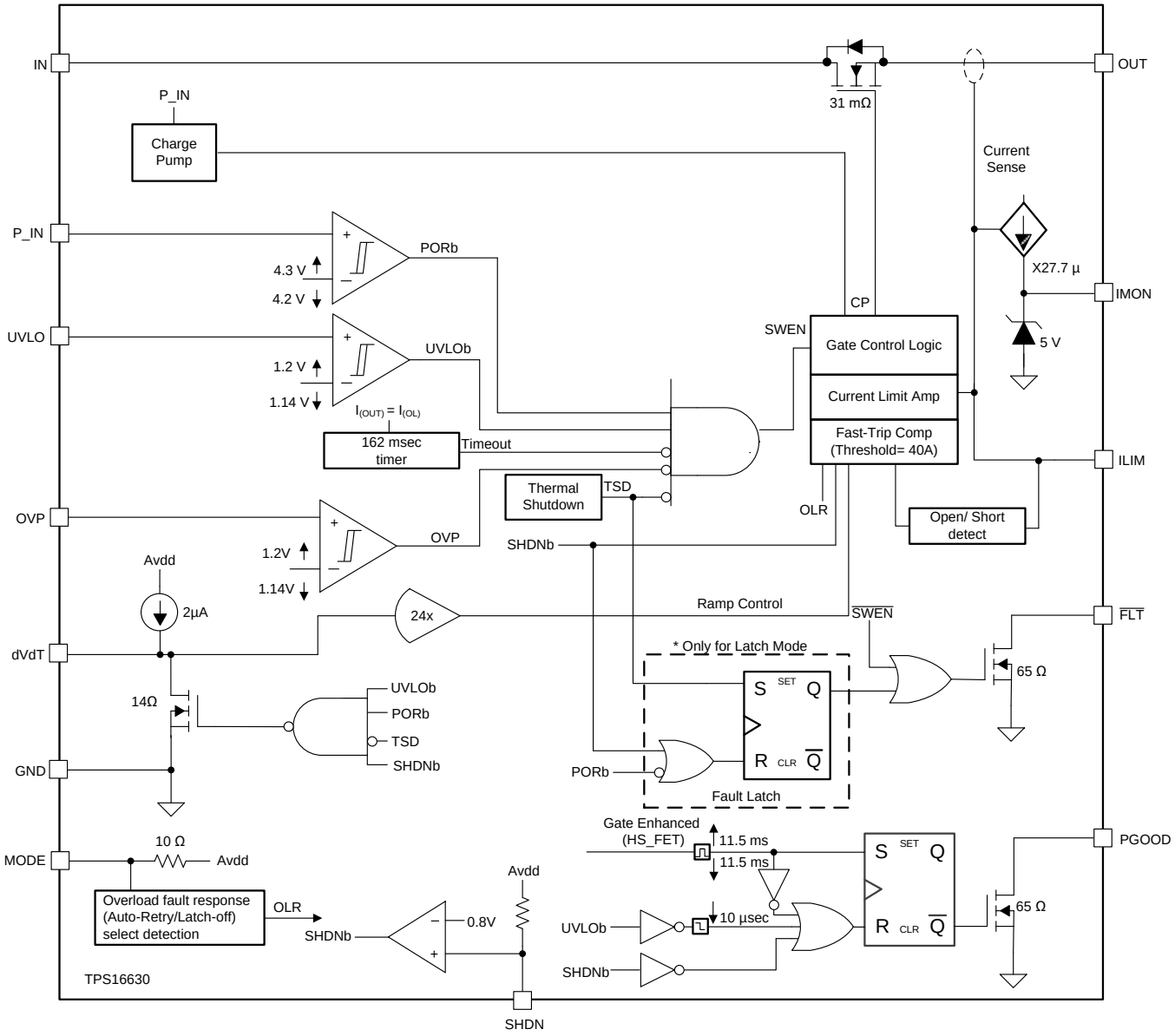
Additional features of the TPS1663x include:

- Current monitor output (IMON) for health monitoring of the system
- A choice of latch off or automatic restart mode response during current limit, Power Limit and thermal fault using MODE pin
- PGOOD indicator output
- Over temperature protection to safely shutdown in the event of an overcurrent event
- De-glitched fault reporting for supply brown-out and overvoltage faults
- Enable/Disable control from an MCU using $\overline{\text{SHDN}}$ pin

ADVANCE INFORMATION

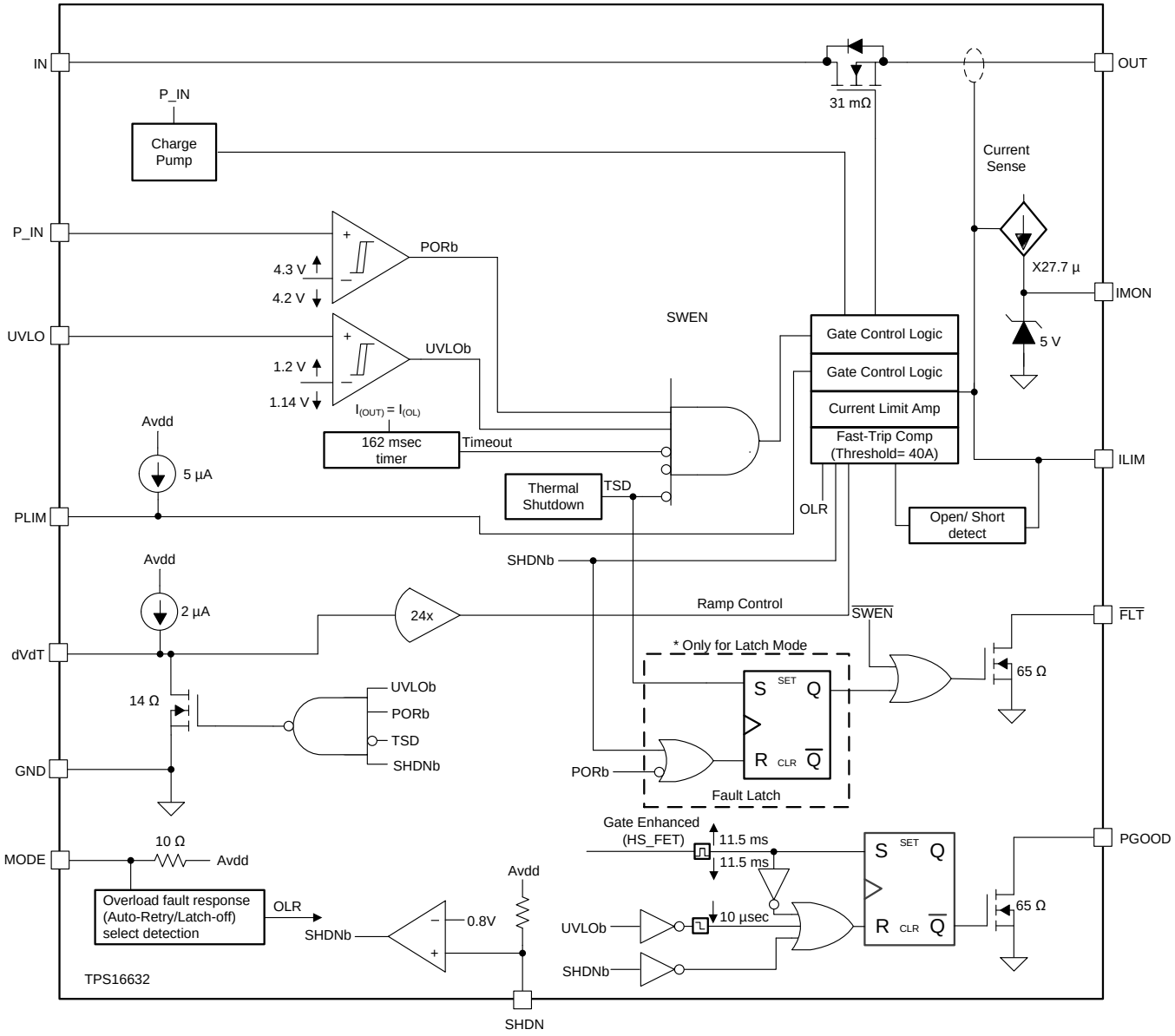
Copyright © 2018, Texas Instruments Incorporated

8.2 Functional Block Diagram



ADVANCE INFORMATION

Functional Block Diagram (continued)



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

Undervoltage comparator input. When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input undervoltage fault, the internal FET quickly turns off and $\overline{FLT}$ is asserted. The UVLO comparator has a hysteresis of 60 mV. To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to GND as shown in the Typical Application circuit. If the Under-Voltage Lock-Out function is not needed, the UVLO terminal must be connected to the IN terminal. UVLO terminal must not be left floating.

ADVANCE INFORMATION

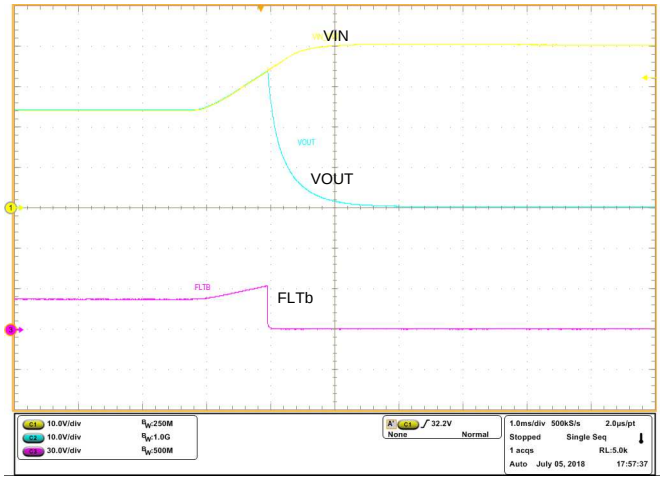
Copyright © 2018, Texas Instruments Incorporated

Feature Description (continued)

8.3.2 Overvoltage Protection (OVP)

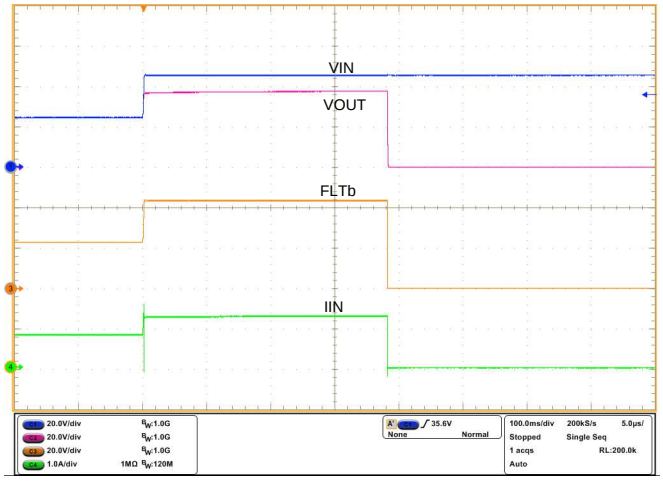
The TPS1663x incorporate circuitry to protect the system during overvoltage conditions. The TPS16630 features over voltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN supply to OVP terminal to GND as shown in the Typical Application circuit. The TPS16632 features an internally fixed 40 V maximum overvoltage clamp $V_{(OVC)}$ functionality. The TPS16632 clamps the output voltage to $V_{(OVC)}$, when the input voltage exceeds 40 V. During the output voltage clamp operation, the power dissipation in the internal MOSFET is PD = $(V_{(IN)} – V_{(OVC)}) \times I_{(OUT)}$. Excess power dissipation for prolonged period can make the device to enter into thermal shutdown.

Figure 1 illustrates the overvoltage cut-off functionality and Figure 2 illustrates the over voltage clamp functionality .



TPS16630 OVP Setting at 33 V

Figure 1. Over Voltage Cut-off Response at 33-V Level



TPS16632 C_{OUT} = 10 µF R_{LOAD} = 30

Figure 2. Over Voltage Clamp Response

8.3.3 Hot Plug-In and In-Rush Current Control

The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to GND defines the slew rate of the output voltage at power-on. The fastest output slew rate of 24/240 µscan be achieved by leaving dVdT pin floating. The inrush current can be calculated using Equation 1.

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \quad (1)$$

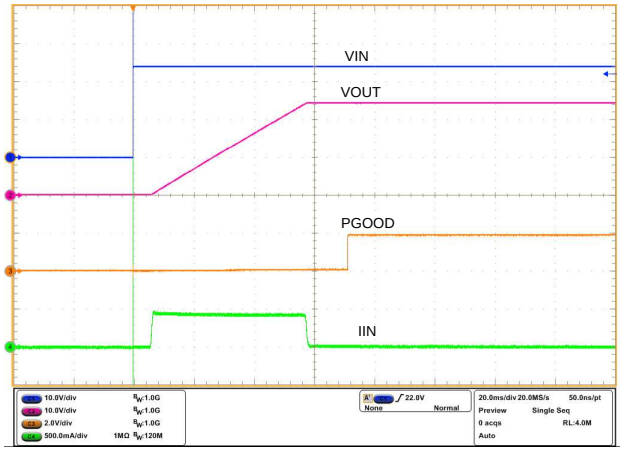
where

$$t_{dVdT} = 20.8 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

Figure 3 illustrates in-rush current control performance of the device during Hot Plug-In.

ADVANCE INFORMATION

Feature Description (continued)



C_{dVdT} = 100 nF C_{OUT} = 1000 µF R_{ILIM} = 4.02 kΩ

Figure 3. Hot Plug In and Inrush Current Control at 24-V Input

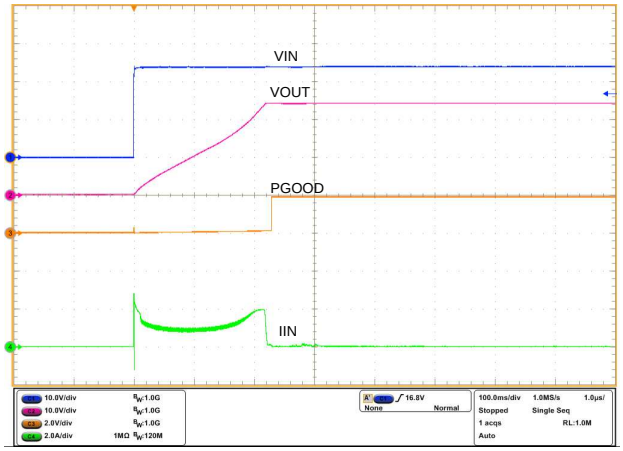
8.3.3.1 Thermal Regulation Loop

The power dissipation during power up can be calculated using Equation 3.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (3)$$

System designs requiring to charge large output capacitors rapidly or powering up an off board load may result in a higher $PD_{(INRUSH)}$ within the device causing the junction temperature to rise. Once the junction temperature rises to $T_{(J_REG)}$ level, the device starts regulating the junction temperature at $T_{(J_REG)}$ by controlling the inrush current profile through the device for a maximum duration of $t_{(Treg_timeout)}$. If the output does not charge up within this time then the internal FET is turned OFF. Subsequent operation of the device depends on the MODE configuration (Auto-Retry or latch OFF). This scheme ensures fast and reliable power up operation. Figure 4 illustrates performance of the device operating in thermal regulation loop during charging of a large output capacitor.

The Thermal regulation loop gets disabled internally after the power up when the internal FET gets fully enhanced or when the $t_{(Treg_timeout)}$ time is elapsed.



C_{dVdT} = Open C_{OUT} = 10 mF R_{ILIM} = 4.02 kΩ

Figure 4. Thermal Regulation Loop Response During Power up with Large Capacitive Load

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

Feature Description (continued)

8.3.4 PGOOD

The devices feature an open drain Power good (PGOOD) indicator output. PGOOD can be used for enable and disable of the downstream loads like DC-DC converters. PGOOD goes high when the internal FET's gate is enhanced. It goes low when the internal FET turns OFF during a fault event or when $\overline{SHDN}$ is pulled low. There is a deglitch of 11.5 msec (typical) at the rising edge and falling edge. PGOOD is a rated for 60 V and can be pulled to IN or OUT through a resistor.

8.3.5 Output Power Limiting, PLIM (TPS16632 Only)

With a fixed over current limit threshold the power limit profile increases linearly with supply input. Electrical Industrial process control equipment such as PLC CPU needs to comply with standards like IEC61010-1 for fire safety which require limited energy and power circuits. Limiting the output power becomes a challenge in such high power applications where the operating supply voltage range is wide. The TPS16632 integrate adjustable output power limiting functionality that simplifies the system design requiring compliance in accordance to this standard.

Connect a resistor from PLIM to GND as shown in Figure 5 to program the output power limiting value. If PLIM is connected to GND then PLIM feature is not activated and the device works normally with current limiting set by the external RLIM resistor.

During an over power load event the TPS16632 limits the output power at the programmed value set by PLIM resistor. This indirectly results in the device operation in current limiting mode with steady state output voltage and current set by the load characteristics and $P_{LIM} = V_{OUT} \times I_{OUT}$. The maximum duration for the device to be in power limiting mode is $t_{CL(dly)}$. Post that the device operates either in auto-retry or latch off mode based on MODE pin configuration.

$$P_{(PLIM)} = 1 \times R_{(PLIM)} \quad (4)$$

Here $P_{(PLIM)}$ is output power limit in watts, $R_{(PLIM)}$ is the power limit setting resistor in kΩ. Figure 6 illustrate output power limiting performance of TPS16632.

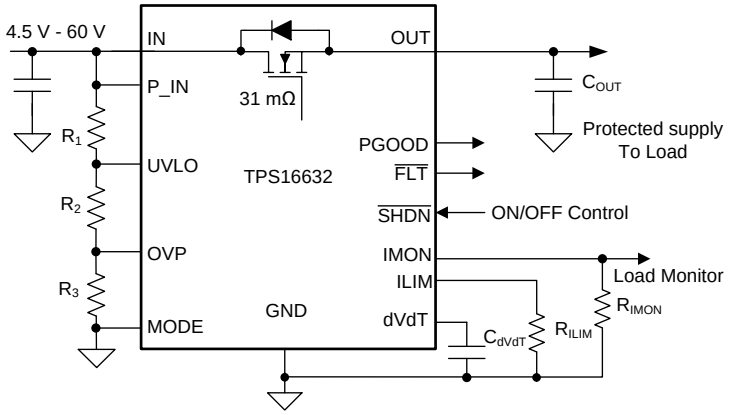
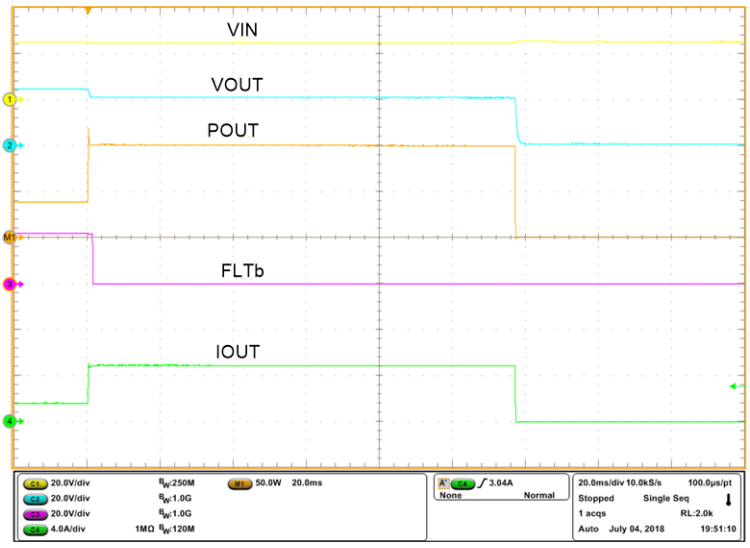


Figure 5. TPS16632 Typical Application Schematic

ADVANCE INFORMATION

Feature Description (continued)



(1)

R_{PLIM} = 100 kΩ R_{ILIM} = 3 kΩ

Figure 6. Output Power Limiting Response of TPS16632

8.3.6 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

8.3.6.1 Overload Protection

The TPS1663x devices feature accurate over load current limiting and fast short circuit protection feature. If the load current exceeds the programmed current limit I_{OL}, the device regulates the current through it at I_{OL} eventually reducing the output voltage. The power dissipation across the device during this operation will be (V_{IN}–V_{OUT}) x I_{OL} and this could heat up the device and eventually enter into thermal shutdown. The maximum duration for the over current through the FET $t_{CL(dly)}$. If the thermal shutdown occurs before this time the internal FET turns OFF and the subsequent operation (auto-retry or latch OFF) will depend on the MODE pin configuration. Set the current limit using Equation 5

$$I_{OL} = \frac{18}{R_{(ILIM)}} \quad (5)$$

where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ

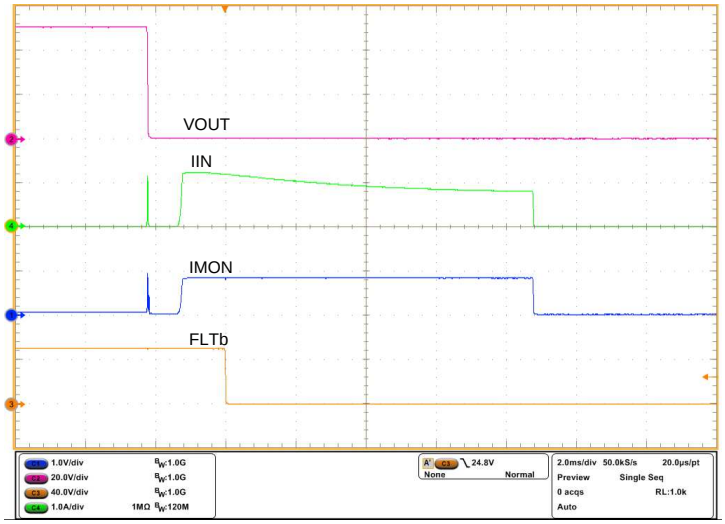
8.3.6.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF $t_{FASTTRIP(dly)}$ = 300 ns (typical) with $I_{(SCP)}$ = 40 A of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{(FASTTRIP)}$. The fasttrip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition. Figure 7 illustrates output hot-short performance of the device.

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

Feature Description (continued)



V_{IN} = 50 V R_{ILIM} = 18 kΩ

Figure 7. Output Hot-Short Response

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the over current level, $I_{(FASTTRIP)}$ through the device. Higher the over current faster the turn OFF time, $t_{FASTTRIP(dly)}$.

8.3.7 Current Monitoring

The current source at IMON terminal is internally configured to be proportional to the current flowing from IN to OUT. This current can be converted into a voltage using a resistor $R_{(IMON)}$ from IMON terminal to GND.;[terminal. The IMON voltage can be used as a means of monitoring current flow through the system. The maximum voltage range ($V_{(IMONmax)}$) for monitoring the current is limited to minimum of to ensure linear output. This puts a limitation on maximum value of $R_{(IMON)}$ resistor and is determined by Equation 6.

$$V(IMON) = \left[I(OUT) \times GAIN(IMON)\right] \times R(IMON) \quad (6)$$

Where,

- $GAIN_{(IMON)}$ is the gain factor $I_{(IMON)}$:$I_{(OUT)}$ = 27.7µA/A (Typical)
- $I_{(OUT)}$ is the load current

This pin must not have a bypass capacitor to avoid delay in the current monitoring information.

ADVANCE INFORMATION

Feature Description (continued)

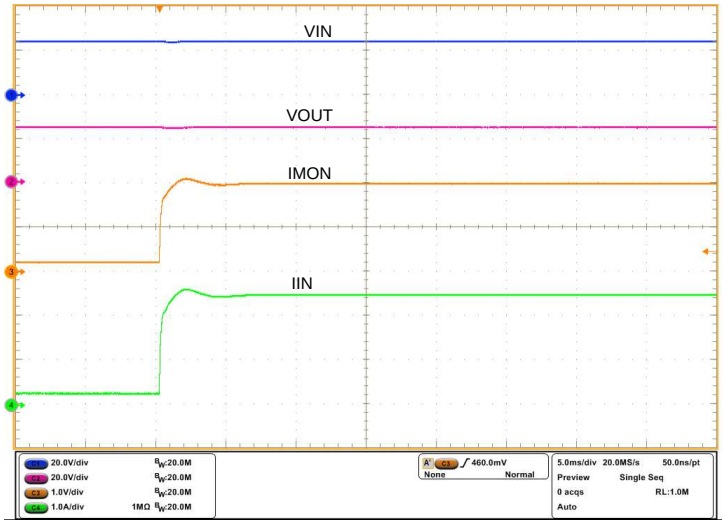


Figure 8. IMON Response During a Load Step

8.3.8 FAULT Response ($\overline{FLT}$)

The $\overline{FLT}$ open-drain output asserts (active low) under the faults events such as undervoltage, overvoltage, over load, power limiting, reverse current and thermal shutdown conditions. The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry. $\overline{FLT}$ can be left open or connected to GND when not used.

8.3.9 IN, P_IN, OUT and GND Pins

Connect a minimum of 0.1 uF capacitor across IN and GND. Connect P_IN and IN together. Do not leave any of the IN and OUT pins un-connected.

8.3.10 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FET, if the junction temperature exceeds $T_{(TSD)}$. After the thermal shutdown event, depending upon the mode of fault response, the device either latches off or commences an auto-retry cycle $t_{(TSD_retry)}$ after $T_J < [T_{(TSD)} – 11°C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ pulls low to indicate a fault condition.

8.3.11 Low Current Shutdown Control ($\overline{SHDN}$)

The internal and the external FET and hence the load current can be switched off by pulling the $\overline{SHDN}$ pin below 0.8 V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device. The device quiescent current reduces to 22 µA (typical) in shutdown state. To assert $\overline{SHDN}$ low, the pull down must sink at least 10 µA at 400 mV. To enable the device, $\overline{SHDN}$ must be pulled up to atleast 2 V. Once the device is enabled, the internal FET turns on with dVdT mode.

8.4 Device Functional Modes

The TPS1663x devices respond differently to overload with MODE pin configurations. The operational differences are explained in Table 1.

Table 1. Device Operational Differences Under Different MODE Configurations

MODE Pin Configuration	Overload Protection Operation
Open	Active Current limiting at 1x for a maximum duration of $t_{CL_PLIM(dly)}$. There after Latches OFF. Latch reset by toggling $\overline{SHDN}$ low to high or power cycling IN
Shorted to GND	Active Current limiting at 1x for a maximum duration of $t_{CL_PLIM(dly)}$. There after auto-retries after a delay of $t_{(TSD_retry)}$.

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS1663x is a 60-V eFuse, typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 60 V with programmable current limit, overvoltage, undervoltage protections. The device aids in controlling in-rush current and provides output power limiting for systems such as PLCs, Telecom Radios, Industrial Printers. The device also provides robust protection for multiple faults on the system rail. The *Detailed Design Procedure* section can be used to select component values for the device.

9.2 Typical Application

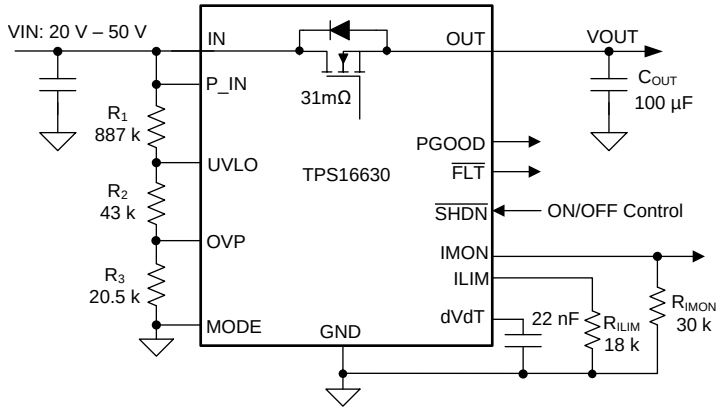


Figure 9. 20 V - 50 V, 1-A eFuse Protection Circuit for Telecom Radios

9.2.1 Design Requirements

Table 2 shows the Design Requirements for TPS16630.

Table 2. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Input voltage range	20 V - 50 V
$V_{(UV)}$	Undervoltage lockout set point	18 V
$V_{(OV)}$	Overvoltage cutoff set point	55 V
$I_{(LIM)}$	Over load Current limit	1 A
C_{OUT}	Output capacitor	100 µF
$I_{(INRUSH)}$	Inrush Current limit	300 mA

ADVANCE INFORMATION

ADVANCE INFORMATION

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Current-Limit Threshold $R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using Equation 7.

$$R_{(ILIM)} = \frac{18}{I_{OL}} = 18k\Omega$$

where

- I_{LIM} = 1 A (7)

Choose the closest standard 1% resistor value : $R_{(ILIM)}$ = 18 kΩ

9.2.2.2 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between IN, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 8 and Equation 9.

$$V_{(OVPR)} = \frac{R3}{R1+R2+R3} \times V_{(OV)} \quad (8)$$

$$V_{(UVLOR)} = \frac{R2+R3}{R1+R2+R3} \times V_{(UV)} \quad (9)$$

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)} / (R_1 + R_2 + R_3)$}, it is recommended to use higher value resistance for R_1, R_2 and R_3.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20x greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)}$ = 1.2 V and $V_{(UVLOR)}$ = 1.2 V. From the design requirements, $V_{(OV)}$ is 55 V and $V_{(UV)}$ is 18 V. To solve the equation, first choose the value of R_3 = 20.5 kΩ and use Equation 8 to solve for (R_1 + R_2) = 930 kΩ. Use Equation 9 and value of (R_1 + R_2) to solve for R_2 = 43 kΩ and finally R_1= 887 kΩ.

Choose the closest standard 1% resistor values: R_1 = 887 kΩ, R_2 = 43 kΩ, and R_3 = 20.5 kΩ.

9.2.2.3 Setting Output Voltage Ramp Time (t_{dVdT})

Use Equation 1 and Equation 2 to calculate required $C_{(dVdT)}$ for achieving an inrush current of 300 mA. $C_{(dVdT)}$ = 22 nF. Figure 10 and Figure 11 illustrates the inrush current limiting performance during 50 V hot-plug in condition.

9.2.2.3.1 Support Component Selections R_{PGOOD} and $C_{(IN)}$

The R_{PGOOD} serves as pull-up for the open-drain output. The current sink by this pin must not exceed 10 mA (see the *Absolute Maximum Ratings* table). Typical resistance value in the range of 10 kΩ to 100 kΩ is recommended for R_{PGOOD}. Figure 13 and Figure 15 illustrate the power up and power down performance of the system respectively. The C_{IN} is a local bypass capacitor to suppress noise at the input. A minimum of 0.1 µF is recommended for $C_{(IN)}$.

Copyright © 2018, Texas Instruments Incorporated

9.2.3 Application Curves

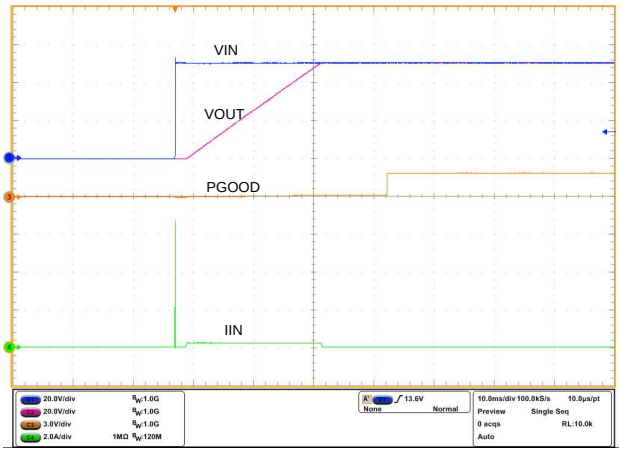


Figure 10. Hot-Plug In at 50 V Supply with No Load

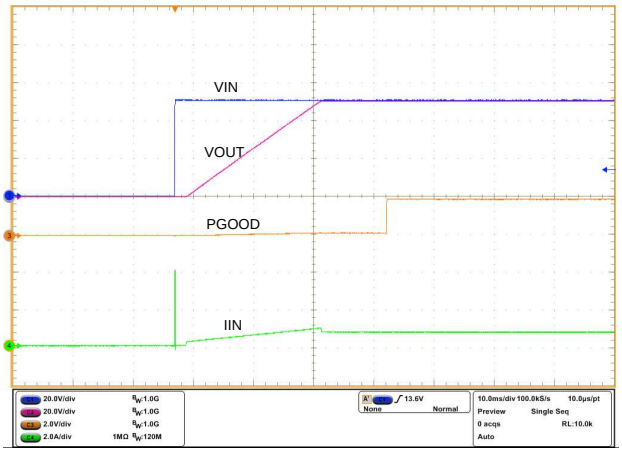


Figure 11. Hot-Plug In at 50 V Supply with 60 Ω Load

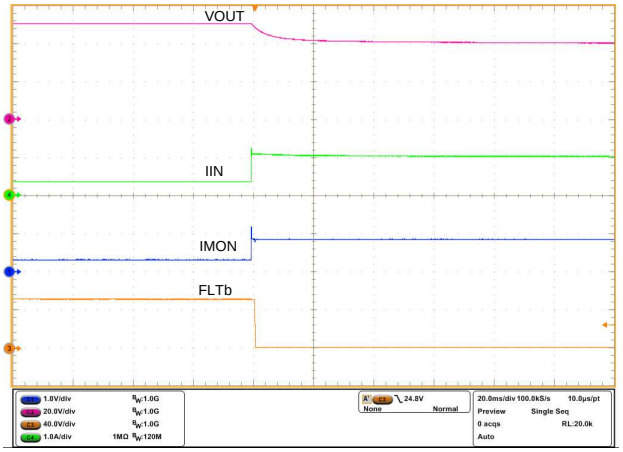


Figure 12. Over Load Performance During Load Step from 140 Ω to 40 Ω

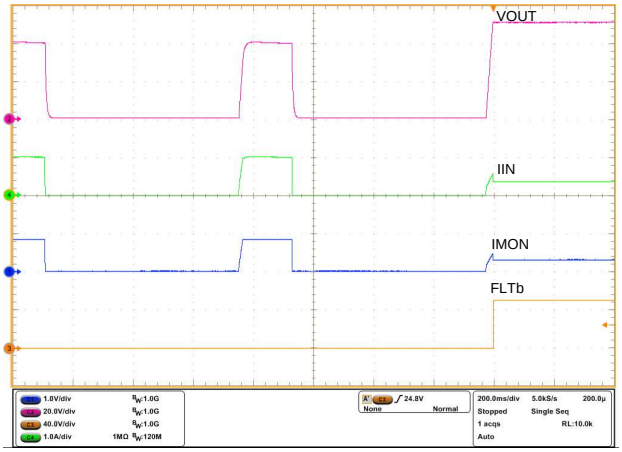


Figure 13. Coming Out of Over Load with Load Step from 40 Ω to 140 Ω

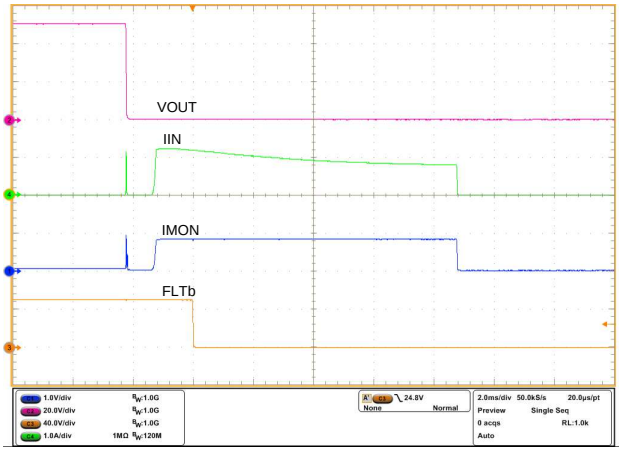


Figure 14. Output Hot-short Performance with 50 V Input Supply

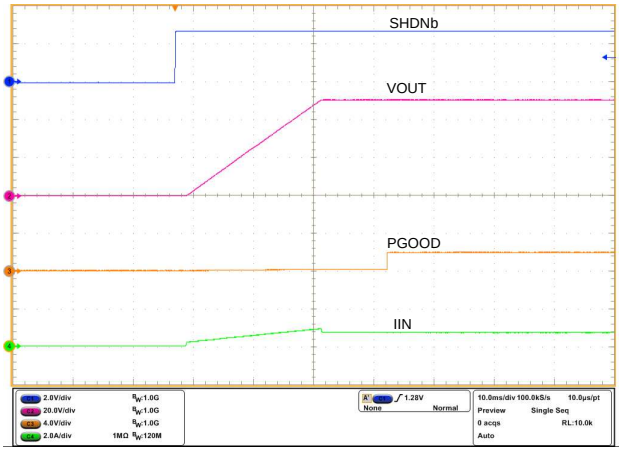


Figure 15. Turn ON using $\overline{\text{SHDN}}$ Control

ADVANCE INFORMATION

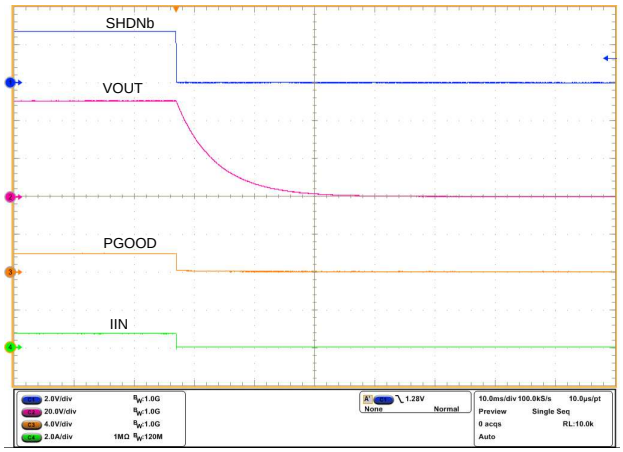


Figure 16. Turn OFF using $\overline{\text{SHDN}}$ Control

9.3 System Examples

9.3.1 Simple 24-V Power Supply Path Protection

With the TPS1663x, a simple 24-V power supply path protection can be realized using a minimum of three external components as shown in the schematic diagram in Figure 17. The external components required are: a $R_{(ILIM)}$ resistor to program the current limit, $C_{(IN)}$ and $C_{(OUT)}$ capacitors.

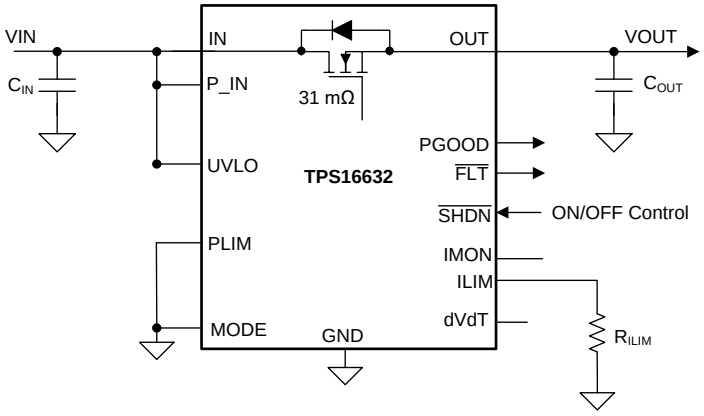


Figure 17. TPS16630 Configured for a Simple Power Supply Path Protection

Protection features with this configuration include:

- 40 V (maximum) over voltage clamp output
- Inrush current control with 24V/240 µs output voltage slew rate
- Accurate current limiting with Auto-Retry

10 Power Supply Recommendations

The TPS1663x eFuse is designed for the supply voltage range of 4.5 V ≤ V_{IN} ≤ 60 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

10.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 10.

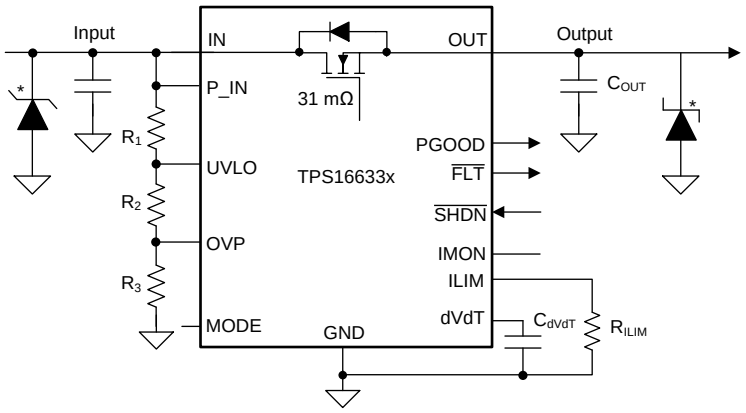
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (10)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications it is recommended to place at least 1 µF of input capacitor.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 18



* Optional components needed for suppression of transients

Figure 18. Circuit Implementation with Optional Protection Components for TPS1663x

10.2 Application Limitations

This section highlights some limitations in the application which were identified during bench evaluation of the existing TPS1663 silicon on the evaluation module (EVM)

ADVANCE INFORMATION

Application Limitations (continued)

10.2.1 Performance during Start up with short on output

The device does not turn off the internal FET after the thermal regulation max timeout of $t_{(Treg_timeout)}$, 1.3 seconds (typical). The device regulates the junction temperature at $T_{(J_REG)}$,150 °C (typical) and keeps the internal FET ON.

- Devices affected: All the variants of TPS1663 Family (TPS16630, TPS16632)

A design fix will be included in the final release of the IC.

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

11 Layout

11.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN terminal and GND.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current. See Figure 19 and Figure 20 for a typical PCB layout example.
- Locate all the TPS1663x family support components $R_{(ILIM)}$, $C_{(dVdT)}$, $R_{(IMON)}$, UVLO, OVP resistors close to their connection pin. Connect the other end of the component to the GND with shortest trace length.
- The trace routing for the R_{ILIM} component to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board GND plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications.

ADVANCE INFORMATION

ADVANCE INFORMATION

11.2 Layout Example

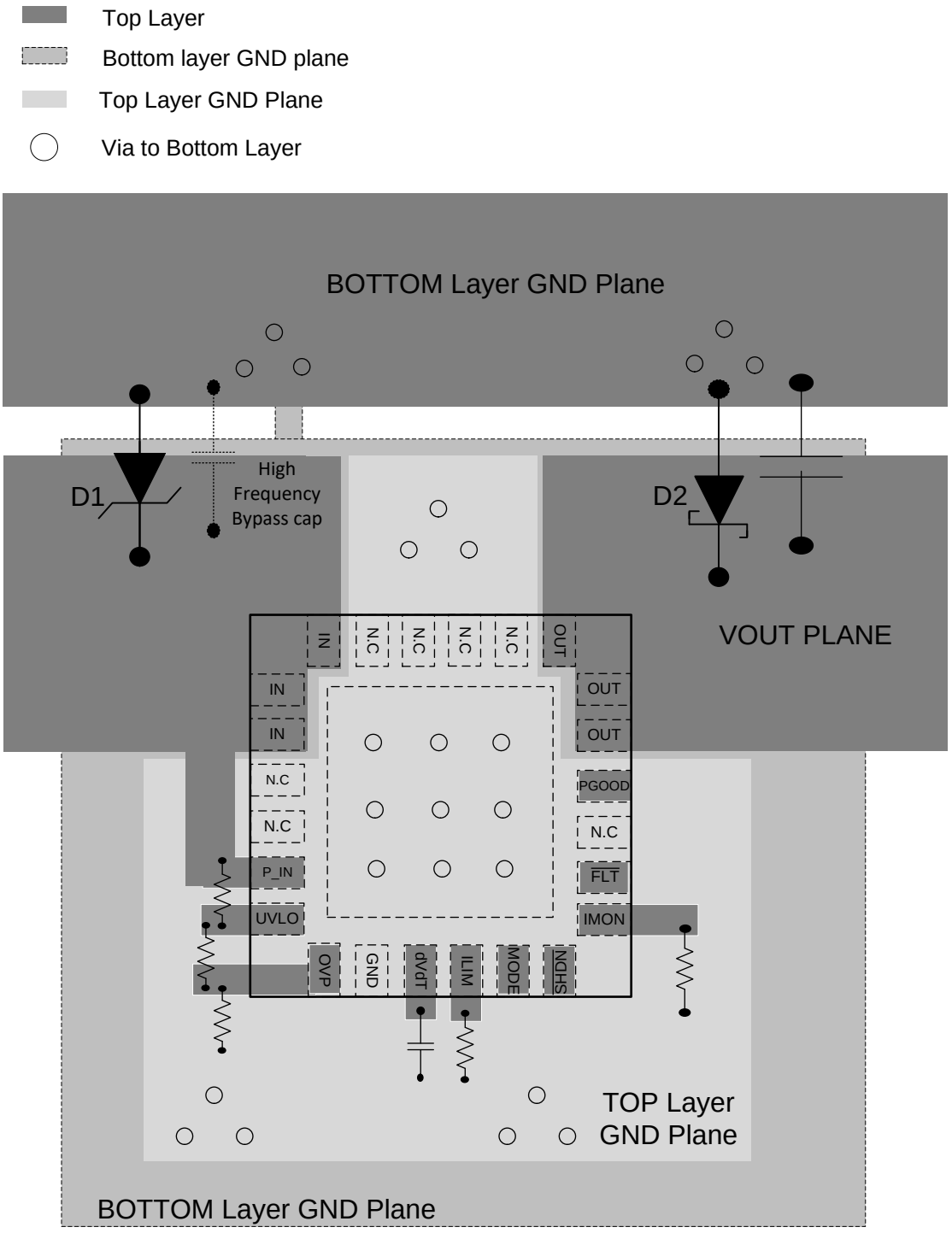


Figure 19. PCB Layout Example with QFN Package with a 2 Layer PCB

Copyright © 2018, Texas Instruments Incorporated

Layout Example (continued)

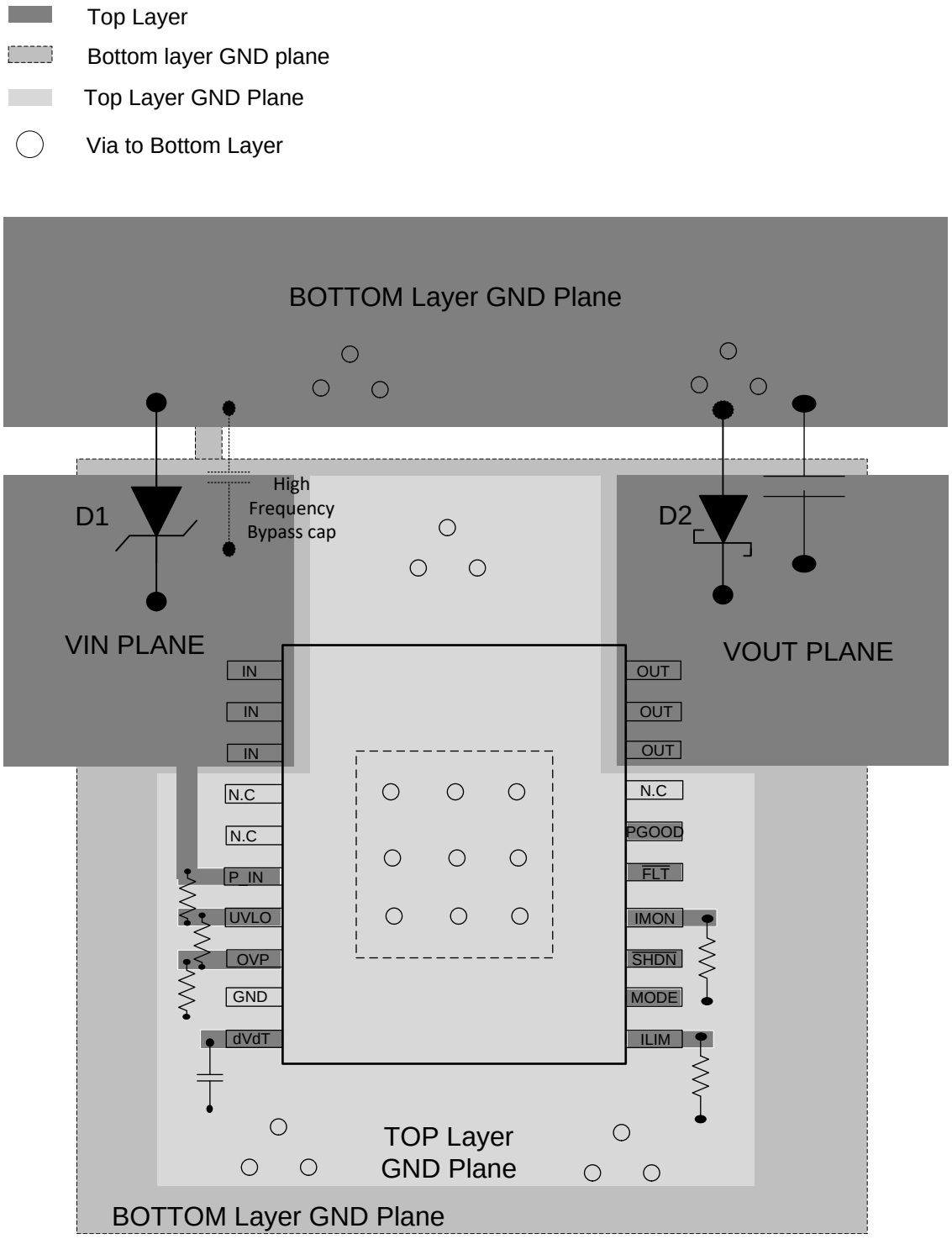


Figure 20. Typical PCB Layout Example with HTSSOP Package with a 2 Layer PCB

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

Copyright © 2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS16630RGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS16632RGET	ACTIVE	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		Samples
TPS16630RGER	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		
TPS16632RGER	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		
TPS16632RGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

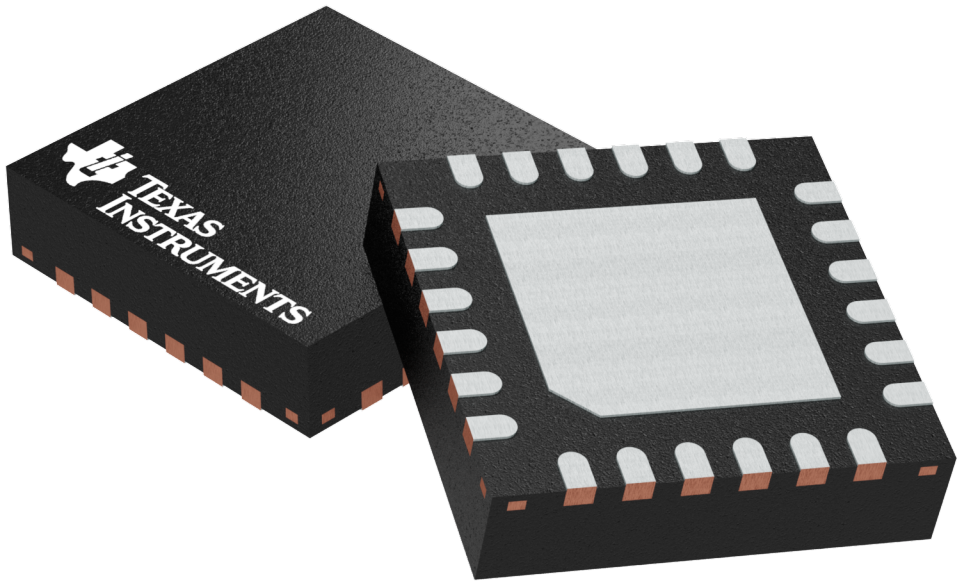
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated