LOW-FREQUENCY ANTENNA DRIVER FOR PASSIVE START AND PASSIVE ENTRY

Check for Samples: TPIC84134-Q1

FEATURES

- **Output Stage Consists of Eight Programmable Half-Bridge MOSFET Drivers (Configurable in Half, Full, or Parallel Bridges) Which Deliver Modulated Current to Each Coil**
- **Linear Mode Output: Generates a Sine Wave Voltage That is Controlled by the Microcontroller**
- **Output Stage is Overload Protected for Short and Over Temperature**
- **Driver Control and Diagnosis Blocks Drive the Gates of the MOSFETS Via Data From the SPI**
- **Antenna Diagnostics: Short to GND, Short to VBAT, And Open Load Via Current Measurement**
- **Divider Block Generates an Internal Frequency From the Input Clock (Main Controller); Used for the Internal Logic**
- **Sophisticated Failure Detection and Handling**
- **HTSSOP (PWP) 28-Pin Package**
- **Operating Temperature Range: -40°C to +105°C**

APPLICATIONS

- **Automotive Passive Start and Passive Entry Applications**

DESCRIPTION

The low-frequency (LF) antenna driver is dedicated to automotive applications requiring passive entry or passive start operational control. It allows for up to eight dedicated drivers, consisting of MOSFET transistors. The device also incorporates sophisticated diagnosis, protection and monitoring features.

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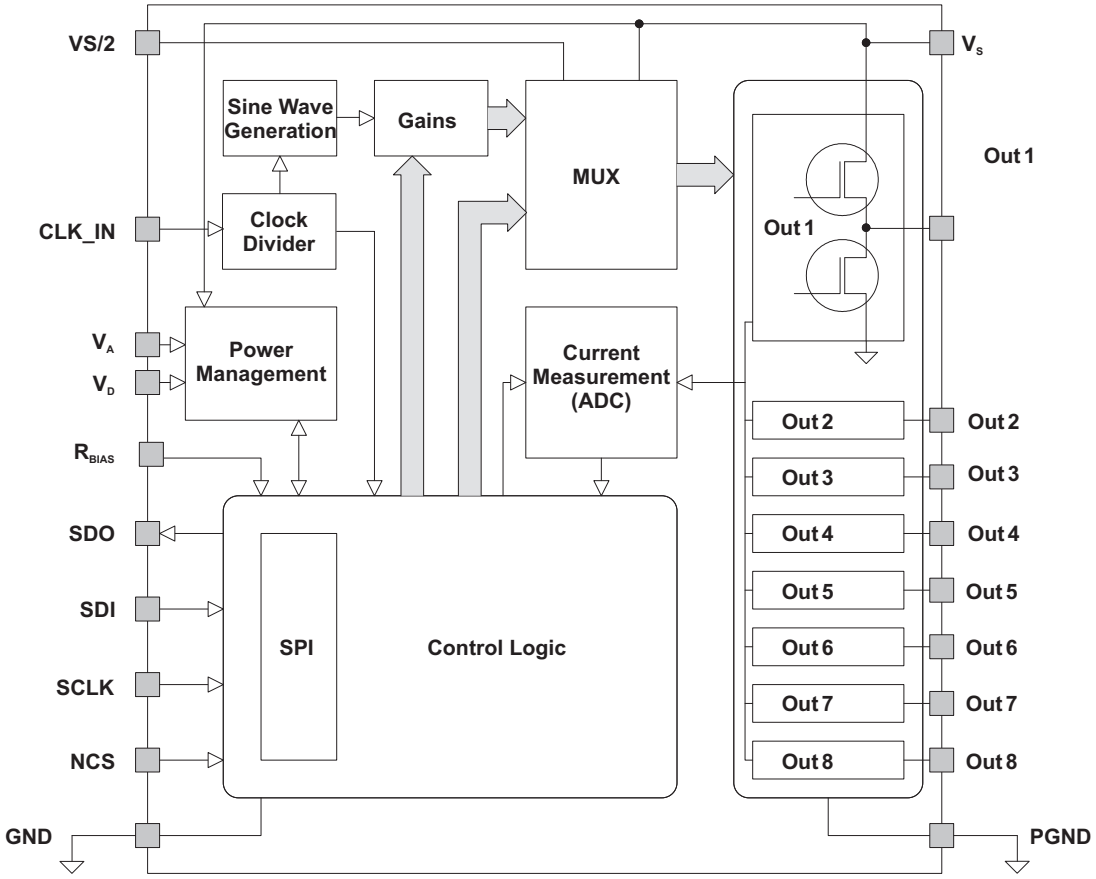

Figure 1. Block Diagram

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	HTSSOP – PWP	Reel of 2000	TPIC84134TPWPRQ1	TPIC84000TPWPRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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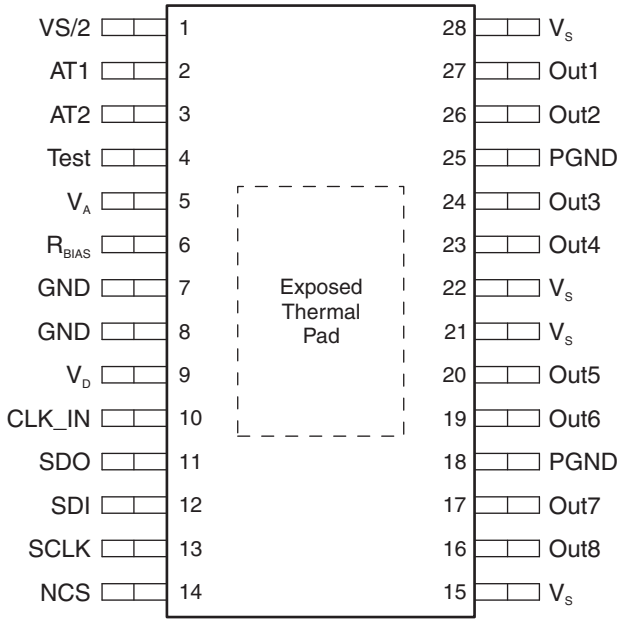
PWP PACKAGE
(TOP VIEW)



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TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
$V_S/2$	1	O	$V_S/2$ decoupling point. (Requires a 100nF, 10%, ESR < 50mΩ capacitor)
AT1	2	O	Internal use, connect to ground
AT2	3	O	Internal use, connect to ground
Test	4	I	Internal use, connect to ground
V_A	5	I	Analog 5V supply
R_{BIAS}	6	O	Current reference resistor (requires a 62kΩ, 1%, 50ppm resistor)
GND	7	-	Analog ground
GND	8	-	Digital ground
V_D	9	I	Digital 5V supply
CLK_IN	10	I	Input clock signal
SDO	11	O	Serial data out for SPI
SDI	12	I	Serial data in for SPI
SCLK	13	I	Serial clock for SPI
NCS	14	I	Chip select for SPI (active low)
V_S	15	I	Supply voltage
Out8	16	O	Output 8
Out7	17	O	Output 7
Pgnd	18	-	Power ground
Out6	19	O	Output 6
Out5	20	O	Output 5
V_S	21	I	Supply voltage
V_S	22	I	Supply voltage
Out4	23	O	Output 4
Out3	24	O	Output 3
Pgnd	25	-	Power ground
Out2	26	O	Output 2
Out1	27	O	Output 1
V_S	28	I	Supply voltage
Thermal Pad	29	-	Must be connected to ground

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DEVICE INFORMATION

The TPIC84134 is designed to control Passive Entry, Passive Start (PEPS) systems as a part of the central body control module. Functionally, the TPIC84134 transmits a magnetic field signal via antenna coils located throughout the vehicle. The data is transmitted using amplitude shift keying (ASK). Such a signal is received by an external RFID card or key, which then activates the card or key to then process and send an authenticating signal back to the vehicle, thus authenticating the driver. Once authenticated, the driver is able to open doors or start the vehicle depending on the systems specific configuration. In general, the antenna load of the TPIC84134 is a coil, which generates a magnetic field which is high enough to transmit data to the ID card, and accurate enough for location recognition outside of the vehicle.

Functional Description

Power Management

The TPIC84134 operates with three types of supply voltage: Digital 5V (V_D), Analog 5V (V_A), and Power (V_S). While V_D is used for the internal digital circuitry and V_A voltage determines:

- The accuracy of the output voltage in data and destroy modes, because the sine wave signal is derived from the V_A voltage.
- The accuracy of the current measurements, because the Current Measurement (ADC) reference voltage is derived from the V_A voltage.
- The supply currents for the IC, as the bias current is derived from the V_A voltage.

NOTE

V_D and V_A must be tied together to avoid latch up.

V_S must be powered on all V_S pins regardless of which outputs are used.

Biasing: Biasing of the circuit is done by an external resistor, R_{BIAS} = 62kΩ, 1%, 50ppm. The value of the R_{BIAS} resistance determines:

- The accuracy of the current measurements, because the ADC reference voltage is proportional to the V_A voltage divided by the value of R_{BIAS}.
- The supply currents for the IC, as the biasing current is proportional to the V_A voltage divided by the value of R_{BIAS}.

Clock Divider

The Clock Divider generates a 2.1472 MHz internal clock signal from the external clock. The internal clock frequency is used for:

- Clearing and latching the fault bits within Control and Status Register (CSR).
- For generating the frequency of the sine wave

The divider can be programmed to either: /1, /2, /4, /8, with the default being /8. Table 1 shows the possible CLK_IN input frequencies to generate 134.2 kHz signal.

Table 1. Clock Divider

Divider	CLK_IN
/1	2.1472 MHz
/2	4.2944 MHz
/4	8.5888 MHz
/8 (default)	17.1776 MHz

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To function properly the following conditions must be satisfied:

- The incoming clock (CLK_IN) has to be provided for at least 4 cycles of the internal clock after writing to Configuration register via SPI
- In the case of a wake up command (i.e. sleep bit = 0 in the Config Reg), CLK_IN has to be provided during 124 additional cycles of the internal clock for fault blanking after writing the Config Register. During that time:
  - Data1 buffer cannot be written to if sending mode bit in Config Reg is set to 1 (autosend mode).
  - SPI command "Start Transmission" cannot be programmed
- In the case of CSR read and if a fault is cleared then, CLK_IN also has to be provided during a total of 128 clock cycles for the same reason of fault blanking.

CLK_IN electrical levels:

- When the CLK_IN is OFF, the electrical level should be high (typically 5V)
- The clock should be turned OFF after a low to high transition of CLK_IN

Sine Wave Generation

The sine wave generation block generates the 134.2 kHz sine wave from the internal clock. This sine wave is used to generate the carrier frequency which is used for transmitting the signal as well as Destroy bits.

Note that the Destroy bits consist of bringing the selected channel to $V_S/2$, transmitting a small number of bits (1-4 programmable through SPI) at a reduced peak-to-peak voltage, then the channel is grounded again (HS off, LS on). The purpose of the destroy bits is to actively stop any unwanted transmission signal that may be present on the antenna due to coupling from the transmitting antenna.

For example, Figure 2 shows the first 6 Transmitted Bits (3 Manchester Bits) of a telegram together with three destroy bits on the non-active outputs. The counter for start of destroy bits is set to 3, and it starts counting down at the beginning of the transmission telegram denoted by "start" in the below diagram.

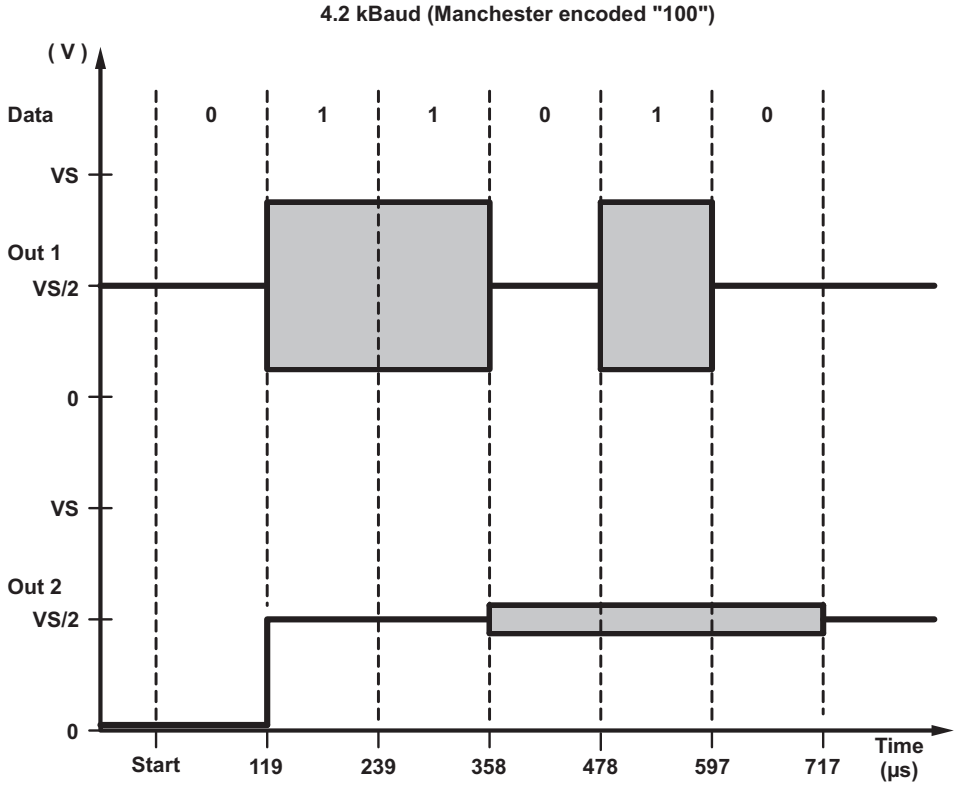

Figure 2. Transmitted Telegram Sample With Destroy Bits

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Gains

Gain1 is a programmable gain for the output antenna working in normal mode to control the transmission power.

Gain2 allows the user to change the gain of the transmitted telegram for a programmable number of data bits after which the telegram is continued in gain1. The time at which gain2 begins is programmable in the CSR; alternatively, if the length of bits sent in gain2 is zero (0) the entire telegram is transmitted in gain1. Note, these gains are not cascaded; it is either Gain1 or Gain2.

Gain for destroy bit transmission dictates the gain for the output channels set to "destroy bits". The gain for destroy bits is a logarithmic scale and it is set to 500 mVpp by default.

Figure 3 shows an example in which Out1 is configured to transmit the telegram, using both Gain1 and Gain2. The counter for start of transmission with Gain2 = 2 Bytes, and the counter for transmission in gain2 = 16 bits. Note that the transmission resumes at Gain1 after the transmission at Gain2. The diagram also displays Out2 with destroy bits where counter for start of destroy bits = 8 bits, and Length of destroy = 4 bits.

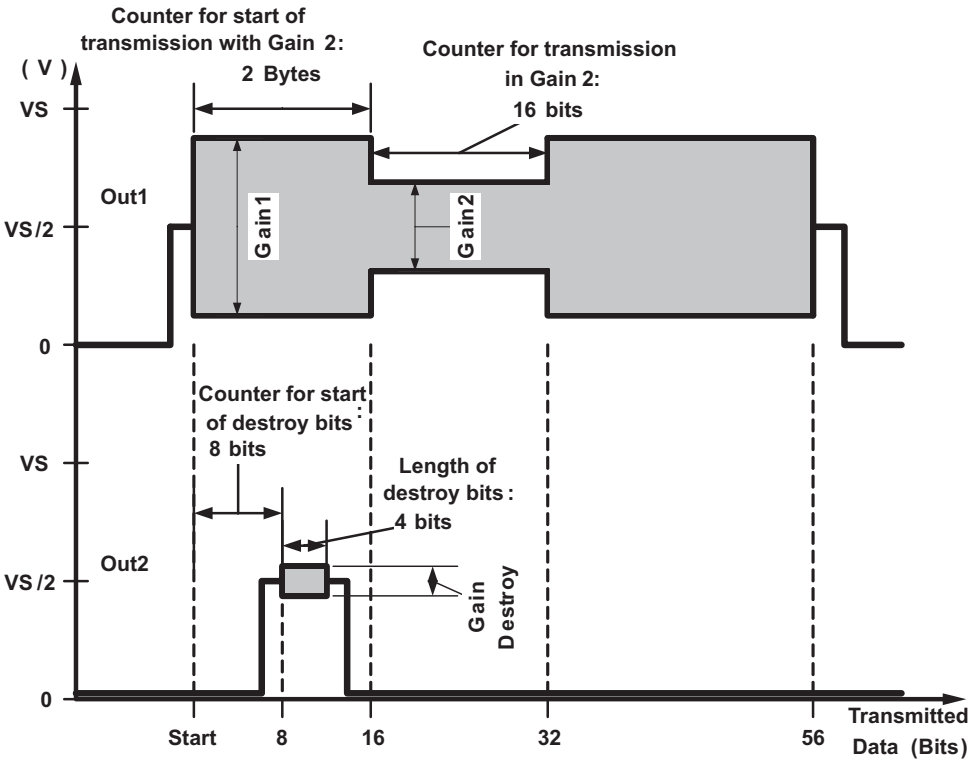

Figure 3. Transmitted Telegram Sample Gain1 And Gain2

Multiplexer (Mux)

A multiplexer is used to pick between the various gains of the signal to each output, as well as selecting the phase (0° or 180°) of the transmitting antennas.

A maximum of two outputs, or 2 half-bridges, can be activated at the same time in normal mode, where each is designed to drive the required power into the antenna. Further, all other outputs can also be activated with destroy bits at the same time(at a lower Vpp). As the bridges operate in a linear mode, the sine wave generation at the bridge output is optimized to reduce EMI emissions and power dissipation.

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Current Measurement

From a system's point of view, diagnostics of the antenna operation is done by measuring the load current across the antenna and providing the measured value to the microcontroller via SPI. The microcontroller retrieves the current value and evaluates if there is a failure or not. Within the TPIC84134 the current measurement is done at each Low Side-transistor (LS), though the measurement of the various currents is done sequentially (i.e. first LS1 measurement followed by the LS2 measurement, etc.). The actual measured analog values are converted into five bit resolution digital values and are then stored in the control and status register.

As the load current can take between 2 to 10 wave-forms to reach its maximum value; current measurement can depend on the actual application and the specific Q-factor of the antenna circuit. Therefore it is necessary to program the exact time when the current measurement must be performed, and it is also necessary to measure at the specific time within the wave to measure the maximum value.

A programmed parameter indicates which outputs are measured, where the low side of the programmed output is measured sequentially. Here the edge (rising or falling) is also programmed, where during the odd (1st, 3rd, 5th, etc) rising or falling edge, the current on the low side of the first programmed output is measured; during the even (2nd, 4th, 6th, etc) rising or falling edge, the current in the low side of the second programmed output is measured. The measurement is performed continuously and the current value updated (over written) every time within the Control and Status register.

Figure 4 shows an example of current measurement in a full-bridge configuration. In order to diagnose the operation of the device in full-bridge, it is necessary to measure the current of LS1 and LS2. The two measured values are stored in the Control and Status register.

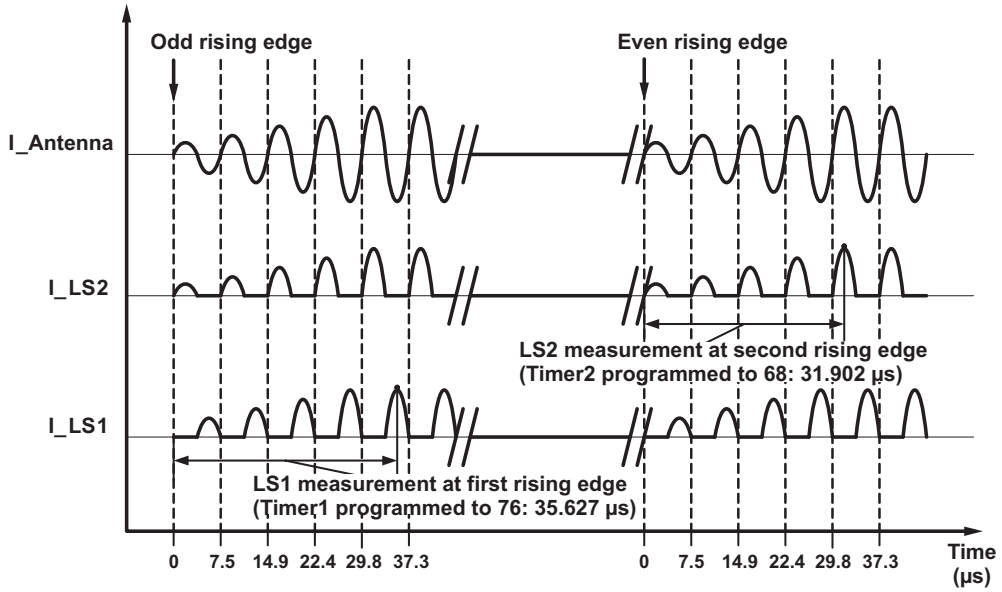

Figure 4. Current Measurement Timing For Full Bridge Setup

Control Logic

The control logic block contains the SPI interface along with all the other circuitry necessary to convert the SPI commands into the desired outputs.

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Operation Modes

There are two operating modes: SLEEP mode and WAKE-UP mode.

In WAKE-UP mode, the device is either ready for the next transmission, or it is transmitting data. The wake-up command and the output configuration command are separated to avoid noise on the $V_S/2$ signal at wake up. Note that the start command must happen at least 128 clock cycles after the wake-up command. The device transitions from the WAKE-UP mode to the SLEEP mode when the following conditions occur:

- The Sleep bit in Configuration Register is set to 1 via SPI
  or
- An over temperature fault condition is detected
  or
- V_S or V_D under voltage is detected

In SLEEP mode, the sine wave generation block is off, the outputs are in tri-state, the SPI is functioning, but the flags are not updated. The device goes from SLEEP mode to WAKE-UP mode when the following conditions occur:

- The Sleep bit is set to 0 via the SPI
  or
- The Sleep bit is set to 0 via the SPI and the CSR is read in case of an over temperature detection or V_S under voltage

NOTE

When operating in the tri-state mode, there is a pull down of typically 150 kΩ at the Outx pins.

Diagnosis

As a function of protecting the TPIC84134 various diagnostic features such as over temperature warning, over temperature pre-warning and energy limiting protection have been implemented. Flags within a register are used to highlight a particular fault, or diagnosis, to the main controller, where each fault is essentially latched within the register until it is read by SPI interface. After having been read by the SPI, the register is then cleared. This protection scheme is implemented within the TPIC84134 itself, as follows:

Over Temperature

When over-temperature occurs while the device is operating in WAKE-UP mode; where upon over temperature the device goes to SLEEP mode and the "over temperature" and "failure" flags are set to 1 in the CSR.

If the device is in SLEEP mode, it stays in this mode but no SPI flag is updated.

Temperature Pre-Warning

Temperature pre-warning has no impact on the operating mode of the device. If the device is in WAKE-UP mode, the "temperature pre-warning" flag is set to 1 in the CSR; if the device is in SLEEP mode, no SPI flag is updated.

Under Voltage

- V_S under voltage: Occurs when V_S goes below the V_S under voltage threshold
  - If the device is in WAKE-UP mode, it goes to SLEEP mode and the "under voltage at V_S" and "failure" flags are set to 1 in the CSR.
  - If the device is in SLEEP mode, it stays in this mode but no SPI flag is updated.
- V_D under voltage: Occurs when V_D goes below the V_D under voltage
  - If the device is in WAKE-UP mode, it goes to SLEEP mode and the "under voltage at V_D" and "failure" flags are set to 1 in the CSR.
  - If the device is in SLEEP mode, it stays in this mode but no SPI flag is updated.

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IFAULT Flag: Energy Limiting Scheme

Two types of output device energy limiting schemes are used:

1. Detection of DC currents flowing in the output transistors

   In normal operation, with an AC coupled load, continuous DC currents of greater than several mA will not flow in the output transistors. If a current greater than 150mA (nominal) flows in either output transistor for a duration greater than 4μs then the IFAULT condition will be activated and that channel will be placed in tri-state. The exact time before the IFAULT is activated is a function of the voltage across the transistor conducting >150mA load current. Larger voltages across this transistor will cause the deglitch time to be shorter. With V_S = 38V and with the output at V_S/2 the minimum deglitch time is 4μs. The deglitch timer is reset when the current level falls below 150mA.

2. Detection of excess bi-directional peak currents flowing in the output transistors

   If a current greater than 0.9A flows in both output transistors when the sine wave signal is driven through the output transistors, then the IFAULT condition will be activated and that channel will be placed in tri-state. The IFAULT condition is activated when both high side and low side transistors have conducted >0.9A at any time during the sine wave burst. The IFAULT signal will be activated immediately when the second output transistor current exceeds 0.9A. The high side and low side detectors are reset during the transmission of a "0" bit.

IFAULT has no impact on the operating mode.

- If the device is in WAKE-UP mode, the "IFAULT" and "failure" flags are set to 1 in the CSR and the channel which has failed is put in tri-state.
- If the device is in SLEEP mode, no SPI flag is updated. However the data buffer will continue to be read out until software stops the data buffer read by sending new Configuration data.

SPI Interface

A Serial Peripheral Interface (SPI) circuit is integrated into the device to set various internal registers and read out current measurement and status information from the drivers. TPIC84134 operates in slave mode and the microcontroller always acts as a master. The interface to the external micro-controller consists of 4 pins: NCS, SCLK, SDO and SDI.

SPI Frame Structure

Each SPI communication frame for the TPIC84134 has a length of 64 bits, where it is forbidden to send more than 64 bits. Each 64bit frame consists of 8 command-bits and 56-data-bits. The format of the 64 bits entering at SDI and sent out at SDO is shown in Figure 5:

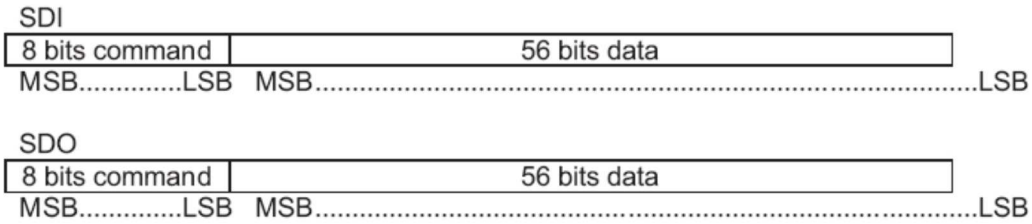

Figure 5. SPI Frame Structure

The MSB is the first "in" at the SDI and first "out" at the SDO, where the command sent out on SDO is the command that was sent in the SDI's previous cycle

When NCS is high, any signals at the SCLK and SDI pins are ignored, and the SDO is forced into a high impedance state.

During a High to Low transition on NCS, the SPI response word is loaded into a shift register, where the SCLK pin must be low when NCS goes low.

At each rising edge of SCLK after NCS goes low, the response bit is serially shifted out on the SDO pin. Further, the Control and Status register has to be cleared after readout at next NCS falling edge.

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At each falling edge of SCLK (after NCS goes low), a new control bit is serially shifted in from the SDI pin. The SPI command is decoded to determine the destination address for the associated data. After a complete frame is received, during the next low to high transition on NCS, the SPI shift register data is transferred into the internal memory at the last decoded address.

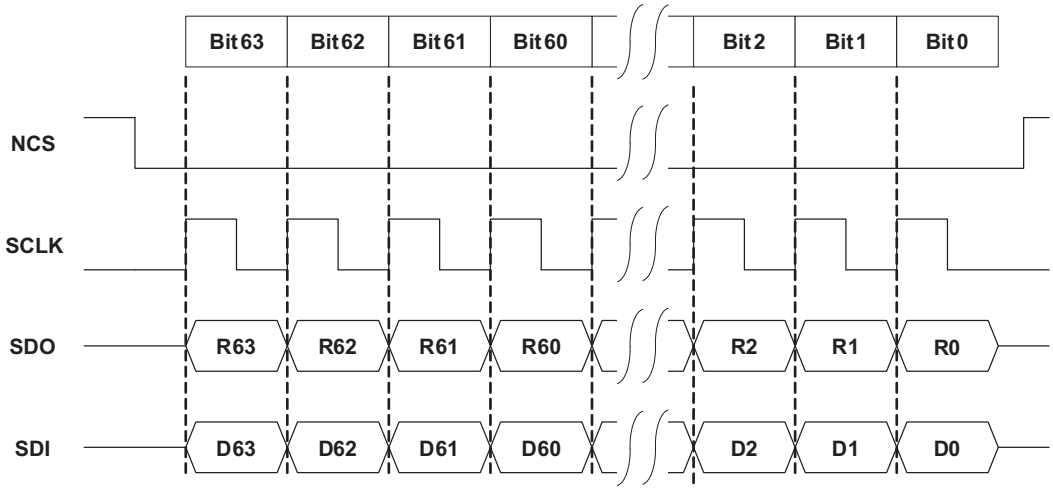

Figure 6. SPI Protocol

Each SPI register in TPIC84134 has a length of 56 bits. The device has two registers for data transmission, one configuration register and one control and status register (CSR).

Buffers for Data Transmission

The TPIC84134 has two buffers for data transmission with a size of 56 bits each, thus a maximum of 112bits can be stored. After transmission begins, in order for the telegram to be endless, the buffers must be reloaded continuously. The inactive buffer can be reloaded while the TPIC84134 is transmitting from the active buffer, and the active buffer cannot be reloaded during transmission.

SPI Command Structure

The encoding of the specific SPI commands is based on, and specifically limited within the SPI shift register, to 64bits. Table 2 highlights the required basic commands to be sent via SPI. The encoding is optimized to reduce the size of the digital part and to fulfill the application software preferences. One command and its associated data are sent in the same frame. Any un-specified command or frame received by TPIC84134 will take the device into an undefined state.

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Basic Commands and Data Structure

Table 2. Commands

COMMAND MSB....LSB	COMMAND DESCRIPTION	DATA SENT ON SDO AT NEXT FALLING EDGE OF NCS
0xxx xxxx	Read back the programmed register. Programmed register will be loaded into SPI register at next falling edge of NCS.	Programmed register
1xxx xxxx	Request control and status register. The control and status register will be loaded into SPI register at next falling edge of NCS.	Control and status register
1000 xxxx x110 xxxx x111 xxxx	No operation only feedback. Data bits are unused. The control and status register will be loaded into SPI register at next falling edge of NCS.	Control and status register
0000 xxxx	No operation only feedback.	All bits '0'
x001 xxxx	Program configuration register. Data bits contain data for configuration register.	Programmed register or control and status register depending on MSB
x010 xxxx	Program control and status register. Data bits contain data for control and status register.	Control and status register whatever is the MSB
x011 xxxx	Program data buffer1. Data bits contain data for buffer1.	Programmed register or control and status register depending to MSB
x100 xxxx	Program data buffer2. Data bits contain data for buffer2.	Programmed register or control and status register depending to MSB
x101 xxxx	Start transmission. Data bits are unused. (When not in automode)	Control and status register

The command that is sent out on SDO is the command that was sent on SDI at the previous cycle. The fifth MSB bit is a failure bit which is set to '1' by the device when one of the following failures occurs: over temperature, temperature pre-warning, under voltage at V_S or V_D, output over-current. Default is '0' for this bit then value is latched until is read by SPI. This bit is the same as bit 18 in Control and Status register.

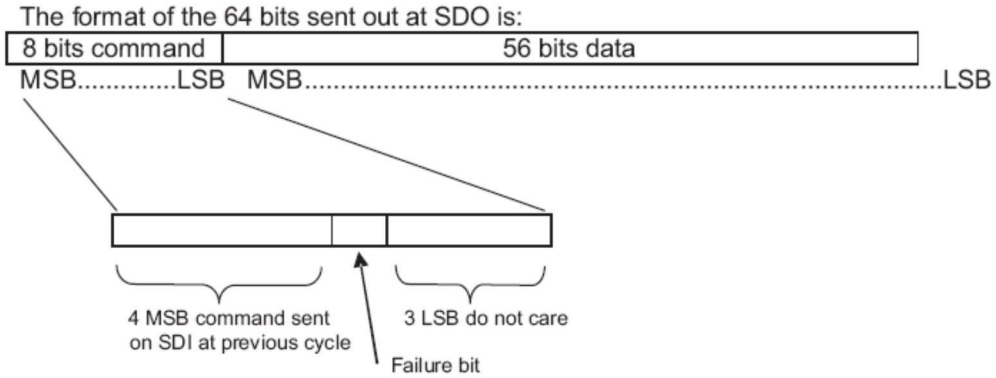

Figure 7. Format for 64 Bits Returned on SDO

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Register Definitions

Table 3. Register Definitions

NAME	NO. OF BITS	DESCRIPTION	DEFAULT VALUE AT POR	MODE R/W
SPI register	64	8 bit command 56 bit data	0.....0 0.....0	R/W
Data buffer 1	56	56 bit data	0.....0	R/W
Data buffer 2	56	56 bit data	0.....0	R/W
Configuration register				
clock division	2	00 = no division 01 = division by 2 10 = division by 4 11 = division by 8	Division by 8	R/W
baud rate	1	0 = 8.37 kHz Baud 1 = 16.75 kHz Baud	1	R/W
output 1	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
output 2	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
output 3	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
output 4	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
output 5	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
output 6	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
output 7	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
output 8	2	00 = LowSide "ON" – HighSide "OFF" 01 = transmit data with 180° phase 10 = transmit data with 0° phase 11 = transmit destroy bits	LowSide "ON" HighSide "OFF"	R/W
Gain1 for data transmission	5	00000 = 1Vpp 00001 = 2Vpp … 11111 = 32Vpp n = (n+1)Vpp	28Vpp (11011)	R/W
Gain2 for data transmission	5	00000 = 1Vpp … 11111 = 32Vpp n = (n+1)Vpp	14Vpp (01101)	R/W
gain for destroy-bit transmission	4	0000 = 32/(2^15) Vpp 0001 = 32/(2^14) Vpp … 1111 = 32 Vpp	32/(2^6) Vpp (1001)	R/W

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Table 3. Register Definitions (continued)

NAME	NO. OF BITS	DESCRIPTION	DEFAULT VALUE AT POR	MODE R/W
counter for start of transmission with gain2	6	00 0000 … 11 1111 = after 63 data bytes after x bytes the transmission will be sent with gain 2	00 0000	R/W
counter for bits transmitted with gain2	7	000 0000 = 0 bit … 1111111 = 127 bit	000 0000	R/W
counter for start of transmit destroy bits	6	After x normal bits, destroy bits will be transmitted. Values '000 000' and '000 001' are not allowed. If they are programmed, this will give '000 010'.	000 010	R/W
length of destroy bit	2	00 = 1 bit … 11 = 4 bit	1 bit	R/W
selection of sending mode	1	0 = wait for trigger command via SPI 1 = start transmission as soon as buffer1 has received the full 56 bits	1	R/W
Sleep bit	1	0 = wake-up mode 1= sleep mode (outputs are tri-state during this mode)	1	R/W
Control and Status Register				
timer1 for current measurement 1	9	time from 699ns to 237.75µs after selected edge (rising or falling) 1st, 3rd ,5th ... 00...000: not used 00..001: 699 ns 00..010: 1164 ns 00..011: 1630 ns … 11..101: 232.63 µs 11..110: 237.75 µs 11..111: not used Timer (ns) = 232.86 ns + Bit data * 465.7228 ns (1) (2)	00..001	R/W
Must be set to "1" by micro	1	Bit must be set to "1" by the microcontroller to ensure accurate current measurement	0	R/W
timer2 for current measurement 2	9	time from 699ns to 237.75µs after selected edge (rising or falling) 1st, 3rd ,5th ... 00...000: not used 00..001: 699 ns 00..010: 1164 ns 00..011: 1630 ns … 11..101: 232.63 µs 11..110: 237.75 µs 11..111: not used Timer (ns) = 232.86 ns + Bit data * 465.7228 ns (3) (4)	00..001	R/W
Must be set to "1" by micro	1	Bit must be set to "1" by microcontroller to ensure accurate current measurement	0	R/W
trigger for measurement1	1	0 = measurement is done at 1st, 3rd ,5th ... rising edge of Data_bit 1 = measurement is done at 1st , 3rd,5th... falling edge of Data_bit	rising edge of Data_bit	R/W
trigger for measurement2	1	0 = measurement is done at 2nd , 4th,6th... rising edge of Data_bit 1 = measurement is done at 2nd , 4th,6th... falling edge of Data_bit	rising edge of Data_bit	R/W
selected output for measurement1	3	000 = output 1 selected 001 = output 2 selected 010 = output 3 selected 011 = output 4 selected …	0	R/W

(1) The programmed value must not exceed the duration of one bit at the chosen baud rate.
(2) The programmed value can not be max value.
(3) The programmed value must not exceed the duration of one bit at the chosen baud rate.
(4) The programmed value can not be max value.

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Table 3. Register Definitions (continued)

NAME	NO. OF BITS	DESCRIPTION	DEFAULT VALUE AT POR	MODE R/W
selected output for measurement2	3	000 = output 1 selected 001 = output 2 selected 010 = output 3 selected 011 = output 4 selected …	1	R/W
unused	2	Bits unused		-
mode of device	2	0x = ready for next transmission 10 = busy – transmitting data 1 11 = busy – transmitting data 2	additional there is the sleep mode	R
Sleep status	1	0 = wake-up mode 1= sleep mode (outputs are tri-state during this mode)	1	R
temperature pre-warning	1	0 = below pre-warning temperature 1 = above pre-warning temperature	Default is '0' then value is latched until it is read by SPI	R
over-temperature	1	0 = no over-temperature 1 = over-temperature	Default is '0' then value is latched until it is read by SPI	R
under voltage at V_D	1	0 = normal supply voltage at V_D 1 = under voltage at V_D	Default is '0' then value is latched until it is read by SPI	R
under voltage at V_S	1	0 = normal supply voltage at V_S 1 = under voltage at V_S	Default is '0' then value is latched until it is read by SPI	R
failure	1	0 = no failure 1 = one of the following failures: over-temperature, under voltage at V_S, or V_D output over-current.	Default is '0' then value is latched until it is read by SPI	R
output over-current	8	0000 0001 = over-current on output 1 0000 0010 = over-current on output 2 0000 0011 = over-current on outputs 1 and 2 0000 0100 = over-current on output 3 …	Default is '0000 0000' then value is latched until it is read by SPI	R
current value 1	5	measured current at one active output	Default is '0 0000' then value is latched until new measurement is done	R
current value 2	5	measured current at other active output	Default is '0 0000' then value is latched until new measurement is done	R

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Table 4. Typical Sequence of Commands

1.)	SPI Frame:	0001 xxxx	Program configuration register for wake up (outputs configured: High Side OFF – Low Side ON)
			SDO: Returns programmed register (config. Reg. in this case) Note 1.
2.)	SPI Frame:	0001 xxxx	Program configuration register for output configuration
			SDO: Returns programmed register (config. Reg. in this case)
3.)	SPI Frame:	0011 xxxx	Program data1
			SDO: Returns configuration data programmed in previous frame
4.)	SPI Frame:	0100 xxxx	Program data2
			SDO: Returns data1 programmed in previous frame
5.)	SPI Frame:	*000 xxxx	No command
			SDO: Returns data2 programmed in previous frame
6.)	SPI Frame:	1010 xxxx	Program triggers & timers for current measurement for diagnosis
			SDO: Returns Config. Reg. or CSR (depending on MSB in last frame)
7.)	SPI Frame:	1101 xxxx	Start transmission
			SDO: Returns CSR (Control and Status register)
8.)	SPI Frame:	1010 xxxx	Re-program triggers & timers for new current measurement for diagnostics
			SDO: Returns updated CSR (Control and Status register)
9.)	SPI Frame:	*000 xxx	No command
			SDO: Returns Config. Reg. or CSR (depending on MSB in last frame)
10.)	SPI Frame:	*001 xxx	Program config. Reg. for Sleep mode
			SDO: Returns Config. Reg. or CSR (depending on MSB in last frame)

SPI Registers

Before being programmed, at POR, the TPIC84134 is in the default configuration. The default mode is sleep mode and waiting for NCS. After POR, the SPI register (8bits command, 56bits data) is all "0". When it is in sleep mode, the device will wake up when a "0" is programmed to "sleep bit" in configuration register. At wake up, the registers remain with the same content as before standby. The wake-up command and the output configuration command are separated to avoid noise on $V_S/2$ signal at wake-up. The start command must happen at least 64 µs after the wake-up command. For transmission of LF on outputs, the MSB which is the first bit in the data buffer is first out on LF driver.

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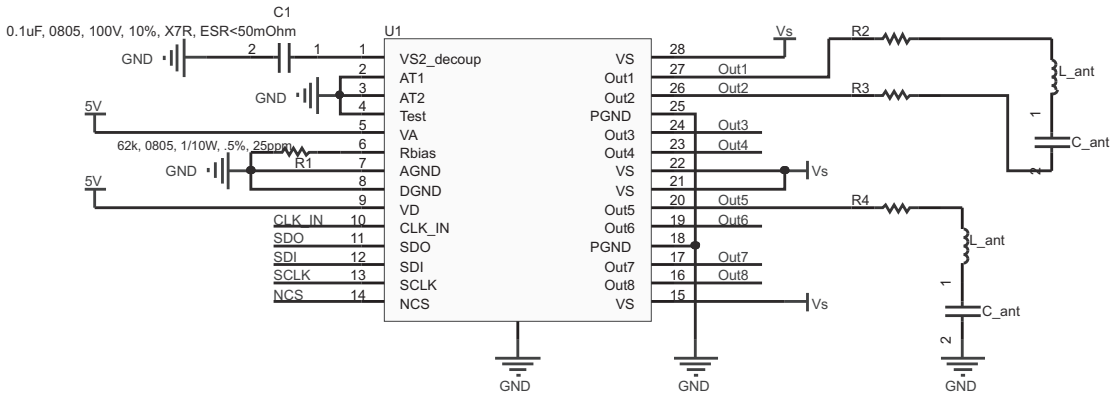
APPLICATION OVERVIEW

Typical Application Circuit



NOTE: Analog ground, digital ground, power ground, as well as the power pad must be connected together with a low impedance path.

Figure 8. Typical Application Circuit

Necessary External Components

$V_S/2$: Pin 1 requires a 100nF capacitor with at least 10% tolerance or better, and ESR (equivalent series resistance) of less than 50mΩ.

R_{BIAS}: Pin 6 requires a 62kΩ, 1% or better tolerance, 50ppm or better temperature coefficient.

Output Channels

The output channels require current limiting resistors to insure the source/sink current of the outputs does not exceed the minimum AC current detection threshold of 0.9 A. Besides current limiting, these resistors affect the Q-factor of the antenna. The output channels require 3V headroom at each rail to avoid clipping. Therefore, for an output signal of 24 Vpp, V_S must be at least 30V.

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ABSOLUTE MAXIMUM RATINGS(1)

			MIN	MAX	UNIT
Supply					
V_S	V_{bat} or $V_{step-up}$		-0.3	42	V
I_V_S	Current on one V_S pin			1.3	A
V_{DD}			-0.3	7	V
Ground offset	Ground offset from PGND to AGND or DGND			0.15	V
VS_RAMP	V_S ramp up rate			0.5	V/µs
Antenna driver outputs					
V_Outx			-0.3	V_S + 0.3	V
I_Outx_source/sink	Sourcing/sinking current at HS, LS ON	Current limit implemented; see parametric section		3	A
I_Outx_reverse	Reverse current at HS, LS OFF		-0.6	0.6	A
Digital					
V_digital	Voltage on digital pins: CS, SDI, SCLK, CLK_IN	Voltage necessary to clamp ±20mA	-0.3	V_{DD} + 0.3	V
I_digital	Current on digital pins: CS, SDI, SCLK, CLK_IN		-20	20	mA
Power dissipation					
T_A	Ambient temperature		-40	105	°C
T_{hSD}	Over-temperature detection and shutdown		150	205	°C
Electrostatic Discharge (ESD)					
HBM	Human Body Model			2000	V
CDM	Charge Device Model			1500	V
MM	Machine Model			50	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		PWP	UNIT
		28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	34.5	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance	25.9	°C/W
θ_{JB}	Junction-to-board thermal resistance	14.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.2	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case(bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_S	Supply voltage	7	38	V
V_D	Digital supply voltage	4.75	5.25	V
T_A	Ambient free-air temperature	-40	105	°C

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DIGITAL ELECTRICAL CHARACTERISTICS

V_S = 38V, V_D = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low input level		-0.3		0.8	V
V_{IH}	High input level		2		V_{DD} + 0.3	V
V_{IHYS}	Input hysteresis		0.2			V
$I_{ILEAKAGE}$	Input leakage current on SDI, SCLK pins	VIN = V_D	-5		5	µA
		VIN = GND	-5		5	
$I_{ILEAKAGE}$	Input leakage current on TEST pin (internal pulldown resistor)	VIN = V_D	23.75		105	µA
		VIN = GND	- 5		5	
$I_{ILEAKAGE}$	Input leakage current on NCS, CLK_IN pins	VIN = V_D	-5		5	µA
		VIN = GND	-105		-23.75	
R_{IPU}	Input pullup resistor only for NCS, CLK_IN		50		200	kΩ
V_{OH_SDO}	High output level on SDO	I_{SDO} = -1.85mA	V_{DD} - 0.4			V
V_{OL_SDO}	Low output level on SDO	I_{SDO} = +1.85mA			0.4	V
I_{OZ_SDO}	Tristate leakage current on SDO		-5		5	µA

ANTENNA DRIVER / POWER AMPLIFIER INCLUDING H-BRIDGE

V_S = 38V, V_D = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_PWR	Output current capability for one output(1)(2)		1.2			App
V_PWR Gain Error	Gain Error of output voltage amplitude peak–peak on 1 half-bridge for normal mode(3)(4)	T_A=-40°C, 25°C, 105°C	-10%		8%	
V_PWR Offset Error	Offset Error of output voltage amplitude peak–peak on 1 half-bridge for normal mode(3)(4)	T_A=-40°C, 25°C, 105°C	-0.17		0.1	V
V_{PWR_7V} Gain Error	Gain Error of output voltage amplitude peak–peak on 1 half-bridge for normal mode with Vs=7V	n=0 to 3 T_A=-40°C, 25°C, 105°C	- 8.75%		1.40%	
V_{PWR_7V} Offset Error	Offset Error of output voltage amplitude peak–peak on 1 half-bridge for normal mode with Vs=7V	n=0 to 3 T_A=-40°C, 25°C, 105°C	-0.25		0.1	V
Δerr	Output voltage load dependency for normal mode(5)	T_A=-40°C, 25°C, 105°C	0		6.5	%
V_{DTOY} Gain Error	Gain Error of output voltage amplitude peak–peak on 1 half-bridge for destroy bits(6)	n=8 to 15	-14%		5.50%	
V_{DTOY} Offset Error	Offset Error of output voltage amplitude peak–peak on 1 half-bridge for destroy bits(6)	n=8 to 15	-0.3		0.15	V
THD	Voltage harmonic distortion at 125kHz including total sine wave generation at 28V output amplitude		0		6.4	%
BR	Baud rate accuracy of transmitted data(7)		-1%		1%	
V_{CT}	Maximum level of peak to peak noise (crosscoupling) at non active output(8)				100	mV
$t_{RVSDIV2}$	Rise Time for V_S/2 at wake-up command, with V_S already set	With 0.1µF capacitor			700	µs

(1) All other parameters in antenna driver section are specified for this I_PWR limit
(2) Test of output current at PGA=31, 23.3Ω connected between Outx and V_S/2 Reference voltage.
(3) Test circuit: 23.3Ω connected between Outx and V_S/2 Reference voltage.
(4) The sine wave output amplitude accuracy is linearly related to V_A: the nominal value is (n+1)×0.95 at V_A = 4.75V and (n+1)*1.05 at V_A = 5.25V.
(5) Formula: for a given programmed gain, Δerr = error at 46.6Ω load – error at 23.3Ω load
(6) The destroy bit amplitude peak to peak is measured at the filtered frequency of 134.2 kHz.
(7) The Baud Rate accuracy is dependant from CLK_IN accuracy
(8) Test conditions: one channel programmed in normal mode with 0.6A peak – all other channels inactive, 48Ω load connected to GND – production test limit = 200mV because of ATE socket.

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DESTROY BIT EMISSION SPECIFICATION

V_S = 38V, V_D = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DTY_{DTOY}	Duty cycle of destroy bits sent on one output				1.3	%

POWER MANAGEMENT

V_S = 38V, V_D = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD_zero}	Current consumption on V_{DD}	All outputs configured LS ON – HS OFF	0	5	6	mA
I_{VDD_active}	Current consumption on V_{DD} per active output – non transmitting mode		0		15	mA
I_{VS_grd}	Current consumption on Vs at all H-Bridges configured LS ON – HS OFF		0		5	mA
I_{TOT_idle}	SLEEP mode current on Vs + V_{DD}	V_S = 16V			50	µA
$I_{channel}$	Current consumption on V_S per active output non-transmitting mode(1)		15		25	mA
P_{d_manch}	Total power dissipation during 100ms(2), 50% duty cycle			5.6		W
P_{d_pulse2}	Continuous 134.2kHz sent during 50ms(3), 100% duty cycle			8.7		W

(1) Test conditions: The current is measured in PGND pin with one output active, the other ones not active.
(2) Typical power dissipation given at 2 channels transmitting 50% duty cycle (data "010101…) – PGA = 28Vpp – Iant = 0.6A peak – the other 6 channels are transmitting 4destroy bits of 1Vpp. The device shall be active for 100ms with this sine wave, having a duty cycle of 50% and 900ms off – simulation results.
(3) Continuous power dissipation at 2 channels transmitting logic "111…" – PGA = 28Vpp – Iant = 0.6A peak – the other 6 channels are in LS ON – HS OFF mode. The device shall be active for 50ms, with this continuous sine wave transmission, then 950ms off – simulated results.

SINE WAVE GENERATION

V_S = 38V, V_D = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_sine	Sine wave frequency	With appropriate CLK_IN(1)		134.2		kHz

(1) The sinewave frequency accuracy depends only on CLK_IN accuracy.

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DIAGNOSTICS

V_S = 38V, V_D = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
U_{VDD}	Under voltage detection threshold on V_{DD} (1)		3		4.5	V
U_{VS}	Under voltage detection on V_S (2)		3	6	7	V
T_{hW}	Over-temperature prewarning		120		170	°C
T_{hM}	Delta between Over-temperature prewarning and Over-temperature Shutdown		23		40	°C
t_{cond1}	Glitch time filter before over-current protection activated (3)		4		12	µs
t_{cond2}	Glitch time filter before over-current protection activated (4)		9		22	µs
I_{DC}	DC current detection threshold in Low Side or in High Side transistor		0.15		0.375	A
I_{DC}	DC current detection threshold when output configured "High Side OFF – Low Side ON"		0.5		1.2	A
I_{Acpeak}	Resonant current detection threshold		0.9		2	A
Acc_IMP	Total accuracy for current measurement	In the peak area (timer code 7, 8)	-2		2	LSB
Acc_IMNP	Total accuracy for current measurement	In the non-peak area (5)	-2.5		2.5	LSB
I_{rge_IM}	Maximum peak current measurement (6)			775	800	mA
t_{rge_IM}	Timer range (for the two timers)		0.699		237.75	µs
t_{res_IM}	Timer resolution (for the two timers)			9		bits
$R_{esA/D}$	A/D resolution			5		bits
$t_{A/D}$	A/D conversion time				10	µs
t_{shift}	Time shift on the A/D measure (7)		-350		150	ns
I_{detect_IM}	Minimum peak current detection		0		50	mA

(1) Test conditions: ramp down on V_A and V_D – Positive hysteresis is specified by design.
(2) Test conditions: ramp down on V_S – Positive hysteresis is specified by design.
(3) Test conditions: V_S = 38V, Vantx = V_S/2, 24Ω connected to V_S or to GND.
(4) Test conditions: V_S = 16V, Vantx = V_S/2, 24Ω connected to V_S or to GND.
(5) This parameter does not include the error due to the time shift of the ADC measurement specified in t_{shift}.
(6) The ADC is 5-bits resolution with a nominal LSB value of 25mA. Two ranges of accuracy are defined:
First for the whole sine wave: 2.5LSB
Second for peak currents in the range of 50mA to 800mA: 2LSB
(7) The propagation delay between the zero-crossing detection at sine output and the power amplifier output results in a phase shift between the timer start and the output current zero-crossing.

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SPI CHARACTERISTICS

V_S = 38V, V_D = 5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	SPI Clock frequency (50% duty cycle)(1)				3	MHz
t_{SDO_trans}	SDO transition speed, 20-80%		10		40	ns
t_{clh}	Minimum time SCLK=HIGH(1)		100			ns
t_{cll}	Minimum time SCLK=LOW(1)		100			ns
t_{pcld}	Propagation delay (SCLK to data at SDO valid)				100	ns
t_{sclch}	SCLK low before NCS low(1) (setup time SCLK to NCS change H/L)		100			ns
t_{hclcl}	SCLK change L/H after NCS=low(1)		100			ns
t_{scld}	SDI input setup time(1) (SCLK change H/L after SDI data valid)		20			ns
t_{hcld}	SDI input hold time(1) (SDI data hold after SCLK change H/L)		20			ns
t_{sclcl}	SCLK low before NCS high(1)		150			ns
t_{hclch}	SCLK high after NCS high(1)		150			ns
t_{pchdz}	NCS L/H to SDO at high impedance				100	ns
t_{onNCS}	NCS min. high time(1)		300			ns
C_{SPI}	Capacitance at SDI; SDO; SCLK; NCS(2)				10	pF
t_{fNCS}	NCS Filter time (Pulses ≤ tfNCS will be ignored)		10		40	ns
	SCLK filter number of cycles(3)			64		
t_{NCS_send}	Delay to send out LF on output after rising edge of NCS (after sending START command)					µs

(1) This parameter is given from the application point of view.
(2) Not measured in series production.
(3) NCS pulse duration must be equal to 64 times SCLK period. If this condition is not met, the SPI message is not understood.

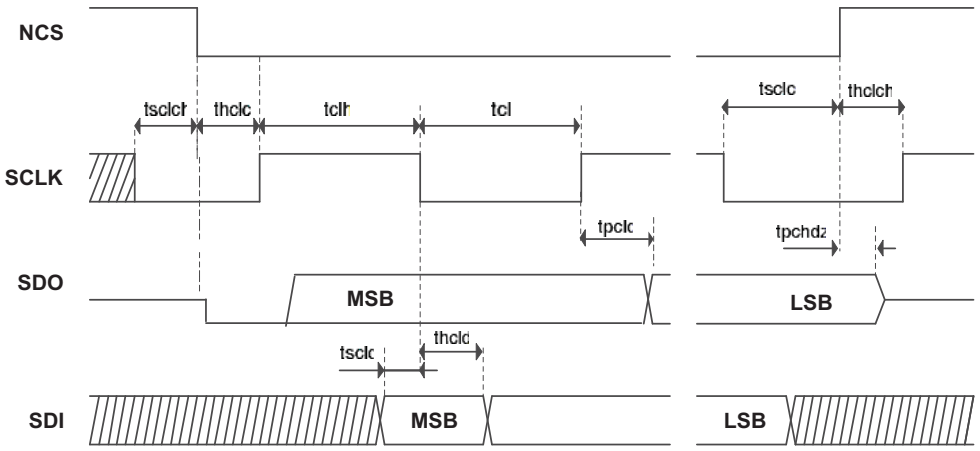

Figure 9. Worst Case SPI Timing

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPIC84000TPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TPIC84134TPWPRQ1	ACTIVE	HTSSOP	PWP	28		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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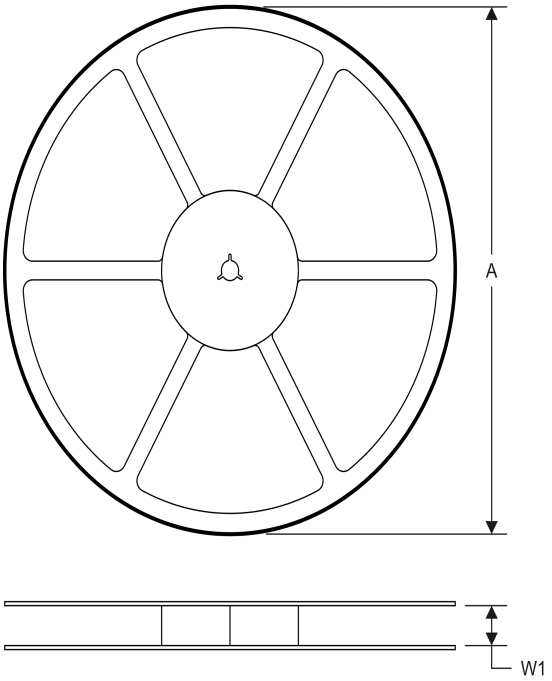
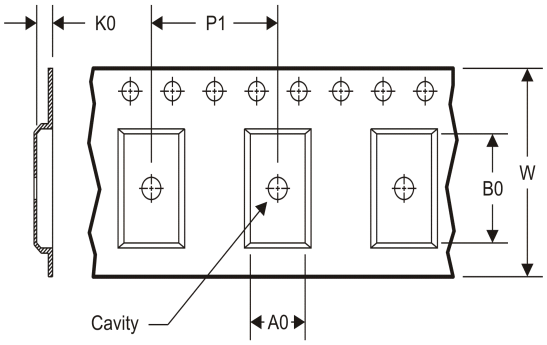
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



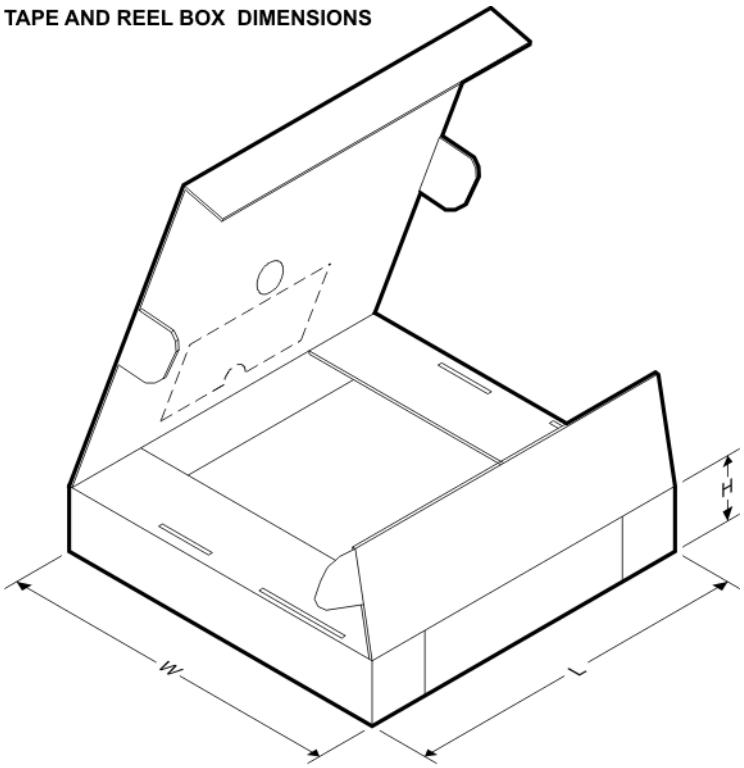
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC84000TPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

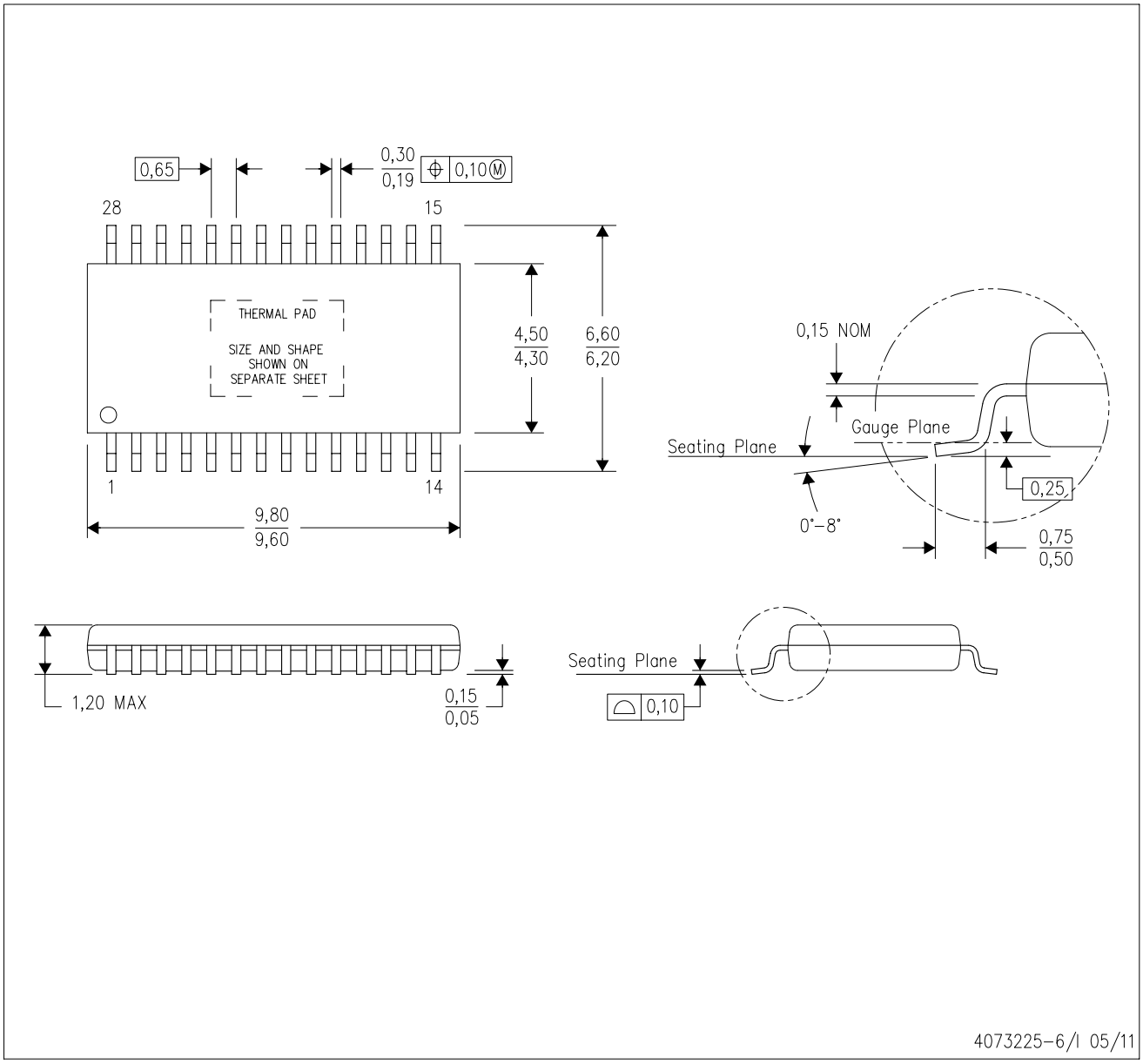
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC84000TPWPRQ1	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

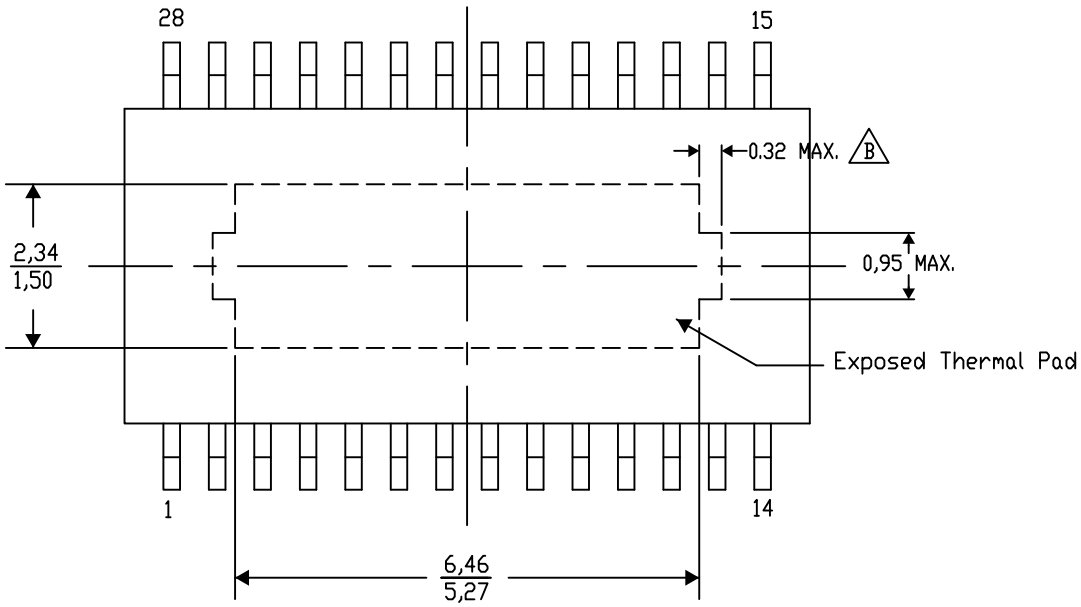
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–36/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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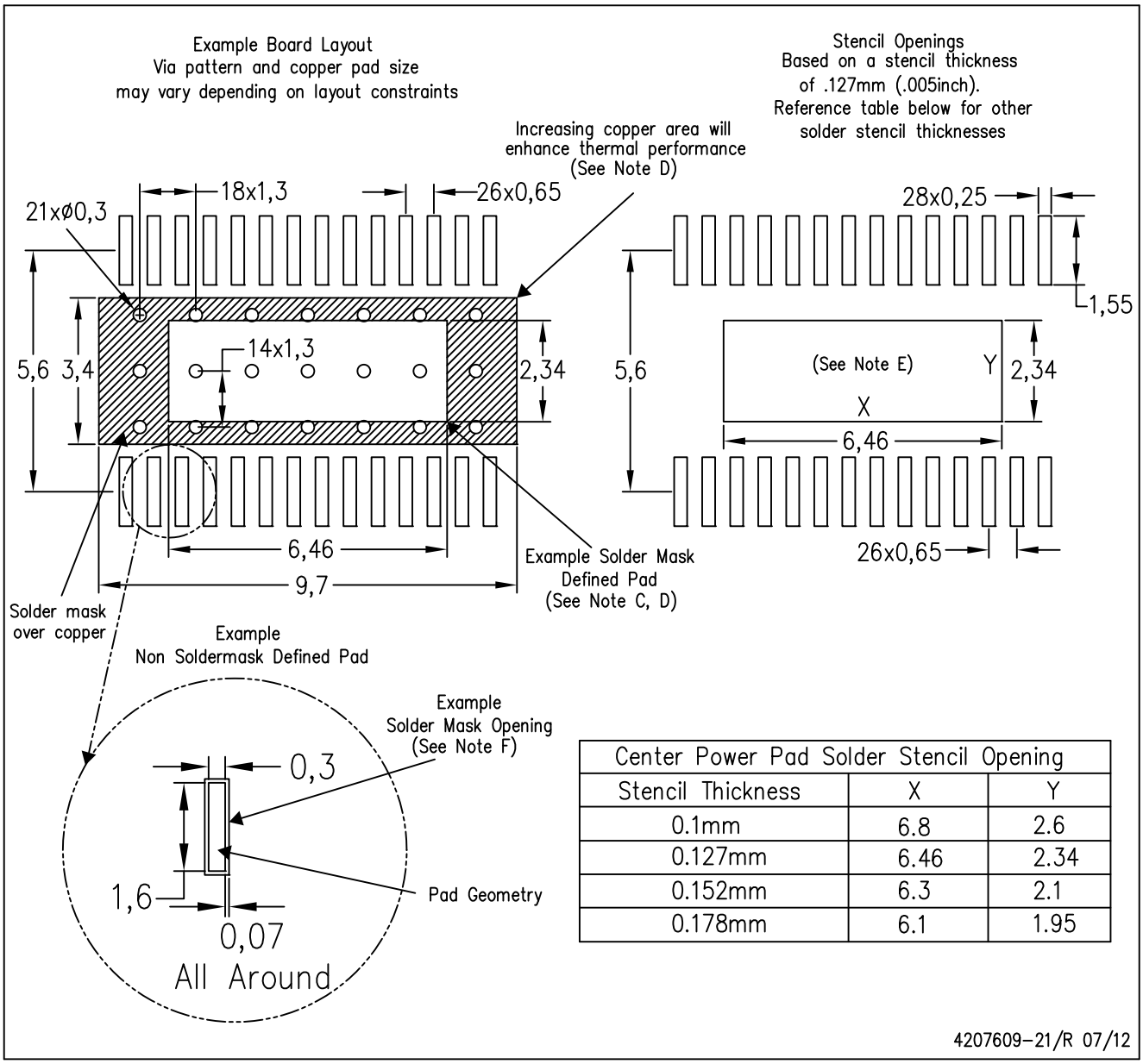
PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.8	2.6
0.127mm	6.46	2.34
0.152mm	6.3	2.1
0.178mm	6.1	1.95

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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