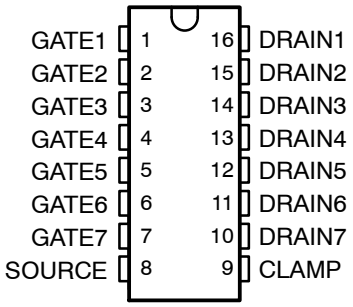
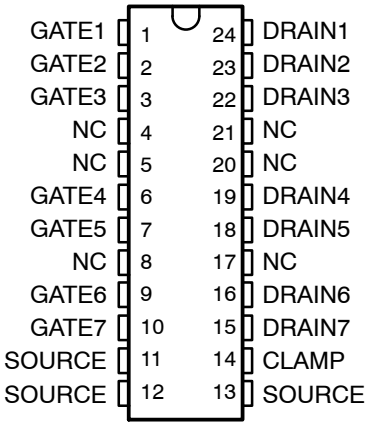
- **Seven 0.5-A Independent Output Channels**
- **Integrated Clamp Diode With Each Output**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Avalanche Energy . . . 22 mJ**

TPIC2701
N PACKAGE
(TOP VIEW)



TPIC2701M
J PACKAGE†
(TOP VIEW)



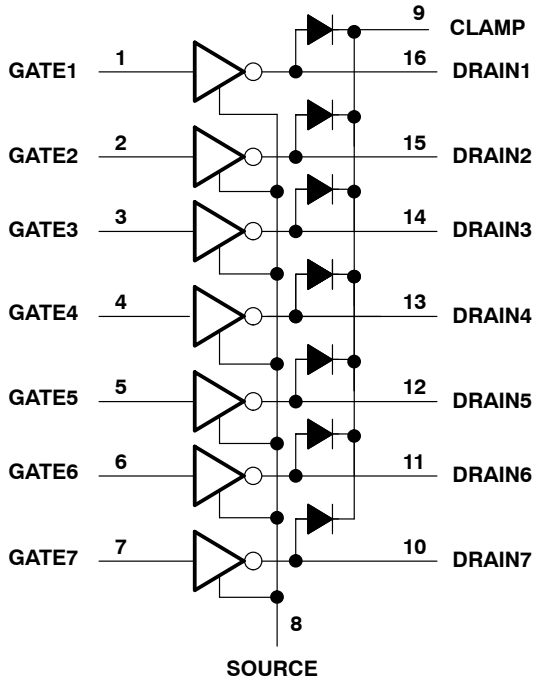
NC – No internal connection
† Refer to the mechanical data for the JW package.

description

The TPIC2701 is a monolithic power DMOS transistor array that consists of seven independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains. The TPIC2701 is pin-for-pin functionally compatible with the Texas Instruments ULN2001A through ULN2004A.

The TPIC2701 is characterized for operation over a temperature range of 0°C to 125°C.The TPIC2701M is characterized for operation over the full military temperature range of −55°C to 125°C.

logic diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1996, Texas Instruments Incorporated

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS} . . . . . 60 V
Gate-source voltage, V_{GS} . . . . . ±20 V
Clamp-drain voltage, V_{CD} . . . . . 60 V
Continuous source-drain diode current . . . . . 0.5 A
Pulsed drain current, each output, I_D (see Note 1 and Figure 17) . . . . . 3 A
Pulsed clamp current, I_{CL} (see Note 1 and Figure 18) . . . . . 3 A
Continuous drain current, each output, all outputs on . . . . . 0.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4) . . . . . 22 mJ
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J: TPIC2701 . . . . . –40°C to 150°C
TPIC2701M . . . . . –55°C to 150°C
Operating case temperature range, T_C: TPIC2701 . . . . . –40°C to 125°C
TPIC2701M . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N Package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J Package . . . . . 300°C

NOTE 1: Pulse duration = 10 ms, duty cycle = 6%.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
J	2660 mW	21.3 mW/°C	1701 mW	1382 mW	530 mW
N	1400 mW	11.0 mW/°C	905 mW	740 mW	300 mW

electrical characteristics, $T_C = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TPIC2701 MIN	TPIC2701 TYP	TPIC2701 MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 μA, V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, $V_{DS} = V_{GS}$		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 0.5 A, V_{GS} = 15 V, See Notes 2 and 3			0.25	0.4	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = –20 V, V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Forward drain-source on-state resistance	V_{GS} = 15 V, I_D = 0.5 A, See Notes 2 and 3 and Figures 5 and 6	T_C = 25°C		0.5	0.8	Ω
			T_C = 125°C		0.8	1.3	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 2 and 3		0.5	0.8		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz			105		pF
C_{oss}	Short-circuit output capacitance, common source				65		
C_{rss}	Short-circuit reverse transfer capacitance, common source				15		

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts with a single output transistor conducting.

electrical characteristics over case temperature operating range (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		T_C†	TPIC2701M			UNIT
					MIN	TYP	MAX	
$V_{(BR)DS}$	Drain-to-source breakdown voltage	I_D = 1 μA,	V_{GS} = 0	25°C	60			V
		I_D = 1 mA,	V_{GS} = 0	Full range				
V_{TGS}	Gate-to-source input threshold voltage	I_D = 1 mA,	V_{DS} = V_{GS}	Full range	1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-to-source on-state voltage	I_D = 0.5 A,	V_{GS} = 15 V	25°C		0.25	0.45	V
				Full range			0.65	
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V,	V_{GS} = 0	25°C		0.05	1	μA
				Full range			10	
I_{GSSF}	Forward gate current, drain short-circuited to source	V_{GS} = 20 V,	V_{DS} = 0	25°C		10	100	nA
				Full range			10	μA
I_{GSSR}	Reverse gate current, drain short-circuited to source	V_{GS} = −20 V,	V_{DS} = 0	25°C		10	100	nA
				Full range			10	μA
$r_{DS(on)}$	Forward drain-source on-state resistance	V_{GS} = 15 V,	I_D = 0.5 A	25°C		0.5	0.9	Ω
				Full range			1.3	
g_{fs}	Forward transconductance	V_{DS} = 15 V,	I_D = 0.5 A	25°C		0.8		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, f = 300 kHz	V_{GS} = 0,	Full range		105		pF
C_{oss}	Short-circuit output capacitance, common source					65		
C_{rss}	Short-circuit reverse transfer capacitance, common source					15		

† Full range is −55°C to 125°C.

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			TPIC2701			UNIT
					MIN	TYP	MAX	
V_{SD}	Forward On voltage	I_S = 0.5 A,	V_{GS} = 0			0.9	1.4	V
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.5 A, di/dt = 25 A/μs,	V_{GS} = 0,	V_{DS} = 48 V, See Figure 1		165		ns
Q_{RR}	Total source-drain diode charge					250		nC

source-to-drain diode characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS			TPIC2701M			UNIT
					MIN	TYP	MAX	
V_{SD}	Forward On voltage	I_S = 0.5 A,	V_{GS} = 0			0.9	1.4	V
t_{rr}	Reverse recovery time	I_S = 0.5 A, di/dt = 25 A/μs,	V_{GS} = 0, T_C = 25°C,	V_{DS} = 48 V, See Figure 1		165		ns
Q_{RR}	Total source-to-drain diode charge					250		nC

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

clamp diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	TPIC2701			UNIT
			MIN	TYP	MAX	
V_F	Forward on-voltage	I_F = 0.5 A		1	1.5	V
V_{BR}	Breakdown voltage	I_R = 1 μA	60			V
I_R	Reverse leakage current	V_R = 48 V		0.05	1	μA
$t_{rr(CD)}$	Reverse-recovery time	I_F = 0.1 A, di/dt = 25 A/μs, V_{CD} = 48 V, See Figure 1		90		ns
Q_{RR}	Total source-drain diode charge			100		nC

clamp diode characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS		TPIC2701M			UNIT
				MIN	TYP	MAX	
V_F	Forward voltage	I_F = 0.5 A			1	1.5	V
$V_{(BR)}$	Breakdown voltage	I_R = 1 μA,	T_C = 25°C	60			V
		I_R = 1 mA					
I_R	Reverse leakage current	V_R = 48 V	T_C = 25°C		0.05	1	μA
						10	
$t_{rr(SD)}$	Reverse recovery time, source-to-drain	I_F = 0.1 A, di/dt = 25 A/μs, T_C = 25°C			90		ns
Q_{RR}	Total source-to-drain diode charge	V_{CD} = 48 V, See Figure 1			100		nC

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	TPIC2701			UNIT
			MIN	TYP	MAX	
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 100 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		10		ns
$t_{d(off)}$	Turn-off delay time			30		
t_r	Rise time			15		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.25 A, V_{GS} = 10 V, See Figure 3		2.8	3.6	nC
Q_{gs}	Gate-source charge			1.6	2	
Q_{gd}	Gate-drain charge			1.2	1.6	

resistive-load switching characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

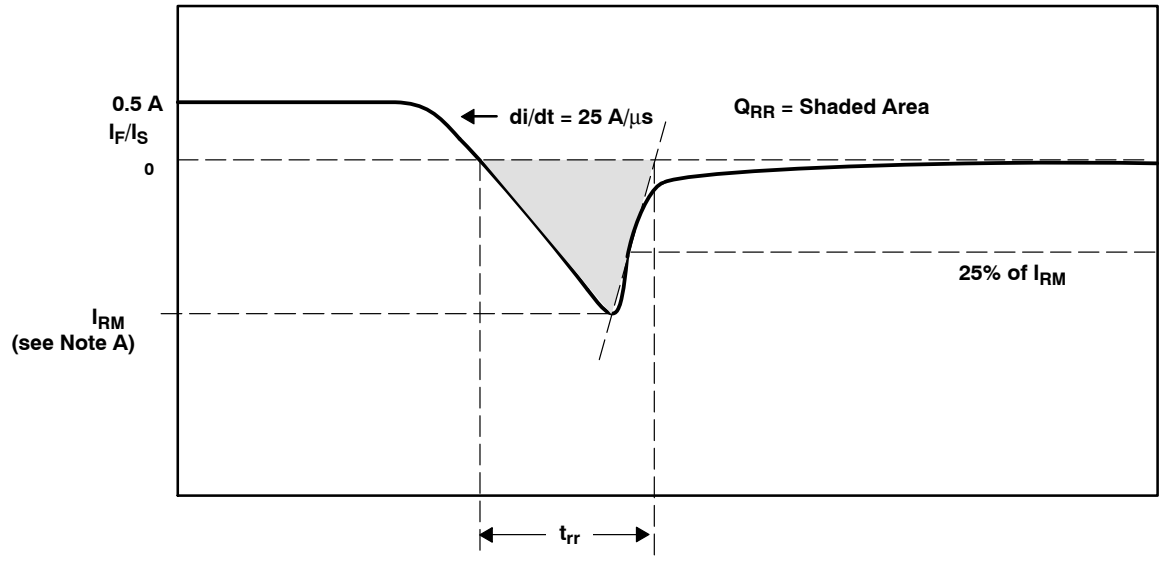
PARAMETER		TEST CONDITIONS	TPIC2701M			UNIT
			MIN	TYP	MAX	
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 100 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		10		ns
$t_{d(off)}$	Turn-off delay time			30		
t_r	Rise time			15		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.25 A, V_{GS} = 10 V, See Figure 3		2.8		nC
Q_{gs}	Gate-to-source charge			1.6		
Q_{gd}	Gate-to-drain charge			1.2		

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	N package with all outputs at equal power			90	°C/W
		J package with all outputs at equal power			66	

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain and Clamp Diodes

PARAMETER MEASUREMENT INFORMATION

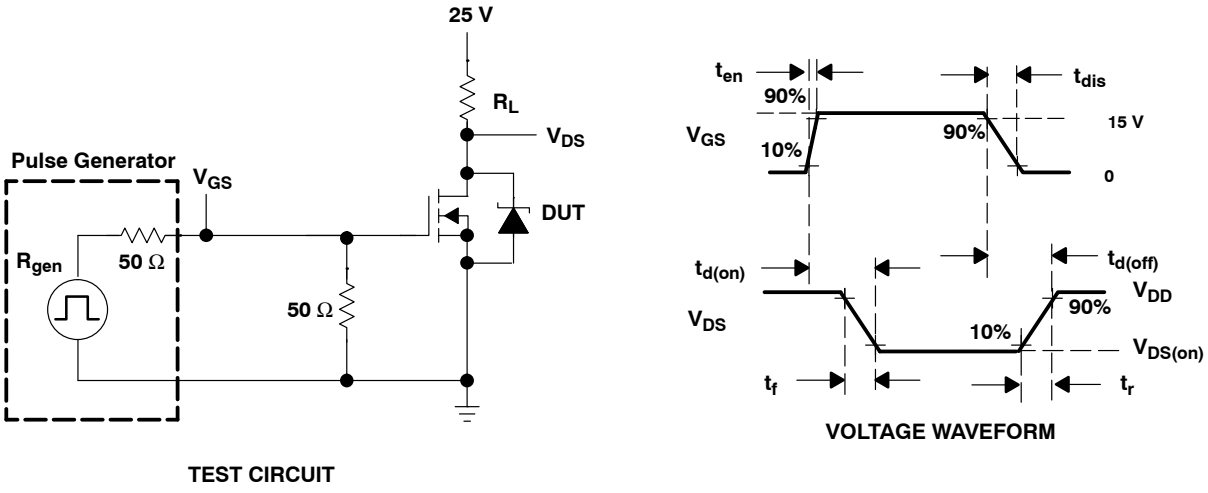


Figure 2. Resistive Switching

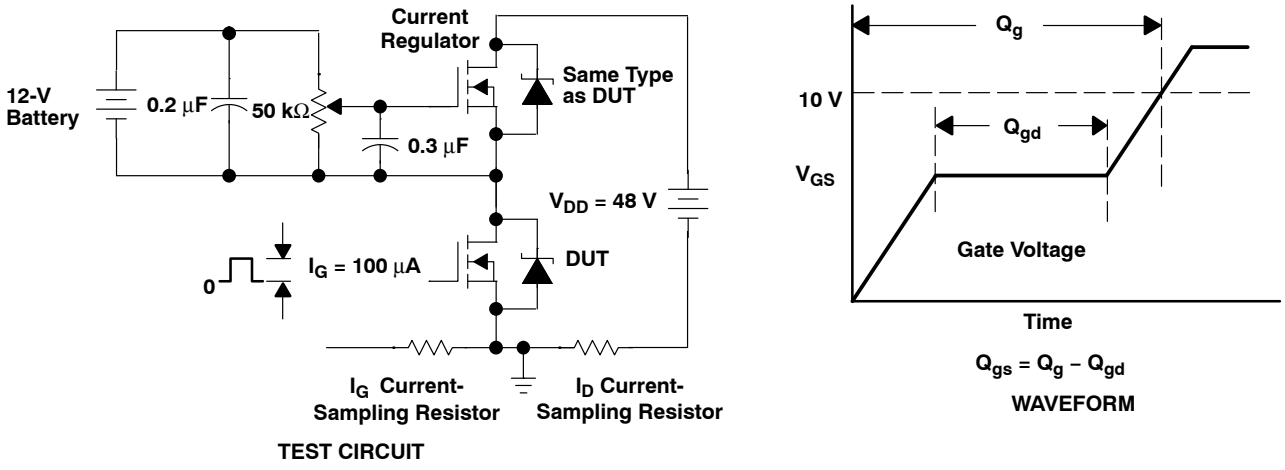
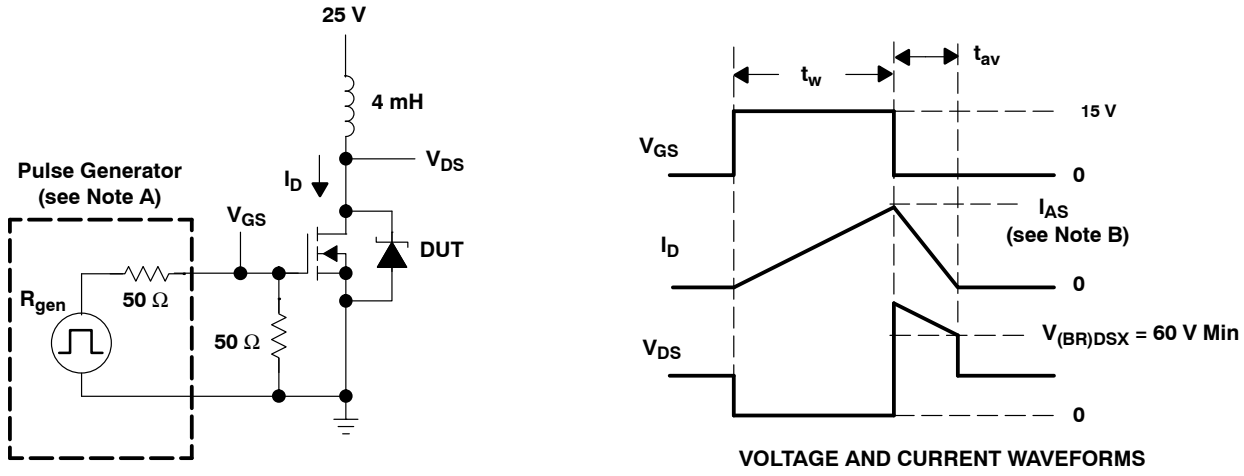


Figure 3. Gate Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 22$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

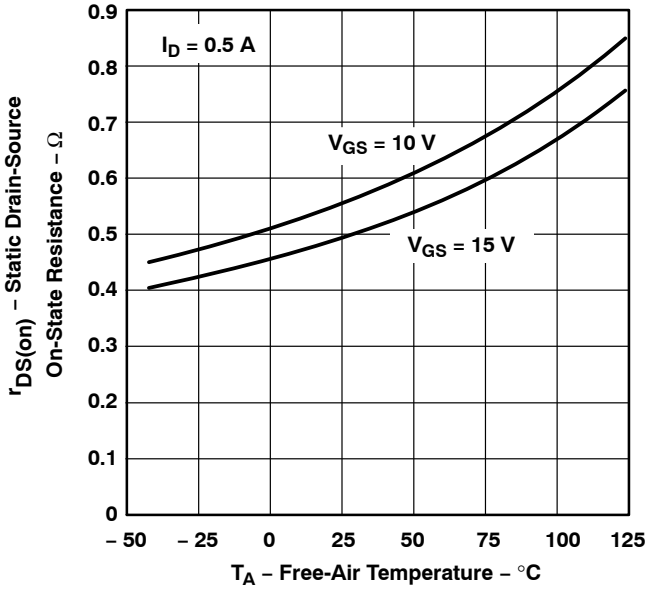


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

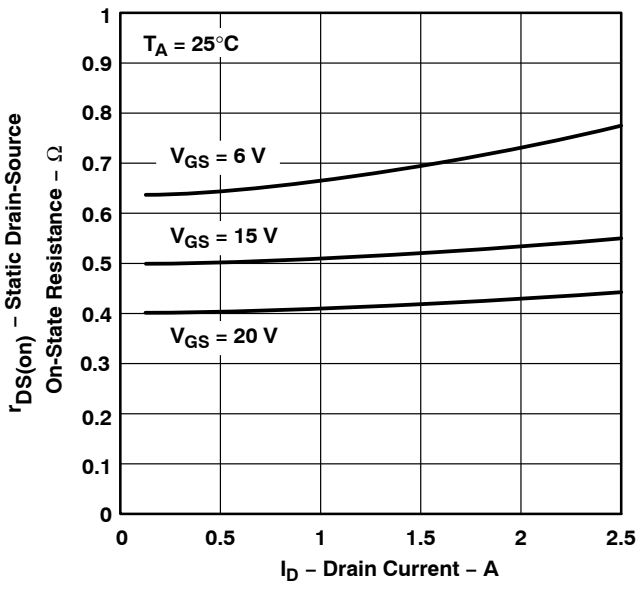


Figure 6

DISTRIBUTION OF FORWARD TRANSCONDUCTANCE

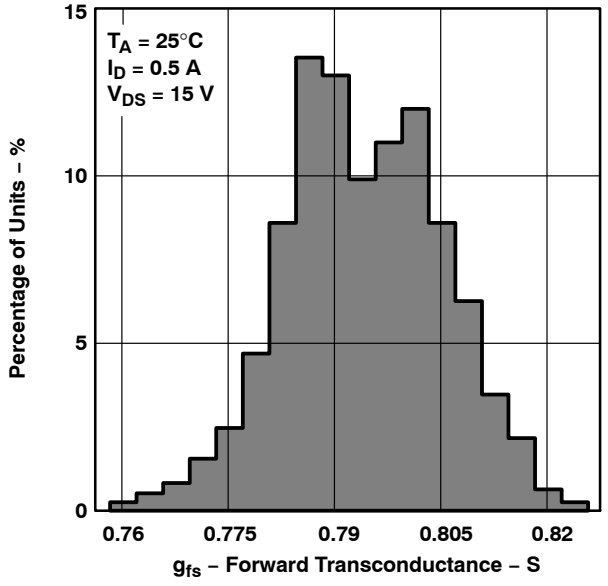


Figure 7

DRAIN-TO-SOURCE CURRENT vs DRAIN-TO-SOURCE VOLTAGE

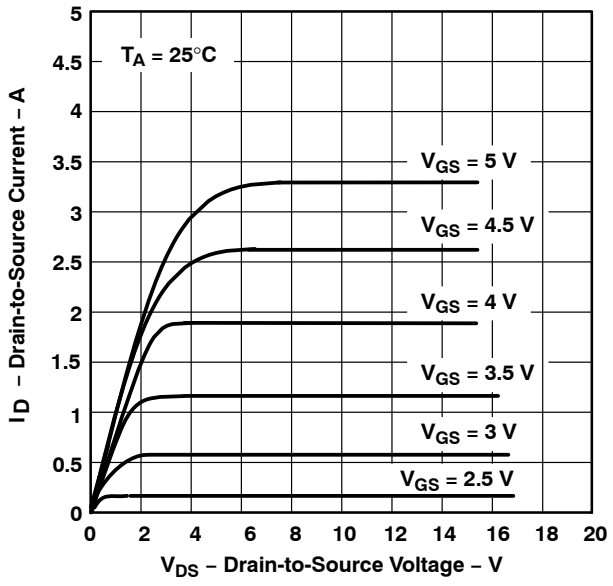


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

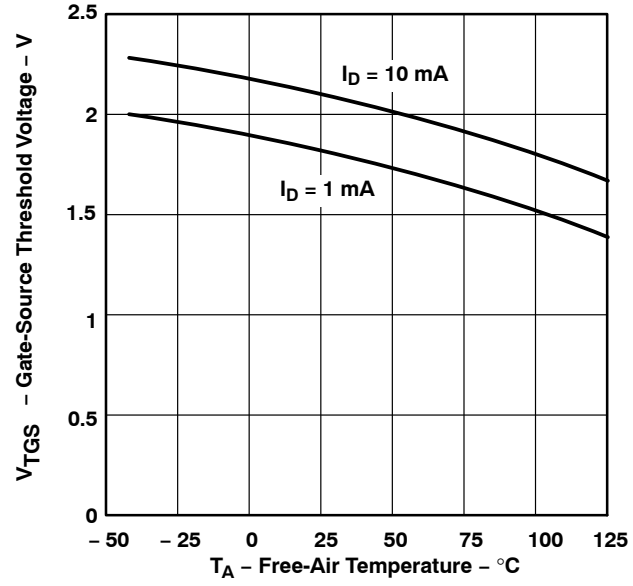


Figure 9

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

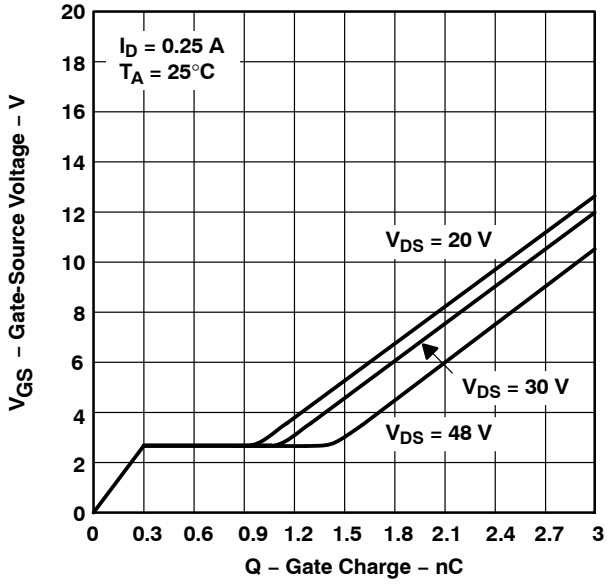


Figure 10

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN DIODE VOLTAGE

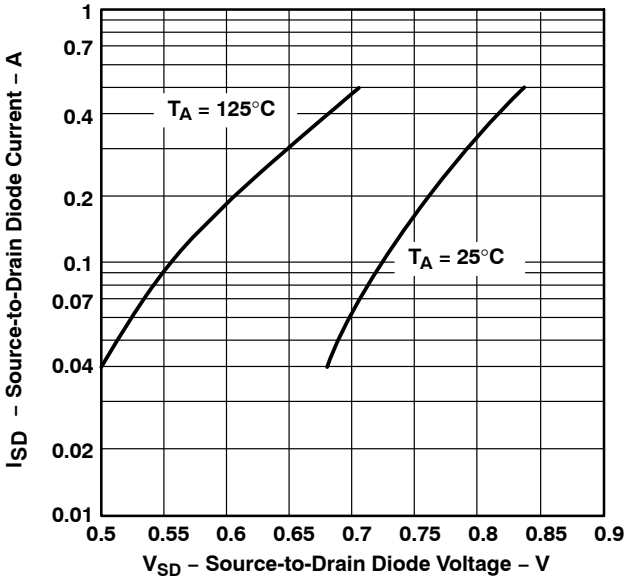


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN DIODE VOLTAGE

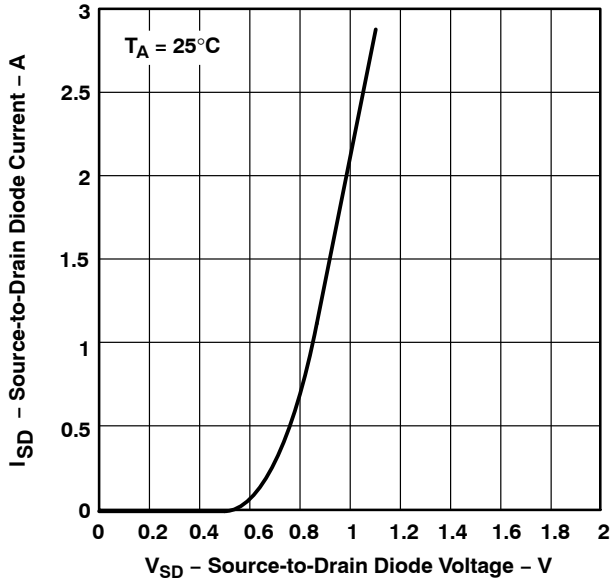


Figure 12

TYPICAL CHARACTERISTICS

CLAMP-DIODE CURRENT vs CLAMP-DIODE VOLTAGE

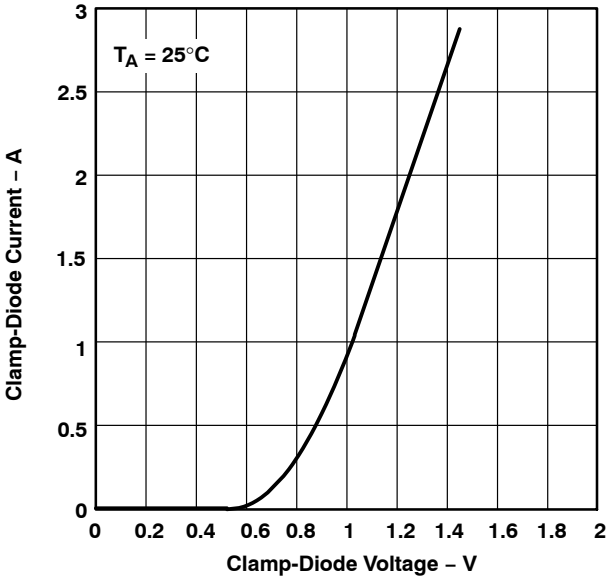


Figure 13

CLAMP-DIODE REVERSE RECOVERY TIME vs REVERSE di/dt

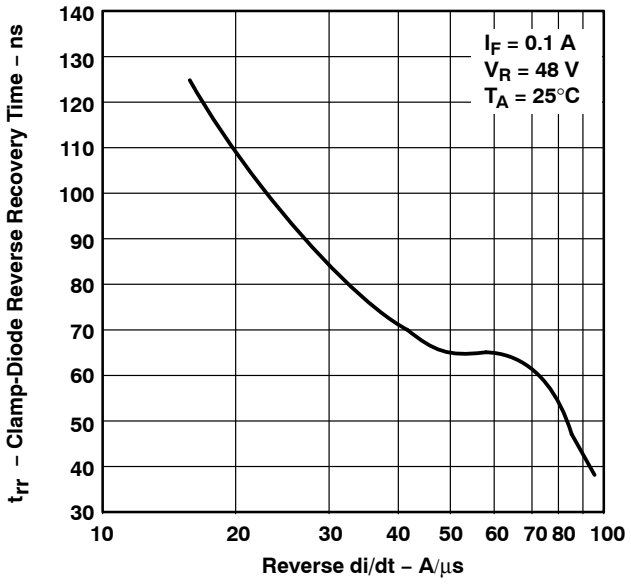
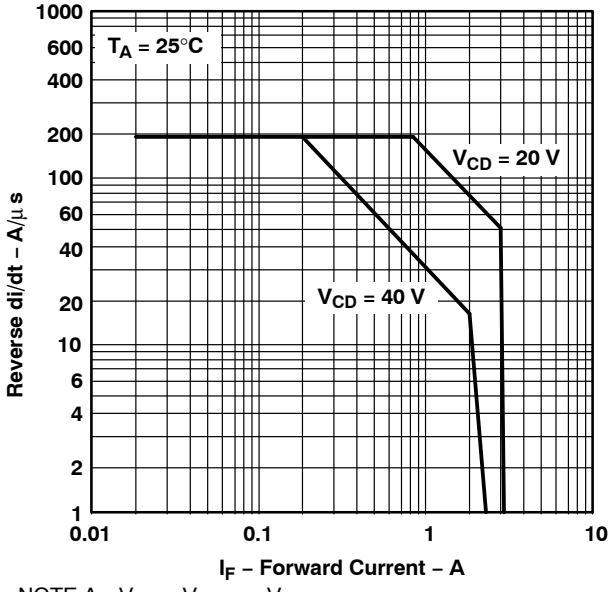


Figure 14

REVERSE di/dt vs FORWARD CURRENT



NOTE A: $V_{CD} = V_{clamp} - V_{drain}$

Figure 15

TYPICAL CHARACTERISTICS

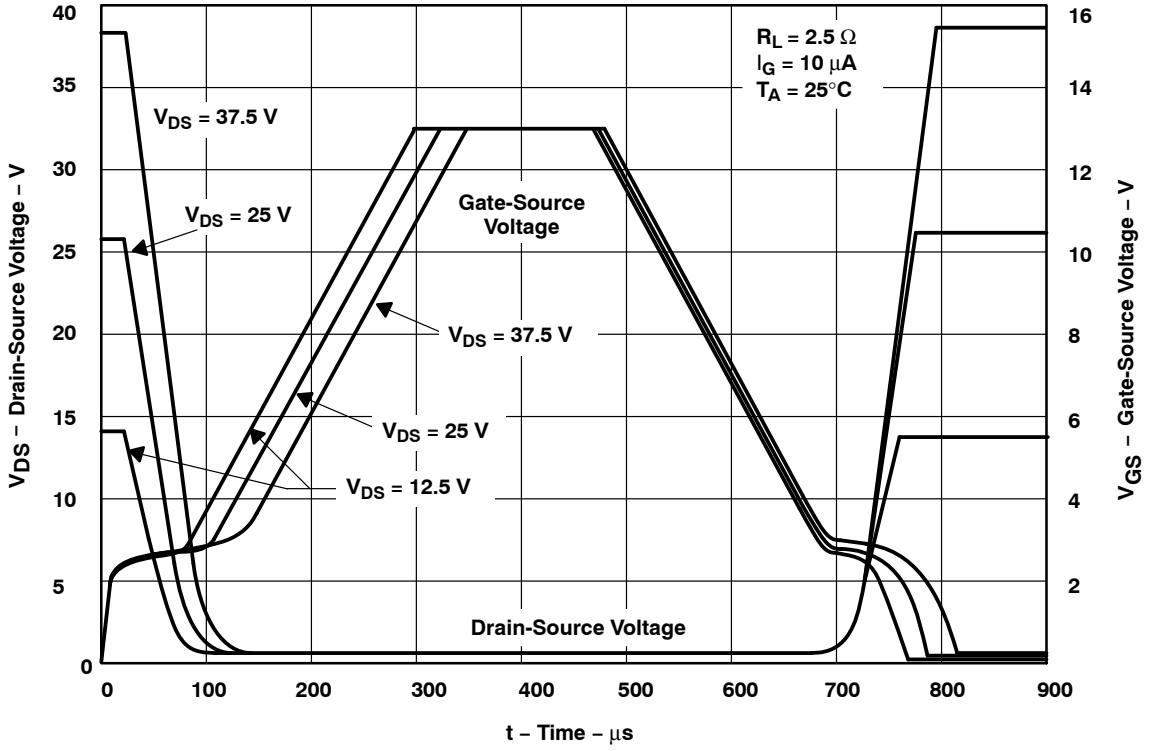


Figure 16. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DUTY CYCLE

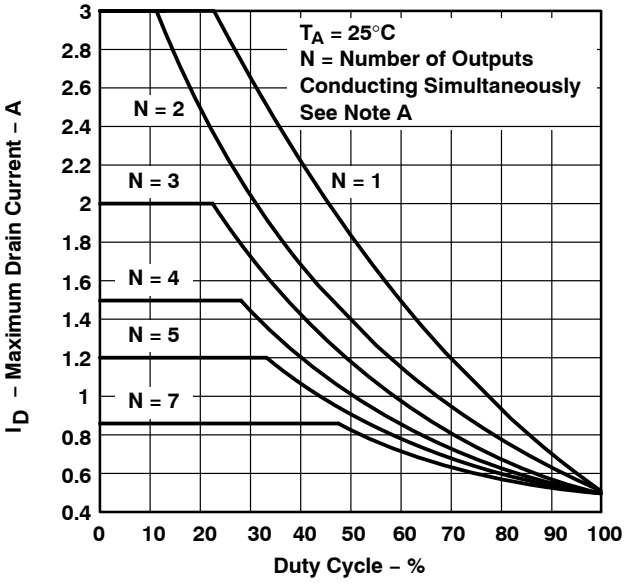


Figure 17

MAXIMUM CLAMP-DIODE CURRENT vs DUTY CYCLE

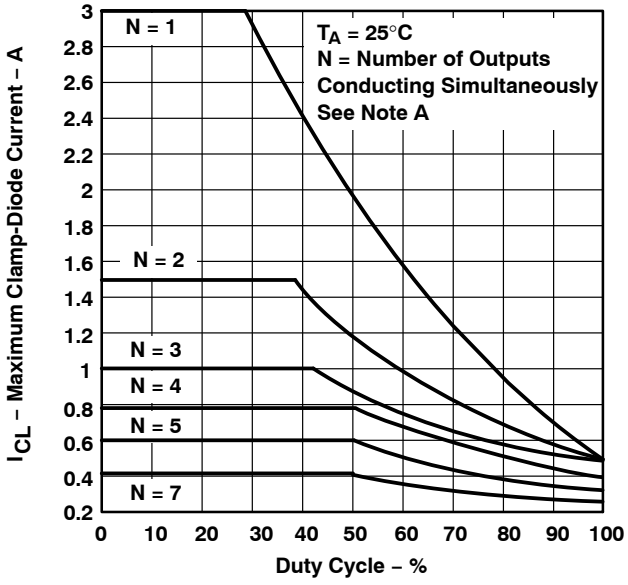
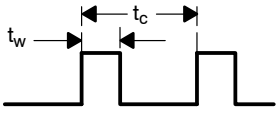


Figure 18



NOTE A: For Figures 17 and 18, $d = t_w/t_c = 10\ ms / t_c$, where t_w and t_c are defined by the following:

PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

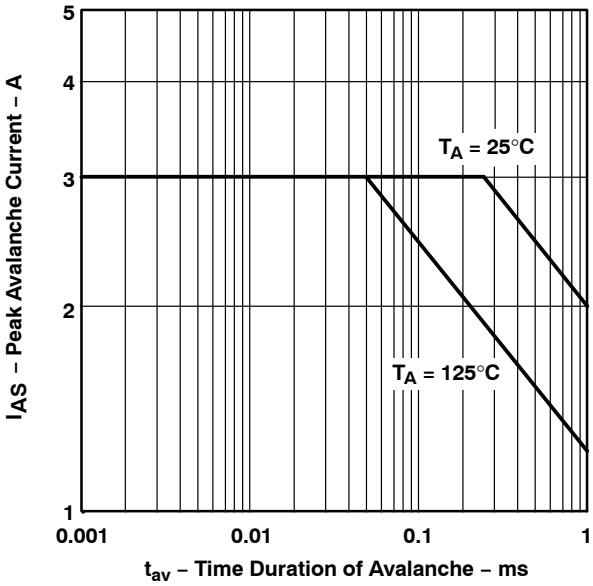


Figure 19

MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE

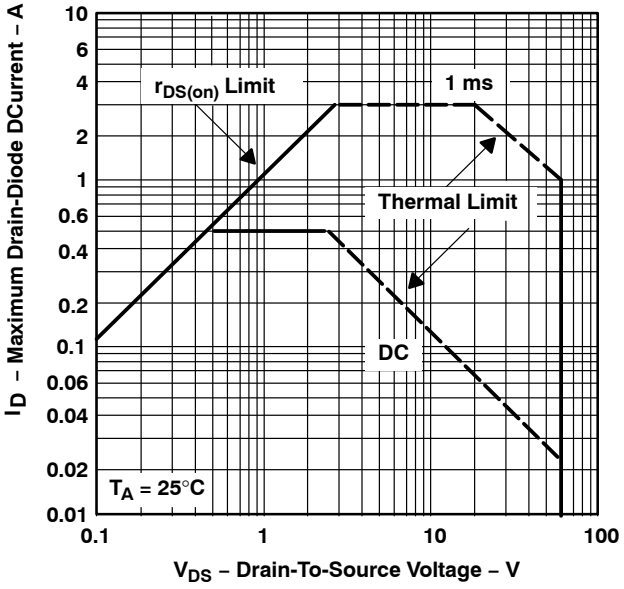
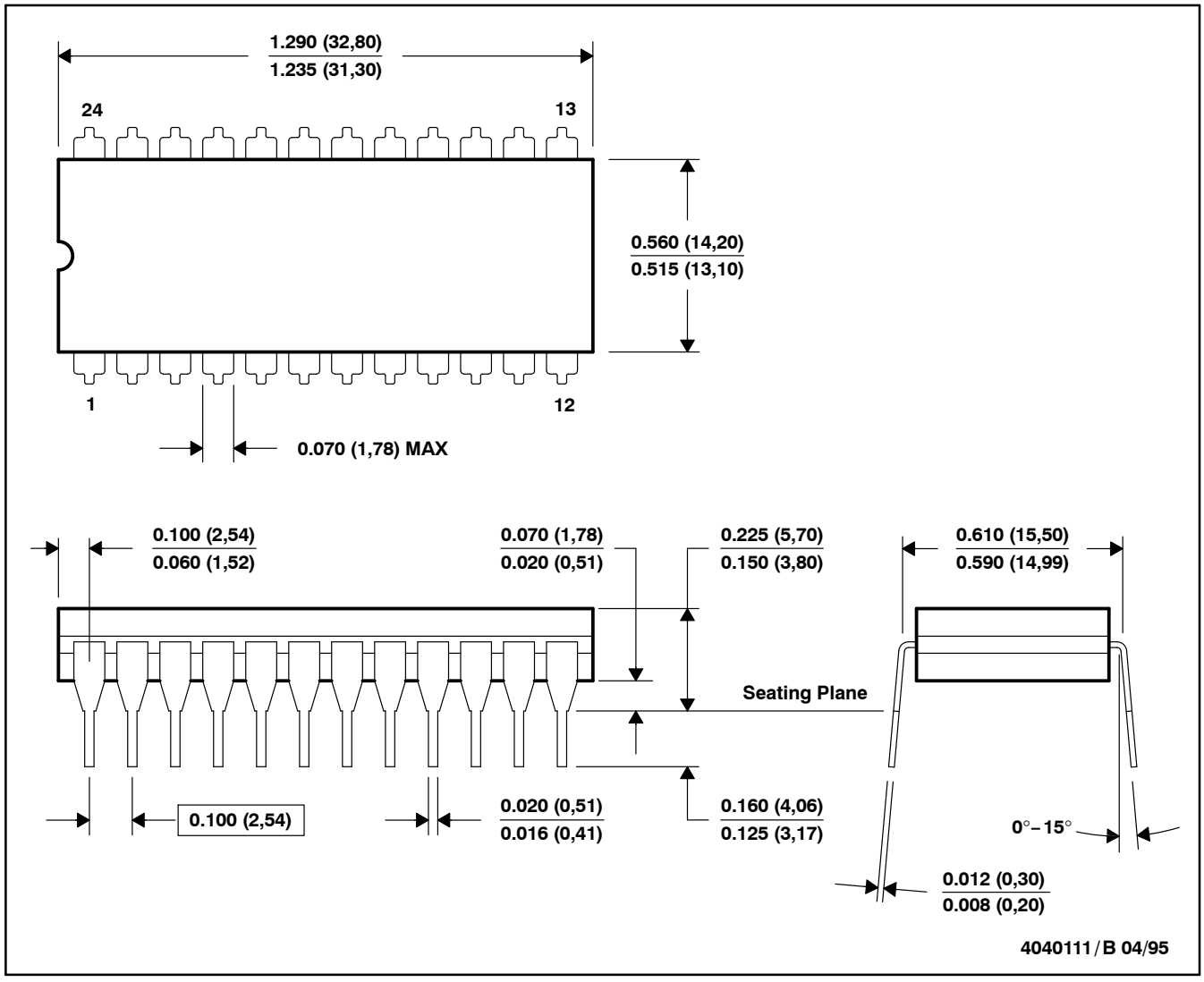


Figure 20

MECHANICAL INFORMATION

JW (R-GDIP-T24) **CERAMIC DUAL-IN-LINE PACKAGE**



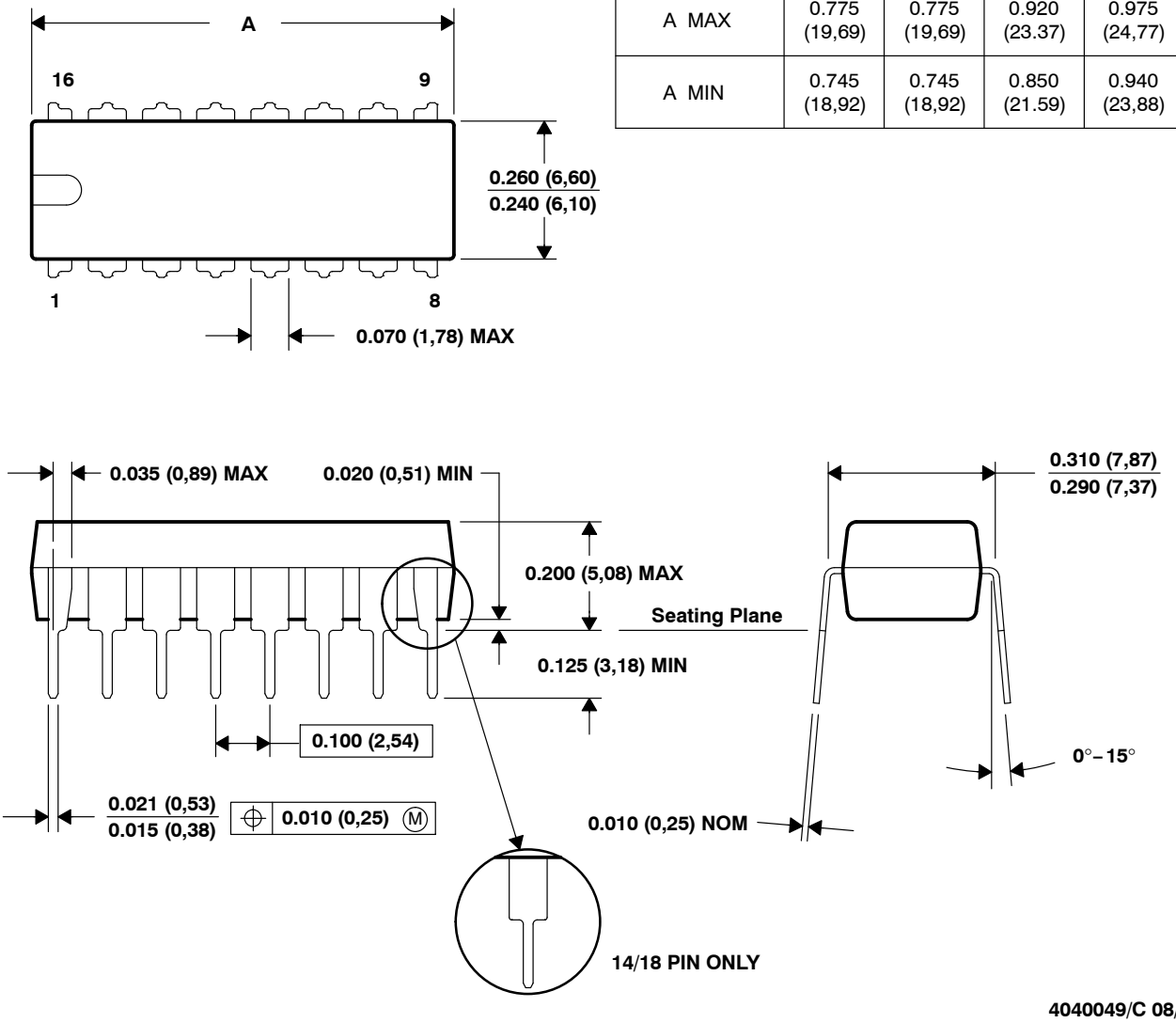
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP5-T24

MECHANICAL INFORMATION

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPIC2701MJB	OBSOLETE	CDIP	J	24		TBD	Call TI	Call TI
TPIC2701N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

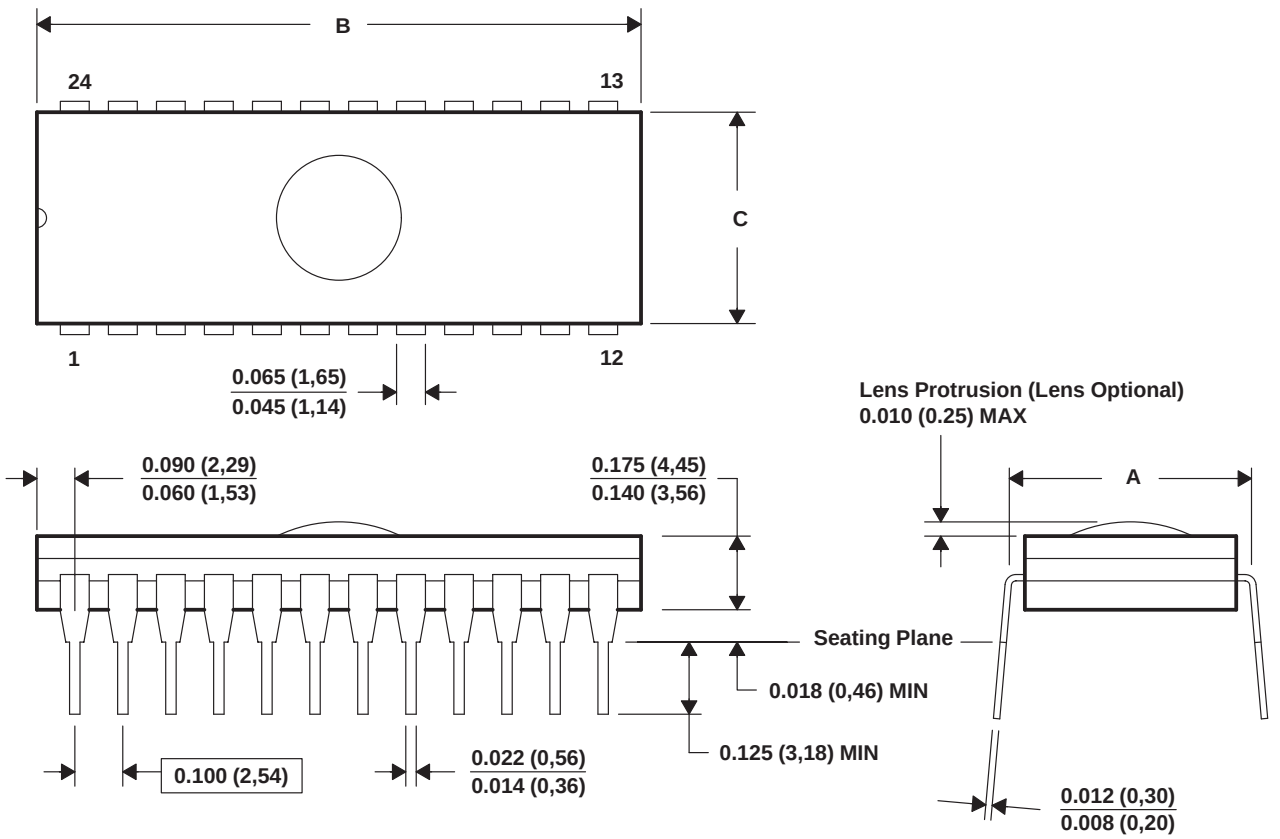
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MCDI004A – JANUARY 1995 – REVISED NOVEMBER 1997

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



DIM \ PINS **		24		28		32		40	
		NARR	WIDE	NARR	WIDE	NARR	WIDE	NARR	WIDE
"A"	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
"B"	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
"C"	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

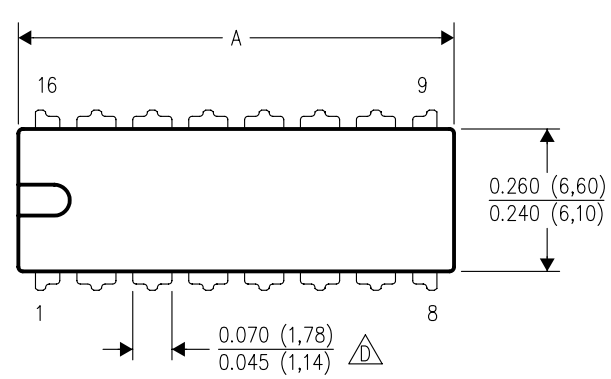
4040084/C 10/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
D. This package can be hermetically sealed with a ceramic lid using glass frit.
E. Index point is provided on cap for terminal identification.

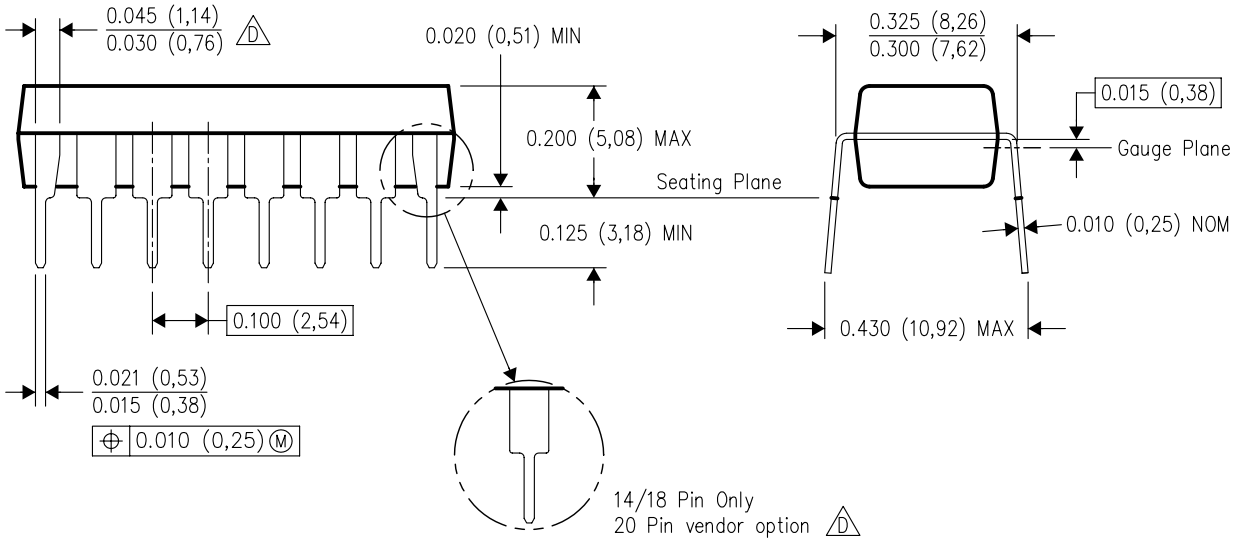
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated