TPD6F002-Q1EVM

This user's guide describes the characteristics, operation, and use of the TPD6F002-Q1EVM evaluation module (EVM). This EVM includes 2 TPD6F002-Q1's for testing. One TPD6F002-Q1 is configured for IEC61000-4-2 compliance testing and one TPD6F002-Q1 is configured for 4-port s-parameter analysis. Additionally, the TPD6F002-Q1 for ESD testing allows the capture of a clamping waveform during an ESD event. This user's guide includes setup instructions, schematic diagrams, a bill of materials, and printed-circuit board layout drawings for the evaluation module.

1 Introduction

Texas Instrument's TPD6F002-Q1 evaluation module helps designers evaluate the operation and performance of the TPD6F002-Q1 device. The TPD6F002-Q1 is a six-channel EMI filter in a space-saving DSV package. This low-pass filter array reduces EMI emissions and provides system-level ESD protection at the data ports. Because of its small package and easy-to-use pin assignments, this device is suitable for a wide array of applications such as mobile handsets, PDAs, video consoles, notebook computers, etc. In particular, the TPD6F002 is ideal for EMI filtering and protecting data lines from ESD at the LCD display, keypad, and memory interfaces. The pi-style (C-R-C) filter provides at least 35 dB attenuation in the carrier frequency range. The TPD6F002 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. This filter includes ESD protection circuitry that prevents damage to the application when subjected to ESD up to IEC 61000-4-2 ±20 kV Contact ESD and ±30 kV Air-Gap ESD. The TPD6F002-Q1 is characterized for operation over an ambient air temperature range of –40°C to 125°C.

The EVM contains two TPD6F002-Q1's. A TPD6F002-Q1 (U1) is configured with test points for striking ESD to the protection pins. It also has an SMB (J5) connector for capturing clamping waveforms with an oscilloscope during an ESD strike. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope. A proper procedure is outlined below in *Oscilloscope Setup*. A TPD6F002-Q1 (U2) is configured with 4 SMA (J1 – J4) connectors to allow 4-port analysis with a vector network analyzer.

Table 1. EVM Configuration

Reference Designator	TI Part Number	Configuration
U1	TPD6F002-Q1	IEC61000-4-2 ESD Tests and ESD Clamping waveforms
U2	TPD6F002-Q1	S-parameters

2 Definitions

Contact Discharge — a method of testing in which the electrode of the ESD simulator is held in contact with the device-under-test (DUT).

Air Discharge — a method of testing in which the charged electrode of the ESD simulator approaches the DUT, and a spark to the DUT actuates the discharge.

ESD simulator — a device that outputs IEC61000-4-2 compliance ESD waveforms shown in Figure 1 with adjustable ranges shown in Table 2 and Table 3.

IEC61000-4-2 has 4 classes of protection levels. Classes 1 – 4 are shown in Table 2. Stress tests should be incrementally tested to level 4 as shown in Table 3 until the point of failure. If the DUT does not fail at 8 kV, testing can continue in 2 kV increments until failure.

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Table 2. IEC61000-4-2 Test Levels

Contact Discharge		Air Discharge	
Class	Test Voltage [± kV]	Class	Test Voltage [± kV]
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

Table 3. Waveform Parameters in Contact Discharge Mode

Stress Level Step	Simulator Voltage [kV]	Ipeak ±15% [A]	Rise Time ±25% [nS]	Current at 30ns ±30% [A]	Current at 60ns ±30% [A]
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

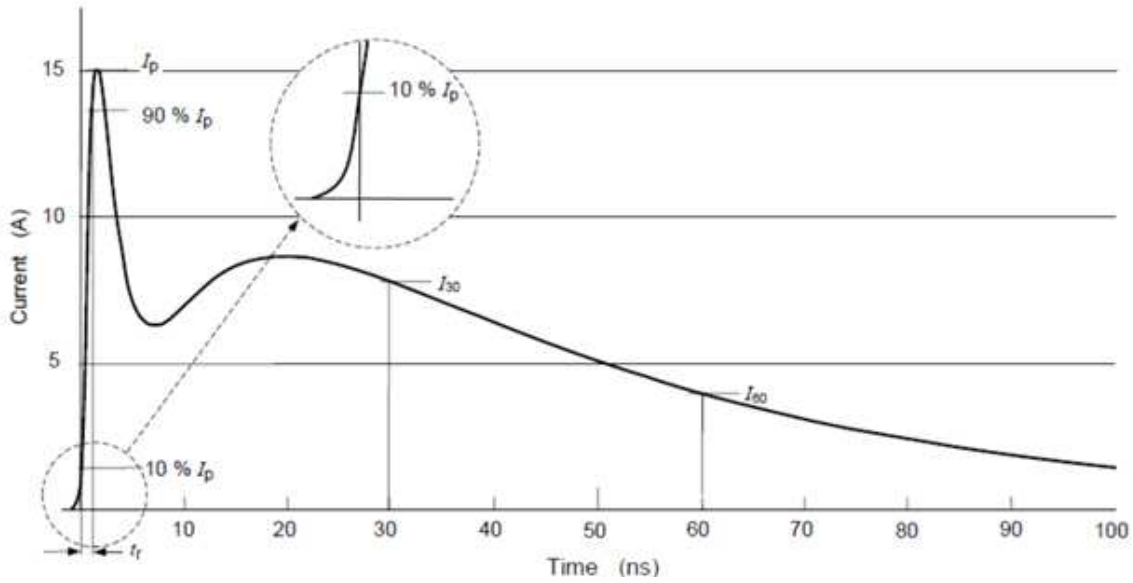


Figure 1. Ideal Contact Discharge Waveform of the Output Current of the ESD Simulator at 4 kV

3 Setup

This section describes the intended use of the EVM. A generalized outline of the procedure given in IEC-61000-4-2 is described here. IEC-61000-4-2 should be referred to for a more specific testing outline. Basic configurations for collecting S-parameters and ESD clamping waveforms are outlined as well.

3.1 U1

TPD6F002-Q1 (U1) can be used for destructive electrostatic discharge (ESD) pass/fail ESD strikes. Specifically, for both IEC-61000-4-2 air and contact discharge tests. The following procedure ensures proper testing setup and methods for both discharge tests. Each IO has a Test Pad (TP1 – TP6) directly connected to it.

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3.1.1 IEC 61000-4-2 Test Method and Set-Up

An example test setup is shown in Figure 2. Details of the testing table and ground planes can be found in the IEC 61000-4-2 test procedure. Ground the EVM using the banana connector labeled GND (J6). Discharge the ESD simulator on any of the Test Points TP1 – TP6. Contact and air-gap discharge are tested using the same simulator with the same discharge waveform. While the simulator is in direct contact with the test point during contact, it is not during air-gap.

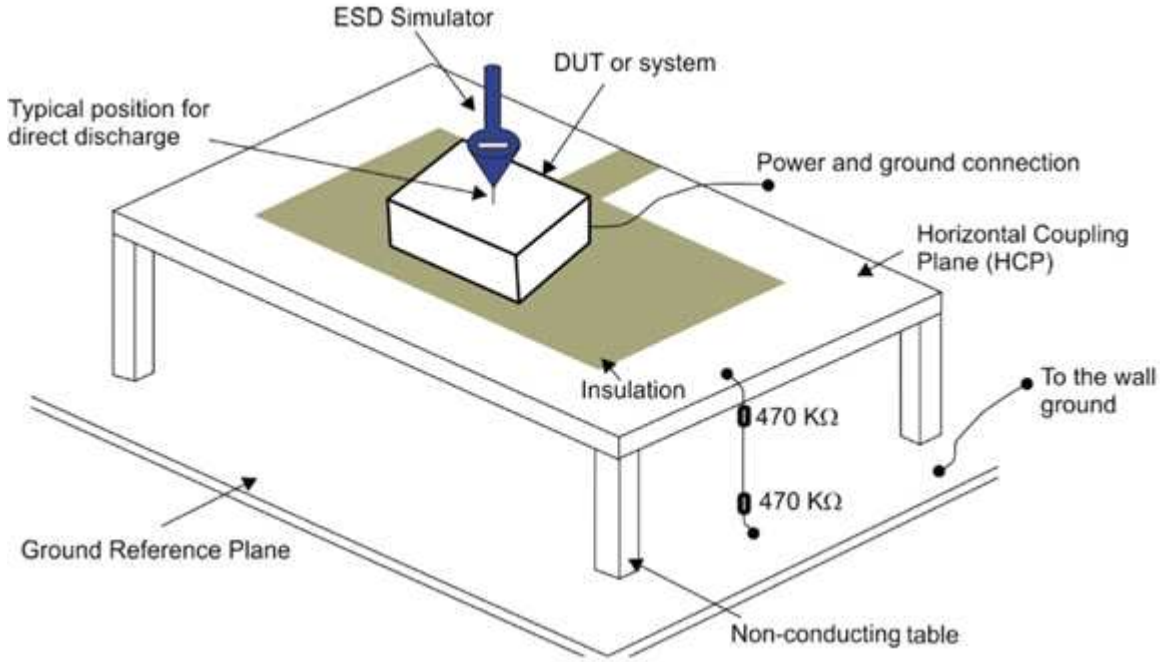


Figure 2. System Level ESD Test Setup

3.1.1.1 Evaluation of Test Results

Connect the tested device on the EVM to a curve tracer both before and after ESD testing. After each incremental level, if the IV curve of the ESD protection diode shifts ±0.1V, or leakage current increases by a factor of ten, then the device is permanently damaged by ESD.

ESD Clamping Waveforms

A TPD6F002-Q1 (U1) also has an SMB (J5) connector for capturing clamping waveforms with an oscilloscope during an ESD strike. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope.

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3.1.1.1 Oscilloscope Setup

Without a proper procedure, capturing ESD clamping waveforms exposes the oscilloscope to potential voltages higher than the rating of the equipment. Proper methodology can mitigate any risk in this operation.

Recommended equipment:

- Minimum of 1GHz bandwidth oscilloscope.
- Either of the following:
  - 2 10X 50 Ω attenuators and a 0 Ω resistor (to be installed at R1).
  - 1 10X 50 Ω attenuator and a 150 Ω resistor (already installed at R1).
- 50 Ω shielded SMB cable.

Procedure

In order to protect the oscilloscope, attenuation of the measured signal is required. Here are two possible procedures for testing U6:

1. Using two 10X attenuators:
   - Install a 0 Ω resistor in R1.
   - Attach two 10X attenuators to the oscilloscope channel being used.
   - Attach the 50 Ω shielded SMB cable between J5 and the attenuator.
   - Set the scope attenuation factor to 100X.
   - Set the oscilloscope to trigger on a positive edge for (+) ESD and a negative edge for (–) ESD strikes. The magnitude should be set to 20 V.
   - Following Section 3.1.1, strike contact ESD to TP1.
2. Using one 10X attenuator:
   - Attach one 10X attenuator to the oscilloscope.
   - Attach the 50 Ω shielded SMB cable between J5 and the attenuator.
   - Set the scope attenuation factor to 40X.
   - Set the oscilloscope to trigger on a positive edge for (+) ESD and a negative edge for (–) ESD strikes. The magnitude should be set to 20 V.
   - Following Section 3.1.1, strike contact ESD to TP1.

Recommended settings for the time axis is 20 ns/div and for the voltage axis is 10 V division.

The voltage levels of the ESD applied to TP1 should not exceed ± 8 kV while capturing clamping waveforms.

3.2 U2

TPD6F002-Q1 (U2) is configured with 4 SMA (J1 – J4) connectors to allow 4-port analysis with a vector network analyzer. Connect Port 1 to J1, Port 2 to J2, Port 3 to J3, and Port 4 to J4. This configuration allows for the following terminology in 4 port analysis:

- S_{11}: Return loss
- S_{21}: Insertion loss
- S_{31}: Near end cross talk
- S_{41}: Far end cross talk

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4 Board Layout

This section provides the TPD6F002-Q1EVM board layout. TPD6F002-Q1EVM is a 4-layer board of FR-4 at 0.062” thickness. Layers 2, 3 and 4 are identical.

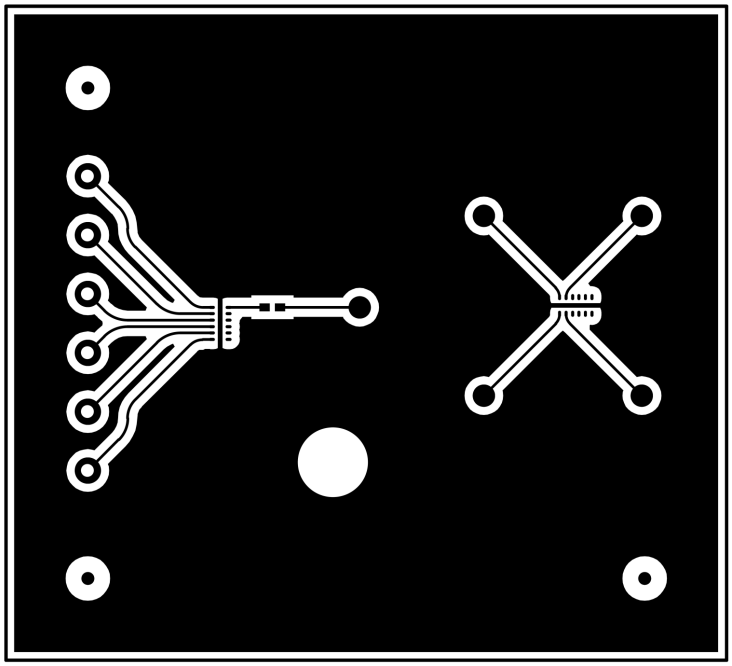


Figure 3. TPD6F002-Q1EVM Top Layer

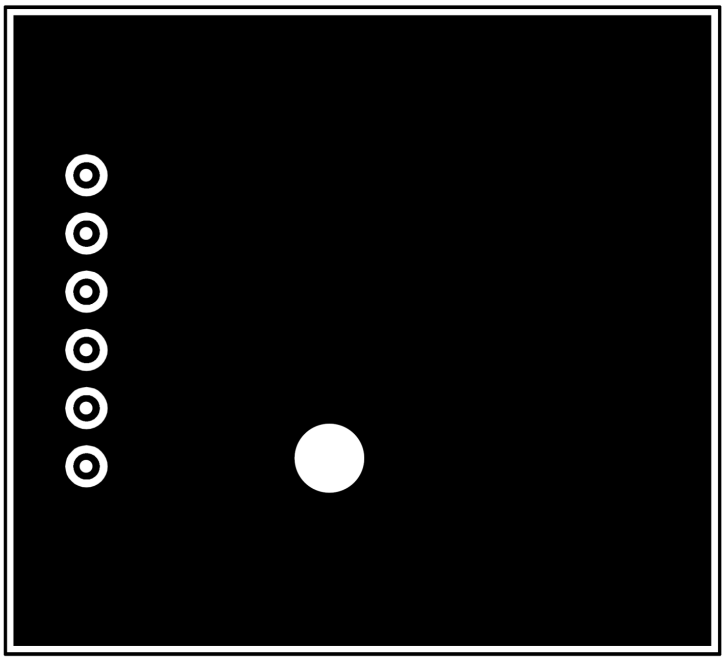


Figure 4. TPD6F002-Q1EVM Midlayer 1, Midlayer 2, and Bottom Layers

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5 Schematics and Bill Of Materials

5.1 Schematics

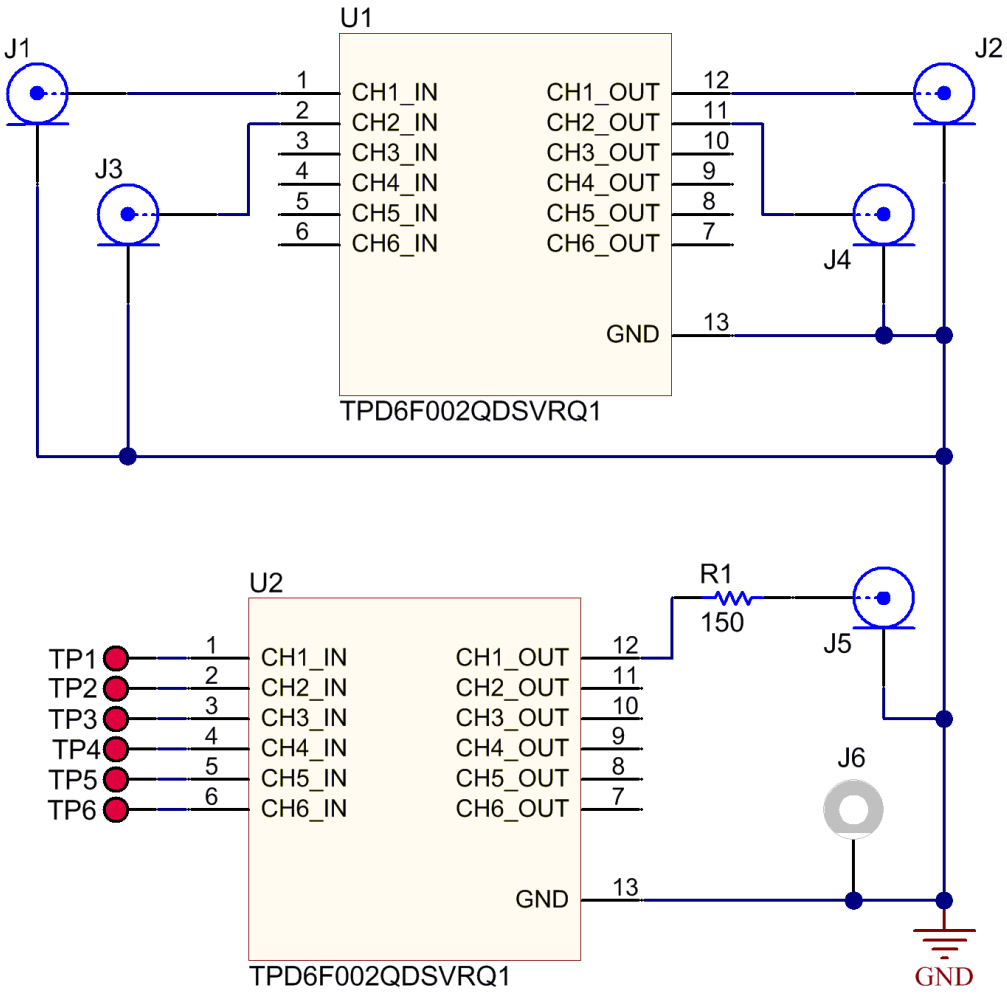


Figure 5. TPD6F002-Q1EVM Schematic

Table 4. Bill of Materials

Count	RefDes	Description	Package Reference	Part Number	MFR
3	H1, H2, H3	Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
5	J1, J2, J3, J4, J5	Connector, SMA Jack, Vertical, Gold, SMD	SMA	142-0711-201	Emerson Network Power
1	J5	Standard Banana Jack, Uninsulated, 5.5mm	SMB	575-4	Keystone
1	R1	RES, 150, 5%, 0.063 W, 0402	0402	CRCW0402150RJNED	Vishay-Dale
2	U1, U2	Six-Channel EMI Filter for LCD Display / Keypad Application, DSV0012A	DSV0012A	TPD6F002QDSVRQ1	Texas Instruments

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- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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