# TPD4E001 Low-Capacitance 4-Channel ESD-Protection for High-Speed Data Interfaces

## 1 Features

- IEC 61000-4-2 ESD Protection (Level 4)
  - ±8-kV Contact Discharge
  - ±15-kV Air-Gap Discharge
- 5.5-A Peak Pulse Current (8/20-µs Pulse)
- IO Capacitance: 1.5 pF (Typical)
- Low Leakage Current: 1 nA (Maximum)
- Low Supply Current: 1 nA
- 0.9-V to 5.5-V Supply-Voltage Range
- Space-Saving DRL, DBV, DCK, DPK, and DRS Package Options
- Alternate 2, 3, 6-Channel options Available: TPD2E001, TPD3E001, TPD6E001

## 2 Applications

- USB 2.0
- Ethernet
- FireWire™ Serial Bus
- LVDS
- SVGA Video Connections
- Glucose Meters

## 3 Description

The TPD4E001 is a four-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD4E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra low leakage current (< 1 nA maximum) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors.

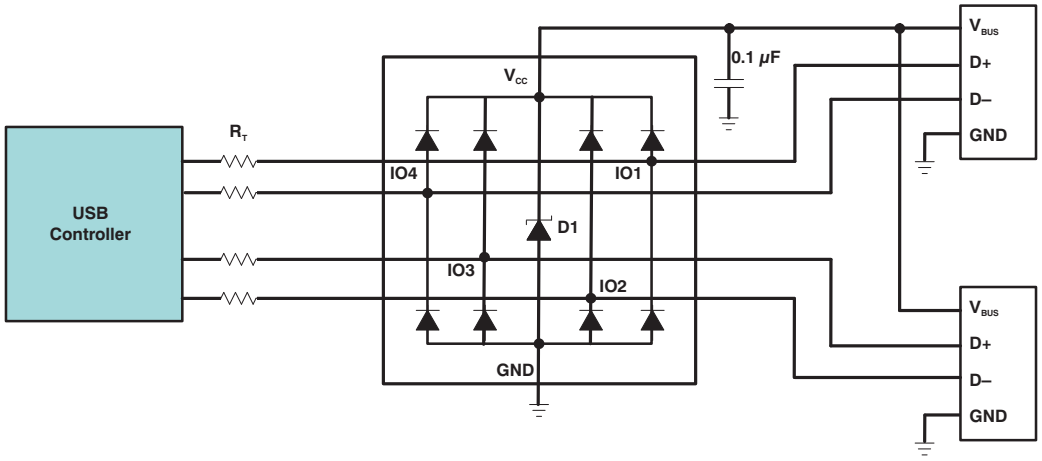
The TPD4E001 is available in DRL(SOT), DBV (SOT-23), DCK (SC-70), DRS (QFN), and DPK (PUSON) packages and is specified for –40°C to +85°C operation. See also TPD4E1U06DCKR and TPD4E1U06DBVR which are p2p compatible with TPD4E001DCKR and TPD4E001DBVR. These devices offer higher IEC protection, lower capacitance, lower clamping voltage, and eliminate the input capacitor requirement.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPD4E001 | SOT (6) | 1.60 mm × 1.20 mm |
| | | 2.90 mm × 1.60 mm |
| | SC70 (6) | 2.00 mm × 1.25 mm |
| | USON (6) | 1.60 mm × 1.60 mm |
| | SON (6) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Application Schematic**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision K (January 2015) to Revision L** — **Page**

- Added frequency test condition to *Channel input capacitance* in the *Electrical Characteristics* table ... 6
- Added *Community Resources* ... 12

**Changes from Revision J (December 2013) to Revision K** — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision I (September 2012) to Revision J** — **Page**

- Updated Description. ... 1
- Removed Ordering Information table. ... 4

**Changes from Revision H (August 2012) to Revision I** — **Page**

- Added DCK2 package to Pin Out drawings. ... 4
- Updated Electrical Characteristics table ... 6

**Changes from Revision G (December 2011) to Revision H** — **Page**

- Updated TOP-SIDE MARKING column in ORDERING INFORMATION table. ... 4

**Changes from Revision F (May 2011) to Revision G** — **Page**

- Updated document formatting. ... 1
- Added DPK (PUSON) package and package information. ... 4


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**Changes from Revision E (April 2011) to Revision F** **Page**

- Added Peak Pulse Waveform Graph to Typical Operating Characteristics. ..... 7

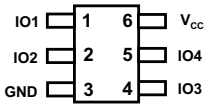
**Changes from Revision C (April 2007) to Revision D** **Page**

- Added DBV (SOT-23) package and package information..... 4

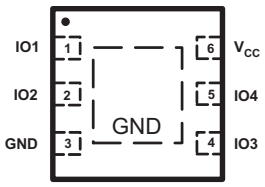
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# 5 Pin Configuration and Functions

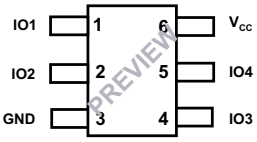
**DRL Package**
**6-Pin SOT**
**Top View**



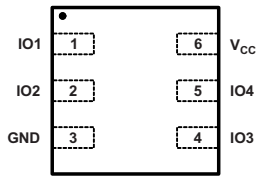

**DRS Package**
**6-Pin SON**
**Top View**



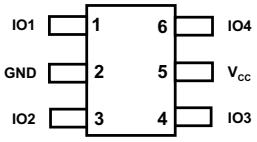

**DCK2 Package**
**6-Pin SC70**
**Top View**




**DPK Package**
**6-Pin USON**
**Top View**




**DBV or DCK Package**
**6-Pin SOT or SC70**
**Top View**




**Pin Functions**

| PIN | | | DESCRIPTION |
|---|---|---|---|
| NAME | DRS, DRL, DPK NO. | DBV, DCK NO. | |
| IOx | 1, 2, 4, 5 | 1, 3, 4, 6 | ESD-protected channel |
| GND | 3 | 2 | Ground |
| $V_{CC}$ | 6 | 5 | Power-supply input. Bypass $V_{CC}$ to GND with a 0.1-µF ceramic capacitor. |
| N/A | Exposed Thermal Pad (DRS package only) | — | Exposed thermal pad. Connect to GND or leave floating. |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | | | –0.3 | 7 | V |
| $V_{I/O}$ | IO voltage tolerance | | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{(Surge)}$ | IEC 61000-4-5 peak pulse current ($T_P$ = 8/20 µs), IOx pins | | | 5.5 | A |
| $P_{(Surge)}$ | IEC 61000-4-5 peak pulse power ($T_P$ = 8/20 µs), IOx pins | | | 100 | W |
| $T_J$ | Junction temperature | | | 150 | °C |
| | Bump temperature (soldering) | Infrared (15 s) | | 220 | °C |
| | | Vapor phase (60 s) | | 215 | |
| | Lead temperature (soldering, 10 s) | | | 300 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| **TPD4E001 in DRS, DRL, and DPK Packages** | | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins except 1, 2, 4, and 5 | ±2000 | V |
| | | | Pins 1, 2, 4, and 5 | ±15000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | All pins | ±1000 | |
| **TPD4E001 in DBV and DCK Packages** | | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins except 1, 3, 4, and 6 | ±2000 | V |
| | | | Pins 1, 3, 4, and 6 | ±15000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | All pins | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 ESD Ratings: Surge Protection

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| **TPD4E001 in DRS, DRL, and DPK Packages** | | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 contact discharge | All pins | ±8000 | V |
| | | IEC 61000-4-2 air-gap discharge | All pins | ±15000 | |
| **TPD4E001 in DBV and DCK Packages** | | | | | |
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 contact discharge | All pins | ±8000 | V |
| | | IEC 61000-4-2 air-gap discharge | All pins | ±15000 | |

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_A$, operating free-air temperature range | | –40 | 85 | °C |
| Operating voltage | $V_{CC}$ pin | 0.9 | 5.5 | V |
| | IO1, IO2 pins | 0 | $V_{CC}$ | |

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## 6.5 Thermal Information

| THERMAL METRIC[1] | | TPD4E001 | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | DRL (SOT) | DBV (SOT) | DCK (SC70) | DPK (USON) | DRS (SON) | |
| | | 6 PINS | 6 PINS | 6 PINS | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 226.4 | 259.7 | 251.1 | 247.6 | 91.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 90.3 | 186.5 | 88.1 | 124.8 | 106.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 61.2 | 107.6 | 54.8 | 204.2 | 64.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.7 | 71.4 | 1.7 | 19.2 | 10.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 61.0 | 107.1 | 54.1 | 209.3 | 64.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | 29.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted), $V_{CC}$ = 5 V ±10%

| PARAMETER | | TEST CONDITIONS | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 0.9 | | 5.5 | V |
| $I_{CC}$ | Supply current | | | | 1 | 100 | nA |
| $V_F$ | Diode forward voltage | $I_F$ = 10 mA | | 0.65 | | 0.95 | V |
| $V_{BR}$ | Breakdown Voltage | $I_{BR}$ = 10 mA | | 11 | | | V |
| $V_C$ | Channel clamp voltage | $T_A$ = 25°C, ±15-kV HBM, $I_F$ = 10 A | Positive transients | | | $V_{CC}$ + 25 | V |
| | | | Negative transients | | | –25 | |
| | | $T_A$ = 25°C, ±8-kV Contact Discharge (IEC 61000-4-2), $I_F$ = 24 A | Positive transients | | | $V_{CC}$ + 60 | |
| | | | Negative transients | | | –60 | |
| | | $T_A$ = 25°C, ±15-kV Air-Gap Discharge (IEC 61000-4-2), $I_F$ = 45 A | Positive transients | | | $V_{CC}$ + 100 | |
| | | | Negative transients | | | –100 | |
| | | Surge strike on IO pin, GND pin grounded, $I_{PP}$ = 5A, 8/20 µs[2] | Positive transients | | 17 | | |
| $V_{RWM}$ | Reverse stand-off voltage | IO pin to GND pin | | | | 5.5 | V |
| $I_{I/O}$ | Channel leakage current | $V_{I/O}$ = GND to $V_{CC}$ | | | | ±1 | nA |
| $C_{I/O}$ | Channel input capacitance | $V_{CC}$ = 5 V, Bias of $V_{CC}$/2; $f$ = 10 MHz | | | 1.5 | | pF |

(1) Typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to ICE61000-4-5.


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## 6.7 Typical Characteristics

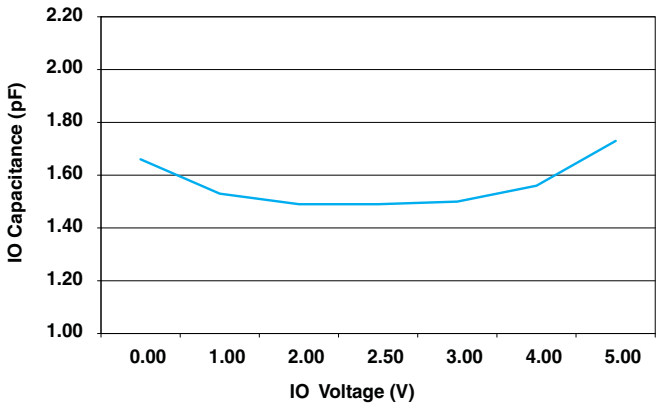



Figure 1. IO Capacitance vs IO Voltage ($V_{CC}$ = 5 V)

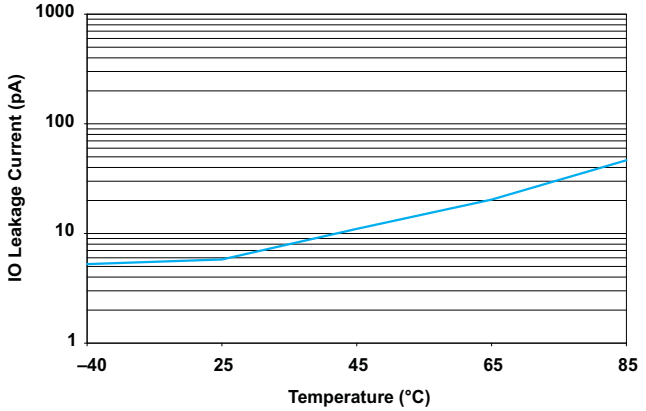



Figure 2. IO Leakage Current vs Temperature ($V_{CC}$ = 5.5 V)

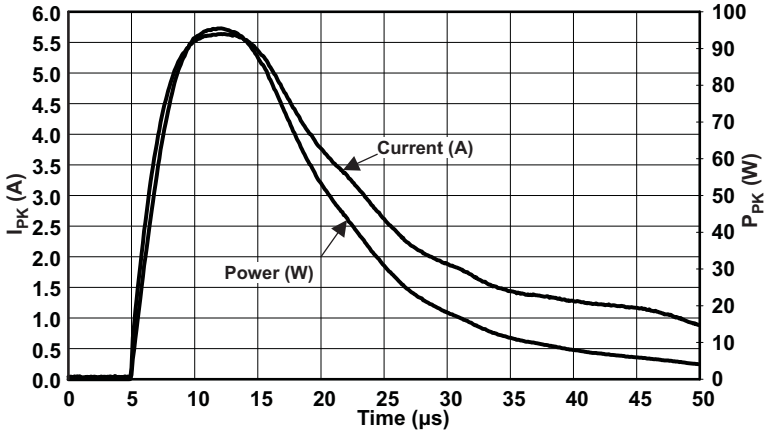


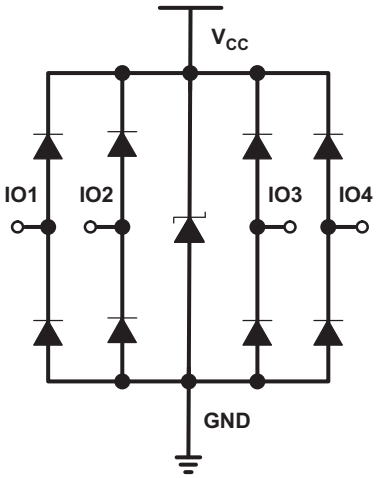

Figure 3. Peak Pulse Waveform, $V_{CC}$ = 5.5 V

# 7 Detailed Description

## 7.1 Overview

The TPD4E001 is a four-channel transient voltage suppressor (TVS) based ESD protection diode array. The TPD4E001 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device has a 1.5-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces. The ultra-low leakage current (<1 nA maximum) is suitable for precision analog measurements in applications like glucose meters and heart rate monitors.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The TPD4E001 is a uni-directional ESD protection device with low capacitance. The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. This central ESD clamp is also connected to $V_{CC}$ to provide protection for the $V_{CC}$ line. Each IO line is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard. The TPD4E001's low loading capacitance makes it ideal for protection high-speed signal terminals.

## 7.4 Device Functional Modes

The TPD4E001 is a passive-integrated circuit that activates whenever voltages above $V_{BR}$ or below the lower diodes $V_{forward}$ (–0.6V) are present upon the circuit being protected. During ESD events, voltages as high as ±15 kV can be directed to ground and $V_{CC}$ via the internal diode network. Once the voltages on the protected lines fall below the trigger voltage of the TPD4E001 (usually within 10's of nano-seconds) the device reverts back to a high-impedance state.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPD4E001 is a diode array type Transient Voltage Suppressor (TVS) which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low $R_{DYN}$ of the triggered TVS holds this voltage, $V_{CLAMP}$, to a tolerable level to the protected IC.

## 8.2 Typical Application

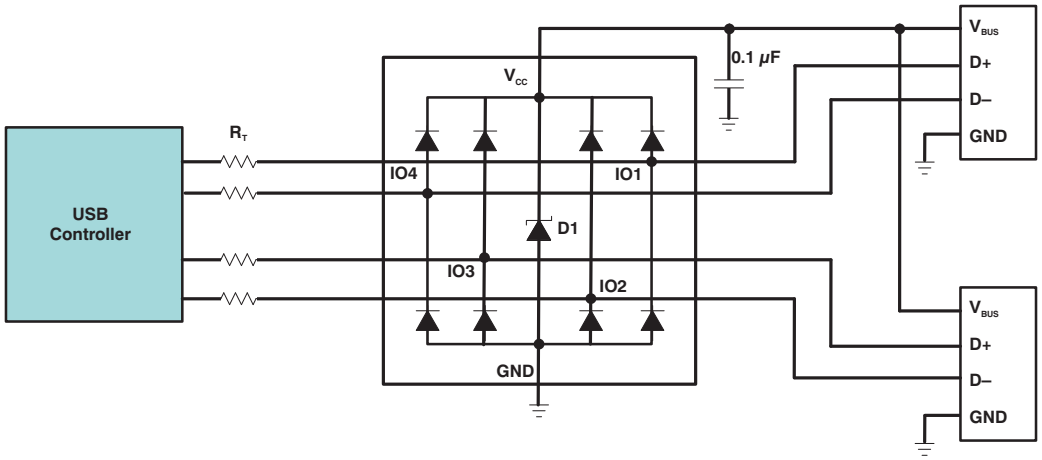



**Figure 4. Typical Application Schematic**

### 8.2.1 Design Requirements

For this design example, a single TPD4E001 is used to protect all the pins of two USB2.0 connectors.

Given the USB application, the following parameters are known.

**Table 1. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Signal range on IO1, IO2, IO3, and IO4 | 0 V to 3.6 V |
| Signal voltage range on $V_{CC}$ | 0 V to 5.25 V |
| Operating Frequency | 240 MHz |

### 8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD4E001 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD4E001 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, the following layout/ design guidelines should be followed:

1. Place the TPD4E001 solution close to the connectors. This allows the TPD4E001 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-µF capacitor very close to the $V_{CC}$ pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.

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3. Ensure that there is enough metallization for the $V_{CC}$ and GND loop. During normal operation, the TPD4E001 consumes nA leakage current. But during the ESD event, $V_{CC}$ and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
4. Leave the unused IO pins floating. In this example of protecting two USB ports, none of the IO pins will be left unused.
5. The $V_{CC}$ pin can be connected in two different ways:
   (a) If the $V_{CC}$ pin is connected to the system power supply, the TPD4E001 works as a transient suppressor for any signal swing above $V_{CC}$ + $V_F$. A 0.1-µF capacitor on the device $V_{CC}$ pin is recommended for ESD bypass.
   (b) If the $V_{CC}$ pin is not connected to the system power supply, the TPD4E001 can tolerate higher signal swing in the range up to 10 V. Please note that a 0.1-µF capacitor is still recommended at the $V_{CC}$ pin for ESD bypass.

### 8.2.3 Application Curve

Figure 5 is a capture of the voltage clamping waveform of TPD4E001DRL on IO3 during a +8kV Contact IEC61000-4-2 ESD strike.

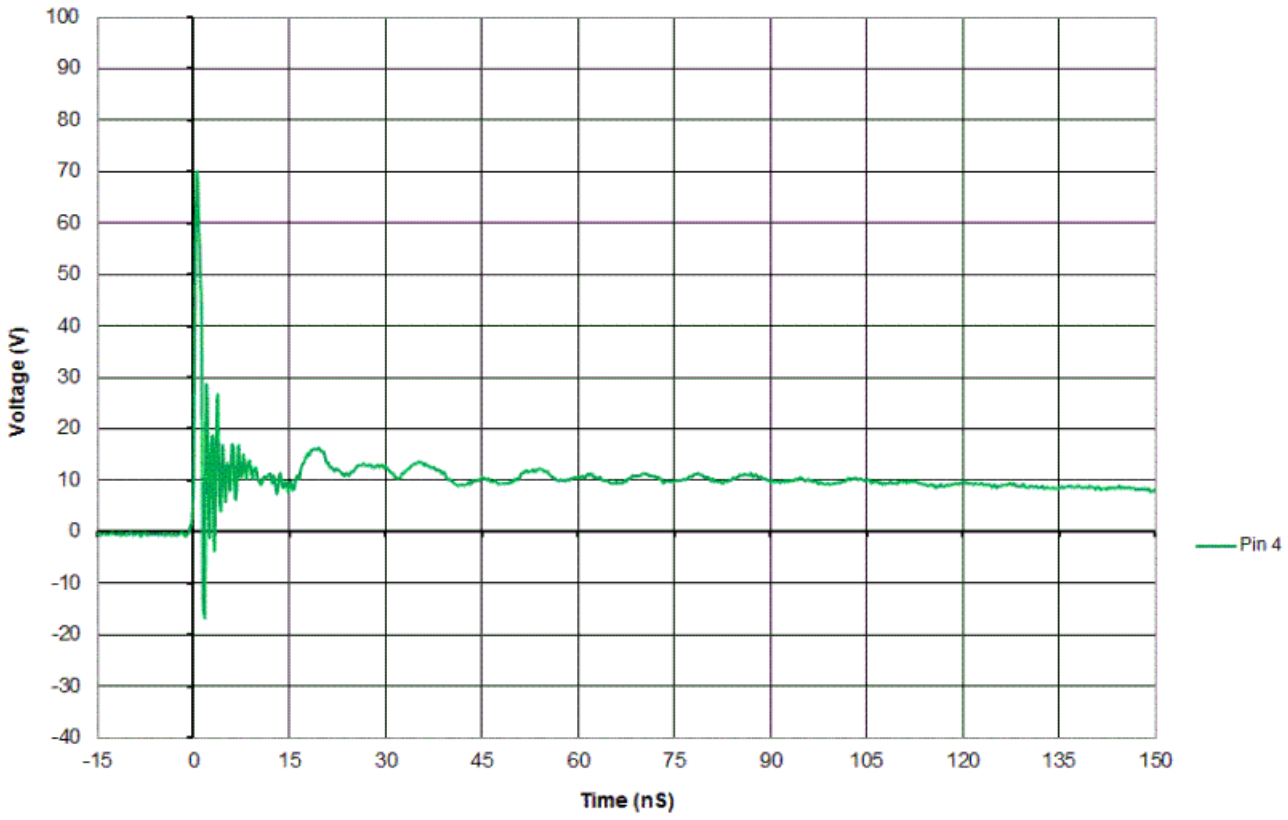



**Figure 5. TPD4E001DRL IEC61000-4-2 Voltage Clamp Waveform +8kV Contact**


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# 9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Take care to make sure that the maximum voltage specifications for each pin are not violated.

# 10 Layout

## 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

## 10.2 Layout Example

The following is a layout example for protecting two interface ports with the TPD4E001. One example would be two USB 2.0 ports, as was discussed in the Application and Implementation section. For the USB 2.0 example, IO1 and IO2 would be D+ and D-, respectively, of USB port 1. IO3 and IO4 would be D- and D+, respectively, of USB port 2.

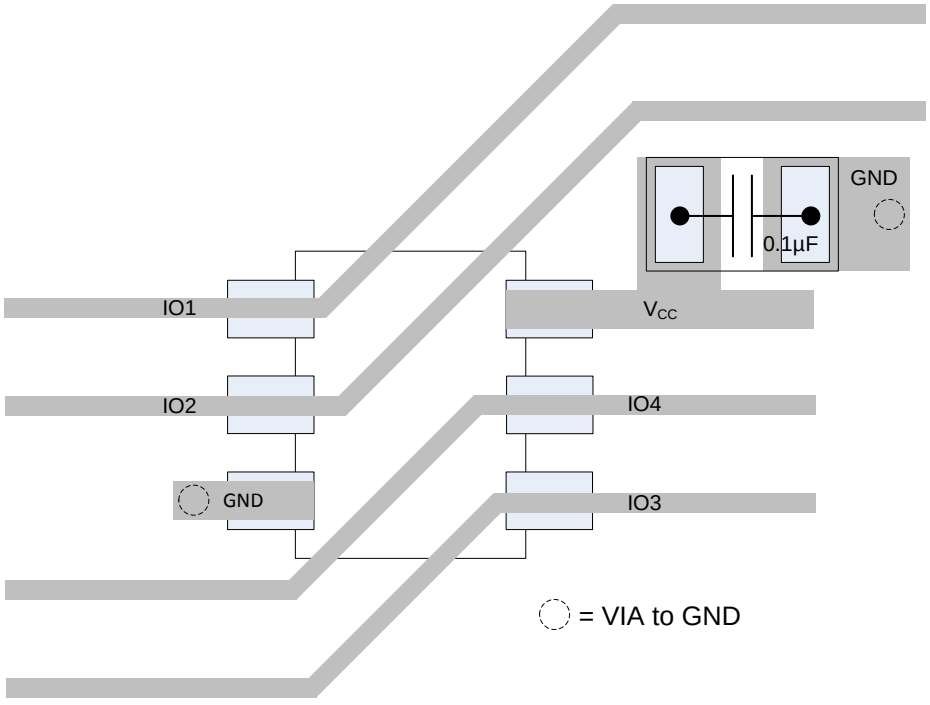



**Figure 6. Routing With DRL Package**

# 11 Device and Documentation Support

## 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPD4E001 | Click here | Click here | Click here | Click here | Click here |
| TPD4E1U06 | Click here | Click here | Click here | Click here | Click here |

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.3 Trademarks

E2E is a trademark of Texas Instruments.
FireWire is a trademark of Apple Inc.
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| HPA00782DRLR | ACTIVE | SOT-5X3 | DRL | 6 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (2C7 ~ 2CR) (2CG ~ 2CH) | Samples |
| TPD4E001DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 85 | (NFY ~ NFY5) NFYS | Samples |
| TPD4E001DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (2CF ~ 2CR) (2CP ~ 2CP) 2CH | Samples |
| TPD4E001DPKR | ACTIVE | USON | DPK | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2C7 | Samples |
| TPD4E001DPKT | ACTIVE | USON | DPK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 2C7 | Samples |
| TPD4E001DRLR | ACTIVE | SOT-5X3 | DRL | 6 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (2C7 ~ 2CR) (2CG ~ 2CH) | Samples |
| TPD4E001DRLRG4 | ACTIVE | SOT-5X3 | DRL | 6 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (2C7 ~ 2CR) (2CG ~ 2CH) | Samples |
| TPD4E001DRSR | ACTIVE | SON | DRS | 6 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ZWM | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPD4E001 :**

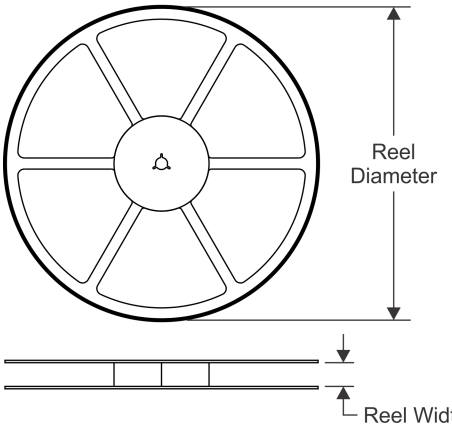
- Automotive: TPD4E001-Q1

NOTE: Qualified Version Definitions:

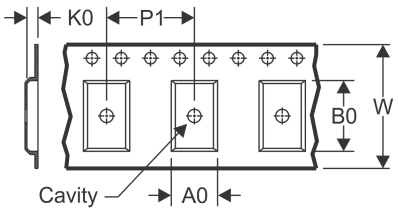
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

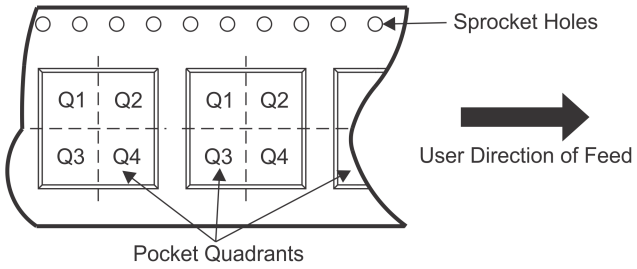



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

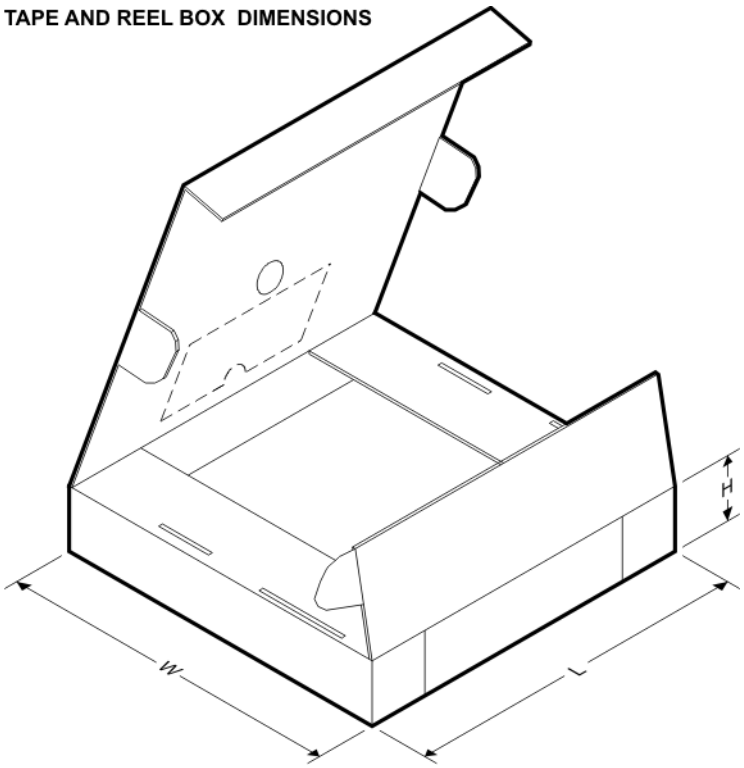
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD4E001DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPD4E001DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TPD4E001DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPD4E001DPKR | USON | DPK | 6 | 5000 | 180.0 | 9.5 | 1.75 | 1.75 | 0.7 | 4.0 | 8.0 | Q2 |
| TPD4E001DPKT | USON | DPK | 6 | 250 | 180.0 | 9.5 | 1.75 | 1.75 | 0.7 | 4.0 | 8.0 | Q2 |
| TPD4E001DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 9.5 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| TPD4E001DRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| TPD4E001DRSR | SON | DRS | 6 | 1000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

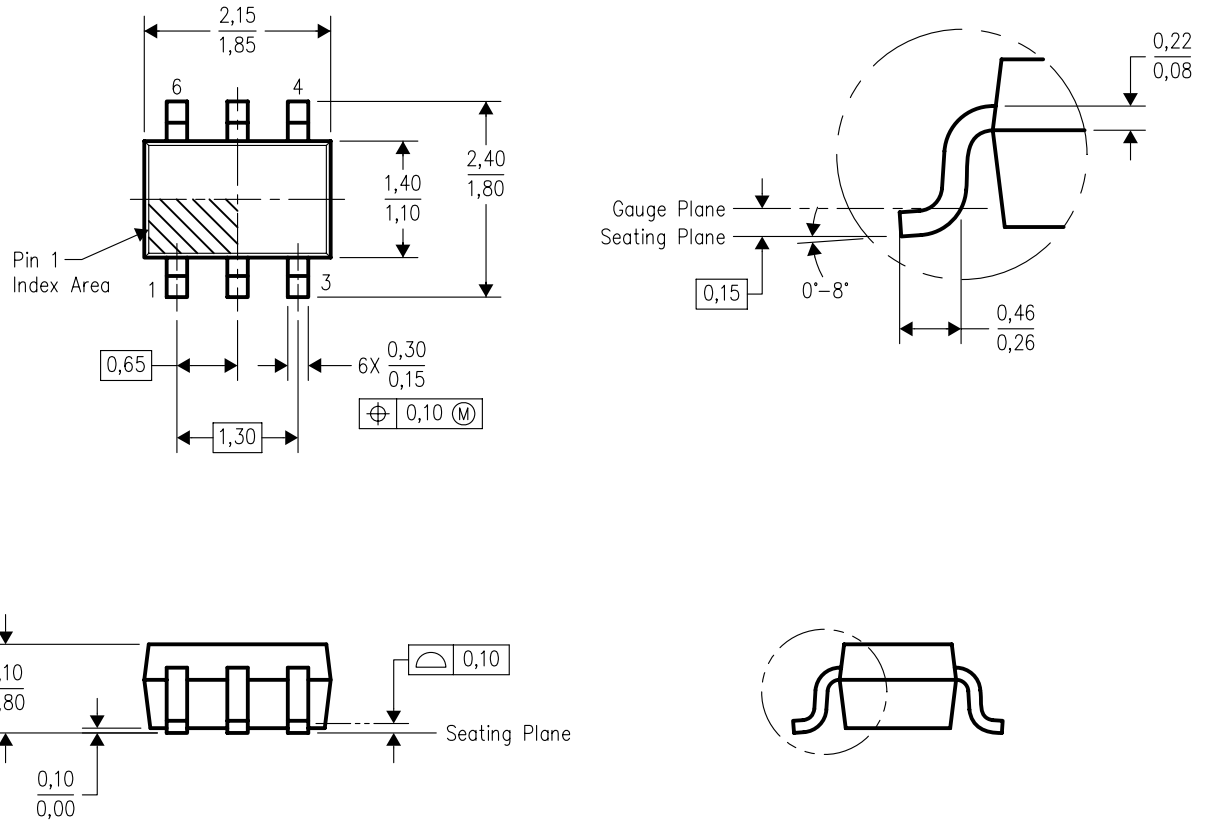
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD4E001DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPD4E001DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TPD4E001DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TPD4E001DPKR | USON | DPK | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| TPD4E001DPKT | USON | DPK | 6 | 250 | 184.0 | 184.0 | 19.0 |
| TPD4E001DRLR | SOT-5X3 | DRL | 6 | 4000 | 184.0 | 184.0 | 19.0 |
| TPD4E001DRLR | SOT-5X3 | DRL | 6 | 4000 | 202.0 | 201.0 | 28.0 |
| TPD4E001DRSR | SON | DRS | 6 | 1000 | 367.0 | 367.0 | 35.0 |

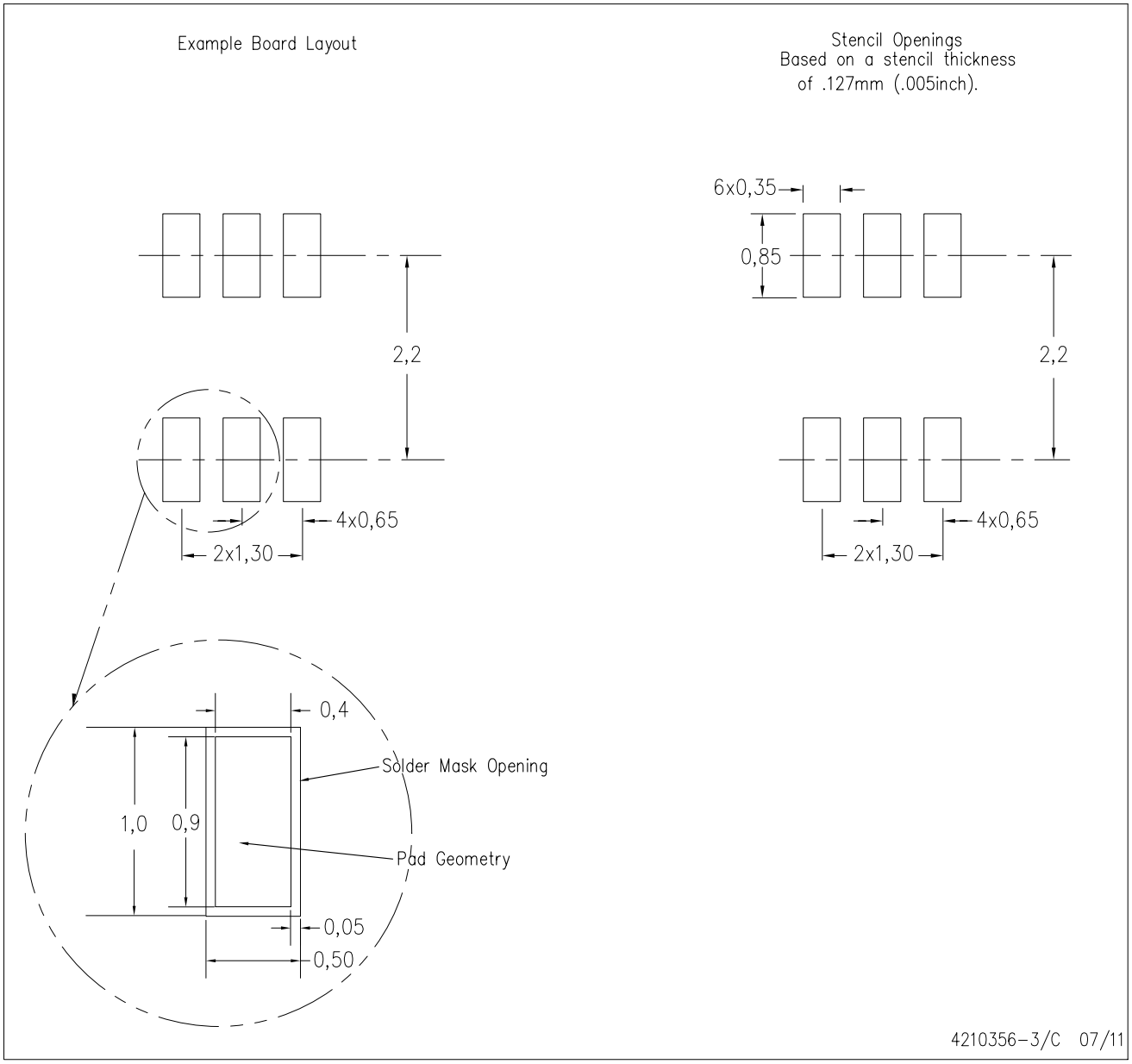
## DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4093553–4/G 01/2007

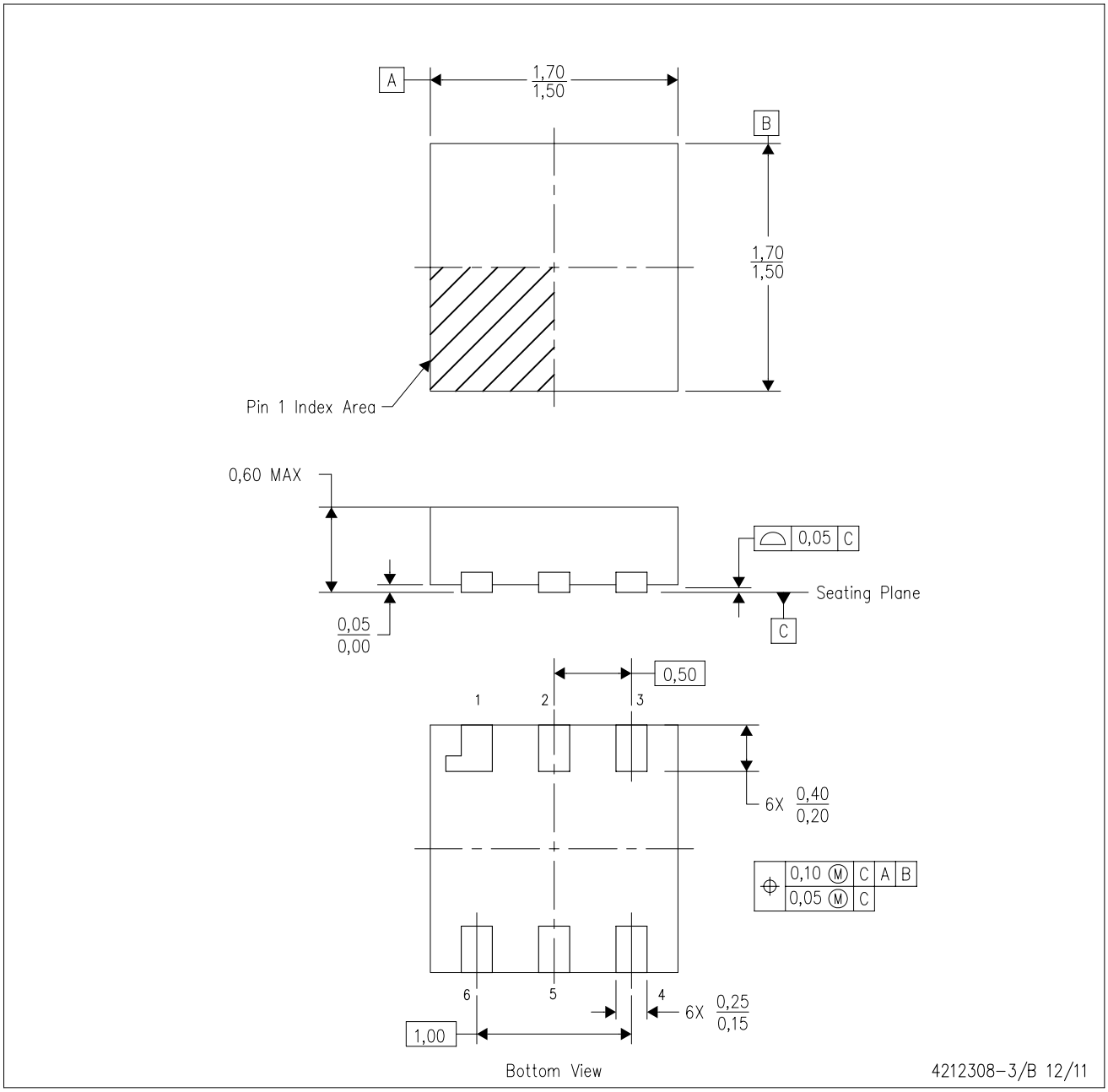
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

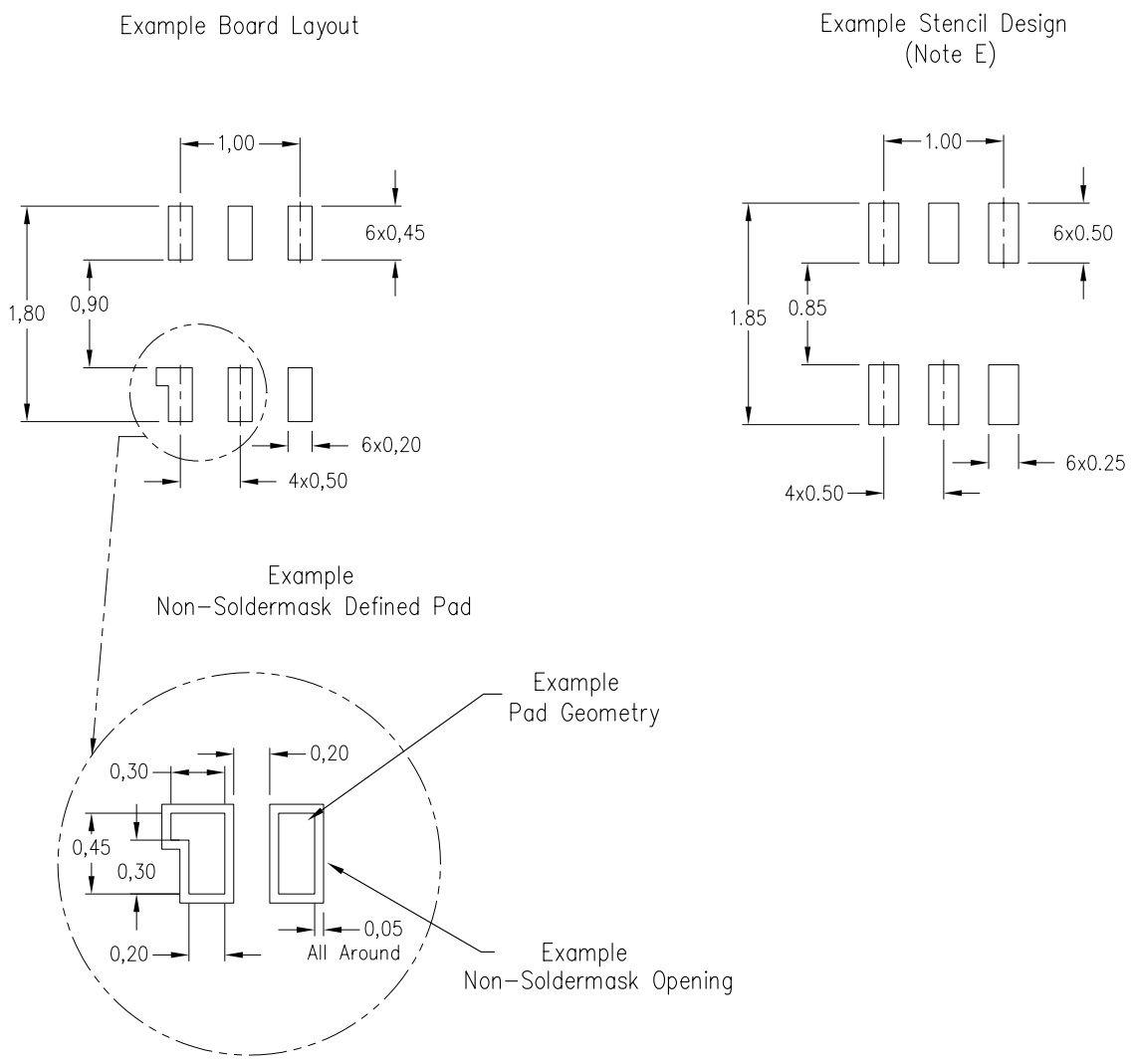
DPK (S–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



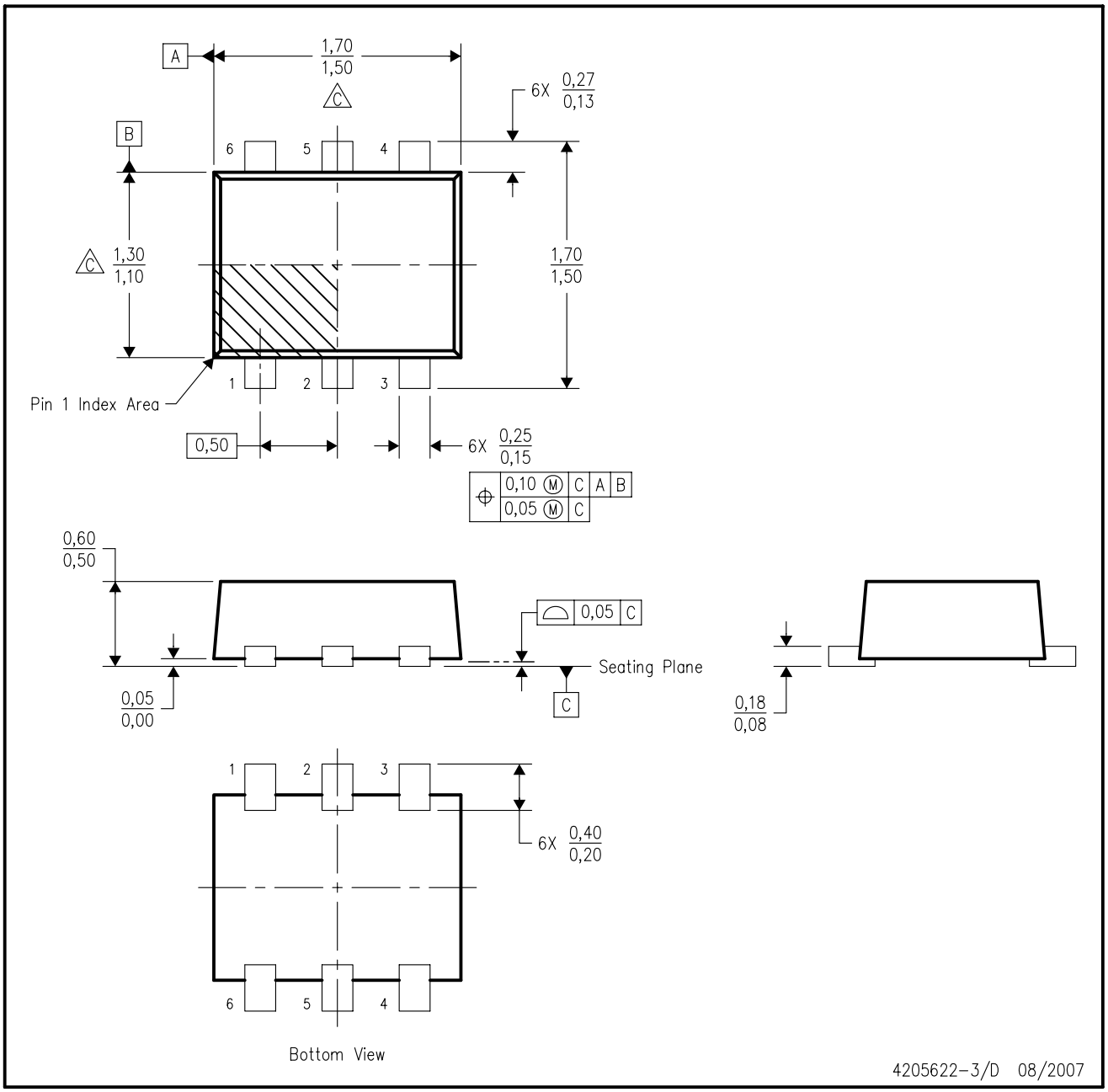

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.

DPK (S–PUSON–N6)

PLASTIC SMALL OUTLINE NO–LEAD

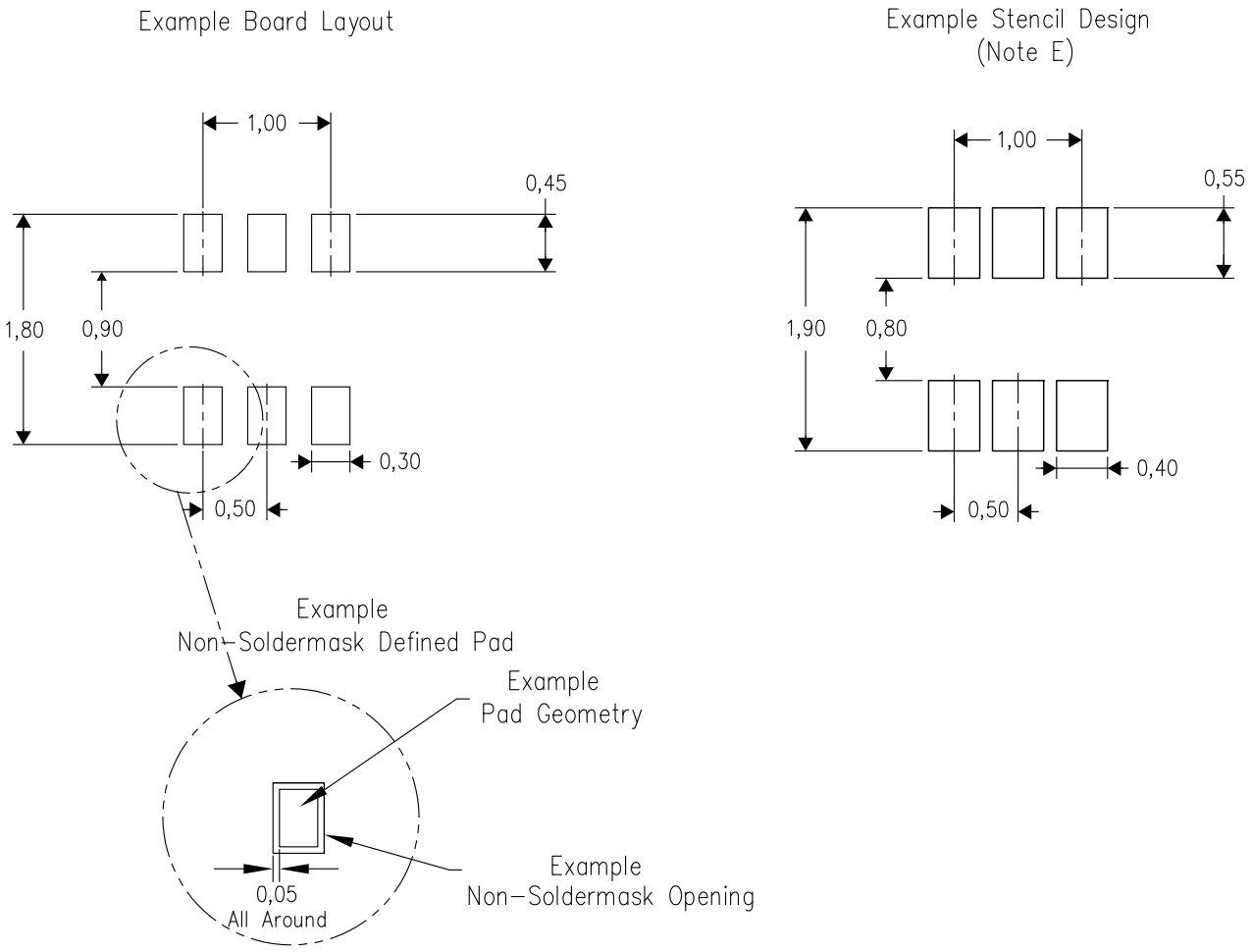



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

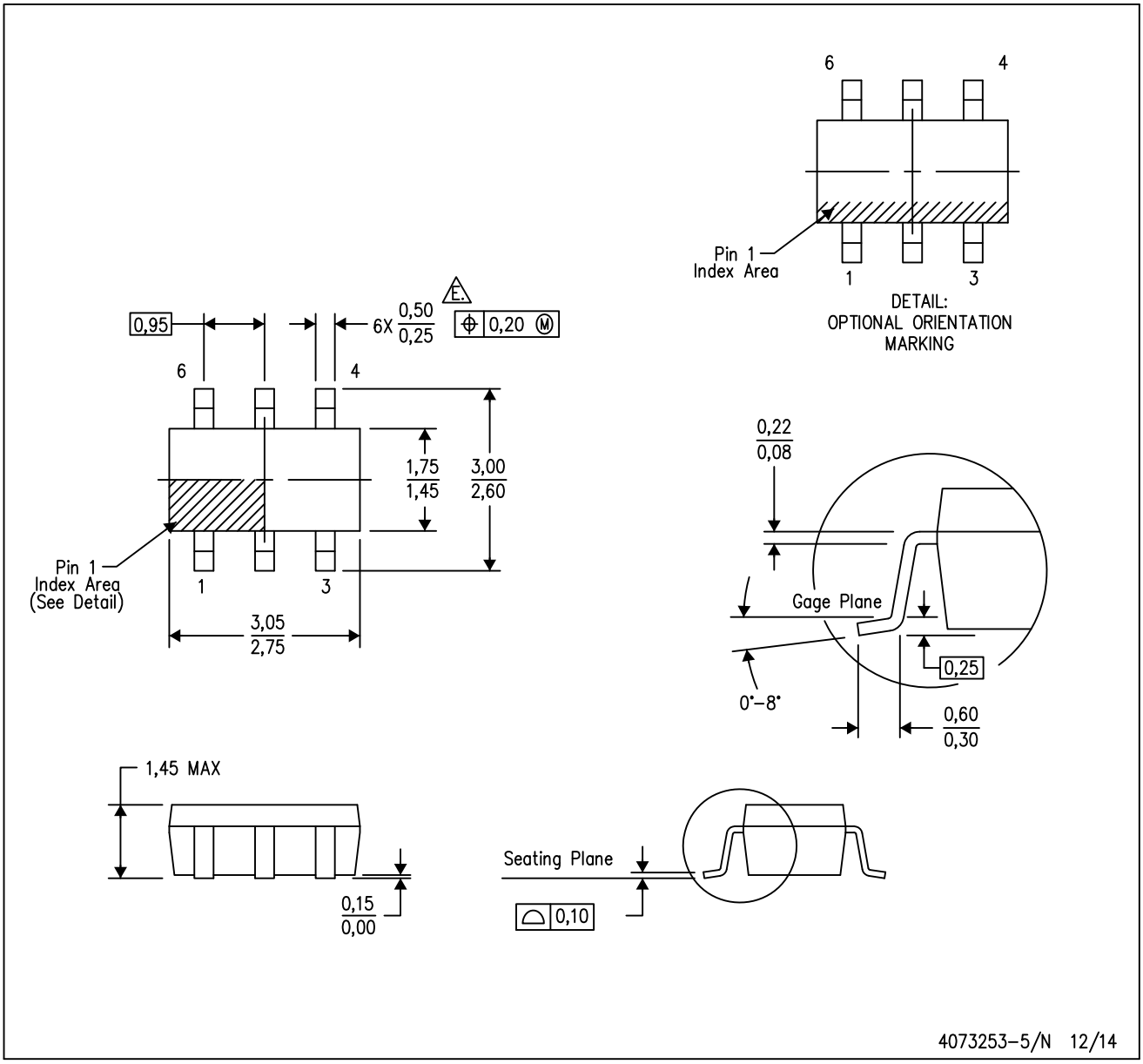
DRL (R–PDSO–N6) PLASTIC SMALL OUTLINE




4208207–3/E 06/12

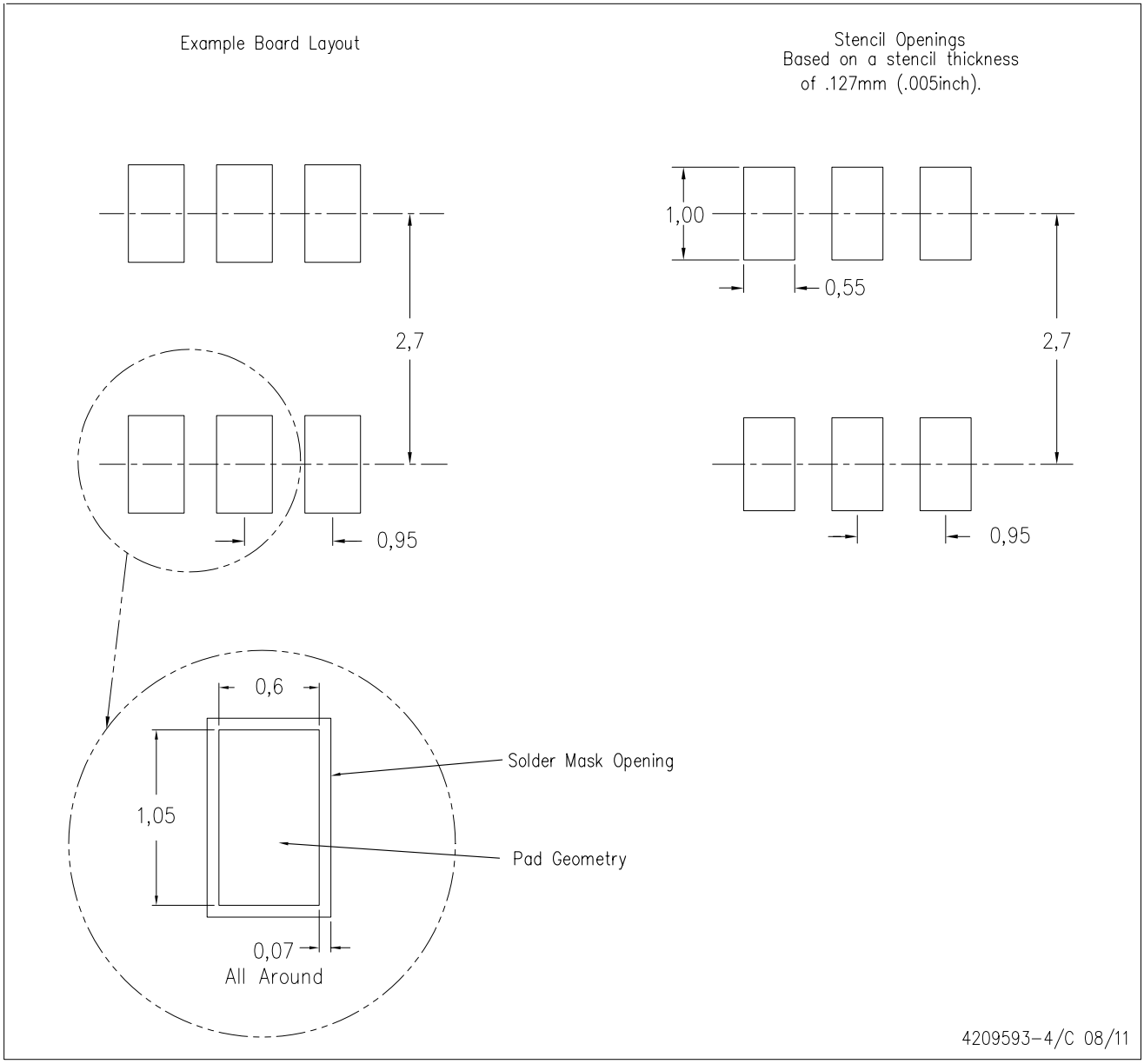
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



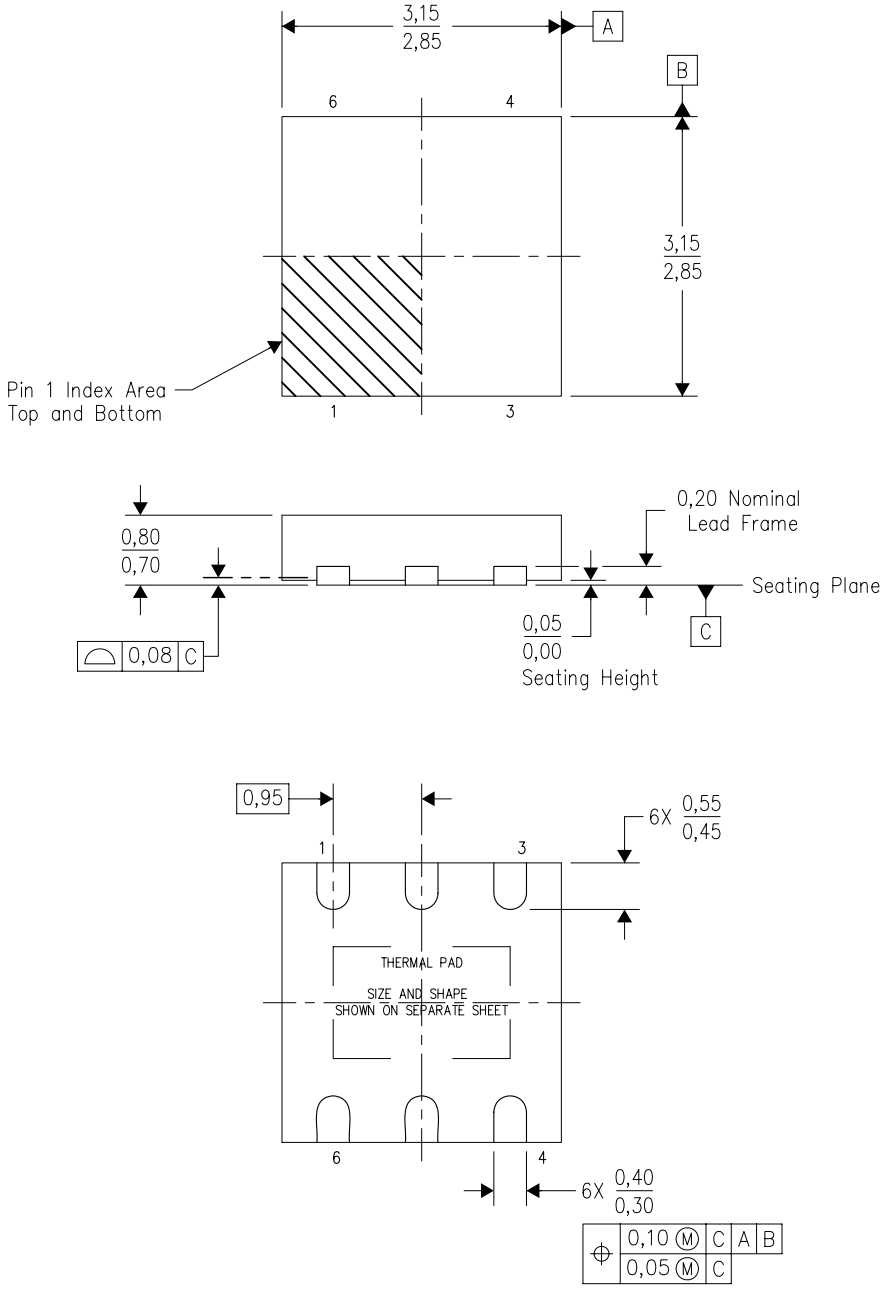

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4206219/F 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

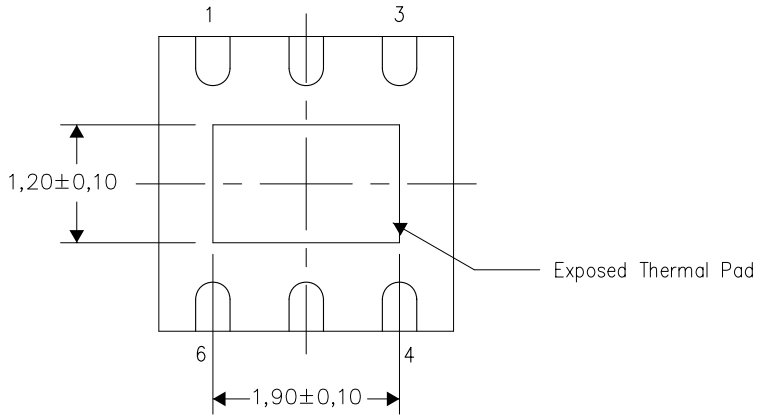
DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



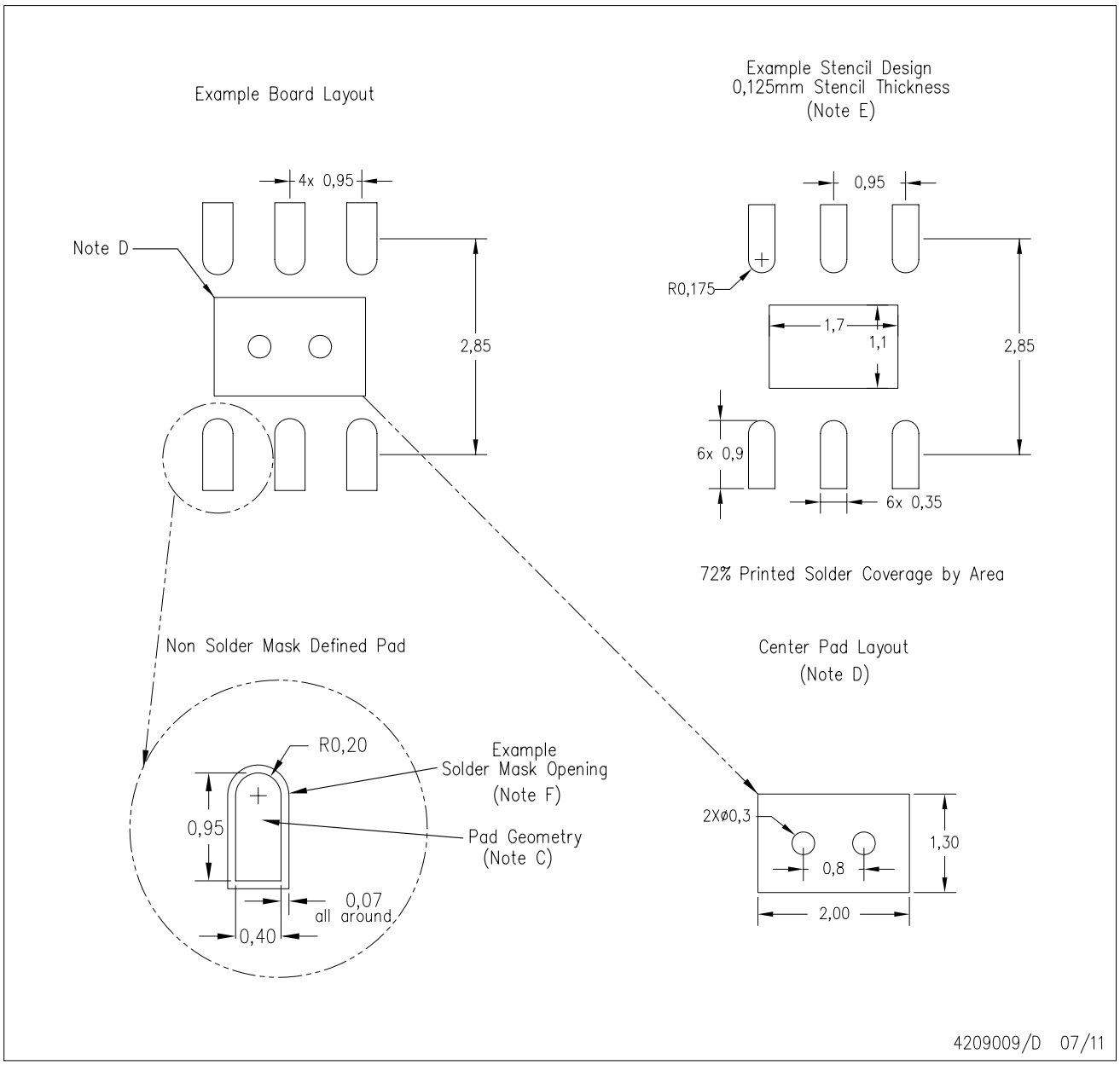

Bottom View

Exposed Thermal Pad Dimensions

4207663/E 07/11

NOTE: All linear dimensions are in millimeters

# DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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