# TPD2E007 2-Channel ESD Protection Array for AC-Coupled/Negative-Rail Data Interfaces

## 1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV IEC 61000-4-2 Contact Discharge
  - ±15-kV IEC 61000-4-2 Air-Gap Discharge
- IEC 61000-4-5 Surge Protection
  - 4.5-A Peak Pulse Current (8/20-µs Pulse)
- IO Capacitance 15 pF (Max)
- Low 50-nA Leakage Current
- Space-Saving PicoStar™ and SOT Package

## 2 Applications

- Cell Phones
- Audio Interface Connections
- Consumer Electronics (DVR, Set-Top Box, TV)
- Industrial Interfaces (RS-232, RS-485, RS-422, LVDS)

## 3 Description

This device is a transient voltage suppressor (TVS) based electrostatic discharge (ESD) protection device designed to offer system level ESD solutions for wide range of portable and industrial applications. The back-to-back diode array allows AC-coupled or negative-going data transmission (audio interface, LVDS, RS-485, RS-232, and so forth) without compromising signal integrity. This device exceeds the IEC 61000-4-2 (Level 4) ESD protection and is ideal for providing system level ESD protection for the internal ICs when placed near the connector.

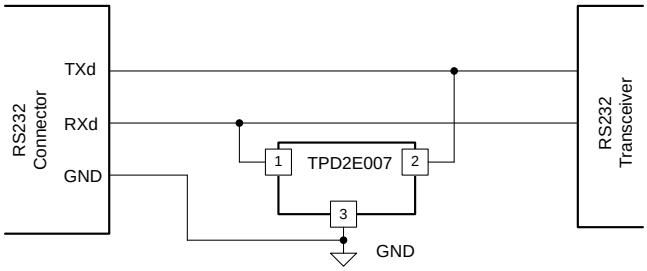
The TPD2E007 is offered in a 4-bump PicoStar and 3-pin SOT (DGK) packages. The PicoStar package (YFM), with only 0.15 mm (Max) package height, is recommended for ultra space saving application where the package height is a key concern. The PicoStar package can be used in either embedded PCB board applications or in surface mount applications. The industry standard SOT package offers straightforward board layout option in legacy designs.

**Device Information(1)**

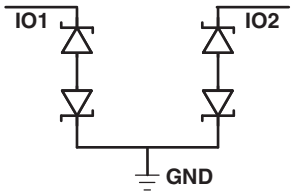
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPD2E007 | SOT (3) | 2.00 mm x 1.25 mm |
| | PicoStar (4) | 0.77 mm x 0.77 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Example Schematic**




**Equivalent Schematic Representation**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision H (January 2016) to Revision I** — **Page**

- Made changes to *ESDS* section ... 1

**Changes from Revision G (December 2015) to Revision H** — **Page**

- Updated the break-down voltage for clarity ... 5

**Changes from Revision F (August 2014) to Revision G** — **Page**

- Updated the *Handling Ratings* table to an *ESD Ratings* table and moved $T_{stg}$ to the *Absolute Maximum Ratings* table ... 4
- Added $f$ = *10 MHz* to the *Channel input capacitance* test condition in the *Electrical Characteristics* table ... 5
- Added *Community Resources* ... 9

**Changes from Revision E (August 2010) to Revision F** — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

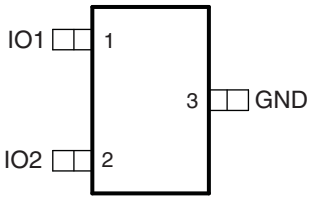
**Changes from Revision D (October 2009) to Revision E** — **Page**

- Added max continuous power dissipation value for DCK package ... 4

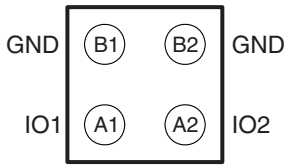

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# 5 Pin Configuration and Functions

**DCK Package**
**3-Pin SOT**
**Top View**




**YFM Package**
**4-Pin PicoStar**
**Bottom View**




0.8 mm × 0.8 mm (0.4 mm pitch)

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | DCK NO. | YFM NO. | | |
| GND | 3 | B1, B2 | G | Ground |
| IO1 | 1 | A1 | IO | ESD protected channel |
| IO2 | 2 | A2 | IO | ESD protected channel |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IO}$ | | | –13.5 | 13.5 | V |
| | Continuous power dissipation ($T_A$ = 70°C) | YFM package | | 270 | mW |
| | | DCK package | | 218 | |
| | Operating temperature | | –40 | 85 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |
| | Bump temperature (soldering) | Infrared (15 s) | | 220 | °C |
| | | Vapor phase (60 s) | | 215 | |
| | Lead temperature (soldering, 10 s) | | | 300 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±15000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 ESD Ratings: Surge Protection

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 ESD ratings | Contact | ±8000 | V |
| | | | Air gap | ±15000 | |

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IO}$ | Operating voltage | –13 | | 13 | V |
| | Operating temperature | –40 | | 85 | °C |

## 6.5 Thermal Information

| THERMAL METRIC(1) | | TPD2E007 | | UNIT |
|---|---|---|---|---|
| | | DCK (SOT) | YFM (PicoStar) | |
| | | 3 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 251.9 | 175.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 115.4 | 39.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 42.4 | 28.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.4 | 8.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 42.2 | 28.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.


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## 6.6 Electrical Characteristics

$T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BRF}$ | Break-down voltage, pin 1 or 2 to GND | $I_{IO}$ = 10 mA | 14 | | | V |
| $V_{BRR}$ | Break-down voltage, GND to pin 1 or 2 | $I_{IO}$ = 10 mA | 14 | | | V |
| $I_{IO}$ | Channel leakage current | | | 20 | 50 | nA |
| $R_d$ | Dynamic resistance | | | 3.5 | | Ω |
| $C_{IN}$ | Channel input capacitance | $V_{IO}$ = 2.5 V; $f$ = 10 MHz | | 10 | 15 | pF |

(1) Typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.

## 6.7 Typical Characteristics

IEC Clamping Waveforms (20 ns/div)

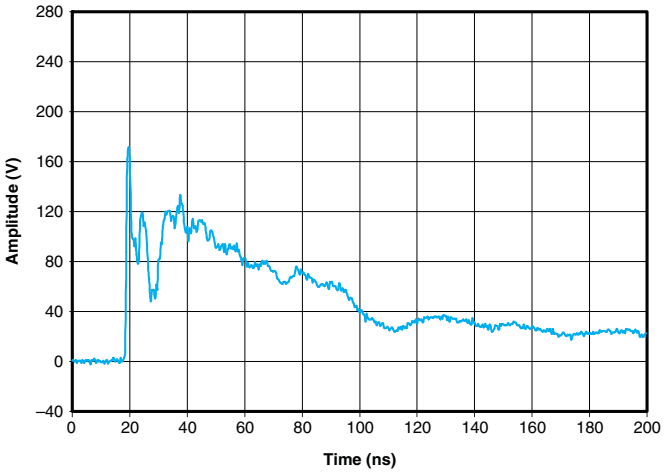



**Figure 1. 8-kV Contact**

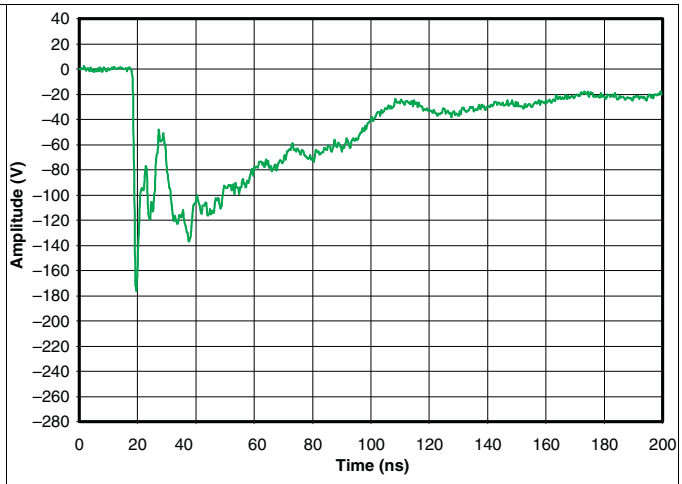



**Figure 2. –8-kV Contact**

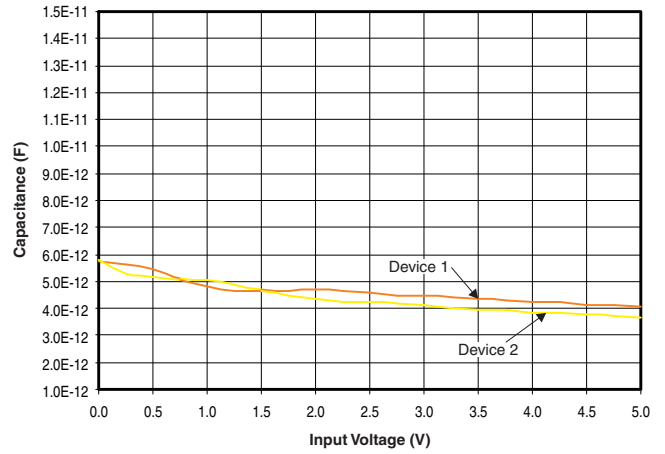



**Figure 3. Capacitance vs Input Voltage at $T_A$ = 27°C**

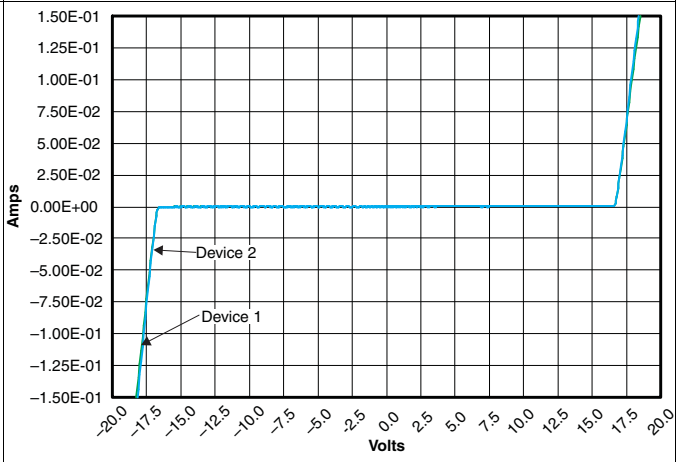



**Figure 4. Diode Breakdown Voltage Data at $T_A$ = 27°C**

# 7 Detailed Description

## 7.1 Overview

The TPD2E007 an ESD protection device designed to offer system level ESD solutions for wide range of portable and industrial applications. The back-to-back diode array allows AC-coupled or negative-going data transmission (audio interface, LVDS, RS-485, RS-232, etc.) without compromising signal integrity. The PicoStar package is intended to be embedded inside the printed circuit board which saves board space in portable applications. This device exceeds the IEC 61000-4-2 (Level 4) ESD protection and is ideal for providing system level ESD protection for the internal ICs when placed near the connector.

## 7.2 Functional Block Diagram

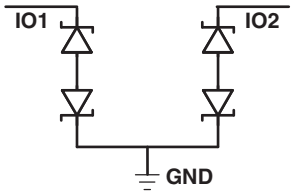



**Figure 5. Equivalent Schematic Representation**

## 7.3 Feature Description

The TPD2E007 an ESD protection device designed to offer system level ESD solutions for wide range of portable and industrial applications. The back-to-back diode array allows AC-coupled or negative-going data transmission (audio interface, LVDS, RS-485, RS-232, etc.) without compromising signal integrity. The PicoStar package is intended to be embedded inside the printed circuit board which saves board space in portable applications. This device exceeds the IEC 61000-4-2 (Level 4) ESD protection and is ideal for providing system level ESD protection for the internal ICs when placed near the connector.

### 7.3.1 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15 kV-air. An ESD/surge clamp diverts the current to ground.

### 7.3.2 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 4.5 A (8/20 µs waveform). An ESD/surge clamp diverts this current to ground.

### 7.3.3 IO Capacitance

The capacitance between each I/O pin to ground is 15 pF.

### 7.3.4 Low 50-nA Leakage Current

The I/O pins feature a low 50-nA (max) leakage current.

### 7.3.5 Space-Saving PicoStar and SOT Package

This device is offered in both a space-saving PicoStar package, as well as a standard DCK package.

## 7.4 Device Functional Modes

TPD2E007 is a passive integrated circuit that triggers when voltages are above or below $V_{BR}$. During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD2E007 (usually within 10's of nano-seconds) the device reverts to passive.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

TPD2E007 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC.

## 8.2 Typical Application

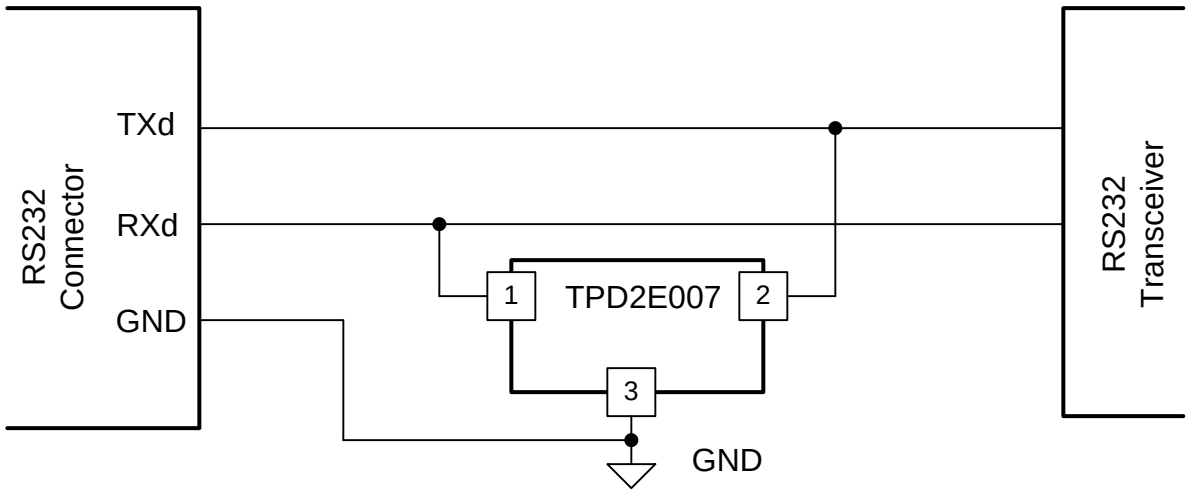



**Figure 6. Example Schematic**

### 8.2.1 Design Requirements

For this design example, a single TPD2E007 is used to protect an RS232 3-wire connector.

Given the application, the following parameters are known.

**Table 1. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Signal range on all pins except GND | –12 V to 12 V |
| Surge Withstand - IEC 61000-4-5 | 150 W |

### 8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal voltage range on all protected lines
- Surge Withstand

#### *8.2.2.1 Signal Range on IO1 and IO2 Pins*

The TPD2E007 has 2 IO pins which can support up to ±13 V.

#### *8.2.2.2 Surge Withstand*

The TPD2E007 can withstand up to 170W of IEC 61000-4-5 8/20-µs surge.

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### 8.2.3 Application Curve

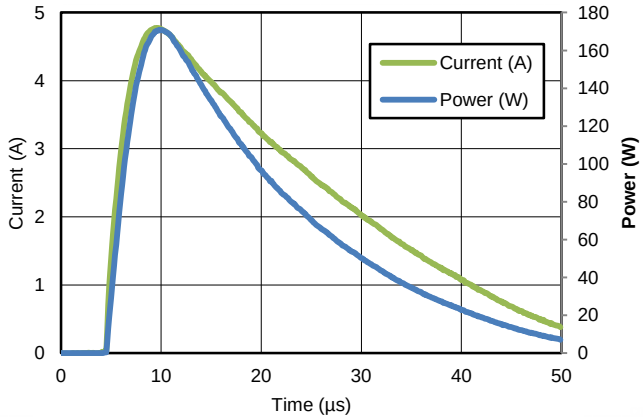



**Figure 7. Surge Pulse Waveform**

## 9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (±13 V) to ensure the device functions properly.

## 10 Layout

### 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 10.2 Layout Example

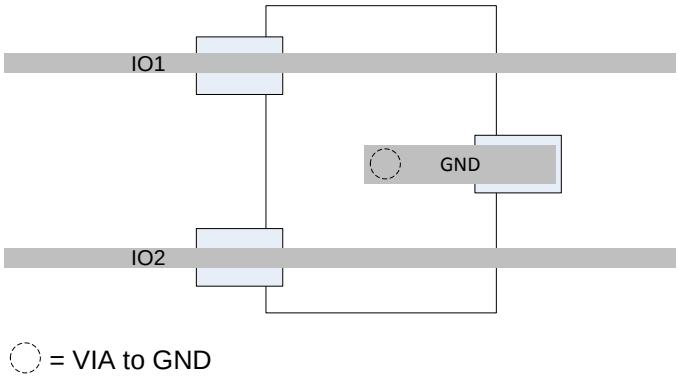



**Figure 8. Layout Recommendation**


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# 11 Device and Documentation Support

## 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.2 Trademarks

PicoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD2E007DCKR | ACTIVE | SC70 | DCK | 3 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 45U | Samples |
| TPD2E007YFMRG4 | ACTIVE | DSLGA | YFM | 4 | 3000 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | -40 to 85 | 45<br>T | Samples |
| TPD2E007YFMTG4 | ACTIVE | DSLGA | YFM | 4 | 250 | Green (RoHS & no Sb/Br) | Call TI | Level-1-260C-UNLIM | -40 to 85 | 45<br>T | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

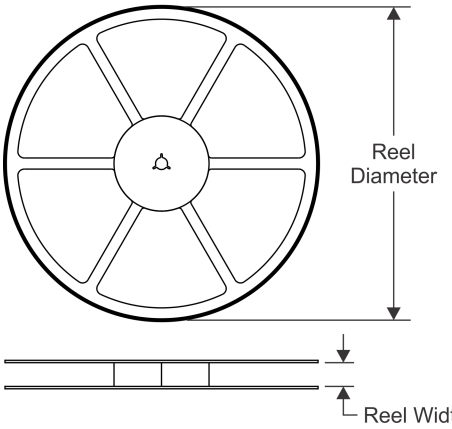
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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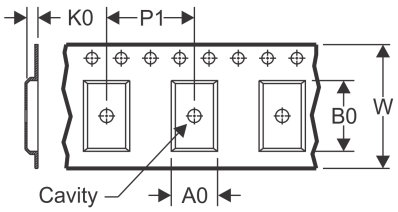
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

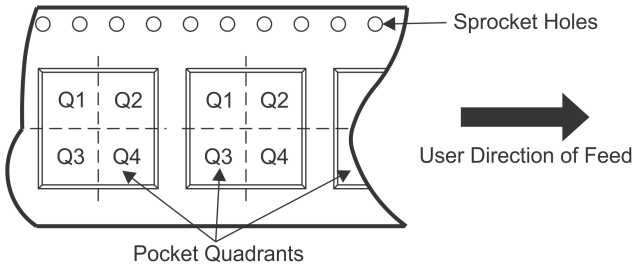



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

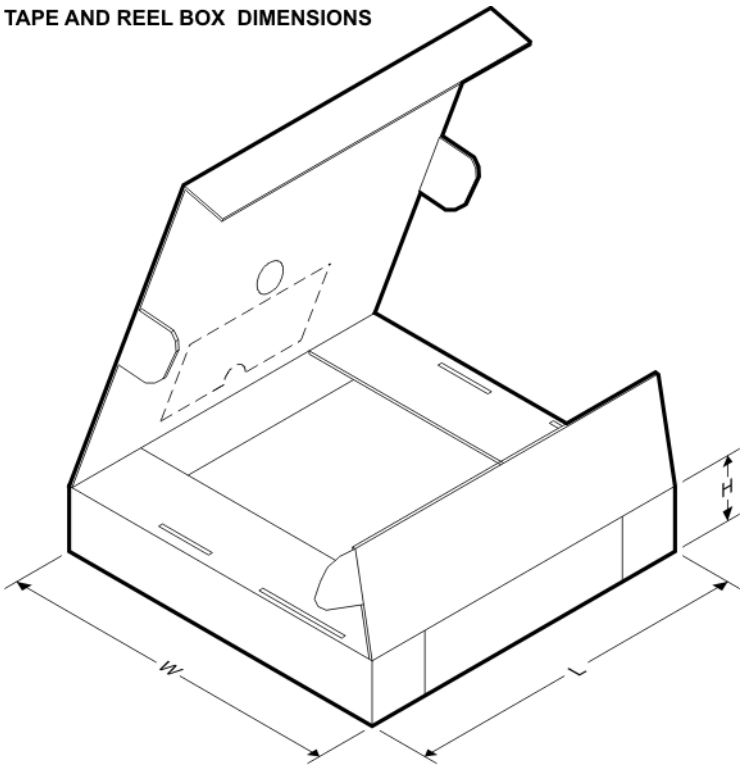
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD2E007DCKR | SC70 | DCK | 3 | 3000 | 179.0 | 8.4 | 2.4 | 2.4 | 1.19 | 4.0 | 8.0 | Q3 |
| TPD2E007YFMRG4 | DSLGA | YFM | 4 | 3000 | 178.0 | 9.2 | 0.83 | 0.83 | 0.19 | 4.0 | 8.0 | Q1 |
| TPD2E007YFMTG4 | DSLGA | YFM | 4 | 250 | 178.0 | 9.2 | 0.83 | 0.83 | 0.19 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

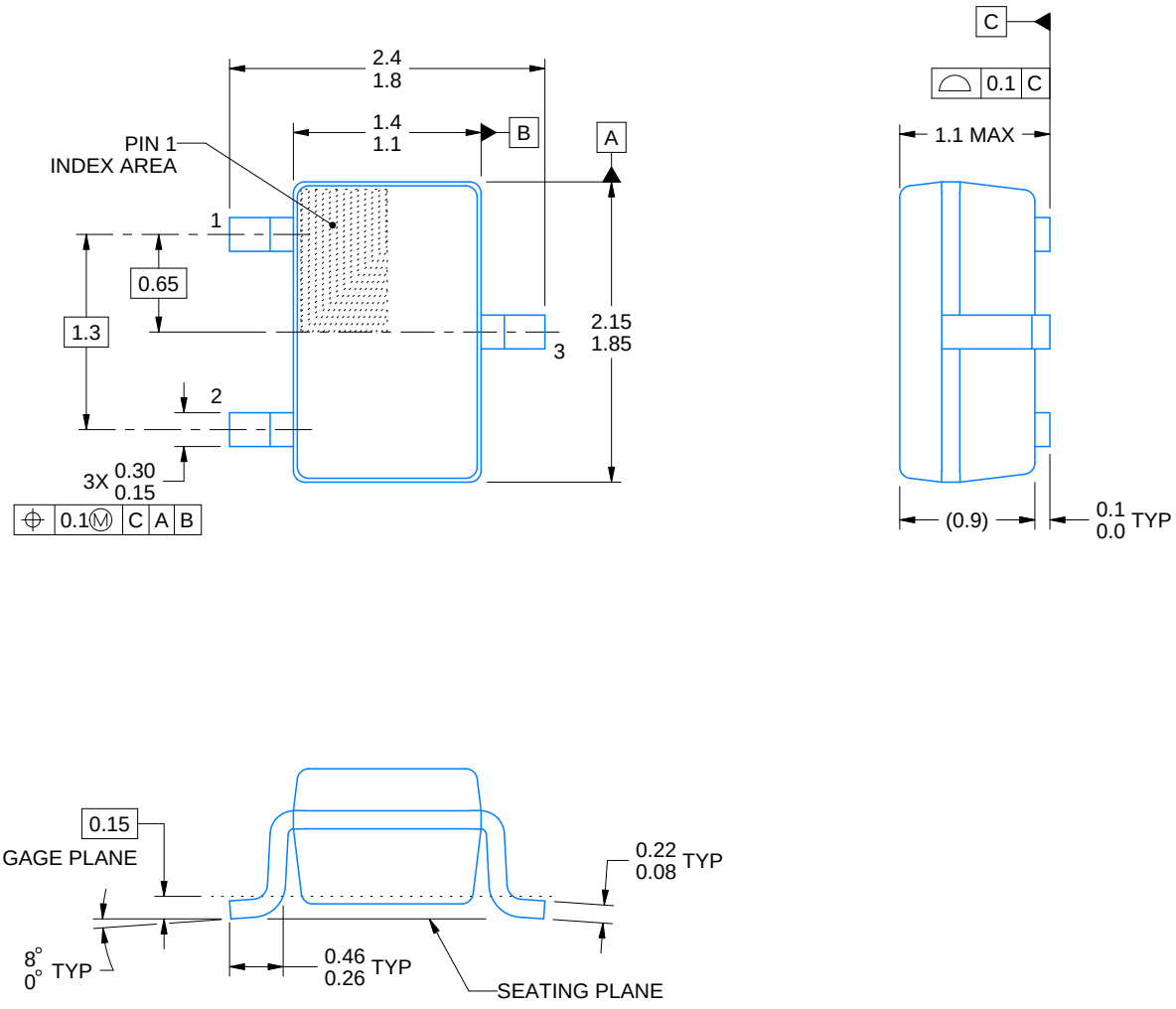
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD2E007DCKR | SC70 | DCK | 3 | 3000 | 195.0 | 200.0 | 45.0 |
| TPD2E007YFMRG4 | DSLGA | YFM | 4 | 3000 | 220.0 | 220.0 | 35.0 |
| TPD2E007YFMTG4 | DSLGA | YFM | 4 | 250 | 220.0 | 220.0 | 35.0 |

# DCK0003A

# PACKAGE OUTLINE

## SOT-SC70 - 1.1 max height

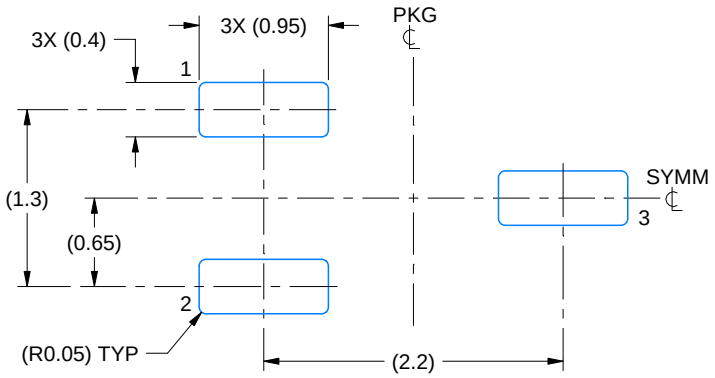
SMALL OUTLINE TRANSISTOR SC70



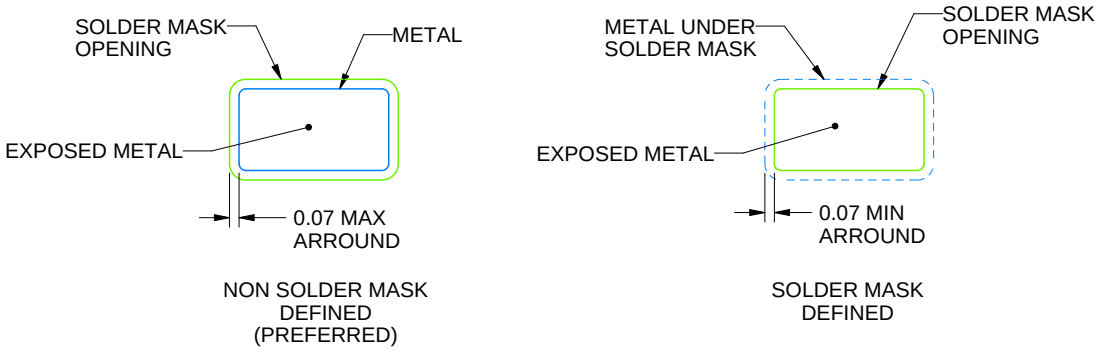

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

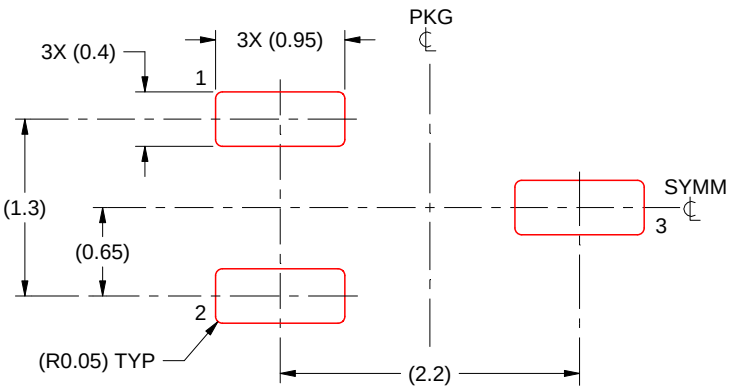



SOLDER MASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



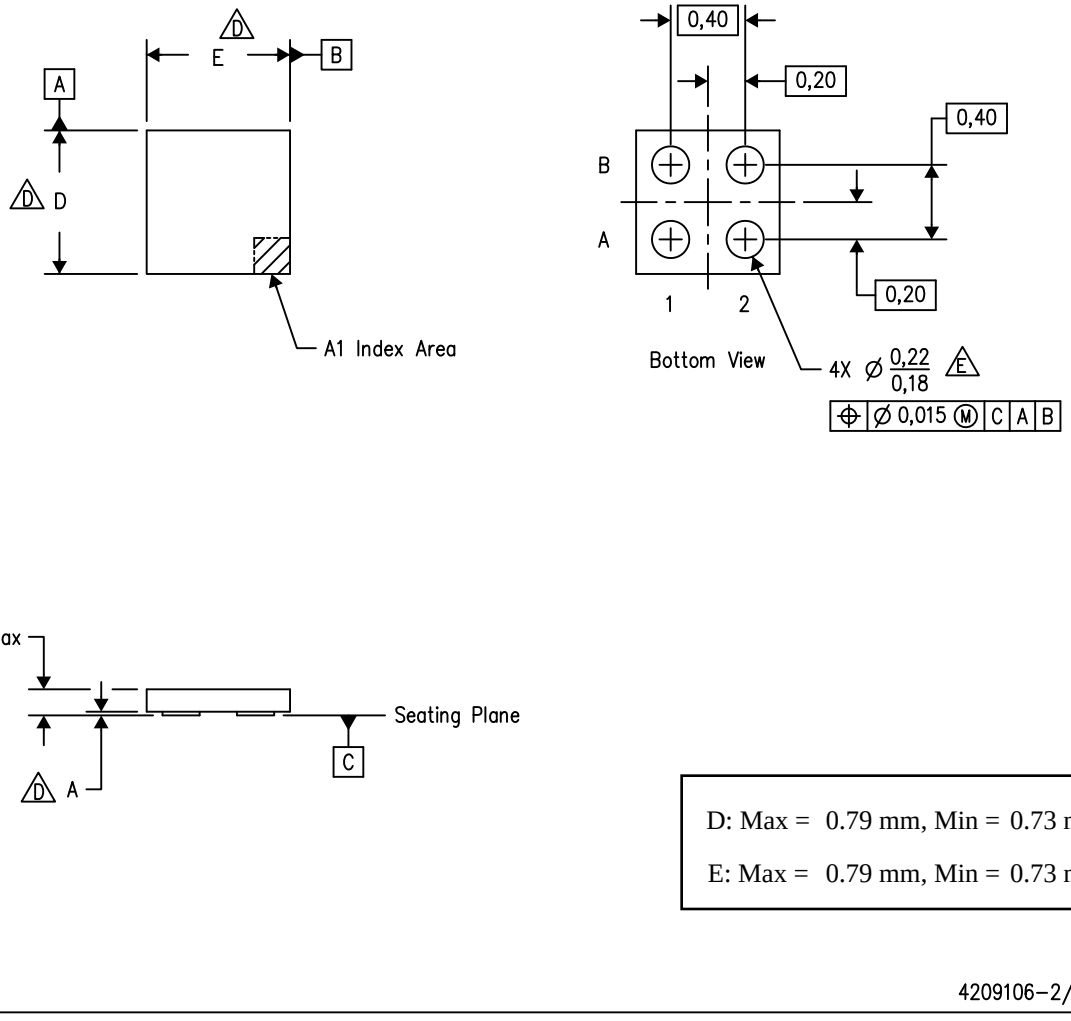

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

YFM (S–pSTAR–N4) PicoStar™




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. PicoStar™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package is a Pb–free solder land design.

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