TPD12S521 Single-Chip HDMI Transmitter Port Protection and Interface Device

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV Contact Discharge on External Lines
- Single-Chip ESD Solution for HDMI Driver
- On-Chip Current Regulator with 55-mA Current Output
- Supports All HDMI 1.3 and HDMI 1.4*b* Data Rates (–3 dB Frequency > 3 GHz)
- 0.8-pF Capacitance for the High Speed TMDS Lines
- 0.05-pF Matching Capacitance Between the Differential Signal Pair
- 38-Pin TSSOP Provides Seamless Layout Option with HDMI Connector
- Backdrive Protection
  - TMDS_D[2:0]+/–
  - TMDS_CK+/–
  - CE_REMOTE_OUT
  - DDC_DAT_OUT
  - DDC_CLK_OUT
  - HOTPLUG_DET_OUT
- Lead-Free Package

2 Applications

- PCs
- Consumer Electronics
- Set-Top Boxes
- DVD Players

3 Description

The TPD12S521 is a single-chip electro-static discharge (ESD) circuit protection device for the high-definition multimedia interface (HDMI) transmitter port. While providing ESD protection with transient voltage suppression (TVS) diodes, the TVS protection adds little or no additional glitch in the high-speed differential signals. The high-speed transition minimized differential signaling (TMDS) ESD protection lines add only 0.8-pF capacitance.

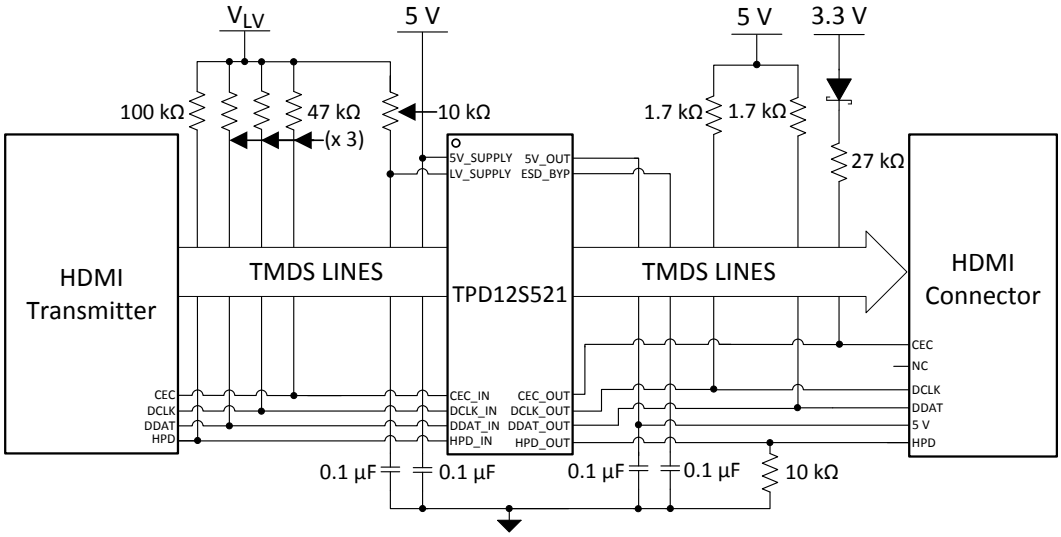
The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line TVS diodes add 3.5-pF capacitance to the control lines. The 38-pin DBT package offers a seamless layout routing option to eliminate the routing glitch for the differential signal pairs. The DBT package pitch (0.5 mm) matches with the HDMI connector pitch. In addition, the pin mapping follows the same order as the HDMI connector pin mapping. The TPD12S521 provides an on-chip current limiting switch with output ratings of 55 mA at pin 38. This enables HDMI receiver detection even when the receiver device is powered off.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD12S521	TSSOP (38)	6.40 mm × 9.70 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Circuit Protection Scheme



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- Add text to Typical Application ... 1

Changes from Revision D (September 2014) to Revision E — **Page**

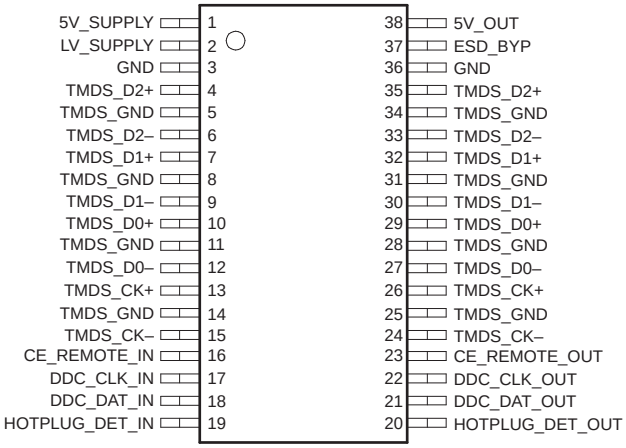
- Added clarification to HDMI data rates. ... 1
- Added clarification to HDMI data rates. ... 8

Changes from Revision C (January 2013) to Revision D — **Page**

- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

6 Pin Configuration and Functions

DBT PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	ESD	DESCRIPTION
NAME	NO.			
5V_SUPPLY	1	PWR	2 kV(1)	Current source for 5V_OUT.
LV_SUPPLY	2			Bias for CE/DDC/HOTPLUG level shifters.
GND, TMDS_GND	3, 5, 8, 11,14, 25, 28, 31, 34, 36	GND	NA	TMDS ESD and parasitic GND return.
TMDS_D2+	4, 35	ESD clamp	8 kV(2)	TMDS 0.8-pF ESD protection.(3)
TMDS_D2–	6, 33			
TMDS_D1+	7, 32			
TMDS_D1–	9, 30			
TMDS_D0+	10, 29			
TMDS_D0–	12, 27			
TMDS_CK+	13, 26			
TMDS_CK–	15, 24			
CE_REMOTE_IN	16	IO	2 kV(1)	LV_SUPPLY referenced logic level into ASIC.
DDC_CLK_IN	17			
DDC_DAT_IN	18			
HOTPLUG_DET_IN	19			
HOTPLUG_DET_OUT	20	IO, ESD clamp	8 kV(2)	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD(4) to connector.
DDC_DAT_OUT	21			5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector.
DDC_CLK_OUT	22			
CE_REMOTE_OUT	23	IO, ESD clamp	8 kV(2)	3.3-V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector.
ESD_BYP	37	ESD Bypass	2 kV(1)	ESD bypass. This pin must be connected to a 0.1-µF ceramic capacitor.
5V_OUT	38	PWR	2 kV(1)	5-V regulator output

(1) Human-Body Model (HBM) per MIL-STD-833, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conitions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connnected to GND.
(2) Standard IEC 61000-4-2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connected to GND.
(3) These two pins must be connected together inline on the PCB.
(4) This output can be connected to an external 0.1-µF ceramic capacitor, resulting in an increased ESD withstand voltage rating.

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{5V_SUPPLY} V_{LV_SUPPLY}	Supply voltage	–0.3	6	V
$V_{I/O}$	DC voltage at any channel input	–0.5	6	V
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ(1)	Pins 1, 2, 16–19, 37, 38	±2000	V
		IEC 61000-4-2 Contact Discharge(2)	Pins 4, 7, 10, 13, 20–24, 27, 30, 33	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
T_A	Operating free-air temperature	–40		85	°C
5V_SUPPLY	Operating supply voltage		5	5.5	V
LV_SUPPLY	Bias supply voltage	1	3.3	5.5	V

7.4 Thermal Information

THERMAL METRIC(1)		TPD12S521 DBT 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.7	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	44.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC5}	Operating supply current	5V_SUPPLY = 5 V				110	130	µA
I_{CC3}	Bias supply current	LV_SUPPLY = 3.3 V				1	5	µA
V_{DROP}	5V_OUT overcurrent output drop	5V_SUPPLY = 5 V, I_{OUT} = 55 mA				150	200	mV
I_{SC}	5V_OUT short-circuit current limit	5V_SUPPLY= 5 V, 5V_OUT = GND			90	135	175	mA
I_{OFF}	OFF-state leakage current, level-shifting NFET	LV_SUPPLY = 0 V				0.1	5	µA
$I_{BACK\ DRIVE}$	Current conducted from output pins to V_SUPPLY rails when powered down	5V_SUPPLY < V_{CH_OUT}	TMDS_D[2:0]+/–, TMDS_CK+/–, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT			0.1	5	µA
V_{ON}	Voltage drop across level-shifting NFET when ON	LV_SUPPLY = 2.5 V, V_S = GND, I_{DS} = 3 mA			75	95	140	mV
V_F	Diode forward voltage	I_F = 8 mA, T_A = 25°C(1)	Top diode			0.85		V
			Bottom diode			0.85		
V_{CL}	Channel clamp voltage at ±8 kV HBM ESD	TA = 25°C(1)(2)	Positive transients			9		V
			Negative transients			-9		
R_{DYN}	Dynamic resistance	I = 1 A, T_A = 25°C(3)	Positive transients			3		Ω
			Negative transients			1.5		
I_{LEAK}	TMDS channel leakage current	T_A = 25°C(1)				0.01	1	µA
C_{IN}, TMDS	TMDS channel input capacitance	5V_SUPPLY= 5 V, Measured at 1 MHz, V_{BIAS} = 2.5 V(1)				0.8	1.0	pF
ΔC_{IN}, TMDS	TMDS channel input capacitance matching	5V_SUPPLY= 5 V, Measured at 1 MHz, V_{BIAS} = 2.5 V(1)(4)				0.05		pF
C_{MUTUAL}	Mutual capacitance between signal pin and adjacent signal pin	5V_SUPPLY= 0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V(1)				0.07		pF
C_{IN}	Level-shifting input capacitance, capacitance to GND	5V_SUPPLY= 0 V, Measured at 100 KHz, V_{BIAS} = 2.5 V(1)		DDC		3.5	4	pF
				CEC		3.5	4	
				HP		3.5	4	

(1) This parameter is specified by design and verified by device characterization
(2) Human-Body Model (HBM) per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ
(3) These measurements performed with no external capacitor on ESD_BYP.
(4) Intrapair matching, each TMDS pair (i.e., D+, D–)

7.6 Typical Characteristics

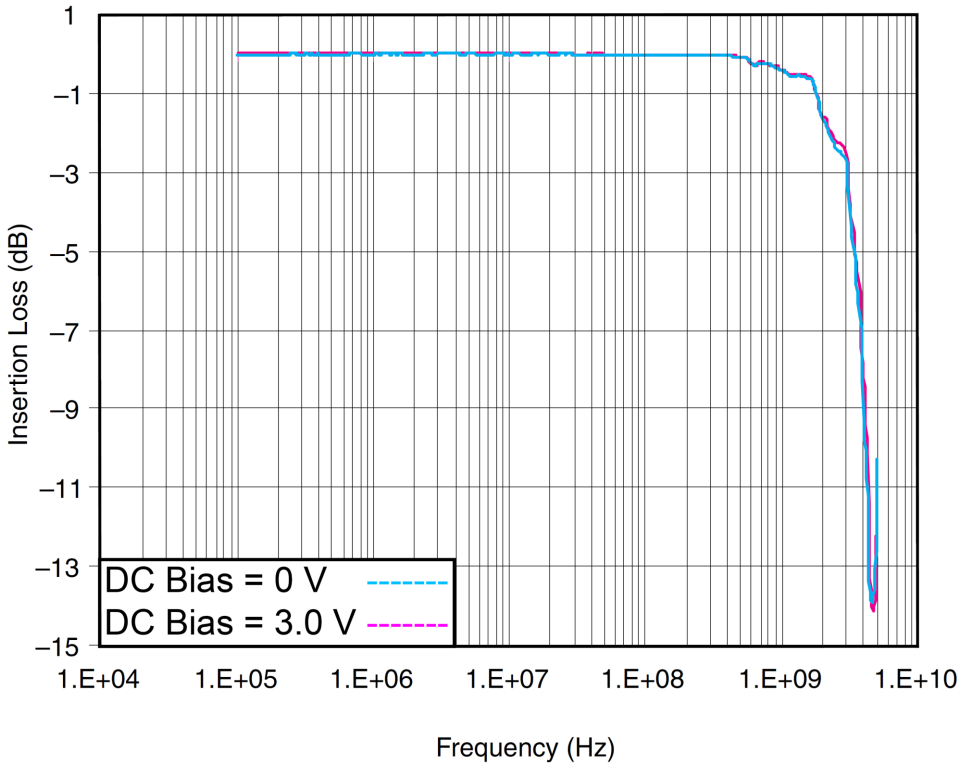


Figure 1. Insertion Loss Performance Across Frequency

8 Detailed Description

8.1 Overview

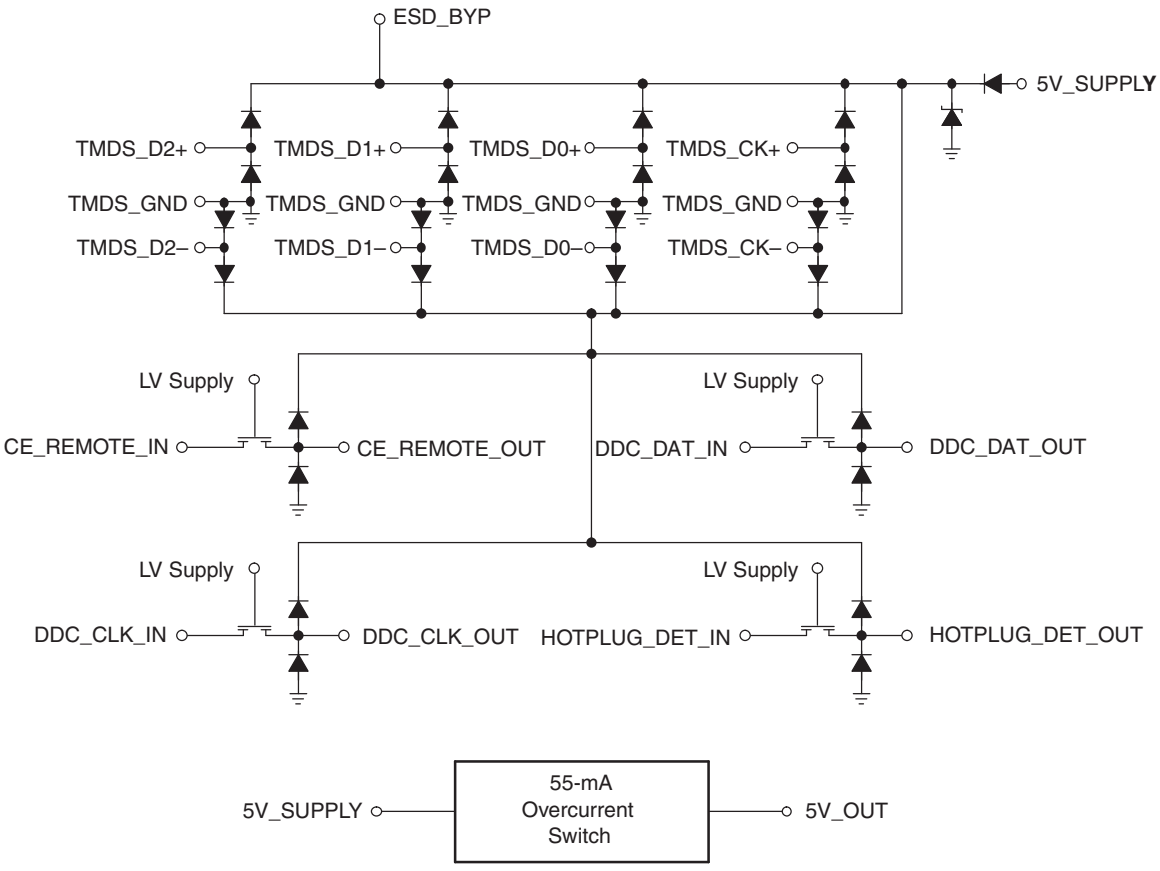
The TPD12S521 is a single-chip ESD solution for the HDMI transmitter port. In many cases the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S521 provides the desired system-level ESD protection, such as the IEC61000-4-2 (Level 4) ESD, by absorbing the energy associated with the ESD strike.

While providing the ESD protection, the TPD12S521 adds little or no additional glitch in the high-speed differential signals (see Figure 5 and Figure 6). The high-speed TMDS lines add only 0.8-pF capacitance to the lines. In addition, the monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line. This is a direct advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality.

The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line ESD clamps add 3.5-pF capacitance to the control lines. The 38-pin DBT package offers a seamless layout routing option to eliminate the routing glitch for the differential signal pairs.

The TPD12S521 provides an on-chip regulator with current output ratings of 55 mA at pin 38. This current enables HDMI receiver detection even when the receiver device is powered off. DBT package pitch (0.5 mm) matches with HDMI connector pitch. In addition, pin mapping follows the same order as the HDMI connector pin mapping.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Single-Chip ESD Solution for HDMI Driver

TPD12S521 provides a complete ESD protection scheme for an HDMI 1.4 compliant port. The monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line. This is a direct advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality. The 38-pin DBT package offers a seamless layout routing option to eliminate the routing glitch for the differential signal pair.

8.3.2 Supports All HDMI 1.3 and HDMI 1.4*b* Data Rates

The high-speed TMDS pins of the TPD12S521 add only 0.8 pF of capacitance to the TMDS lines. Excellent intra-pair capacitance matching of 0.05 pF provides ultra low intra-pair skew. Insertion loss -3 dB point > 3 GHz provides enough bandwidth to pass all HDMI 1.4*b* TMDS data rates.

8.3.3 Integrated Level Shifting for the Control Lines

The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line ESD clamps add 3.5-pF capacitance to the control lines.

8.3.4 ±8-kV Contact ESD Protection on External Lines

In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S521 provides the desired system-level ESD protection, such as the the IEC61000-4-2 (Level 4) ESD, by absorbing the energy associated with the ESD strike.

8.3.5 38-Pin TSSOP Provides Seamless Layout Option With HDMI Connector

The 38-pin DBT package offers seamless layout routing option to eliminate the routing glitch for the differential signal pair. DBT package pitch (0.5 mm) matches with HDMI connector pitch. In addition, pin mapping follows the same order as the HDMI connector pin mapping. This HDMI receiver port protection and interface device is specifically designed for next-generation HDMI transmitter protection.

8.3.6 Backdrive Protection

Backdrive protection is offered on the following pins: TMDS_D[2:0]+/–, TMDS_CK+/–, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT.

8.3.7 Lead-Free Package

Lead-Free Package for RoHS Compliance.

8.3.8 On-Chip Current Regulator With 55-mA Current Output

The TPD12S521 provides an on-chip regulator with current output ratings of 55 mA at pin 38. This current enables HDMI receiver detection even when the receiver device is powered off.

8.4 Device Functional Modes

TPD12S521 is active with the conditions in the *Recommended Operating Conditions* met. The bi-directional voltage-level translators provide non-inverting level shifting from V_{LV} on the system side to either 5V (for SDA , SCL, HPD), or 3.3 V (for CEC) on the connector side. Each connector side pin has an ESD clamp that triggers when voltages are above V_{BR} or below the lower diode's V_f. During ESD events, voltages as high as ±8-kV (contact ESD) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below these trigger levels (usually within 10's of nano-seconds), these pins revert to a non-conductive state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TPD12S521 provides IEC61000-4-2 Level 4 Contact ESD rating to the HDMI 1.4 transmitter port. Integrated voltage-level shifting reduces the board space needed to implement the control lines.

9.2 Typical Application

Refer to Figure 2 for a typical schematic for an HDMI 1.4 transmitter port protected with TPD12S521. The eight TMDS data lines (D2+/-, D1+/-, D0+/-, CLK+/-) each have two pins on TPD12S521 to connect to. The TMDS data lines flow through their respective pin pairs, attaching to the passive ESD protection circuitry. To block reverse current to the 3.3-V logic power rail, connect CEC_OUT to the 3.3-V logic level with a 27-kΩ pull-up resistor in series with a Schottky diode.

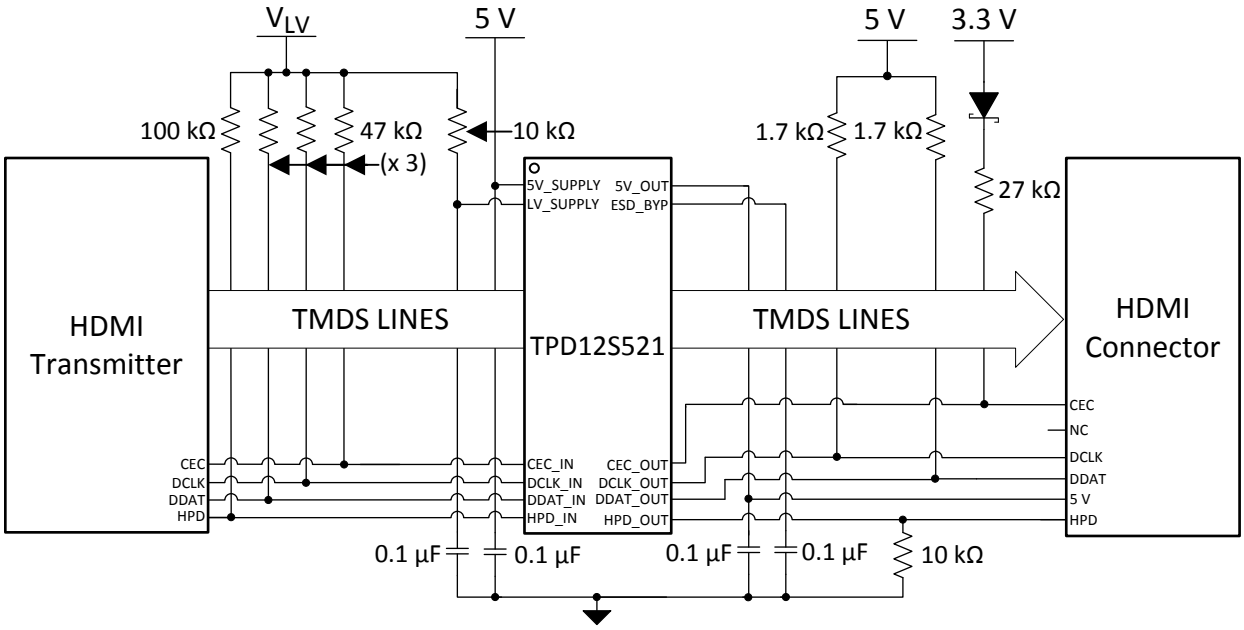


Figure 2. TPD12S521 Configured With an HDMI 1.4 Transmitter Port

9.2.1 Design Requirements

For this example, use the following table as input parameters:

Design Parameters	Example Value
Voltage on 5V_SUPPLY	4.5 V - 5.5 V
Voltage on LV_SUPPLY	1.7 V - 1.9 V

9.2.2 Detailed Design Procedure

To begin the design process the designer needs to know the 5V_SUPPLY voltage range and the logic level, LV_SUPPLY, voltage range.

9.2.3 Application Curves

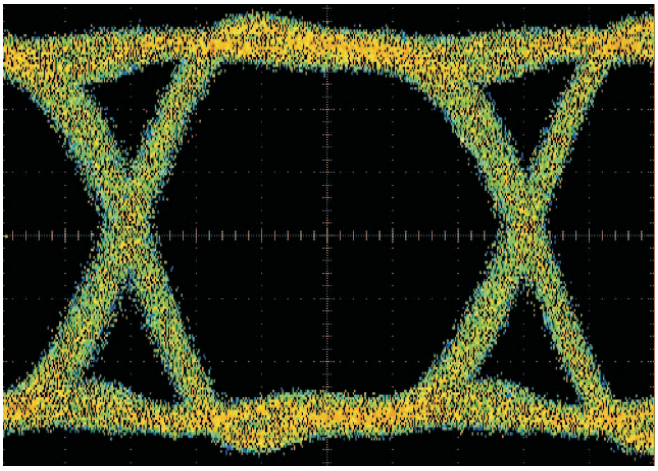


Figure 3. HDMI 1.65Gbps Eye Diagram With TPD12S521 on a Test Board

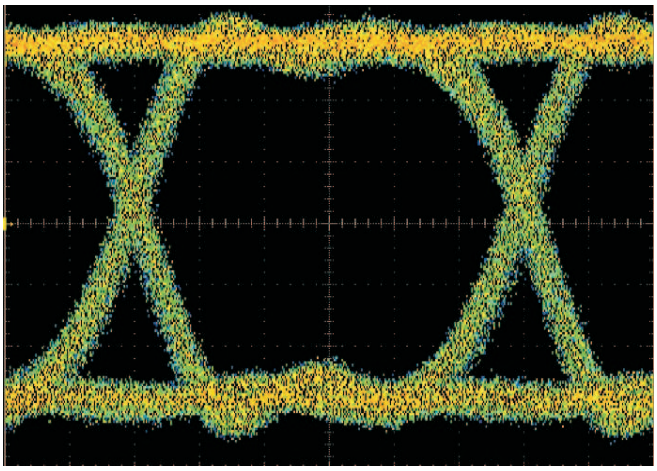


Figure 4. HDMI 1.65Gbps Eye Diagram Without TPD12S521 on a Test Board

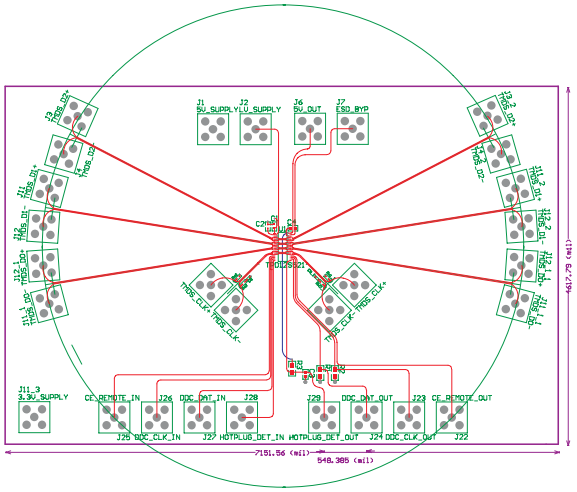


Figure 5. Test Board to Measure Eye Diagram for the TPD12S521 (Refer to Eye Diagram Plot)

10 Power Supply Recommendations

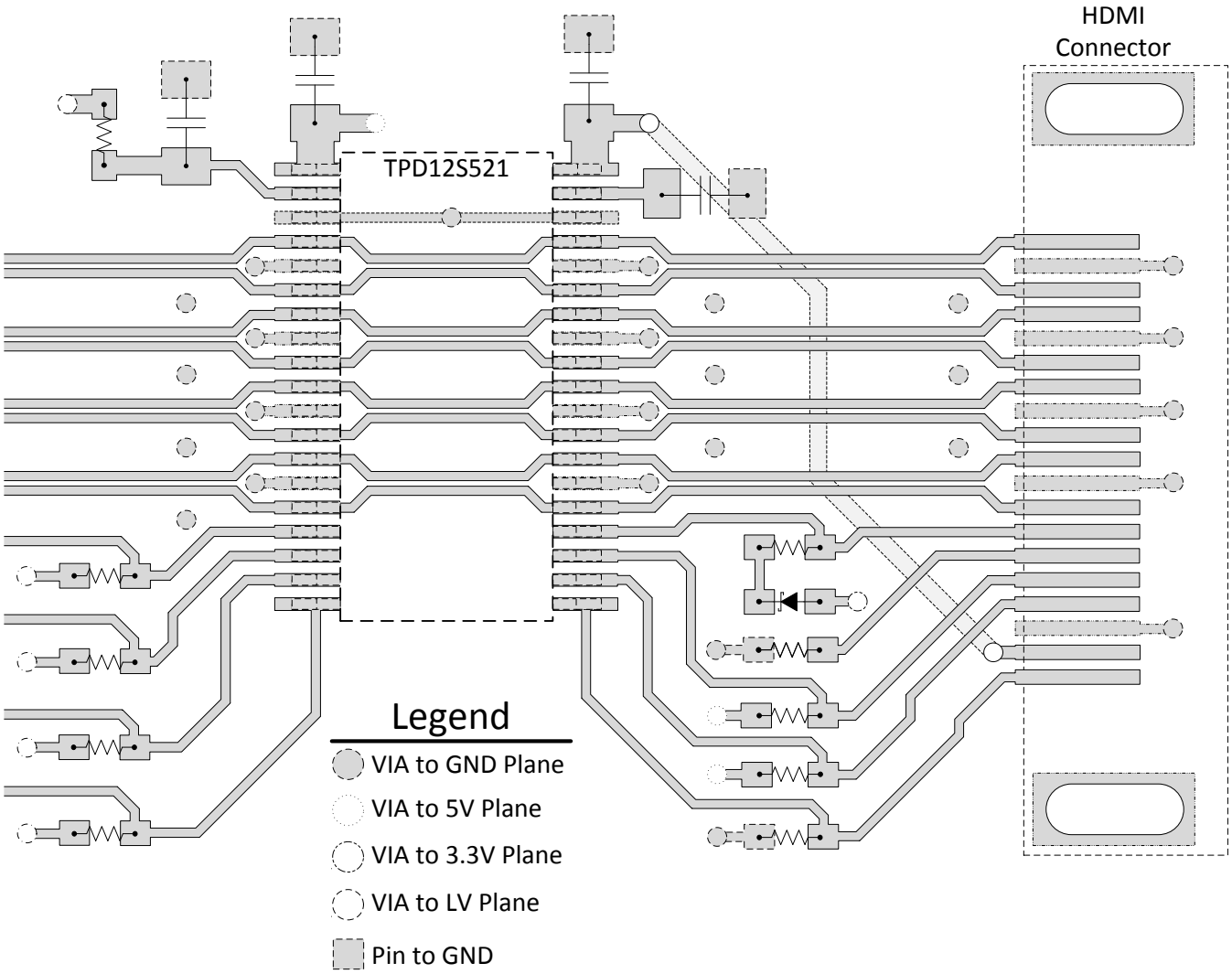
The designer needs to consider the requirement for the HDMI Transmitters Hot Plug Detect (HPD) scheme. If it is a requirement, then the V_{IH} of HPD on the core scalar chip is the minimum voltage needed to detect a Hot Plug event. The minimum voltage requirement is $V_{5V\_SUPPLY} — V_{DROP\_MAX} — V_{DROP\_SYSTEM} — V_{ON\_MAX} > V_{IH} \Rightarrow V_{5V\_SUPPLY} > V_{IH} + V_{DROP\_MAX} + V_{DROP\_SYSTEM} + V_{ON\_MAX}$; where V_{DROP_MAX} is the maximum voltage drop across TPD12S521's current limiter, V_{DROP_SYSTEM} is the voltage drop across the path from Pin 38 of TPD12S521 through the sink and back to Pin 20, and V_{ON_MAX} is the maximum voltage drop across TPD12S521's level shifting NFET when ON. Otherwise, TPD12S521 is a passive ESD protection device and there is no need to power it.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example



Use external and internal ground planes and stitch them together with VIAs as close to the GND pins of TPD12S521 as possible. This allows for a low impedance path to ground so that the device can properly dissipate an ESD event.

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD12S521DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PN521	Samples
TPD12S521DBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PN521	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

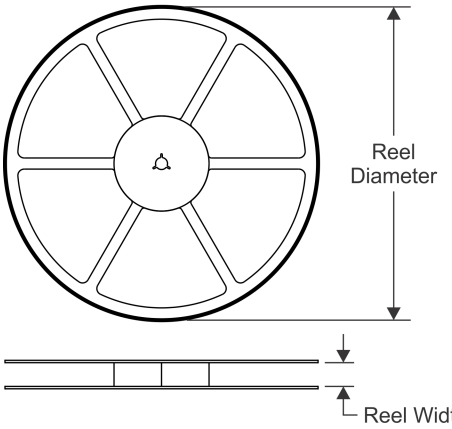
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

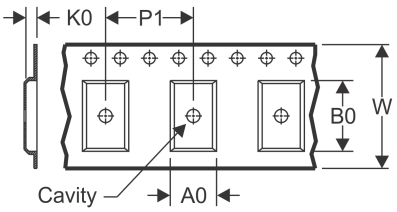
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

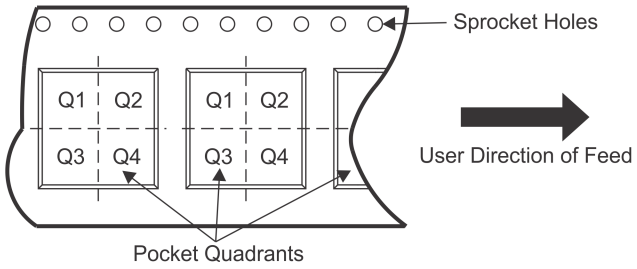


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

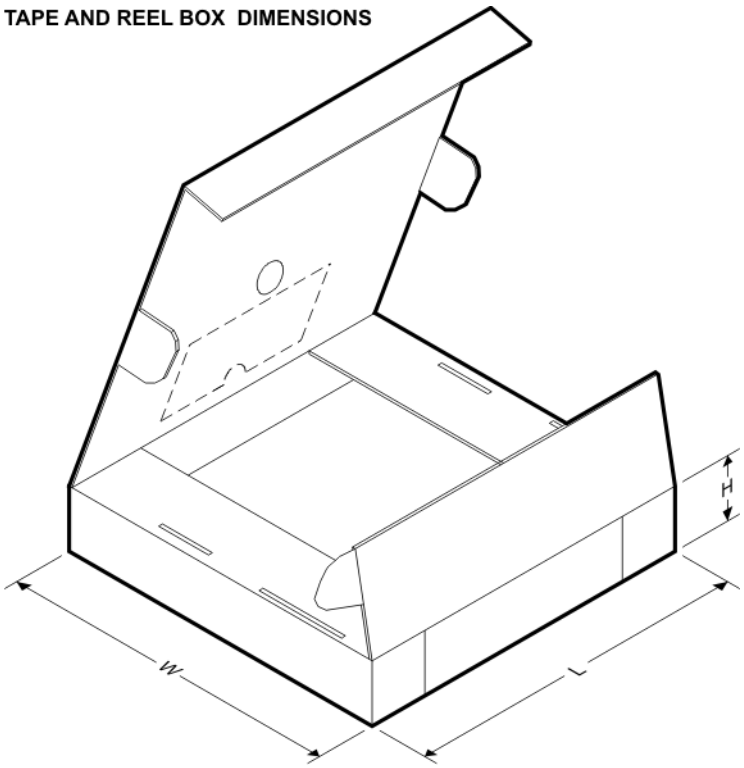
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD12S521DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

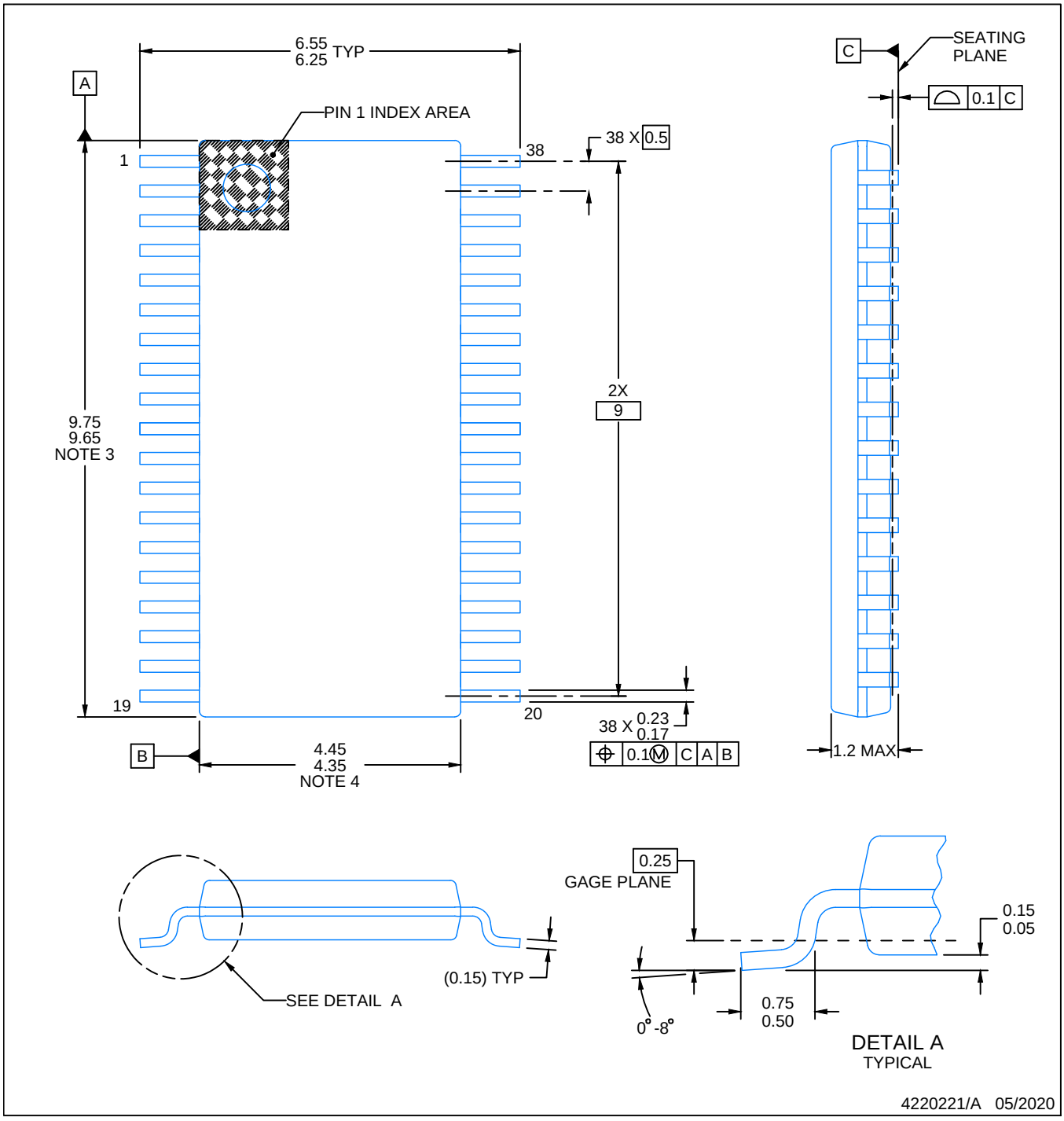
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD12S521DBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DBT0038A

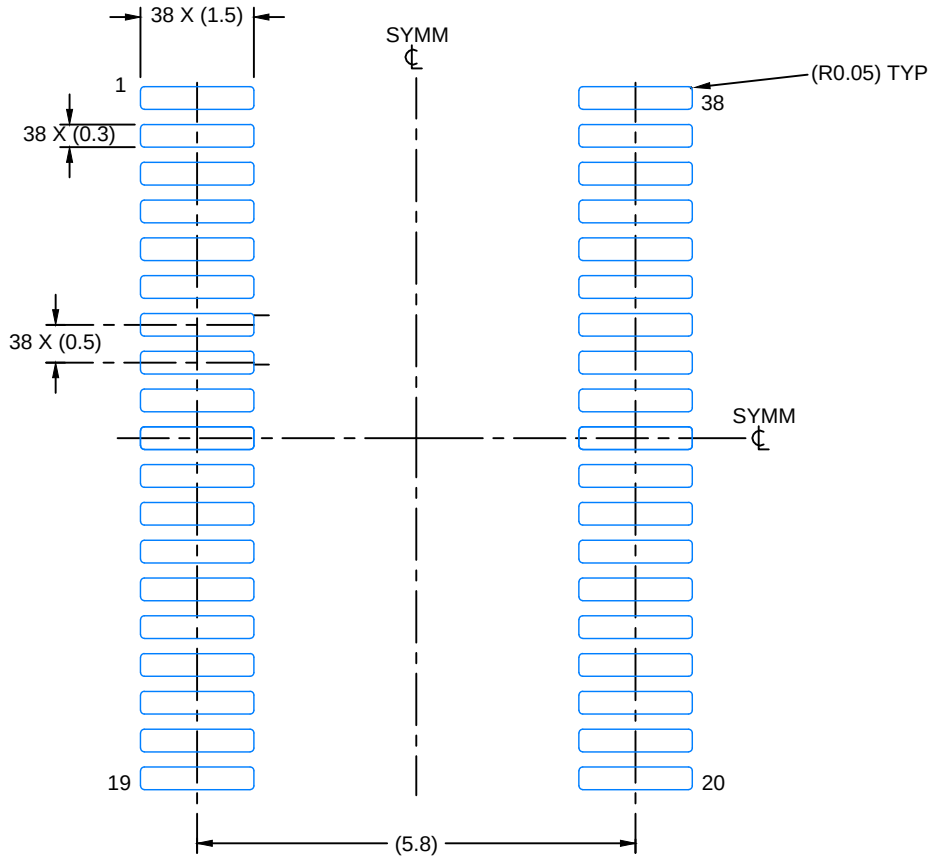
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

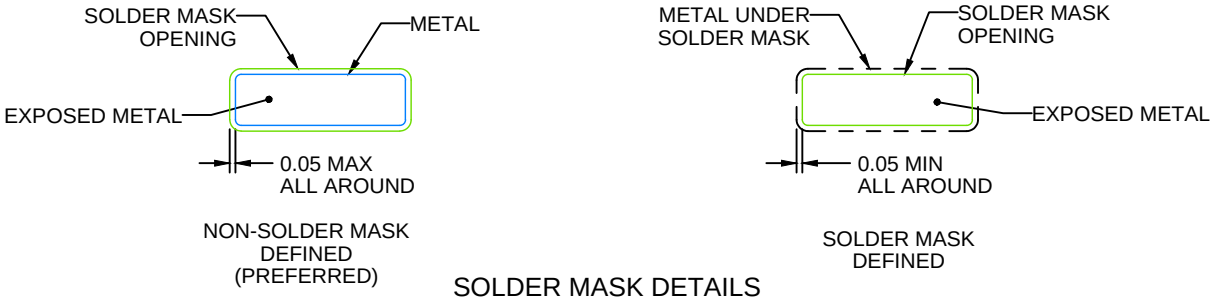


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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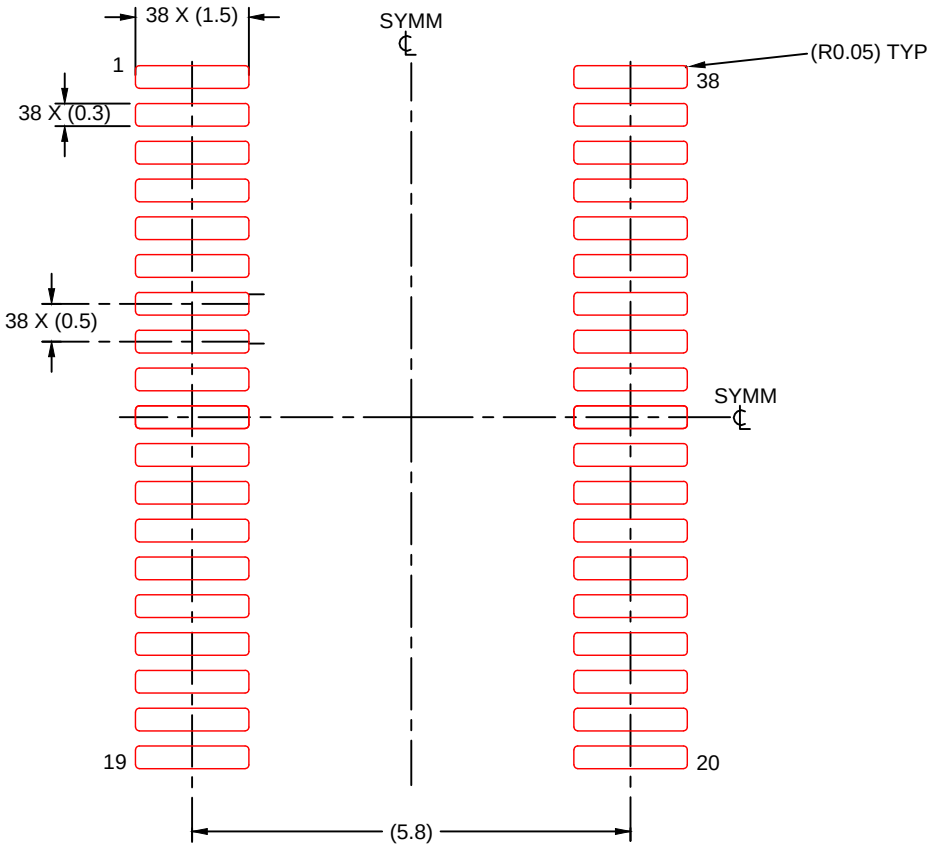
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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