N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-243AA*	DIE
250V	3.5Ω	1.5A	TN2425N8	TN2425ND

Product marking for TO-243AA:

TN4C✻

where ✻ = 2-week alpha date code

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

Features

- ❑ Low threshold
- ❑ High input impedance
- ❑ Low input capacitance
- ❑ Fast switching speeds
- ❑ Low on resistance
- ❑ Free from secondary breakdown
- ❑ Low input and output leakage
- ❑ Complementary N- and P-channel devices

Low Threshold DMOS Technology

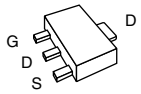
These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ❑ Logic level interfaces – ideal for TTL and CMOS
- ❑ Solid state relays
- ❑ Photo voltaic drives
- ❑ Analog switches
- ❑ General purpose line drivers
- ❑ Telecom switches

Package Option



TO-243AA
(SOT-89)

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

11/12/01

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Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_A = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	480mA	1.9A	1.6W†	15	78†	480mA	1.9A

* I_D (continuous) is limited by max rated T_j.

† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

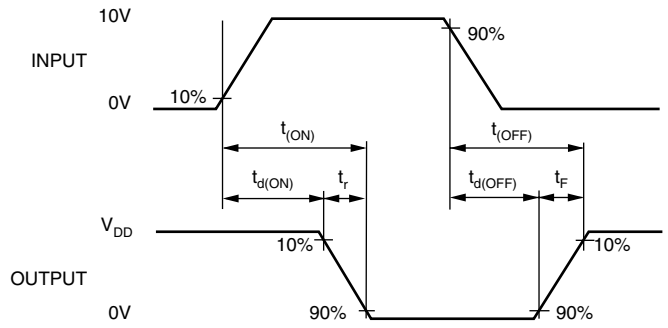
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250			V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	0.8			V	V_{GS} = V_{DS}, I_D= 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-5.5	mV/°C	V_{GS} = V_{DS}, I_D= 1.0mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ± 20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{GS} = 0V, V_{DS} = Max Rating
				1.0	mA	V_{GS} = 0V, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	0.8			A	V_{GS} = 4.5V, V_{DS} = 25V
		1.5				V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			6.0	Ω	V_{GS} = 3.0V, I_D = 150mA
				5.0		V_{GS} = 4.5V, I_D = 250mA
				3.5		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.7	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance	500			m℧	V_{DS} = 25V, I_D = 250mA
C_{ISS}	Input Capacitance		105	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common Source Output Capacitance		25	100		
C_{RSS}	Reverse Transfer Capacitance		7	40		
$t_{d(ON)}$	Turn-ON Delay Time		5	15	ns	V_{DD} = 25V, I_D = 500mA, R_{GEN} = 25Ω
t_r	Rise Time		10	25		
$t_{d(OFF)}$	Turn-OFF Delay Time		25	35		
t_f	Fall Time		5	15		
V_{SD}	Diode Forward Voltage Drop			1.5	V	V_{GS} = 0V, I_{SD} = 500mA
t_{rr}	Reverse Recovery Time		300		ns	V_{GS} = 0V, I_{SD} = 500mA

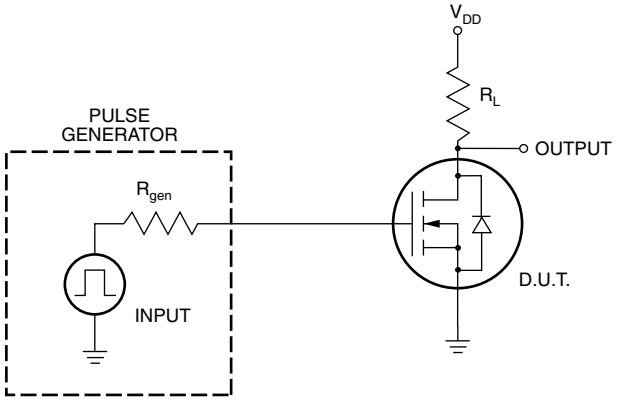
Notes:

1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

2.All A.C. parameters sample tested.

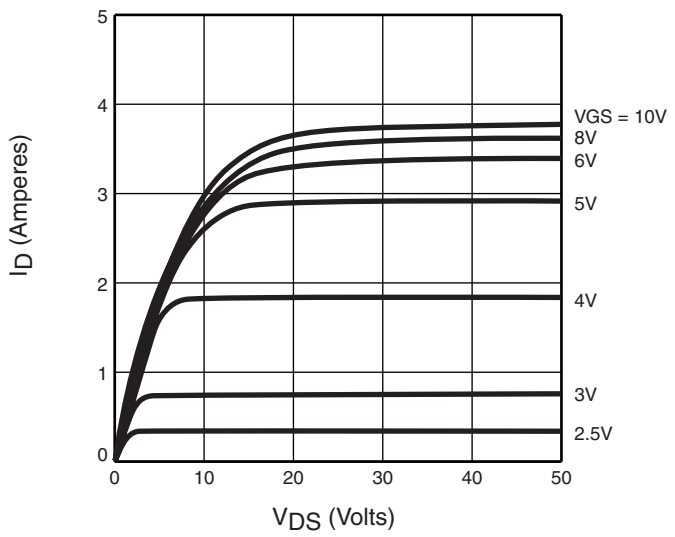
Switching Waveforms and Test Circuit



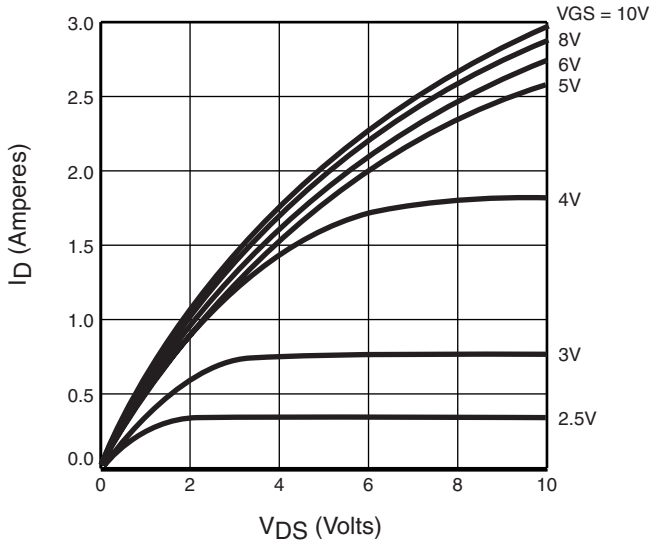


Typical Performance Curves

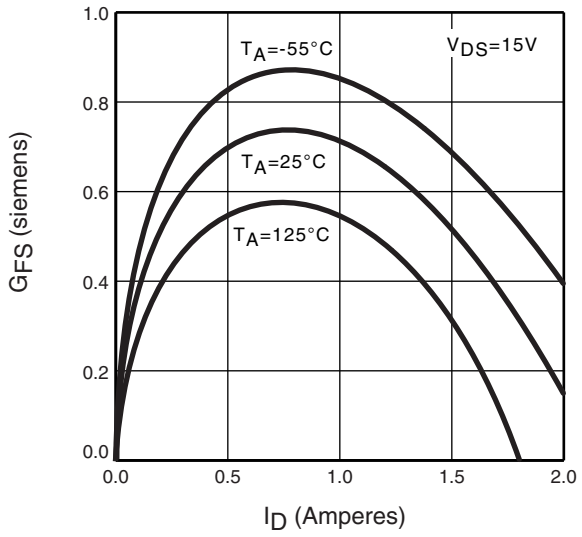
Output Characteristics



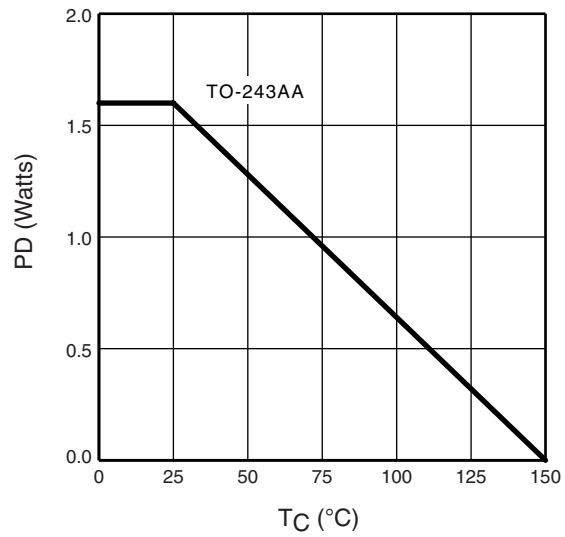
Saturation Characteristics



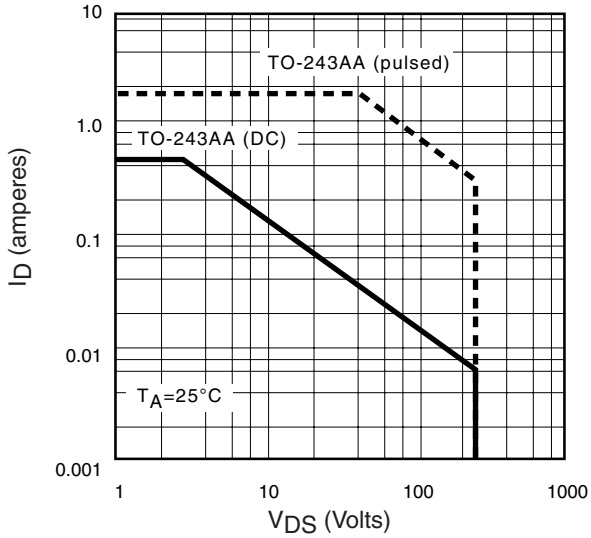
Transconductance vs. Drain Current



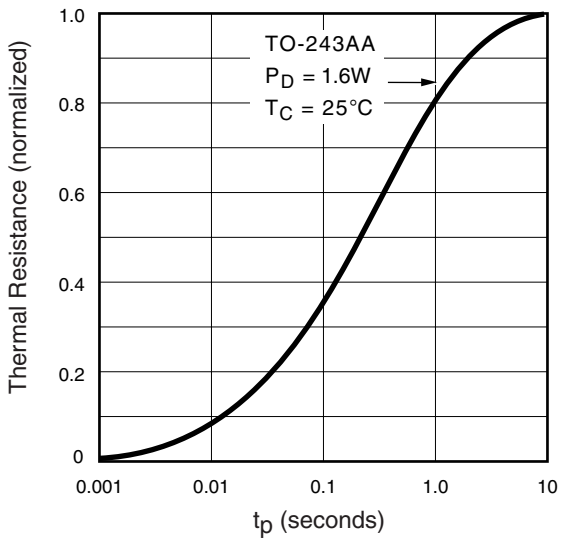
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

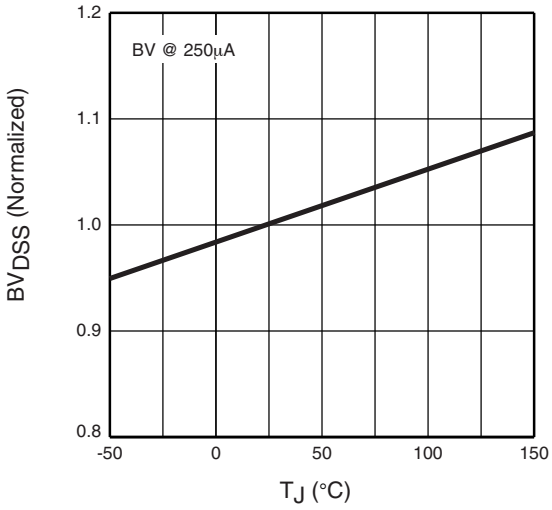


Thermal Response Characteristics

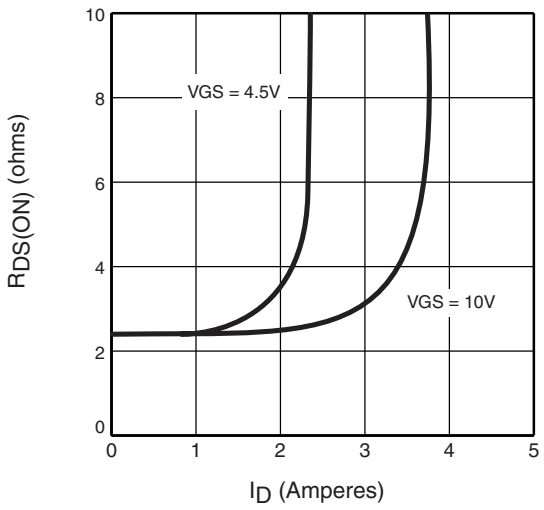


Typical Performance Curves

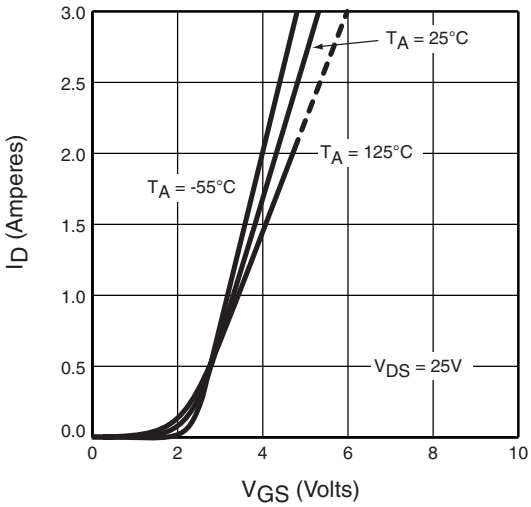
BV_{DSS} Variation with Temperature



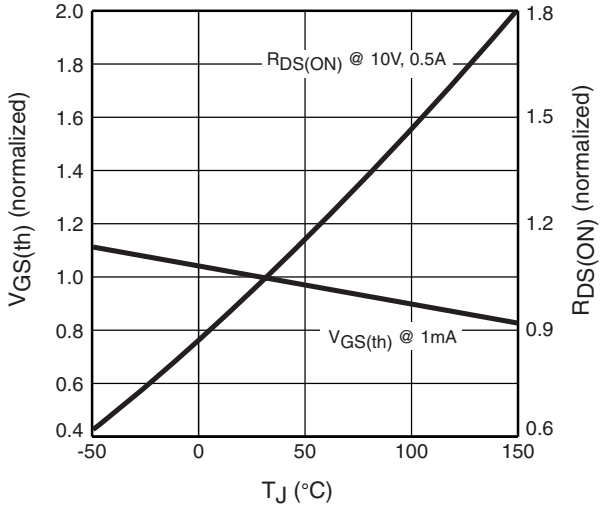
On Resistance vs. Drain Current



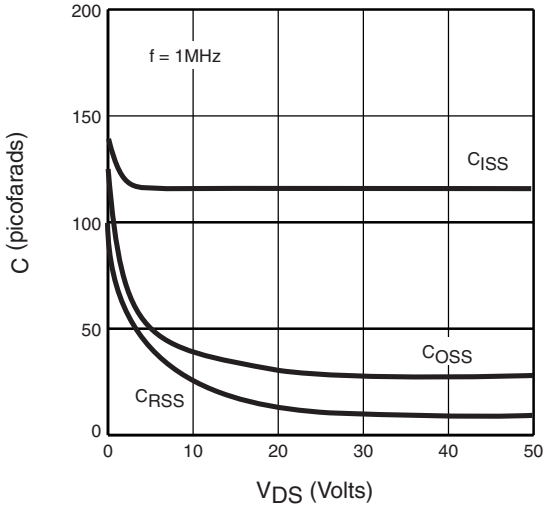
Transfer Characteristics



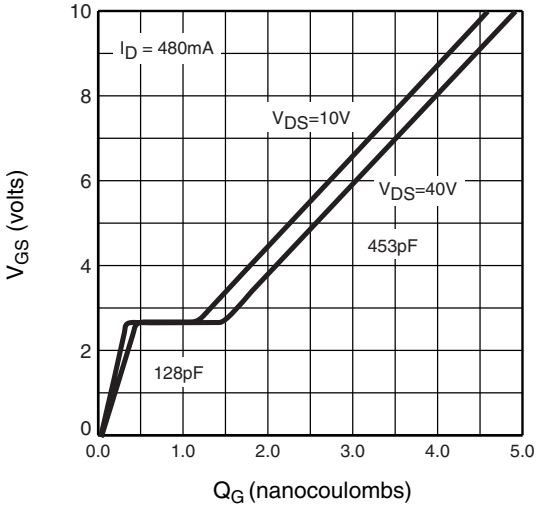
$V_{GS(TH)}$ and $R_{DS(ON)}$ w/ Temperature



Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics



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