TMS570LS0914 16- and 32-Bit RISC Flash Microcontroller

1 Device Overview

1.1 Features

- High-Performance Automotive-Grade Microcontroller (MCU) for Safety-Critical Applications
  - Dual CPUs Running in Lockstep
  - ECC on Flash and RAM Interfaces
  - Built-In Self-Test (BIST) for CPU and On-chip RAMs
  - Error Signaling Module With Error Pin
  - Voltage and Clock Monitoring
- ARM® Cortex®-R4F 32-Bit RISC CPU
  - 1.66 DMIPS/MHz With 8-Stage Pipeline
  - FPU With Single and Double Precision
  - 12-Region Memory Protection Unit (MPU)
  - Open Architecture With Third-Party Support
- Operating Conditions
  - Up to 160-MHz System Clock
  - Core Supply Voltage (VCC): 1.14 to 1.32 V
  - I/O Supply Voltage (VCCIO): 3.0 to 3.6 V
- Integrated Memory
  - 1MB of Flash With ECC
  - 128KB of RAM With ECC
  - 64KB of Flash for Emulated EEPROM With ECC
- Common Platform Architecture
  - Consistent Memory Map Across Family
  - Real-Time Interrupt Timer (RTI) OS Timer
  - 128-Channel Vectored Interrupt Module (VIM)
  - 2-Channel Cyclic Redundancy Checker (CRC)
- Direct Memory Access (DMA) Controller
  - 16 Channels and 32 Peripheral Requests
  - Parity for Control Packet RAM
  - DMA Accesses Protected by Dedicated MPU
- Frequency-Modulated Phase-Locked Loop (FMPLL) With Built-In Slip Detector
- IEEE 1149.1 JTAG, Boundary Scan and ARM CoreSight™ Components
- Advanced JTAG Security Module (AJSM)
- Up to 101 General-Purpose I/O (GIO) Pins
  - Up to 16 GIO Pins With Interrupt Generation Capability
- Enhanced Timing Peripherals
  - 7 Enhanced Pulse Width Modulators (ePWM) Modules
  - 6 Enhanced Capture (eCAP) Modules
  - 2 Enhanced Quadrature Encoder Pulse (eQEP) Modules
- Two Next Generation High-End Timer (N2HET) Modules
  - N2HET1: 32 Programmable Channels
  - N2HET2: 18 Programmable Channels
  - 160-Word Instruction RAM With Parity Protection Each
  - Each N2HET Includes Hardware Angle Generator
  - Dedicated High-End Timer Transfer Unit (HTU) for Each N2HET
- Two 12-Bit Multibuffered ADC Modules
  - ADC1: 24 Channels
  - ADC2: 16 Channels
  - 16 Shared Channels
  - 64 Result Buffers With Parity Protection Each
- Multiple Communication Interfaces
  - Three CAN Controllers (DCANs)
    - 64 Mailboxes With Parity Protection Each
    - Compliant to CAN Protocol Version 2.0A and 2.0B
  - Inter-Integrated Circuit (I^2C)
  - Three Multibuffered Serial Peripheral Interfaces (MibSPIs)
    - 128 Words With Parity Protection Each
    - 8 Transfer Groups
  - Up to Two Standard Serial Peripheral Interface (SPI) Modules
  - Two UART (SCI) Interfaces, One With Local Interconnect Network (LIN 2.1) Interface Support
- Packages
  - 144-Pin Quad Flatpack (PGE) [Green]
  - 100-Pin Quad Flatpack (PZ) [Green] (TMX Only)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.2 Applications

- Electric Power Steering (EPS)
- Braking Systems (ABS and ESC)
- HEV and EV Inverter Systems
- Battery-Management Systems
- Active Driver Assistance Systems
- Aerospace and Avionics
- Railway Communications
- Off-road Vehicles

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1.3 Description

The TMS570LS0914 device is part of the Hercules TMS570 series of high-performance automotive-grade ARM® Cortex®-R-based MCUs. Comprehensive documentation, tools, and software are available to assist in the development of ISO 26262 and IEC 61508 functional safety applications. Start evaluating today with the Hercules TMS570 LaunchPad Development Kit. The TMS570LS0914 device has on-chip diagnostic features including: dual CPUs in lockstep; CPU and memory Built-In Self-Test (BIST) logic; ECC on both the flash and the SRAM; parity on peripheral memories; and loopback capability on most peripheral I/Os.

The TMS570LS0914 device integrates the ARM Cortex-R4F floating-point CPU which offers an efficient 1.66 DMIPS/MHz, and has configurations which can run up to 160 MHz providing up to 265 DMIPS. The TMS570 device supports the word invariant big-endian [BE32] format.

The TMS570LS0914 device has 1MB of integrated flash and 128KB of RAM configurations with single-bit error correction and double-bit error detection. The flash memory on this device is nonvolatile, electrically erasable and programmable, and is implemented with a 64-bit-wide data bus interface. The flash operates on a 3.3-V supply input (same level as the I/O supply) for all read, program, and erase operations. The SRAM supports single-cycle read and write accesses in byte, halfword, word, and doubleword modes throughout the supported frequency range.

The TMS570LS0914 device features peripherals for real-time control-based applications, including two Next-Generation High-End Timer (N2HET) timing coprocessors with up to 44 total I/O terminals, seven Enhanced PWM (ePWM) modules with up to 14 outputs, six Enhanced Capture (eCAP) modules, two Enhanced Quadrature Encoder Pulse (eQEP) modules, and two 12-bit Analog-to-Digital Converters (ADCs) supporting up to 24 inputs.

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse-width-modulated outputs, capture or compare inputs, or general-purpose I/O (GIO). The N2HET is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. A High-End Timer Transfer Unit (HTU) can transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HTU.

The ePWM module can generate complex pulse width waveforms with minimal CPU overhead or intervention. The ePWM is easy to use and supports complementary PWMs and deadband generation. With integrated trip zone protection and synchronization with the on-chip MibADC, the ePWM is ideal for digital motor control applications.

The eCAP module is essential in systems where the accurately timed capture of external events is important. The eCAP can also be used to monitor the ePWM outputs or to generate simple PWM when not needed for capture applications.

The eQEP module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine as used in high-performance motion and position-control systems.

The device has two 12-bit-resolution MibADCs with 24 total inputs and 64 words of parity-protected buffer RAM each. The MibADC channels can be converted individually or can be grouped by software for sequential conversion sequences. Sixteen inputs are shared between the two MibADCs. There are three separate groups. Each group can be converted once when triggered or configured for continuous conversion mode. The MibADC has a 10-bit mode for use when compatibility with older devices or faster conversion time is desired.

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The device has multiple communication interfaces: three MibSPIs; two SPIs; two SCIs, one of which can be used as LIN; three DCANs; and one I^2C module. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The LIN supports the Local Interconnect standard 2.0 and can be used as a UART in full-duplex mode using the standard Non-Return-to-Zero (NRZ) format. The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 Mbps. The DCAN is ideal for applications operating in noisy and harsh environments (for example, automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

The I2C module is a multimaster communication module providing an interface between the microcontroller and an I^2C-compatible device through the I^2C serial bus. The I2C module supports speeds of 100 and 400 kbps.

A Frequency-Modulated Phase-Locked Loop (FMPLL) clock module is used to multiply the external frequency reference to a higher frequency for internal use. The FMPLL provides one of the six possible clock source inputs to the Global Clock Module (GCM). The GCM manages the mapping between the available clock sources and the device clock domains.

The device also has an external clock prescaler (ECP) circuit that when enabled, outputs a continuous external clock on the ECLK terminal. The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency. This low-frequency output can be monitored externally as an indicator of the device operating frequency.

The Direct Memory Access (DMA) controller has 16 channels, 32 peripheral requests,
and parity protection on its memory. An MPU is built into the DMA to protect memory against erroneous transfers.

The Error Signaling Module (ESM) monitors device errors and determines whether an interrupt or external error signal (nERROR) is asserted when a fault is detected. The nERROR terminal can be monitored externally as an indicator of a fault condition in the microcontroller.

With integrated functional safety features and a wide choice of communication and control peripherals, the TMS570LS0914 device is an ideal solution for high-performance, real-time control applications with safety-critical requirements.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TMS570LS0914PGE	LQFP (144)	20.0 mm × 20.0 mm
TMS570LS0914PZ	LQFP (100)	14.0 mm × 14.0 mm

(1) For more information, see Section 10, *Mechanical Packaging and Orderable Information*.

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1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

NOTE: The block diagram reflects the 144PGE package. Some functions are multiplexed or not available in other packages. For details, see the respective terminal functions table in Section 4.2, *Terminal Functions*.

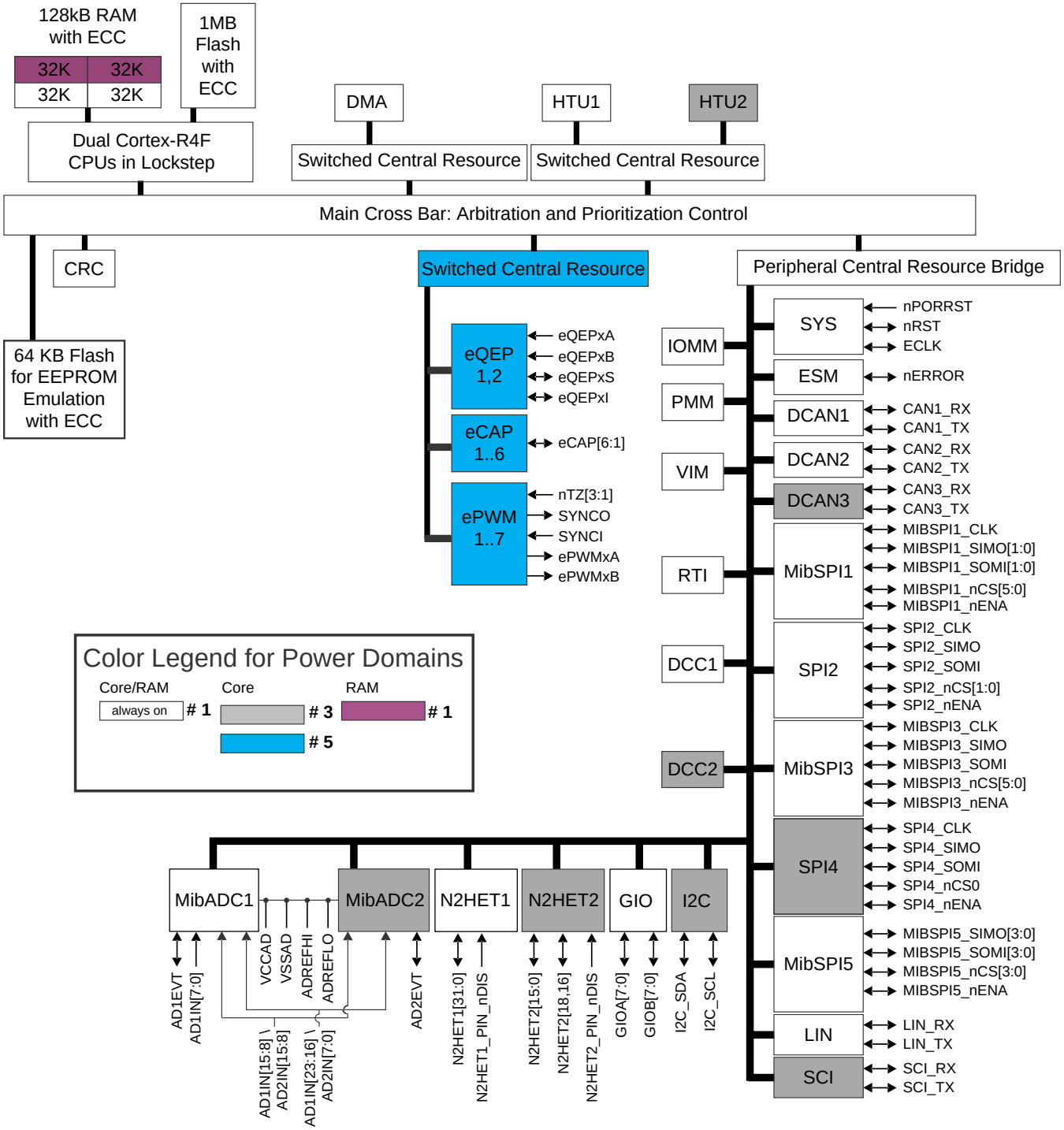


Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the SPNS225B device-specific data manual to make it an SPNS225C revision.

Scope: Applicable updates to the TMS570LS09114 device family, specifically relating to the TMS570LS0914 devices (Silicon Revision A), which are now in the production data (PD) stage of development have been incorporated.

Changes from November 13, 2014 to September 15, 2015 (from B Revision (November 2014) to C Revision) **Page**

- Section 1.1 (Features): Updated/Changed the N2HET feature 1
- Section 1.1: Removed ZWT package; no longer supported [along with ZWT performance characteristics] 1
- Section 1.3 (Description): Corrected DMA description, 32 peripheral requests, not 32 control packets 4
- Section 1.3: Updated/Changed ESM paragraph 4
- Table 3-1 (TMS570LS0914 Device Comparison): Updated/Changed the GPIO pin count for PZ package devices from "55" to "45" 9
- Section 4.2 (Signal Descriptions): Updated/Changed "Default Pull Type" to "Reset Pull Type" 12
- Table 4-2 (PGE Enhanced High-End Timer Modules (N2HET)): Updated/Changed N2HET1 time input capture or output compare pin description 14
- Table 4-2: Updated/Changed N2HET2 time input capture or output compare pin description 14
- Table 4-5 (PGE Enhanced Pulse-Width Modulator Modules (ePWM)): Updated/Changed EPWM1SYNCI 16
- Table 4-15 (PGE Test and Debug Modules Interface): Updated/Changed TEST pin description 21
- Table 4-20 (PZ Enhanced High-End Timer Modules (N2HET)): Updated/Changed N2HET1 time input capture or output compare pin description 23
- Table 4-23 (PZ Enhanced Pulse-Width Modulator Modules (ePWM)): Updated/Changed EPWM1SYNCI 24
- Table 4-32 (PZ Test and Debug Modules Interface): Updated/Changed TEST pin description 29
- Table 4-41 (Selectable 8mA/2mA Control): 36
- Section 5.1 (Absolute Maximum Ratings): Moved Storage temperature range back to Absolute Maximum Ratings table. 37
- Section 5.3 (Power-On Hours (POH)): Added associated footnotes 37
- Updated/Changed Section 5.5, Input/Output Electrical Characteristics - changed UNIT for Input Current (I/O pins) ***from*** mA ***to*** µA 39
- Section 5.6 (Power Consumption Over Recommended Operating Conditions): Updated/Changed I_{CC} TYP and MAX values 40
- Section 5.7 (Thermal Resistance Characteristics): Added new section 41
- Table 5-1 (Thermal Resistance Characteristics (PGE Package)): Added $R\Theta_{JA}$ test conditions and added Ψ_{JT} 41
- Table 5-2 (Thermal Resistance Characteristics (PZ Package)): Added $R\Theta_{JA}$ test conditions and added Ψ_{JT} 41
- Section 5.8.1.2 (Wait States Required): Updated/Changed "The TCM flash can support ..." paragraph 43
- Section 6.1 (Device Power Domains): Updated/Changed the core power domains count to "5" 44
- Section 6.1: Deleted "The logic in the modules ..." NOTE, no longer applicable 44
- Table 6-1 (Voltage Monitoring Specifications): Updated/Changed the V_{MON}, VCC low MAX from "1.0" to "1.13" V 44
- Table 6-4 (Electrical Requirements for nPORRST): Updated/Changed $t_{f(nPORRST)}$ MIN from "500" to "475" ns 46
- Table 6-6 (nRST Timing Requirements): Updated/Changed $t_{v(RST)}$ number of cycles from " **2252**$t_{c(OSC)}$" to "**2256**$t_{c(OSC)}$" 47
- Table 6-6: Updated/Changed $t_{f(nRST)}$ MIN from "500" to "475" ns 47
- Section 6.5.1 Added Quantity of Breakpoints and Watchpoints 48
- Table 6-10 (LPO Specifications): Updated/Changed LPO - HF oscillator, untrimmed frequency TYP value from "9.6" to "9" MHz 53
- Table 6-10: Added LPO - HF oscillator, trimmed frequency MIN/TYP/MAX values 53
- Table 6-19 (Glitch Filter Timing Specifications): Updated/Changed nRST, nPORRST, and TEST MIN values from "500" to "475" ns 60
- Table 6-23 (Timing Requirements for Program Flash): Added footnote to $t_{erase(bank0)}$, Sector/Bank erase time 68
- Table 6-25 (PBIST RAM Grouping): Added table notes identifying address ranges of ESRAM PBIST groups 71
- Table 6-25: Added missing values for PBIST_ROM and STC_ROM 71
- Table 6-32 (Reset/Abort/Error Sources): Added POWER DOMAIN CONTROL rows 85
- Section 6.20.3 (JTAG Identification Code): Added Table 6-34, JTAG ID Code 88

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- Table 6-36 (JTAG Scan Interface Timing): Updated/Changed NO. 2, tsu(TDI/TMS - RTCKr) MIN from "21" to "26" ns 90
- Table 6-36: Updated/Changed NO. 5, td(TCKf -TDO) MAX from "10" to "12" ns 90
- Table 7-2 (Switching Characteristics for Output Timings versus Load Capacitance (C_L)): Corrected the rise/fall times of the 8/2 mA buffers in 8 mA mode 94
- Figure 7-3 (ePWMx Module Interconnections): Added footnote A, ePWMx Input Synchronziation Selection detail reference 96
- Figure 7-4 (ePWMx Input Synchronization Selection Detail): Added paragraph and new figure 96
- Table 7-6 (Connection to ePWMx Modules for Device-Level Trip Zone Inputs): Add "filter width is 6 VCLK4 cycles" footnote 99
- Table 7-8 (ePWMx Timing Requirements): Added "filter width is 6 VCLK4 cycles" footnote 101
- Table 7-10 (ePWMx Trip-Zone Timing Requirements): Updated/Change $t_{w(TZ)}$ Asynchronous MIN value 101
- Table 7-10: Add "filter width is 6 VCLK4 cycles" footnote 101
- Figure 7-3 (eCAPx Module Interconnections): Added footnote A, eCAPx Input Synchronziation Selection detail reference 102
- Figure 7-7 (eCAPx Input Synchronization Selection Detail): Added paragraph and new figure 102
- Table 7-12 (Device-Level Input Connection to eCAPx Modules): Add "filter width is 6 VCLK4 cycles" footnote 103
- Table 7-13 (eCAPx Timing Requirements): Add "filter width is 6 VCLK4 cycles" footnote 104
- Figure 7-8 (eQEP Module Interconnections): Added footnote A, eQEPx Input Synchronziation Selection detail 105
- Figure 7-9 (eQEPx Input Synchronization Selection Detail): Added paragraph and new figure 105
- Table 7-16 (Device-Level Input Connection to eQEPx Modules): Add "filter width is 6 VCLK4 cycles" footnote 106
- Table 7-17 (eQEPx Timing Requirements): Added "filter width is 6 VCLK4 cycles" footnote 106
- Section 7.5.2.1 (MibADC1 Event Trigger Hookup): NOTE: Updated/Changed "ePWM_S2" to "ePWM_A2" 109
- Table 7-21 (MibADC2 Event Trigger Hookup): Updated/Changed "AD1EVT" to "AD2EVT" for Option A and Option B of EVSRC 000 110
- Section 7.5.2.2 (MibADC2 Event Trigger Hookup): NOTE: Updated/Changed "ePWM_S2" to "ePWM_A2" 110
- Table 7-23 (MibADC Recommended Operating Conditions): Added associated footnotes to V_{CCAD} MAX, V_{SSAD} MIN, and I_{AIC} 113
- Table 7-24 (MibADC Electrical Characteristics): Updated/Changed the V_{CCAD} = 5.5 V maximum test condition 113
- Table 7-26 (MibADC Operating Characteristics): Updated/Changed the MAX value of the Conversion Range (CR) to "5.25" V 115
- Table 7-26: Updated/Changed "(See Figure 76)" text to crossreference Figure 7-12, Differential Nonlinearity (DNL) Error 115
- Section 7.12.1 Corrected size of SPI baud rate generator, 11 bit, not 8 bit 130
- Section 7.12.4 (MibSPI/SPI Master Mode I/O Timing Specifications): Updated/Changed MibSPI timings 134
- Section 7.12.5 (SPI Slave Mode I/O Timings): Updated/Changed MibSPI timings 138
- Section 8 (Applications, Implementation, and Layout): Added new section 142
- Section 9.1 (Development Support): Added new subsection 143
- Figure 9-1 (TMS570LS0914 Device Numbering Conventions): Updated/Changed Die Revision 143
- Section 9.7.1 (Device Identification Code Register): Added device identification code register value for silicon "Rev A" 146
- Section 9.8 (Module Certifications): Added missing subsections numbering. 147
- Section 10.1 (Packaging Information): Updated/Changed paragraph 152

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3 Device Comparison

Table 3-1 lists the features of the TMS57LS0914 devices.

Table 3-1. TMS570LS0914 Device Comparison

FEATURES	TMS570LS DEVICES					
Generic Part Number	**3137ZWT**(1)	**1227ZWT**(1)	**1224PGE**(1)	0914PGE	0914PZ(2)	0432PZ
Package	337 BGA	337 BGA	144 QFP	144 QFP	100 QFP	100 QFP
CPU	ARM Cortex-R4F	ARM Cortex-R4F	ARM Cortex-R4F	ARM Cortex-R4F	ARM Cortex-R4F	ARM Cortex-R4
Frequency (MHz)	180	180	160	160	100	80
Flash (KB)	3072	1280	1280	1024	1024	384
RAM (KB)	256	192	192	128	128	32
Data Flash [EEPROM] (KB)	64	64	64	64	64	16
EMAC	10/100	10/100	–	–	–	–
FlexRay	2-ch	2-ch	–	–	–	–
CAN	3	3	3	3	2	2
MibADC 12-bit (Ch)	2 x (24ch)	2 x (24ch)	2 x (24ch)	2 x (24ch)	2 x (16ch)	1 x (16ch)
N2HET (Ch)	2 (44)	2 (44)	2 (40)	2 (40)	2 (21)	1 (19)
ePWM Channels	–	14	14	14	8	–
eCAP Channels	–	6	6	6	4	0
eQEP Channels	–	2	2	2	1	2
MibSPI (CS)	3 (6 + 6 + 4)	3 (6 + 6 + 4)	3 (5 + 6 + 1)	3 (5 + 6 + 1)	2 (5 + 1)	1 (4)
SPI (CS)	2 (2 + 1)	2 (2 + 1)	1 (1)	1 (1)	1 (1)	2
SCI (LIN)	2 (1 with LIN)	2 (1 with LIN)	2 (1 with LIN)	2 (1 with LIN)	1 (with LIN)	1 (with LIN)
I2C	1	1	1	1	–	–
GPIO (INT)	120 (with 16 interrupt capable)	101 (with 16 interrupt capable)	64 (with 10 interrupt capable)	64 (with 10 interrupt capable)	45 (with 9 interrupt capable)	45 (with 8 interrupt capable)
EMIF	16-bit data	16-bit data	–	–	–	–
ETM (Trace)	32-bit	N/A	–	–	–	–
RTP/DMM	YES	N/A	–	–	–	–
Operating Temperature	-40ºC to 125ºC	-40ºC to 125ºC	-40ºC to 125ºC	-40ºC to 125ºC	-40ºC to 125ºC	-40ºC to 125ºC
Core Supply (V)	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V	1.14 V – 1.32 V
I/O Supply (V)	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V	3.0 V – 3.6 V

(1) Bolding denotes a superset device. For additional device variants, see www.ti.com/tms570
(2) PZ package only available as TMX samples.

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4 Terminal Configuration and Functions

4.1 Pin Diagrams

4.1.1 PGE QFP Package Pinout (144-Pin)

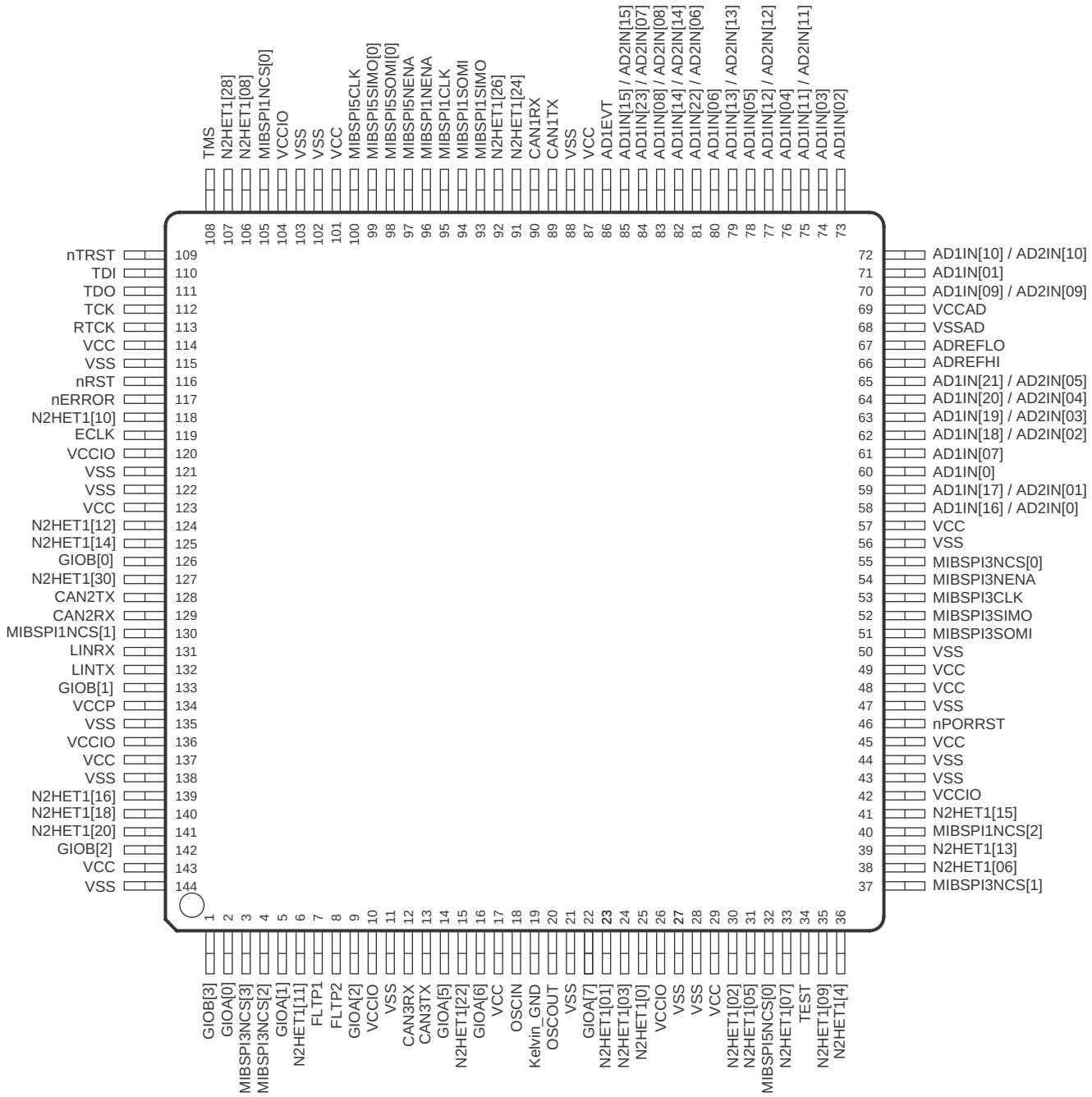


Figure 4-1. PGE QFP Package Pinout (144-Pin)

Note: Pins can have multiplexed functions. Only the default function is shown in Figure 4-1.

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4.1.2 PZ QFP Package Pinout (100-Pin)

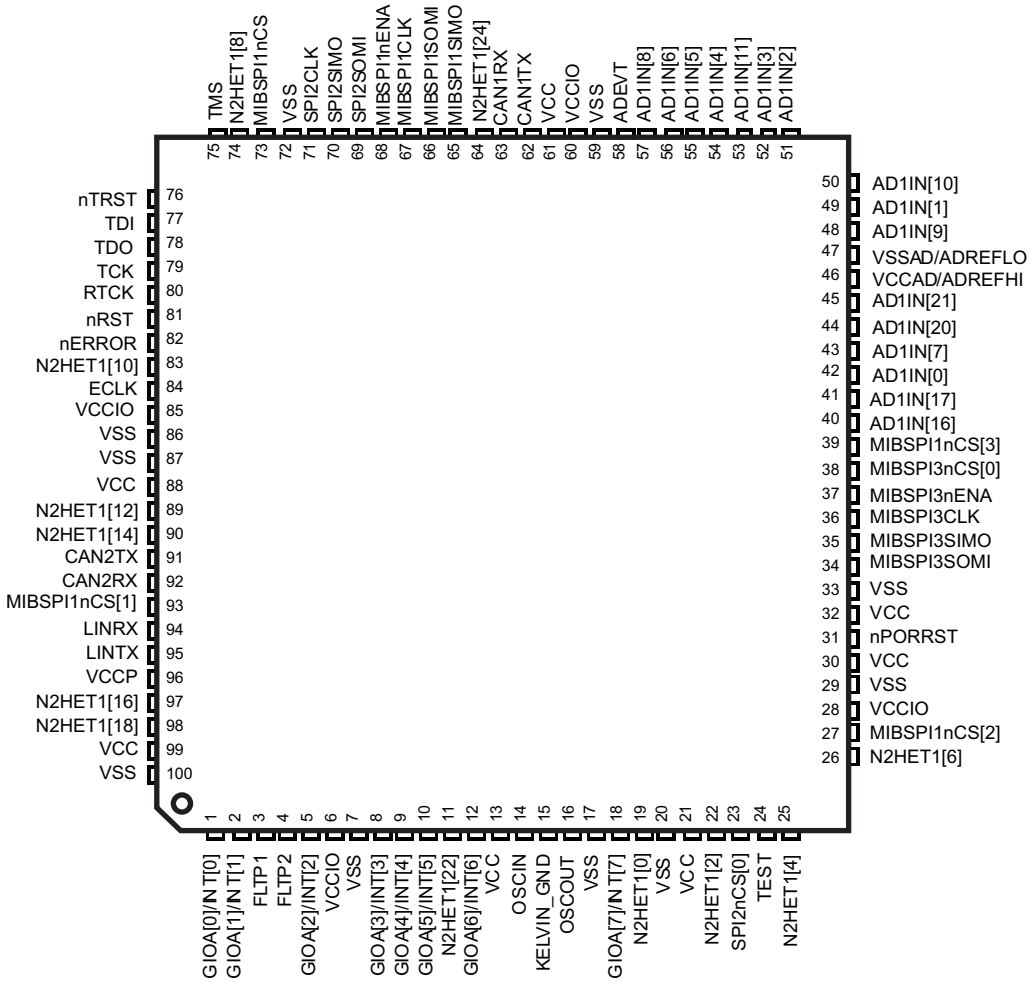


Figure 4-2. PZ QFP Package Pinout (100-Pin)

4.2 Signal Descriptions

The signal descriptions section shows pin information in module function order per package.

Section 4.2.1 and Section 4.2.2 identify the external signal names, the associated pin or ball numbers along with the mechanical package designator, the pin or ball type (Input, Output, I/O, Power, or Ground), whether the pin or ball has any internal pullup/pulldown, whether the pin or ball can be configured as a GIO, and a functional pin or ball description. The first signal name listed is the primary function for that terminal (pin or ball). The signal name in **Bold** is the function being described. For information on how to select between different multiplexed functions, see Section 4.3, *Pin Multiplexing*, of this document or see the I/O Multiplexing Module (IOMM) User Guide.

NOTE

All I/O signals except nRST are configured as inputs while nPORRST is low and immediately after nPORRST goes high.

All output-only signals are configured as high impedance while nPORRST is low, and are configured as outputs immediately after nPORRST goes high.

While nPORRST is low, the input buffers are disabled, and the output buffers are high impedance.

In the Terminal Functions tables of Section 4.2.1 and Section 4.2.2, the RESET PULL STATE is the state of the pullup or pulldown while nPORRST is low and immediately after nPORRST goes high. The default pull direction may change when software configures the pin for an alternate function. The PULL TYPE is the type of pull asserted when the signal name in bold is enabled for the given terminal.

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4.2.1 PGE Package Terminal Functions

4.2.1.1 Multibuffered Analog-to-Digital Converters (MibADC)

Table 4-1. PGE Multibuffered Analog-to-Digital Converters (MibADC1, MibADC2)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
ADREFHI(1)	66	Power	–	None	ADC high reference supply
ADREFLO(1)	67	Power			ADC low reference supply
VCCAD(1)	69	Power			Operating supply for ADC
VSSAD(1)	68	Ground			
AD1EVT	86	I/O	Pulldown	Programmable, 20 µA	ADC1 event trigger input, or GIO
MIBSPI3NCS[0]/**AD2EVT**/GIOB[2]/ EQEP1I/N2HET2_PIN_nDIS	55	I/O	Pullup	Programmable, 20 µA	ADC2 event trigger input, or GIO
AD1IN[0]	60	Input	–	None	ADC1 analog input
AD1IN[01]	71				
AD1IN[02]	73				
AD1IN[03]	74				
AD1IN[04]	76				
AD1IN[05]	78				
AD1IN[06]	80				
AD1IN[07]	61				
AD1IN[08] / AD2IN[08]	83	Input	–	None	ADC1/ADC2 shared analog inputs
AD1IN[09] / AD2IN[09]	70				
AD1IN[10] / AD2IN[10]	72				
AD1IN[11] / AD2IN[11]	75				
AD1IN[12] / AD2IN[12]	77				
AD1IN[13] / AD2IN[13]	79				
AD1IN[14] / AD2IN[14]	82				
AD1IN[15] / AD2IN[15]	85				
AD1IN[16] / AD2IN[0]	58				
AD1IN[17] / AD2IN[01]	59				
AD1IN[18] / AD2IN[02]	62				
AD1IN[19] / AD2IN[03]	63				
AD1IN[20] / AD2IN[04]	64				
AD1IN[21] / AD2IN[05]	65				
AD1IN[22] / AD2IN[06]	81				
AD1IN[23] / AD2IN[07]	84				
MIBSPI3SOMI[0]/**AWM1_EXT_ENA**/ECAP2	51	Output	Pullup	–	AWM1 external analog mux enable
MIBSPI3SIMO[0]/**AWM1_EXT_SEL[0]**/ECAP3	52	Output	Pullup	–	AWM1 external analog mux select line0
MIBSPI3CLK/**AWM1_EXT_SEL[1]**/EQEP1A	53	Output	Pullup	–	AWM1 external analog mux select line0

(1) The ADREFHI, ADREFLO, VCCAD and VSSAD connections are common for both ADC cores.

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4.2.1.2 Enhanced High-End Timer Modules (N2HET)

Table 4-2. PGE Enhanced High-End Timer Modules (N2HET)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	144 PGE				
N2HET1[0]/SPI4CLK/EPWM2B	25	I/O	Pulldown	Programmable, 20 µA	N2HET1 timer input capture or output compare, or GIO. Each terminal has a suppression filter with a programmable duration.
N2HET1[01]/SPI4NENA/N2HET2[8]/EQEP2A	23				
N2HET1[02]/SPI4SIMO[0]/EPWM3A	30				
N2HET1[03]/SPI4NCS[0]/N2HET2[10]/EQEP2B	24				
N2HET1[04]/EPWM4B	36				
N2HET1[05]/SPI4SOMI[0]/N2HET2[12]/EPWM3B	31				
N2HET1[06]/SCIRX/EPWM5A	38				
N2HET1[07]/N2HET2[14]/EPWM7B	33				
N2HET1[08]/MIBSPI1SIMO[1]/	106				
N2HET1[09]/N2HET2[16]/EPWM7A	35				
N2HET1[10]/nTZ3	118				
N2HET1[11]/MIBSPI3NCS[4]/N2HET2[18]/EPWM1SYNCO	6				
N2HET1[12]	124				
N2HET1[13]/SCITX/EPWM5B	39				
N2HET1[14]	125				
N2HET1[15]/MIBSPI1NCS[4]/ECAP1	41				
N2HET1[16]/EPWM1SYNCI/EPWM1SYNCO	139				
MIBSPI1NCS[1]/**N2HET1[17]**/EQEP1S	130		Pullup		
N2HET1[18]/EPWM6A	140		Pulldown		
MIBSPI1NCS[2]/**N2HET1[19]**	40		Pullup		
N2HET1[20]/EPWM6B	141		Pulldown		
N2HET1[22]	15				
MIBSPI1NENA/**N2HET1[23]**/ECAP4	96		Pullup		
N2HET1[24]/MIBSPI1NCS[5]	91		Pulldown		
MIBSPI3NCS[1]/**N2HET1[25]**	37		Pullup		
N2HET1[26]	92		Pulldown		
MIBSPI3NCS[2]/I2CSDA/**N2HET1[27]**/nTZ2	4		Pullup		
N2HET1[28]	107		Pulldown		
MIBSPI3NCS[3]/I2CSCL/**N2HET1[29]**/nTZ1	3		Pullup		
N2HET1[30]/EQEP2S	127		Pulldown		
MIBSPI3NENA/MIBSPI3NCS[5]/**N2HET1[31]**/EQEP1B	54		Pullup		
GIOA[5]/EXTCLKIN1/EPWM1A/**N2HET1_PIN_nDIS**	14		Pulldown		
GIOA[2]/**N2HET2[0]**/EQEP2I	9	I/O	Pulldown	Programmable, 20 µA	N2HET2 timer input capture or output compare, or GIO Each terminal has a suppression filter with a programmable duration.
GIOA[6]/**N2HET2[4]**/EPWM1B	16				
GIOA[7]/**N2HET2[6]**EPWM2A	22				
N2HET1[01]/SPI4NENA//**N2HET2[8]**	23				
N2HET1[03]/SPI4NCS[0]/**N2HET2[10]**/EQEP2B	24				
N2HET1[05]/SPI4SOMI[0]/**N2HET2[12]**/EQEP3B	31				
N2HET1[07]/**N2HET2[14]**/EPWM7B	33				
N2HET1[09]/**N2HET2[16]**	35				
N2HET1[11]/MIBSPI3NCS[4]/**N2HET2[18]**/EPWM1SYNCO	6				
MIBSPI3NCS[0]/AD2EVT/GIOB[2]/EQEP1I/**N2HET2_PIN_nDIS**	55		Pullup		

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4.2.1.3 Enhanced Capture Modules (eCAP)

Table 4-3. PGE Enhanced Capture Modules (eCAP)(1)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	144 PGE				
N2HET1[15]/MIBSPI1NCS[4]/**ECAP1**	41	I/O	Pulldown	Fixed, 20 µA	Enhanced Capture Module 1 I/O
MIBSPI3SOMI[0]/AWM1_EXT_ENA/**ECAP2**	51		Pullup		Enhanced Capture Module 2 I/O
MIBSPI3SIMO[0]/AWM1_EXT_SEL[0]/**ECAP3**	52				Enhanced Capture Module 3 I/O
MIBSPI1NENA/N2HET1[23]/**ECAP4**	96				Enhanced Capture Module 4 I/O
MIBSPI5NENA/MIBSPI5SOMI[1]/**ECAP5**	97				Enhanced Capture Module 5 I/O
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/**ECAP6**	105				Enhanced Capture Module 6 I/O

(1) These signals, when used as inputs, are double-synchronized and then optionally filtered with a 6-cycle VCLK4-based counter.

4.2.1.4 Enhanced Quadrature Encoder Pulse Modules (eQEP)

Table 4-4. PGE Enhanced Quadrature Encoder Pulse Modules (eQEP)(1)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	144 PGE				
MIBSPI3CLK/AWM1_EXT_SEL[1]/**EQEP1A**	53	Input	Pullup	Fixed, 20 µA	Enhanced QEP1 Input A
MIBSPI3NENA/MIBSPI3NCS[5]/N2HET1[31]/**EQEP1B**	54	Input			Enhanced QEP1 Input B
MIBSPI3NCS[0]/AD2EVT/GIOB[2]/**EQEP1I**/N2HET2_PIN_nDIS	55	I/O			Enhanced QEP1 Index
MIBSPI1NCS[1]/N2HET1[17]//**EQEP1S**	130	I/O			Enhanced QEP1 Strobe
N2HET1[01]/SPI4NENA/N2HET2[8]/**EQEP2A**	23	Input	Pulldown		Enhanced QEP2 Input A
N2HET1[03]/SPI4NCS[0]/N2HET2[10]/**EQEP2B**	24	Input			Enhanced QEP2 Input B
GIOA[2]/N2HET2[0]/**EQEP2I**	9	I/O			Enhanced QEP2 Index
N2HET1[30]/**EQEP2S**	127	I/O			Enhanced QEP2 Strobe

(1) These signals are double-synchronized and then optionally filtered with a 6-cycle VCLK4-based counter.

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4.2.1.5 Enhanced Pulse-Width Modulator Modules (ePWM)

Table 4-5. PGE Enhanced Pulse-Width Modulator Modules (ePWM)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	144 PGE				
GIOA[5]/EXTCLKIN1/**EPWM1A**/N2HET1_PIN_nDIS	14	Output	Pulldown	–	Enhanced PWM1 Output A
GIOA[6]/N2HET2[4]/**EPWM1B**	16				Enhanced PWM1 Output B
N2HET1[11]/MIBSPI3NCS[4]/N2HET2[18]/**EPWM1SYNCO**	6				External ePWM Sync Pulse Output
N2HET1[16]/**EPWM1SYNCI**/EPWM1SYNCO	139	Input	Pullup	Fixed, 20 µA	External ePWM Sync Pulse Output
GIOA[7]/N2HET2[6]/**EPWM2A**	22	Output	Pulldown	–	Enhanced PWM2 Output A
N2HET1[0]/SPI4CLK/**EPWM2B**	25				Enhanced PWM2 Output B
N2HET1[02]/SPI4SIMO[0]/**EPWM3A**	30				Enhanced PWM3 Output A
N2HET1[05]/SPI4SOMI[0]/N2HET2[12]/**EPWM3B**	31				Enhanced PWM3 Output B
MIBSPI5NCS[0]/**EPWM4A**	32	Output	Pullup	–	Enhanced PWM4 Output A
N2HET1[04]/**EPWM4B**	36	Output	Pulldown	–	Enhanced PWM4 Output B
N2HET1[06]/SCIRX/**EPWM5A**	38				Enhanced PWM5 Output A
N2HET1[13]/SCITX/**EPWM5B**	39				Enhanced PWM5 Output B
N2HET1[18]/**EPWM6A**	140				Enhanced PWM6 Output A
N2HET1[20]/**EPWM6B**	141				Enhanced PWM6 Output B
N2HET1[09]/N2HET2[16]/**EPWM7A**	35				Enhanced PWM7 Output A
N2HET1[07]/N2HET2[14]/**EPWM7B**	33				Enhanced PWM7 Output B
MIBSPI3NCS[3]/I2CSCL/N2HET1[29]/**nTZ1**	3	Input	Pullup	Fixed, 20 µA	Trip Zone Inputs 1, 2 and 3. These signals are either connected asynchronously to the ePWMx trip zone inputs, or double-synchronized with VCLK4, or double-synchronized and then filtered with a 6-cycle VCLK4-based counter before connecting to the ePWMx trip zone inputs.
MIBSPI3NCS[2]/I2CSDA/N2HET1[27]/**nTZ2**	4				
N2HET1[10]/**nTZ3**	118		Pulldown		

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4.2.1.6 General-Purpose Input / Output (GIO)

Table 4-6. PGE General-Purpose Input / Output (GIO)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
GIOA[0]	2	I/O	Pulldown	Programmable, 20 µA	General-purpose I/O. All GIO terminals are capable of generating interrupts to the CPU on rising / falling / both edges.
GIOA[1]	5				
GIOA[2]/N2HET2[0]/EQEPII	9				
GIOA[5]/EXTCLKIN1/EPWM1A/N2HET1_PIN_nDIS	14				
GIOA[6]/N2HET2[4]/EPWM1B	16				
GIOA[7]/N2HET2[6]/EPWM2A	22				
GIOB[0]	126				
GIOB[1]	133				
GIOB[2]	142				
MIBSPI3NCS[0]/AD2EVT/**GIOB[2]**/EQEP1I/N2HET2_PIN_nDIS	55 (1)		Pullup		
GIOB[3]	1		Pulldown		

(1) GIOB[2] cannot output a level on to pin 55. Only the input functionality is supported so that the application can generate an interrupt whenever the N2HET2_PIN_nDIS is asserted (driven low). Also, a pullup is enabled on the input. This is not programmable using the GIO module control registers.

4.2.1.7 Controller Area Network Controllers (DCAN)

Table 4-7. PGE Controller Area Network Controllers (DCAN)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE A				
CAN1RX	90	I/O	Pullup	Programmable, 20 µA	CAN1 receive, or GIO
CAN1TX	89				CAN1 transmit, or GIO
CAN2RX	129				CAN2 receive, or GIO
CAN2TX	128				CAN2 transmit, or GIO
CAN3RX	12				CAN3 receive, or GIO
CAN3TX	13				CAN3 transmit, or GIO

4.2.1.8 Local Interconnect Network Interface Module (LIN)

Table 4-8. PGE Local Interconnect Network Interface Module (LIN)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
LINRX	131	I/O	Pullup	Programmable, 20 µA	LIN receive, or GIO
LINTX	132				LIN transmit, or GIO

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4.2.1.9 Standard Serial Communication Interface (SCI)

Table 4-9. PGE Standard Serial Communication Interface (SCI)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
N2HET1[06]/**SCIRX**/EPWM5A	38	I/O	Pulldown	Programmable, 20 µA	SCI receive, or GIO
N2HET1[13]/**SCITX**/EPWM5B	39				SCI transmit, or GIO

4.2.1.10 Inter-Integrated Circuit Interface Module (I2C)

Table 4-10. PGE Inter-Integrated Circuit Interface Module (I2C)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
MIBSPI3NCS[2]/**I2CSDA**/N2HET1[27]/nTZ2	4	I/O	Pullup	Programmable, 20 µA	I2C serial data, or GIO
MIBSPI3NCS[3]/**I2CSCL**/N2HET1[29]/nTZ1	3				I2C serial clock, or GIO

4.2.1.11 Standard Serial Peripheral Interface (SPI)

Table 4-11. PGE Standard Serial Peripheral Interface (SPI)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
N2HET1[0]/**SPI4CLK**/EPWM2B	25	I/O	Pulldown	Programmable, 20 µA	SPI4 clock, or GIO
N2HET1[03]/**SPI4NCS[0]**/N2HET2[10]/EQEP2B	24				SPI4 chip select, or GIO
N2HET1[01]/**SPI4NENA**/N2HET2[8]/EQEP2A	23				SPI4 enable, or GIO
N2HET1[02]/**SPI4SIMO[0]**/EPWM3A	30				SPI4 slave-input master-output, or GIO
N2HET1[05]/**SPI4SOMI[0]**/N2HET2[12]/EPWM3B	31				SPI4 slave-output master-input, or GIO

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4.2.1.12 Multibuffered Serial Peripheral Interface Modules (MibSPI)

Table 4-12. PGE Multibuffered Serial Peripheral Interface Modules (MibSPI)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
MIBSPI1CLK	95	I/O	Pullup	Programmable, 20 µA	MibSPI1 clock, or GIO
MIBSPI1NCS[0]/MIBSPI1SOMI[1]/ECAP6	105				MibSPI1 chip select, or GIO
MIBSPI1NCS[1]/N2HET1[17]//EQEP1S	130				
MIBSPI1NCS[2]/N2HET1[19]/	40				
N2HET1[15]/**MIBSPI1NCS[4]**/ECAP1	41		Pulldown	Programmable, 20 µA	MibSPI1 chip select, or GIO
N2HET1[24]/**MIBSPI1NCS[5]**	91				
MIBSPI1NENA/N2HET1[23]/ECAP4	96		Pullup	Programmable, 20 µA	MibSPI1 enable, or GIO
MIBSPI1SIMO[0]	93				MibSPI1 slave-in master-out, or GIO
N2HET1[08]/**MIBSPI1SIMO[1]**	106		Pulldown	Programmable, 20 µA	MibSPI1 slave-in master-out, or GIO
MIBSPI1SOMI[0]	94		Pullup	Programmable, 20 µA	MibSPI1 slave-out master-in, or GIO
MIBSPI1NCS[0]/**MIBSPI1SOMI[1]**/ECAP6	105				
MIBSPI3CLK/AWM1_EXT_SEL[1]/EQEP1A	53	I/O	Pullup	Programmable, 20 µA	MibSPI3 clock, or GIO
MIBSPI3NCS[0]/AD2EVT/GIOB[2]/EQEP1I/N2HET2_PIN_nDIS	55				MibSPI3 chip select, or GIO
MIBSPI3NCS[1]/N2HET1[25]	37				
MIBSPI3NCS[2]/I2CSDA/N2HET1[27]/nTZ2	4				
MIBSPI3NCS[3]/I2CSCL/N2HET1[29]/nTZ1	3				
N2HET1[11]/**MIBSPI3NCS[4]**/N2HET2[18]/EPWM1SYNCO	6		Pulldown	Programmable, 20 µA	MibSPI3 chip select, or GIO
MIBSPI3NENA /**MIBSPI3NCS[5]**/N2HET1[31]/EQEP1B	54		Pullup	Programmable, 20 µA	MibSPI3 chip select, or GIO
MIBSPI3NENA/MIBSPI3NCS[5]/N2HET1[31]/EQEP1B	54				MibSPI3 enable, or GIO
MIBSPI3SIMO[0]/AWM1_EXT_SEL[0]/ECAP3	52				MibSPI3 slave-in master-out, or GIO
MIBSPI3SOMI[0]/AWM1_EXT_ENA/ECAP2	51				MibSPI3 slave-out master-in, or GIO
MIBSPI5CLK	100	I/O	Pullup	Programmable, 20 µA	MibSPI5 clock, or GIO
MIBSPI5NCS[0]/EPWM4A	32				MibSPI5 chip select, or GIO
MIBSPI5NENA/MIBSPI5SOMI[1]/ECAP5	97				MibSPI5 enable, or GIO
MIBSPI5SIMO[0]/MIBSPI5SOMI[2]	99				MibSPI5 slave-in master-out, or GIO
MIBSPI5SOMI[0]	98				MibSPI5 slave-out master-in, or GIO
MIBSPI5NENA/**MIBSPI5SOMI[1]**/ECAP5	97				MibSPI5 SOMI[0], or GIO
MIBSPI5SIMO[0]/**MIBSPI5SOMI[2]**	99				MibSPI5 SOMI[0], or GIO

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4.2.1.13 System Module Interface

Table 4-13. PGE System Module Interface

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	144 PGE				
nPORRST	46	Input	Pulldown	100 µA	Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter. See .
nRST	116	I/O	Pullup	100 µA	System reset, warm reset, bidirectional. The internal circuitry indicates any reset condition by driving nRST low. The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal. This terminal has a glitch filter. See .
nERROR	117	I/O	Pulldown	20 µA	ESM Error Signal Indicates error of high severity. See .

4.2.1.14 Clock Inputs and Outputs

Table 4-14. PGE Clock Inputs and Outputs

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
OSCIN	18	Input	–	None	From external crystal/resonator, or external clock input
KELVIN_GND	19	Input			Kelvin ground for oscillator
OSCOUT	20	Output			To external crystal/resonator
ECLK	119	I/O	Pulldown	Programmable, 20 µA	External prescaled clock output, or GIO.
GIOA[5]/**EXTCLKIN1**/EPWM1A /N2HET1_PIN_nDIS	14	Input	Pulldown	20 µA	External clock input #1

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4.2.1.15 Test and Debug Modules Interface

Table 4-15. PGE Test and Debug Modules Interface

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
TEST	34	Input	Pulldown	Fixed, 100 µA	Test enable. This terminal must be connected to ground directly or via a pulldown resistor.
nTRST	109	Input			JTAG test hardware reset
RTCK	113	Output	-	None	JTAG return test clock
TCK	112	Input	Pulldown	Fixed, 100 µA	JTAG test clock
TDI	110	Input	Pullup		JTAG test data in
TDO	111	Output	Pulldown		JTAG test data out
TMS	108	Input	Pullup		JTAG test select

4.2.1.16 Flash Supply and Test Pads

Table 4-16. PGE Flash Supply and Test Pads

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
VCCP	134	3.3-V Power	–	None	Flash pump supply
FLTP1	7	–	–	None	Flash test pads. These terminals are reserved for TI use only. For proper operation these terminals must connect only to a test pad or not be connected at all [no connect (NC)].
FLTP2	8				

4.2.1.17 Supply for Core Logic: 1.2V nominal

Table 4-17. PGE Supply for Core Logic: 1.2V nominal

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
VCC	17	1.2-V Power	–	None	Core supply
VCC	29				
VCC	45				
VCC	48				
VCC	49				
VCC	57				
VCC	87				
VCC	101				
VCC	114				
VCC	123				
VCC	137				
VCC	143				

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4.2.1.18 Supply for I/O Cells: 3.3V nominal

Table 4-18. PGE Supply for I/O Cells: 3.3V nominal

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
VCCIO	10	3.3-V Power	–	None	Operating supply for I/Os
VCCIO	26				
VCCIO	42				
VCCIO	104				
VCCIO	120				
VCCIO	136				

4.2.1.19 Ground Reference for All Supplies Except VCCAD

Table 4-19. PGE Ground Reference for All Supplies Except VCCAD

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	144 PGE				
VSS	11	Ground	–	None	Ground reference
VSS	21				
VSS	27				
VSS	28				
VSS	43				
VSS	44				
VSS	47				
VSS	50				
VSS	56				
VSS	88				
VSS	102				
VSS	103				
VSS	115				
VSS	121				
VSS	122				
VSS	135				
VSS	138				
VSS	144				

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4.2.2 PZ Package Terminal Functions

4.2.2.1 High-End Timer (N2HET)

Table 4-20. PZ Enhanced High-End Timer Modules (N2HET)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	100 PZ				
N2HET1[0]/ SPI4CLK / EPWM2B	19	I/O	Pulldown	Programmable, 20 µA	N2HET2 timer input capture or output compare, or GIO. Each terminal has a suppression filter with a programmable duration. Timer input capture or output compare. The N2HET applicable terminals can be programmed as general-purpose input/output (GIO).
N2HET1[2] / SPI4SIMO / EPWM3A	22				
N2HET1[4] / EPWM4B	25				
N2HET1[6] / SCIRX / EPWM5A	26				
N2HET1[8] / MIBSPI1SIMO[1]	74				
N2HET1[10] / nTZ3	83				
N2HET1[12]	89				
N2HET1[14]	90				
N2HET1[16] / EPWM1SYNCI / EPWM1SYNCO	97				
MIBSPI1nCS[1] / **N2HET1[17]** / EQEP1S	93		Pullup		
N2HET1[18] / EPWM6A	98		Pulldown		
MIBSPI1nCS[2] / **N2HET1[19]**	27		Pullup		
MIBSPI1nCS[3] / **N2HET1[21]**	39				
N2HET1[22]	11		Pulldown		
MIBSPI1nENA / **N2HET1[23]** / ECAP4	68		Pullup		
N2HET1[24] / MIBSPI1nCS[5]	64		Pulldown		
MIBSPI3nENA / MIBSPI3nCS[5] / **N2HET1[31]** / EQEP1B	37		Pullup		
GIOA[2] / INT[2] / **N2HET2[0]** / EQEP2I	5		Pulldown		
GIOA[3] / INT[3] / **N2HET2[2]**	8				
GIOA[6] / INT[6] / **N2HET2[4]** / EPWM1B	12				
GIOA[7] / INT[7] / **N2HET2[6]** / EPWM2A	18				

4.2.2.2 Enhanced Capture Modules (eCAP)

Table 4-21. PZ Enhanced Capture Modules (eCAP)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	100 PZ				
MIBSPI3SOMI[0] / AWM1_EXT_ENA / **ECAP2**	34	I/O	Pullup	Fixed, 20 µA	Enhanced Capture Module 2 I/O
MIBSPI3SIMO[0] / AWM1_EXT_SEL[0] / **ECAP3**	35				Enhanced Capture Module 3 I/O
MIBSPI1NENA / N2HET1[23] / **ECAP4**	68				Enhanced Capture Module 4 I/O
MIBSPI1NCS[0] / MIBSPI1SOMI[1] / **ECAP6**	73				Enhanced Capture Module 6 I/O

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4.2.2.3 Enhanced Quadrature Encoder Pulse Modules (eQEP)

Table 4-22. PZ Enhanced Quadrature Encoder Pulse Modules (eQEP)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
MIBSPI3CLK / AWM1_EXT_SEL[1] / **EQEP1A**	36	I/O	Pullup	Fixed, 20 µA	Enhanced QEP1 Input A
MIBSPI3nENA / MIBSPI3nCS[5] / N2HET1[31] / **EQEP1B**	37				Enhanced QEP1 Input B
MIBSPI3nCS[0] / AD2EVT / GIOB[2] / **EQEP1I**/N2HET2_PIN_nDIS	38				Enhanced QEP1 Index
MIBSPI1nCS[1] / N2HET1[17] / **EQEP1S**	93				Enhanced QEP1 Strobe
GIOA[2] / INT[2] / N2HET2[0] / **EQEP2I**	5		Pulldown		Enhanced QEP2 Index

4.2.2.4 Enhanced Pulse-Width Modulator Modules (ePWM)

Table 4-23. PZ Enhanced Pulse-Width Modulator Modules (ePWM)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
GIOA[5] / INT[5] / EXTCLKIN / **EPWM1A**/N2HET1_PIN_nDIS	10	Output	Pulldown	–	Enhanced PWM1 Output A
GIOA[6] / INT[6] / N2HET2[4] / **EPWM1B**	12		Pulldown		Enhanced PWM1 Output B
N2HET1[16] / **EPWM1SYNCI** / EPWM1SYNCO	97	Input	Pulldown	Fixed, 20 µA	External ePWM Sync Pulse Input
N2HET1[16] / EPWM1SYNCI / **EPWM1SYNCO**	97	Output	Pulldown	–	External ePWM Sync Pulse Output
GIOA[7] / INT[7] / N2HET2[6] / **EPWM2A**	18				Enhanced PWM2 Output A
N2HET1[0] / SPI4CLK / **EPWM2B**	19				Enhanced PWM2 Output B
N2HET1[2] / SPI4SIMO / **EPWM3A**	22				Enhanced PWM3 Output A
N2HET1[4] / **EPWM4B**	25				Enhanced PWM4 Output B
N2HET1[6] / SCIRX / **EPWM5A**	26				Enhanced PWM5 Output A
N2HET1[18] / **EPWM6A**	98				Enhanced PWM6 Output A
N2HET1[10] / **nTZ3**	83	Input	Pulldown		Trip Zone 1 input 3

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4.2.2.5 General-Purpose Input/Output (GIO)

Table 4-24. PZ General-Purpose Input/Output (GIO)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	**100 PZ**				
GIOA					
GIOA[0] / INT[0]	1	I/O	Pulldown	Programmable, 20 µA	General-purpose input/output All GPIO terminals are capable of generating interrupts to the CPU on rising/falling/both edges.
GIOA[1] / INT[1]	2				
GIOA[2] / INT[2] / N2HET2[0] / EQEP2I	5				
GIOA[3] / INT[3] / N2HET2[2]	8				
GIOA[4]/ INT[4]	9				
GIOA[5] / INT[5] / EXTCLKIN / EPWM1A/ N2HET1_PIN_nDIS	10				
GIOA[6] / INT[6] / N2HET2[4] / EPWM1B	12				
GIOA[7] / INT[7] / N2HET2[6] / EPWM2A	18				
GIOB					
MIBSPI3nCS[0] / AD2EVT / **GIOB[2]** / EQEP1I/N2HET2_PIN_nDIS	38	I/O			General-purpose input/output

4.2.2.6 Controller Area Network Interface Modules (DCAN1, DCAN2)

Table 4-25. PZ Controller Area Network Interface Modules (DCAN1, DCAN2)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	**100 PZ**				
DCAN1					
CAN1RX	63	I/O	Pullup	Programmable, 20 µA	CAN1 Receive, or general-purpose I/O (GPIO)
CAN1TX	62				CAN1 Transmit, or GPIO
DCAN2					
CAN2RX	92	I/O	Pullup	Programmable, 20 µA	CAN2 Receive, or GPIO
CAN2TX	91				CAN2 Transmit, or GPIO

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4.2.2.7 Standard Serial Peripheral Interfaces (SPI2 and SPI4)

Table 4-26. PZ Standard Serial Peripheral Interfaces (SPI2 and SPI4)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	**100 PZ**				
SPI2					
SPI2CLK	71	I/O	Pullup	Programmable, 20 µA	SPI2 Serial Clock, or GPIO
SPI2nCS[0]	23				SPI2 Chip Select, or GPIO
SPI2SIMO	70				SPI2 Slave-In-Master-Out, or GPIO
SPI2SOMI	69				SPI2 Slave-Out-Master-In, or GPIO
The drive strengths for the SPI2CLK, SPI2SIMO and SPI2SOMI signals are selected individually by configuring the respective SRS bits of the SPIPC9 register fo SPI2. SRS = 0 for 8mA drive (fast). This is the default mode as the SRS bits in the SPIPC9 register default to 0. SRS = 1 for 2mA drive (slow)					
SPI4					
N2HET1[0] / **SPI4CLK** / EPWM2B	19	I/O	Pulldown	Programmable, 20 µA	SPI2 Serial Clock, or GPIO
N2HET1[2] / **SPI4SIMO** / EPWM3A	22				SPI2 Slave-In-Master-Out, or GPIO

4.2.2.8 Multibuffered Serial Peripheral Interface (MibSPI1 and MibSPI3)

Table 4-27. PZ Multibuffered Serial Peripheral Interface (MibSPI1 and MibSPI3)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	**100 PZ**				
MibSPI1					
MIBSPI1CLK	67	I/O	Pullup	Programmable, 20 µA	MibSPI1 Serial Clock, or GPIO
MIBSPI1nCS[0]/MIBSPI1SOMI[1]/ ECAP6	73				MibSPI1 Chip Select, or GPIO
MIBSPI1nCS[1]/N2HET1[17]/ EQEP1S	93				
MIBSPI1nCS[2]/N2HET1[19]	27				
MIBSPI1nCS[3]/N2HET1[21]	39				
MIBSPI1nENA/N2HET1[23]/ ECAP4	68				MibSPI1 Enable, or GPIO
MIBSPI1SIMO[0]	65				MibSPI1 Slave-In-Master-Out, or GPIO
N2HET1[8]/**MIBSPI1SIMO[1]**	74				
MIBSPI1SOMI[0]	66				MibSPI1 Slave-Out-Master-In, or GPIO
MIBSPI1nCS[0]/**MIBSPI1SOMI[1]**/ ECAP6	73				
MibSPI3					
MIBSPI3CLK/AWM1_EXT_SEL[1]/ EQEP1A	36	I/O	Pullup	Programmable, 20 µA	MibSPI3 Serial Clock, or GPIO
MIBSPI3nCS[0]/AD2EVT/GIOB[2]/ EQEP1I/N2HET2_PIN_nDIS	38				MibSPI3 Chip Select, or GPIO
MIBSPI3nENA/**MIBSPI3nCS[5]**/ N2HET1[31]/EQEP1B	37				
MIBSPI3nENA/MIBSPI3nCS[5]/ N2HET1[31]/EQEP1B	37				MibSPI3 Enable, or GPIO
MIBSPI3SIMO[0]/AWM1_EXT_SEL[0]/ ECAP3	35				MibSPI3 Slave-In-Master-Out, or GPIO
MIBSPI3SOMI[0]/AWM1_EXT_ENA/ ECAP2	34				MibSPI3 Slave-Out-Master-In, or GPIO

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4.2.2.9 Local Interconnect Network Controller (LIN)

Table 4-28. PZ Local Interconnect Network Controller (LIN)

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
LINRX	94	I/O	Pullup	Programmable, 20 µA	LIN Receive, or GPIO
LINTX	95				LIN Transmit, or GPIO

4.2.2.10 Multibuffered Analog-to-Digital Converter (MibADC)

Table 4-29. PZ Multibuffered Analog-to-Digital Converter (MibADC)

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	100 PZ				
MibADC1					
AD1EVT	58	I/O	Pulldown	Programmable, 20 µA	ADC1 Event Trigger or GPIO
AD1IN[0]	42	Input	–	–	Analog Inputs
AD1IN[1]	49				
AD1IN[2]	51				
AD1IN[3]	52				
AD1IN[4]	54				
AD1IN[5]	55				
AD1IN[6]	56				
AD1IN[7]	43				
AD1IN[8]/AD2IN[8]	57				
AD1IN[9]/AD2IN[9]	48				
AD1IN[10]/AD2IN[10]	50				
AD1IN[11]/AD2IN[11]	53				
AD1IN[16]/AD2IN[0]	40				
AD1IN[17]/AD2IN[1]	41				
AD1IN[20]/AD2IN[4]	44				
AD1IN[21]/AD2IN[5]	45				
ADREFHI/VCCAD	46	Input/ Power	–	–	ADC High Reference Level/ADC Operating Supply
ADREFLO/VSSAD	47	Input/ Ground	–	–	ADC Low Reference Level/ADC Supply Ground
MIBSPI3SOMI[0]/**AWM1_EXT_ENA**/ ECAP2	34				AWM external analog mux enable
MIBSPI3SIMO[0]/**AWM1_EXT_SEL[0]**/ ECAP3	35				AWM external analog mux select line 0
MIBSPI3CLK/**AWM1_EXT_SEL[1]**/ EQEP1A	36				AWM external analog mux select line1
MibADC2					
MIBSPI3nCS[0]/**AD2EVT**/GIOB[2]/ EQEP1I/N2HET2_PIN_nDIS	38	I/O			ADC2 Event Trigger or GPIO

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4.2.2.11 System Module Interface

Table 4-30. PZ System Module Interface

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
nPORRST	31	Input	Pullup	100 µA	Power-on reset, cold reset External power supply monitor circuitry must drive nPORRST low when any of the supplies to the microcontroller fall out of the specified range. This terminal has a glitch filter. See .
nRST	81	I/O	Pullup	100 µA	The external circuitry can assert a system reset by driving nRST low. To ensure that an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal. This terminal has a glitch filter. See .
nERROR	82	I/O	Pulldown	20 µA	ESM Error Signal. Indicates error of high severity. See .

4.2.2.12 Clock Inputs and Outputs

Table 4-31. PZ Clock Inputs and Outputs

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
OSCIN	14	Input	–	–	From external crystal/resonator, or external clock input
KELVIN_GND	15	Input	–	–	Dedicated ground for oscillator
OSCOUT	16	Output	–	–	To external crystal/resonator
ECLK	84	I/O	Pulldown	Programmable, 20 µA	External prescaled clock output, or GIO.
GIOA[5]/INT[5]/**EXTCLKIN**/EPWM1A /N2HET1_PIN_nDIS	10	Input	Pulldown	20 µA	External Clock In

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4.2.2.13 Test and Debug Modules Interface

Table 4-32. PZ Test and Debug Modules Interface

TERMINAL		SIGNAL TYPE	RESET PULL STATE	PULL TYPE	DESCRIPTION
SIGNAL NAME	100 PZ				
nTRST	76	Input	Pulldown	Fixed, 100 µA	JTAG test hardware reset
RTCK	80	Output	–	–	JTAG return test clock
TCK	79	Input	Pulldown	Fixed, 100 µA	JTAG test clock
TDI	77	I/O	Pullup	Fixed, 100 µA	JTAG test data in
TDO	78	I/O	Pulldown	Fixed, 100 µA	JTAG test data out
TMS	75	I/O	Pullup	Fixed, 100 µA	JTAG test select
TEST	24	I/O	Pulldown	Fixed, 100 µA	Test enable. This terminal must be connected to ground directly or via a pulldown resistor.

4.2.2.14 Flash Supply and Test Pads

Table 4-33. PZ Flash Supply and Test Pads

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	100 PZ				
VCCP	96	3.3-V Power	–	–	Flash external pump voltage (3.3 V). This terminal is required for both Flash read and Flash program and erase operations.
FLTP1	3	Input	–	–	Flash Test Pins. For proper operation this terminal must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event.
FLTP2	4	Input	–	–	

4.2.2.15 Supply for Core Logic: 1.2-V Nominal

Table 4-34. PZ Supply for Core Logic: 1.2-V Nominal

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	100 PZ				
VCC	13	1.2-V Power	–	–	Digital logic and RAM supply
VCC	21				
VCC	30				
VCC	32				
VCC	61				
VCC	88				
VCC	99				

4.2.2.16 Supply for I/O Cells: 3.3-V Nominal

Table 4-35. PZ Supply for I/O Cells: 3.3-V Nominal

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	100 PZ				
VCCIO	6	3.3-V Power	–	–	I/O Supply
VCCIO	28				
VCCIO	60				
VCCIO	85				

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4.2.2.17 Ground Reference for All Supplies Except VCCAD

Table 4-36. PZ Ground Reference for All Supplies Except VCCAD

Terminal		Signal Type	Reset Pull State	Pull Type	Description
Signal Name	100 PZ				
VSS	7	Ground	–	–	Device Ground Reference. This is a single ground reference for all supplies except for the ADC Supply.
VSS	17				
VSS	20				
VSS	29				
VSS	33				
VSS	59				
VSS	72				
VSS	86				
VSS	87				
VSS	100				

4.3 Pin Multiplexing

This microcontroller has several interfaces and uses extensive multiplexing to bring out the functions as required by the target application. The multiplexing is mostly on the output signals. A few inputs are also multiplexed to allow the same input signal to be driven in from a selected terminal.

4.3.1 Output Multiplexing

Table 4-37 and Table 4-38 show the pin multiplexing control x register (PINMMRx) and the associated bit fields that control each pin mux function.

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Table 4-37. Multiplexing for Outputs on 144-Pin PGE Package(1)

144-PIN PGE	DEFAULT FUNCTION	CTRL1	OPTION 2	CTRL2	OPTION 3	CTRL3	OPTION 4	CTRL4	OPTION 5	CTRL5	OPTION 6	CTRL6
86	AD1EVT	10[0]										
2	GIOA[0]	0[8]										
5	GIOA[1]	1[0]										
9	GIOA[2]	2[0]					N2HET2[0]	2[3]	EQEP2I	2[4]		
14	GIOA[5]	2[24]	EXTCLKIN1	2[25]	EPWM1A	2[26]						
16	GIOA[6]	3[16]	N2HET2[4]	3[17]	EPWM1B	3[18]						
22	GIOA[7]	4[0]	N2HET2[6]	4[1]	EPWM2A	4[2]						
126	GIOB[0]	18[24]										
133	GIOB[1]	21[8]										
1	GIOB[3]	0[0]										
105	MIBSPI1NCS[0]	13[24]	MIBSPI1SOMI[1]	13[25]					ECAP6	13[28]		
130	MIBSPI1NCS[1]	20[16]	N2HET1[17]	20[17]					EQEP1S	20[20]		
40	MIBSPI1NCS[2]	8[8]	N2HET1[19]	8[9]								
96	MIBSPI1NENA	12[16]	N2HET1[23]	12[17]					ECAP4	12[20]		
53	MIBSPI3CLK	33[24]	AWM1_EXT_SEL[1]	33[25]	EQEP1A	33[26]						
55	MIBSPI3NCS[0]	9[16]	AD2EVT	9[17]	GIOB[2]	9[18]	EQEP1I	9[19]				
37	MIBSPI3NCS[1]	7[8]	N2HET1[25]	7[9]								
4	MIBSPI3NCS[2]	0[24]	I2C_SDA	0[25]	N2HET1[27]	0[26]	nTZ2	0[27]				
3	MIBSPI3NCS[3]	0[16]	I2C_SCL	0[17]	N2HET1[29]	0[18]	nTZ1	0[19]				
54	MIBSPI3NENA	9[8]	MIBSPI3NCS[5]	9[9]	N2HET1[31]	9[10]	EQEP1B	9[11]				
52	MIBSPI3SIMO	33[16]	AWM1_EXT_SEL[0]	33[17]	ECAP3	33[18]						
51	MIBSPI3SOMI	33[8]	AWM1_EXT_ENA	33[9]	ECAP2	33[10]						
100	MIBSPI5CLK	13[16]										
32	MIBSPI5NCS[0]	27[0]	EPWM4A	27[2]								
97	MIBSPI5NENA	12[24]					MIBSPI5SOMI[1]	12[28]	ECAP5	12[29]		
99	MIBSPI5SIMO[0]	13[8]					MIBSPI5SOMI[2]	13[12]				
98	MIBSPI5SOMI[0]	13[0]										
25	N2HET1[0]	5[0]	SPI4CLK	5[1]	EPWM2B	5[2]						
23	N2HET1[01]	4[16]	SPI4NENA	4[17]				4[19]	N2HET2[8]	4[20]	EQEP2A	4[21]
30	N2HET1[02]	5[8]	SPI4SIMO	5[9]	EPWM3A	5[10]						
24	N2HET1[03]	4[24]	SPI4NCS[0]	4[25]				4[27]	N2HET2[10]	4[28]	EQEP2B	4[29]
36	N2HET1[04]	33[0]	EPWM4B	33[1]								
31	N2HET1[05]	5[16]	SPI4SOMI	5[17]	N2HET2[12]	5[18]	EPWM3B	5[19]				
38	N2HET1[06]	7[16]	SCIRX	7[17]	EPWM5A	7[18]						
33	N2HET1[07]	6[0]					N2HET2[14]	6[3]	EPWM7B	6[4]		

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Table 4-37. Multiplexing for Outputs on 144-Pin PGE Package(1) (continued)

144-PIN PGE	DEFAULT FUNCTION	CTRL1	OPTION 2	CTRL2	OPTION 3	CTRL3	OPTION 4	CTRL4	OPTION 5	CTRL5	OPTION 6	CTRL6
106	N2HET1[08]	14[0]	MIBSPI1SIMO[1]	14[1]								
35	N2HET1[09]	6[16]	N2HET2[16]	6[17]					EPWM7A	6[20]		
118	N2HET1[10]	17[0]							nTZ3	17[4]		
6	N2HET1[11]	1[8]	MIBSPI3NCS[4]	1[9]	N2HET2[18]	1[10]					EPWM1SYNCO	1[13]
124	N2HET1[12]	17[16]										
39	N2HET1[13]	8[0]	SCITX	8[1]	EPWM5B	8[2]						
125	N2HET1[14]	18[8]										
41	N2HET1[15]	8[16]	MIBSPI1NCS[4]	8[17]	ECAP1	8[18]						
139	N2HET1[16]	34[0]	EPWM1SYNCI	34[1]	EPWM1SYNCO	34[2]						
140	N2HET1[18]	34[8]	EPWM6A	34[9]								
141	N2HET1[20]	34[16]	EPWM6B	34[17]								
15	N2HET1[22]	3[8]										
91	N2HET1[24]	11[24]	MIBSPI1NCS[5]	11[25]								
92	N2HET1[26]	12[0]										
107	N2HET1[28]	14[8]										
127	N2HET1[30]	19[8]					EQEP2S	19[11]				

(1) The CTRLx columns contain a value of type x[y], which indicates the pin multiplexing control x register (PINMMRx) and the associated bit field [y].

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Table 4-38. Multiplexing for Outputs on 100-Pin PZ Package(1)

100-PIN PZ	DEFAULT FUNCTION	CTRL1	OPTION 2	CTRL2	OPTION 3	CTRL3	OPTION 4	CTRL4	OPTION 5	CTRL5	OPTION 6	CTRL6
2	GIOA[1]/INT[1]	1[0]										
5	GIOA[2]/INT[2]	2[0]					N2HET2[0]	2[3]	EQEP2I	2[4]		
10	GIOA[5]/INT[5]	2[24]	EXTCLKIN1	2[25]	EPWM1A	2[26]						
12	GIOA[6]/INT[6]	3[16]	N2HET2[4]	3[17]	EPWM1B	3[18]						
18	GIOA[7]/INT[7]	4[0]	N2HET2[6]	4[1]	EPWM2A	4[2]						
73	MIBSPI1NCS[0]	13[24]	MIBSPI1SOMI[1]	13[25]					ECAP6	13[28]		
93	MIBSPI1NCS[1]	20[16]	N2HET1[17]	20[17]					EQEP1S	20[20]		
27	MIBSPI1NCS[2]	8[8]	N2HET1[19]	8[9]								
68	MIBSPI1NENA	12[16]	N2HET1[23]	12[17]					ECAP4	12[20]		
36	MIBSPI3CLK	33[24]	AWM1_EXT_SEL[1]	33[25]	EQEP1A	33[26]						
38	MIBSPI3NCS[0]	9[16]	AD2EVT	9[17]	GIOB[2]	9[18]	EQEP1I	9[19]				
37	MIBSPI3NENA	9[8]	MIBSPI3NCS[5]	9[9]	N2HET1[31]	9[10]	EQEP1B	9[11]				
35	MIBSPI3SIMO[0]	33[16]	AWM1_EXT_SEL[0]	33[17]	ECAP3	33[18]						
34	MIBSPI3SOMI[0]	33[8]	AWM1_EXT_ENA	33[9]	ECAP2	33[10]						
19	N2HET1[0]	5[0]	SPI4CLK	5[1]	EPWM2B	5[2]						
22	N2HET1[02]	5[8]	SPI4SIMO	5[9]	EPWM3A	5[10]						
25	N2HET1[04]	33[0]	EPWM4B	33[1]								
26	N2HET1[06]	7[16]	SCIRX	7[17]	EPWM5A	7[18]						
74	N2HET1[08]	14[0]	MIBSPI1SIMO[1]	14[1]								
83	N2HET1[10]	17[0]							nTZ3	17[4]		
97	N2HET1[16]	34[0]	EPWM1SYNCI	34[1]	EPWM1SYNCO	34[2]						
98	N2HET1[18]	34[8]	EPWM6A	34[9]								
64	N2HET1[24]	11[24]	MIBSPI1NCS[5]	11[25]								

(1) The CTRLx columns contain a value of type x[y], which indicates the pin multiplexing control x register (PINMMRx) and the associated bit field [y].

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4.3.2 Multiplexing of Inputs

Some signals are connected to more than one terminal, the inputs for these signals can come from any of the terminals. A multiplexor is implemented to let the application choose the terminal that will be used, providing the input signal is from among the available options.

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Table 4-39. Input Multiplexing and Control for All Packages [144-Pin PGE, and 100-Pin PZ](1)

SIGNAL NAME	DEDICATED INPUTS		MULTIPLEXED INPUTS		INPUT MULTIPLEXOR CONTROL		INPUT PATH SELECTED	
	144 PGE	100 PZ	144 PGE	100 PZ	BIT1	BIT2	DEDICATED, IF	MUXED, IF
GIOB[2]	142	–	55	38	PINMUX29[16]	PINMUX29[16]	BIT1 = 0(3)	BIT1 = 1(3)
N2HET1[17]	–	–	130	93	PINMUX20[17]	PINMUX24[16]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1
N2HET1[19]	–	–	40	27	PINMUX8[9]	PINMUX24[24]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1
N2HET1[21]	–	–	–	–	PINMUX9[25]	PINMUX25[0]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1
N2HET1[23]	–	–	96	68	PINMUX12[17]	PINMUX25[8]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1
N2HET1[25]	–	–	37	–	PINMUX7[9]	PINMUX25[16]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1
N2HET1[27]	–	–	4	–	PINMUX0[26]	PINMUX25[24]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1
N2HET1[29]	–	–	3	–	PINMUX0[18]	PINMUX26[0]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1
N2HET1[31]	–	–	54	37	PINMUX9[10]	PINMUX26[8]	not(BIT1) or (BIT1 and BIT2) = 1	BIT1 and not(BIT2) = 1

(1) The default inputs to the modules are from the dedicated input terminals. The application must configure the PINMUX registers as shown in order to select the multiplexed input path, if required.

(2) The SPI4CLK, SPI4SIMO, SPI4SOMI, SPI4nENA and SPI4nCS[0] signals do not have a dedicated signal pad on this device. Therefore, the input multiplexors on these inputs are not required. The control registers are still available to maintain compatibility to the emulation device.

(3) When the muxed input is selected for GIOB[2], the PINMUX9[16] and PINMUX9[17] must be cleared. These bits affect the control over the PULDIS (pull disable) and PSEL (pull select). When the multiplexed input path is selected for GIOB[2], the PULDIS is tied to 0 (pull is enabled, cannot be disabled) and the PULSEL is tied to 1 (pull up selected, not programmable).

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4.4 Buffer Type

Table 4-40. Output Buffer Drive Strengths

Low-level Output Current, I_{OL} for $V_I = V_{OLmax}$ or High-level Output Current, I_{OH} for $V_I = V_{OHmin}$	Signals
8mA	MIBSPI5CLK, MIBSPI5SOMI[0], MIBSPI5SOMI[1], MIBSPI5SOMI[2], MIBSPI5SOMI[3], MIBSPI5SIMO[0], MIBSPI5SIMO[1], MIBSPI5SIMO[2], MIBSPI5SIMO[3], TMS, TDI, TDO, RTCK, SPI4CLK, SPI4SIMO, SPI4SOMI, SPI4NCS[0], SPI4NENA, nERROR, N2HET2[1], N2HET2[3], N2HET2[5], N2HET2[7], N2HET2[9], N2HET2[11], N2HET2[13], N2HET2[15] ECAP1, ECAP4, ECAP5, ECAP6 EQEP1I, EQEP1S, EQEP2I, EQEP2S EPWM1A, EPWM1B, EPWM1SYNCO, EPW2A, EPWM2B, EPWM3A, EPWM3B, EPWM4A, EPWM4B, EPWM5A, EPWM5B, EPWM6A, EPWM6B, EPWM7A, EPWM7B
4mA	TEST, MIBSPI3SOMI, MIBSPI3SIMO, MIBSPI3CLK, MIBSPI1SIMO, MIBSPI1SOMI, MIBSPI1CLK, ECAP2, ECAP3 nRST
2mA zero-dominant	AD1EVT, CAN1RX, CAN1TX, CAN2RX, CAN2TX, CAN3RX, CAN3TX, GIOA[0-7], GIOB[0-7], LINRX, LINTX, MIBSPI1NCS[0], MIBSPI1NCS[1-3], MIBSPI1NENA, MIBSPI3NCS[0-3], MIBSPI3NENA, MIBSPI5NCS[0-3], MIBSPI5NENA, N2HET1[0-31], N2HET2[0], N2HET2[2], N2HET2[4], N2HET2[6], N2HET2[8], N2HET2[10], N2HET2[12], N2HET2[14], N2HET2[16], N2HET2[18],
selectable 8mA / 2mA	ECLK, SPI2CLK, SPI2SIMO, SPI2SOMI The default output buffer drive strength is 8mA for these signals.

Table 4-41. Selectable 8mA/2mA Control

SIGNAL	CONTROL BIT	ADDRESS	8mA (DEFAULT)	2mA
ECLK	SYSPC10[0]	0xFFFF FF78	0	1
SPI2CLK	SPI2PC9[9]	0xFFF7 F668	0	1
SPI2SIMO	SPI2PC9[10]	0xFFF7 F668	0	1
SPI2SOMI	SPI2PC9[11] (1)	0xFFF7 F668	0	1

(1) Either SPI2PC9[11] or SPI2PC9[24] can change the output strength of the SPI2SOMI pin. In case of a 32-bit write where these two bits differ, SPI2PC9[11] determines the drive strength.

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5 Specifications

5.1 Absolute Maximum Ratings(1)

Over Operating Free-Air Temperature Range

		MIN	MAX	UNIT
Supply voltage range:	V_{CC}(2)	-0.3	1.43	V
	V_{CCIO}, V_{CCP}(2)	-0.3	4.6	V
	V_{CCAD}(2)	-0.3	6.25	V
Input voltage range:	All input pins, with exception of ADC pins	-0.3	4.6	V
	ADC input pins	-0.3	6.25	V
Output voltage range:	All output pins	-0.3	4.6	V
Input clamp current:	I_{IK} (V_I < 0 or V_I > V_{CCIO}) All pins, except AD1IN[23:0] or AD2IN[15:0]	-20	+20	mA
	I_{IK} (V_I < 0 or V_I > V_{CCAD}) AD1IN[23:0] or AD2IN[15:0]	-10	+10	mA
	Total	-40	+40	mA
Output clamp current:	I_{OK} (V_O < 0 or V_O > V_{CCIO}) All pins, except AWM1_EXT_x	-20	+20	mA
	Total	-40	+40	mA
Operating free-air temperature range, T_A:		-40	125	°C
Operating junction temperature range, T_J:		-40	150	°C
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to their associated grounds.

5.2 ESD Ratings

				MIN	MAX	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance:	Human Body Model (HBM), per AEC Q100-002(1)		-2	2	kV
		Charged Device Model (CDM), per AEC Q100-011	All pins	-500	500	V
			100-pin PZ Corner pins (1, 25, 26, 50, 51, 75, 76, 100)	-750	750	V
			144-pin PGE Corner pins (1, 36, 37, 72, 73, 108, 109, 144)	-750	750	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Power-On Hours (POH)(1)(2)

NOMINAL CVDD VOLTAGE (V)	JUNCTION TEMPERATURE (Tj)	LIFETIME POH
1.2	105ºC	100K

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) To avoid significant degradation, the device power-on hours (POH) must be limited to those specified in this table. To convert to equivalent POH for a specific temperature profile, see the *Calculating Equivalent Power-on-Hours for Hercules Safety MCUs Application Report* (SPNA207).

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5.4 Recommended Operating Conditions[1]

over operating free-air temperature range (unless otherwise noted)

			TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)			1.14	1.2	1.32	V
V_{CCIO}	Digital logic supply voltage (I/O)			3	3.3	3.6	V
V_{CCAD}	MibADC supply voltage			3		5.25	V
V_{CCP}	Flash pump supply voltage			3	3.3	3.6	V
V_{SS}	Digital logic supply ground				0		V
V_{SSAD}	MibADC supply ground			–0.1		0.1	V
$V_{ADREFHI}$	A-to-D high-voltage reference source			V_{SSAD}		V_{CCAD}	V
$V_{ADREFLO}$	A-to-D low-voltage reference source			V_{SSAD}		V_{CCAD}	V
V_{SLEW}	Maximum positive slew rate for V_{CCIO}, V_{CCAD} and V_{CPP} supplies					1	V/µs
V_{hys}	Input hysteresis	All inputs		180			mV
V_{IL}	Low-level input voltage	All inputs		–0.3		0.8	V
V_{IH}	High-level input voltage	All inputs		2		V_{CCIO} + 0.3	V
T_A	Operating free-air temperature			–40		125	°C
T_J	Operating junction temperature[2]			–40		150	°C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}
(2) Reliability data is based upon a temperature profile that is equivalent to 100,000 power-on hours at 105°C junction temperature.

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5.5 Input/Output Electrical Characteristics Over Recommended Operating Conditions(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		$I_{OL} = I_{OLmax}$			0.2 V_{CCIO}	V
			I_{OL} = 50 µA, standard output mode			0.2	
			I_{OL} = 50 µA, low-EMI output mode (see Section 7.1.2.1)			0.2 V_{CCIO}	
V_{OH}	High-level output voltage		$I_{OH} = I_{OHmax}$	0.8 V_{CCIO}			V
			I_{OH} = 50 µA, standard output mode	V_{CCIO} - 0.3			
			I_{OH} = 50 µA, low-EMI output mode (see Section 7.1.2.1)	0.8 V_{CCIO}			
I_{IC}	Input clamp current (I/O pins)		$V_I < V_{SSIO}$ - 0.3 or $V_I > V_{CCIO}$ + 0.3	–3.5		3.5	mA
I_I	Input current (I/O pins)	I_{IH} Pulldown 20µA	$V_I = V_{CCIO}$	5		40	µA
		I_{IH} Pulldown 100µA	$V_I = V_{CCIO}$	40		195	
		I_{IL} Pullup 20µA	$V_I = V_{SS}$	–40		–5	
		I_{IL} Pullup 100µA	$V_I = V_{SS}$	–195		–40	
		All other pins	No pullup or pulldown	–1		1	
C_I	Input capacitance				2		pF
C_O	Output capacitance				3		pF

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.

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5.6 Power Consumption Over Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{CC} digital supply current (operating mode) $f_{VCLK} = f_{HCLK}/2$; Flash in pipelined mode; V_{CCmax}	f_{HCLK} = 100MHz		130 (1)	270 (2)	mA
		f_{HCLK} = 160MHz		160 (1)	300 (2)	mA
	V_{CC} Digital supply current (LBIST/PBIST mode)	LBIST/PBIST clock frequency = 50MHz		150 (1)	290 (3) (4)	mA
		LBIST/PBIST clock frequency = 80MHz		215 (1)	360 (3) (4)	mA
		LBIST/PBIST clock frequency = 90MHz		240 (1)	390 (3) (4)	mA
I_{CCIO}	V_{CCIO} Digital supply current (operating mode)	No DC load, V_{CCmax}			15	mA
I_{CCAD}	V_{CCAD} supply current (operating mode)	Single ADC operational, $V_{CCADmax}$			15	mA
		Both ADCs operational, $V_{CCADmax}$			30	
$I_{CCREFHI}$	AD_{REFHI} supply current (operating mode)	Single ADC operational, $AD_{REFHImax}$			3	mA
		Both ADCs operational, $AD_{REFHImax}$			6	
I_{CCP}	V_{CCP} supply current	read from 1 bank and program another bank, V_{CCPmax}			55	mA

(1) The typical value is the average current for the nominal process corner and junction temperature of 25°C.
(2) The maximum $I_{CC,}$ value can be derated
- linearly with voltage
- by 0.85 ma/MHz for lower operating frequency when f_{HCLK}= 2 * f_{VCLK}
- for lower junction temperature by the equation below where T_{JK} is the junction temperature in Kelvin and the result is in milliamperes. **$126 - 0.005\ e^{0.024\ T_{JK}}$**

(3) The maximum $I_{CC,}$ value can be derated
- linearly with voltage
- by 0.85 ma/MHz for lower operating frequency
- for lower junction temperature by the equation below where T_{JK} is the junction temperature in Kelvin and the result is in milliamperes. **$126 - 0.005\ e^{0.024\ T_{JK}}$**

(4) LBIST and PBIST currents are for a short duration, typically less than 10ms. They are usually ignored for thermal calculations for the device and the voltage regulator

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5.7 Thermal Resistance Characteristics

Table 5-1 shows the thermal resistance characteristics for the QFP - PGE mechanical package.

Table 5-2 shows the thermal resistance characteristics for the QFP - PZ mechanical package.

Table 5-1. Thermal Resistance Characteristics (PGE Package)

		°C/W
$R\Theta_{JA}$	Junction-to-free air thermal resistance, Still air using JEDEC 2S2P test board	37.5
$R\Theta_{JB}$	Junction-to-board thermal resistance	19.7
$R\Theta_{JC}$	Junction-to-case thermal resistance	9.4
Ψ_{JT}	Junction-to-package top, Still air	0.40

Table 5-2. Thermal Resistance Characteristics (PZ Package)

		°C/W
$R\Theta_{JA}$	Junction-to-free air thermal resistance, Still air using JEDEC 2S2P test board	43.5
$R\Theta_{JB}$	Junction-to-board thermal resistance	21.6
$R\Theta_{JC}$	Junction-to-case thermal resistance	11.2
Ψ_{JT}	Junction-to-package top, Still air	0.50

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5.8 Timing and Switching Characteristics

5.8.1 SYSCLK (Frequencies)

5.8.1.1 Switching Characteristics over Recommended Operating Conditions for Clock Domains

Table 5-3. Clock Domain Timing Specifications

PARAMETER	DESCRIPTION	CONDITIONS		MIN	MAX	UNIT
f_{HCLK}	HCLK - System clock frequency	PZ (1)	Pipeline mode enabled		100	MHz
			Pipeline mode disabled		45	MHz
		PGE	Pipeline mode enabled		160	MHz
			Pipeline mode disabled		50	MHz
f_{GCLK}	GCLK - CPU clock frequency				f_{HCLK}	MHz
f_{VCLK}	VCLK - Primary peripheral clock frequency				100	MHz
f_{VCLK2}	VCLK2 - Secondary peripheral clock frequency				100	MHz
f_{VCLK4}	VCLK4 - Secondary peripheral clock frequency				150	MHz
f_{VCLKA1}	VCLKA1 - Primary asynchronous peripheral clock frequency				100	MHz
f_{RTICLK}	RTICLK - clock frequency				f_{VCLK}	MHz

(1) PZ package is only available as TMX samples.

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5.8.1.2 Wait States Required - PGE and PZ Packages

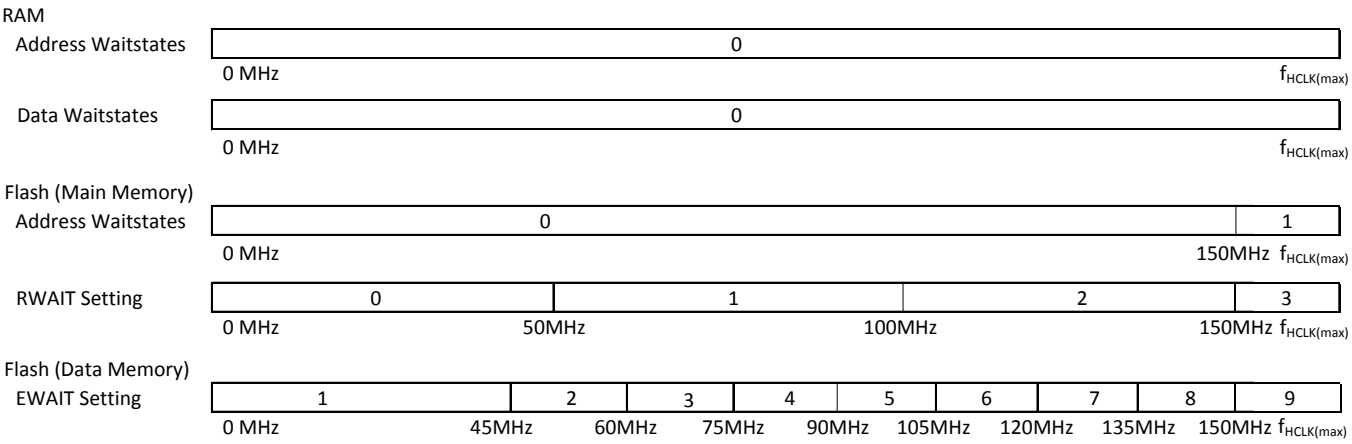


Figure 5-1. Wait States Scheme — PGE, 160 MHz

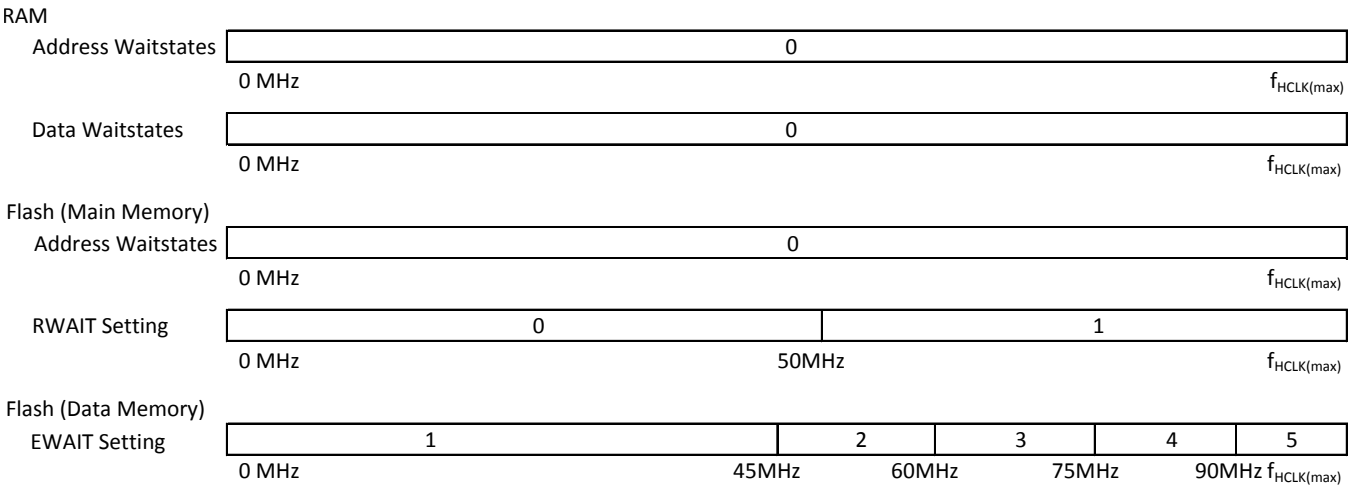


Figure 5-2. Wait States Scheme — PZ, 100 MHz

As shown in the figure above, the TCM RAM can support program and data fetches at full CPU speed without any address or data wait states required.

The TCM flash can support zero address and data wait states up to a CPU speed of 50 MHz in non-pipelined mode. The flash supports a maximum CPU clock speed of 160 MHz in pipelined mode for the PGE Package, and 100 MHz for the PZ package.

The flash wrapper defaults to non-pipelined mode with zero address wait state and one random-read data wait state.

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6 System Information and Electrical Specifications

6.1 Device Power Domains

The device core logic is split up into multiple power domains in order to optimize the power for a given application use case. There are 5 core power domains in total: PD1, PD2, PD3, PD5, and RAM_PD1. Refer to Section 1.4 for more information.

PD1 is an "always-ON" power domain, which cannot be turned off. Each of the other core power domains can be turned ON/OFF one time during device initialization as per the application requirement. Refer to the Power Management Module (PMM) chapter of the device technical reference manual for more details.

NOTE

The clocks to a module must be turned off before powering down the core domain that contains the module.

6.2 Voltage Monitor Characteristics

A voltage monitor is implemented on this device. The purpose of this voltage monitor is to eliminate the requirement for a specific sequence when powering up the core and I/O voltage supplies.

6.2.1 Important Considerations

- The voltage monitor does not eliminate the need of a voltage supervisor circuit to guarantee that the device is held in reset when the voltage supplies are out of range.
- The voltage monitor only monitors the core supply (VCC) and the I/O supply (VCCIO). The other supplies are not monitored by the VMON. For example, if the VCCAD or VCCP are supplied from a source different from that for VCCIO, then there is no internal voltage monitor for the VCCAD and VCCP supplies.

6.2.2 Voltage Monitor Operation

The voltage monitor generates the Power Good MCU signal (PGMCU) as well as the I/Os Power Good IO signal (PGIO) on the device. During power-up or power-down, the PGMCU and PGIO are driven low when the core or I/O supplies are lower than the specified minimum monitoring thresholds. The PGIO and PGMCU being low isolates the core logic as well as the I/O controls during the power-up or power-down of the supplies. This allows the core and I/O supplies to be powered up or down in any order.

When the voltage monitor detects a low voltage on the I/O supply, it will assert a power-on reset. When the voltage monitor detects an out-of-range voltage on the core supply, it asynchronously makes all output pins high impedance, and asserts a power-on reset. The voltage monitor is disabled when the device enters a low power mode.

The VMON also incorporates a glitch filter for the nPORRST input. Refer to Section 6.3.3.1 for the timing information on this glitch filter.

Table 6-1. Voltage Monitoring Specifications

PARAMETER			MIN	TYP	MAX	UNIT
V_{MON}	Voltage monitoring thresholds	VCC low - VCC level below this threshold is detected as too low.	0.75	0.9	1.13	V
		VCC high - VCC level above this threshold is detected as too high.	1.40	1.7	2.1	
		VCCIO low - VCCIO level below this threshold is detected as too low.	1.85	2.4	2.9	

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6.2.3 Supply Filtering

The VMON has the capability to filter glitches on the VCC and VCCIO supplies.

The following table shows the characteristics of the supply filtering. Glitches in the supply larger than the maximum specification cannot be filtered.

Table 6-2. VMON Supply Glitch Filtering Capability

PARAMETER	MIN	MAX
Width of glitch on VCC that can be filtered	250 ns	1 µs
Width of glitch on VCCIO that can be filtered	250 ns	1 µs

6.3 Power Sequencing and Power On Reset

6.3.1 Power-Up Sequence

There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage. The power-up sequence starts with the I/O voltage rising above the minimum I/O supply threshold, (see Table 6-4 for more details), core voltage rising above the minimum core supply threshold and the release of power-on reset. The high frequency oscillator will start up first and its amplitude will grow to an acceptable level. The oscillator start up time is dependent on the type of oscillator and is provided by the oscillator vendor. The different supplies to the device can be powered up in any order.

The device goes through the following sequential phases during power up.

Table 6-3. Power-Up Phases

Oscillator start-up and validity check	1032 oscillator cycles
eFuse autoload	1160 oscillator cycles
Flash pump power-up	688 oscillator cycles
Flash bank power-up	617 oscillator cycles
Total	**3497 oscillator cycles**

The CPU reset is released at the end of the above sequence and fetches the first instruction from address 0x00000000.

6.3.2 Power-Down Sequence

The different supplies to the device can be powered down in any order.

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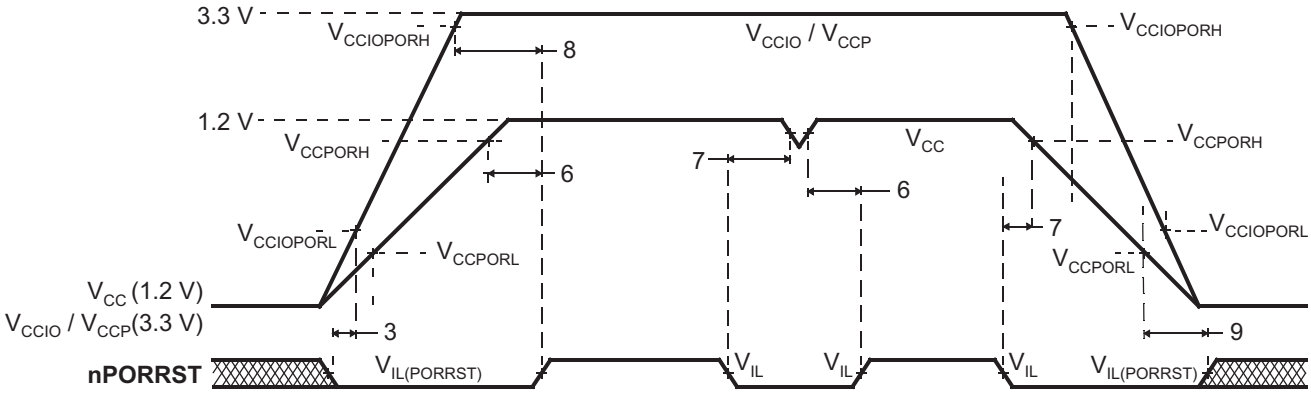
6.3.3 Power-On Reset: nPORRST

This is the power-on reset. This reset must be asserted by an external circuitry whenever any power supply is outside the specified recommended range. This signal has a glitch filter on it. It also has an internal pulldown.

6.3.3.1 nPORRST Electrical and Timing Requirements

Table 6-4. Electrical Requirements for nPORRST

NO.	PARAMETER		MIN	MAX	UNIT
	V_{CCPORL}	V_{CC} low supply level when nPORRST must be active during power-up		0.5	V
	V_{CCPORH}	V_{CC} high supply level when nPORRST must remain active during power-up and become active during power down	1.14		V
	$V_{CCIOPORL}$	V_{CCIO} / V_{CCP} low supply level when nPORRST must be active during power-up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} / V_{CCP} high supply level when nPORRST must remain active during power-up and become active during power down	3.0		V
	$V_{IL(PORRST)}$	Low-level input voltage of nPORRST V_{CCIO} > 2.5V		0.2 * V_{CCIO}	V
		Low-level input voltage of nPORRST V_{CCIO} < 2.5V		0.5	V
3	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CCIO} and V_{CCP} > $V_{CCIOPORL}$ during power-up	0		ms
6	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} > V_{CCPORH}	1		ms
7	$t_{su(PORRST)}$	Setup time, nPORRST active before V_{CC} < V_{CCPORH} during power down	2		µs
8	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CCIO} and V_{CCP} > $V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)}$	Hold time, nPORRST active after V_{CC} < V_{CCPORL}	0		ms
	$t_{f(nPORRST)}$	Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset.	475	2000	ns



NOTE: There is no timing dependency between the ramp of the VCCIO and the VCC supply voltage; this is just an exemplary drawing.

Figure 6-1. nPORRST Timing Diagram

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6.4 Warm Reset (nRST)

This is a bidirectional reset signal. The internal circuitry drives the signal low on detecting any device reset condition. An external circuit can assert a device reset by forcing the signal low. On this terminal, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor is connected to this terminal.

This terminal has a glitch filter. It also has an internal pullup

6.4.1 Causes of Warm Reset

Table 6-5. Causes of Warm Reset

DEVICE EVENT	SYSTEM STATUS FLAG
Power-Up Reset	Exception Status Register, bit 15
Oscillator fail	Global Status Register, bit 0
PLL slip	Global Status Register, bits 8 and 9
Watchdog exception / Debugger reset	Exception Status Register, bit 13
CPU Reset (driven by the CPU STC)	Exception Status Register, bit 5
Software Reset	Exception Status Register, bit 4
External Reset	Exception Status Register, bit 3

6.4.2 nRST Timing Requirements

Table 6-6. nRST Timing Requirements(1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, nRST active after nPORRST inactive	$2256t_{c(OSC)}$		ns
	Valid time, nRST active (all other System reset conditions)	$32t_{c(VCLK)}$		
$t_{f(nRST)}$	Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	475	2000	ns

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see Table 7-2.

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6.5 ARM© Cortex-R4F™ CPU Information

6.5.1 Summary of ARM Cortex-R4F™ CPU Features

The features of the ARM Cortex-R4F™ CPU include:

- An integer unit with integral EmbeddedICE-RT logic.
- High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced eXtensible Interfaces (AXI) for Level two (L2) master and slave interfaces.
- Floating Point Coprocessor
- Dynamic branch prediction with a global history buffer, and a 4-entry return stack
- Low interrupt latency.
- Non-maskable interrupt.
- A Harvard Level one (L1) memory system with:
  - Tightly-Coupled Memory (TCM) interfaces with support for error correction or parity checking memories
  - ARMv7-R architecture Memory Protection Unit (MPU) with 12 regions
- Dual core logic for fault detection in safety-critical applications.
- An L2 memory interface:
  - Single 64-bit master AXI interface
  - 64-bit slave AXI interface to TCM RAM blocks
- A debug interface to a CoreSight Debug Access Port (DAP).
- Six Hardware Breakpoints
- Two Watchpoints
- A Performance Monitoring Unit (PMU).
- A Vectored Interrupt Controller (VIC) port.

For more information on the ARM Cortex-R4F™ CPU please see www.arm.com.

6.5.2 ARM Cortex-R4F™ CPU Features Enabled by Software

The following CPU features are disabled on reset and must be enabled by the application if required.

- ECC On Tightly-Coupled Memory (TCM) Accesses
- Hardware Vectored Interrupt (VIC) Port
- Floating Point Coprocessor
- Memory Protection Unit (MPU)

6.5.3 Dual Core Implementation

The device has two Cortex-R4F cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed by 2 clock cycles as shown in Figure 6-3.

The CPUs have a diverse CPU placement given by following requirements:

- different orientation; e.g. CPU1 = "north" orientation, CPU2 = "flip west" orientation
- dedicated guard ring for each CPU



Figure 6-2. Dual - CPU Orientation

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6.5.4 Duplicate clock tree after GCLK

The CPU clock domain is split into two clock trees, one for each CPU, with the clock of the 2nd CPU running at the same frequency and in phase to the clock of CPU1. See Figure 6-3.

6.5.5 ARM Cortex-R4F™ CPU Compare Module (CCM) for Safety

This device has two ARM Cortex-R4F™ CPU cores, where the output signals of both CPUs are compared in the CCM-R4 unit. To avoid common mode impacts the signals of the CPUs to be compared are delayed in a different way as shown in the figure below.

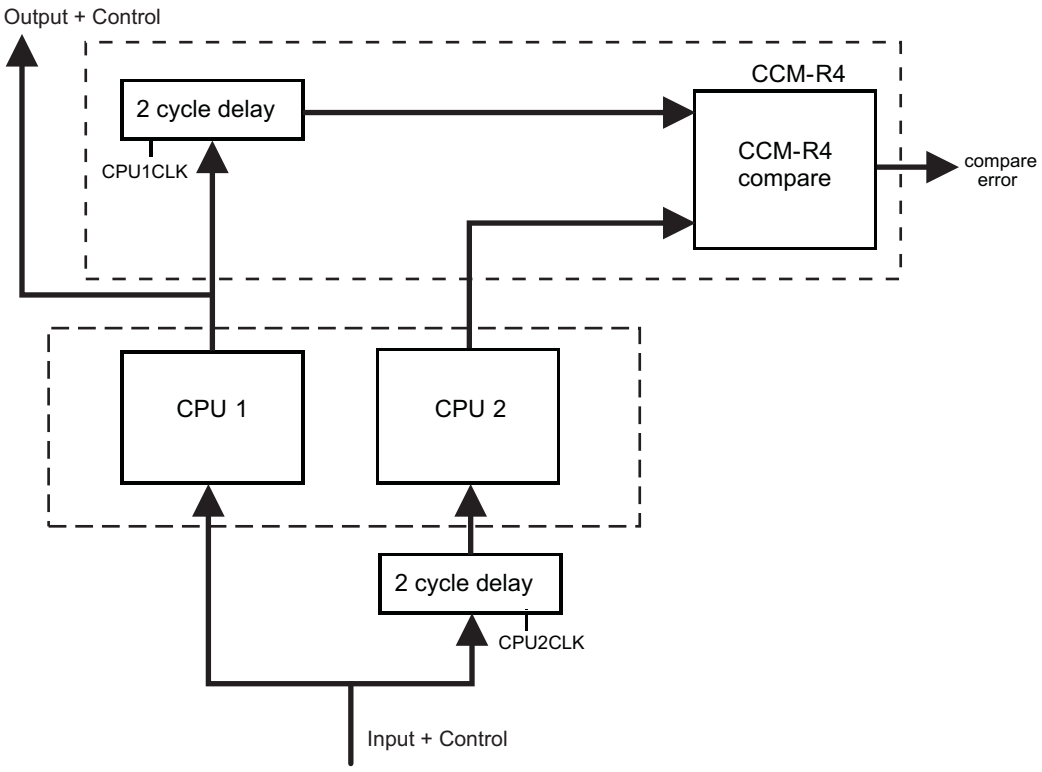


Figure 6-3. Dual Core Implementation

To avoid an erroneous CCM-R4 compare error, the application software must initialize the registers of both CPUs before the registers are used, including function calls where the register values are pushed onto the stack.

6.5.6 CPU Self-Test

The CPU STC (Self-Test Controller) is used to test the two Cortex-R4F CPU Cores using the Deterministic Logic BIST Controller as the test engine.

The main features of the self-test controller are:

- Ability to divide the complete test run into independent test intervals
- Capable of running the complete test as well as running few intervals at a time
- Ability to continue from the last executed interval (test set) as well as ability to restart from the beginning (First test set)
- Complete isolation of the self-tested CPU core from rest of the system during the self-test run
- Ability to capture the Failure interval number
- Timeout counter for the CPU self-test run as a fail-safe feature

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6.5.6.1 Application Sequence for CPU Self-Test

1. Configure clock domain frequencies.
2. Select number of test intervals to be run.
3. Configure the timeout period for the self-test run.
4. Enable self-test.
5. Wait for CPU reset.
6. In the reset handler, read CPU self-test status to identify any failures.
7. Retrieve CPU state if required.

For more information see the device Technical Reference Manual.

6.5.6.2 CPU Self-Test Clock Configuration

The maximum clock rate for the self-test is HCLKmax/2. The STCCLK is divided down from the CPU clock. This divider is configured by the STCCLKDIV register at address 0xFFFFE108.

For more information see the device Technical Reference Manual.

6.5.6.3 CPU Self-Test Coverage

Table 6-7 shows CPU test coverage achieved for each self-test interval. It also lists the cumulative test cycles. The test time can be calculated by multiplying the number of test cycles with the STC clock period.

Table 6-7. CPU Self-Test Coverage

INTERVALS	TEST COVERAGE, %	STCCLK CYLCES
0	0	0
1	62.13	1365
2	70.09	2730
3	74.49	4095
4	77.28	5460
5	79.28	6825
6	80.90	8190
7	82.02	9555
8	83.10	10920
9	84.08	12285
10	84.87	13650
11	85.59	15015
12	86.11	16380
13	86.67	17745
14	87.16	19110
15	87.61	20475
16	87.98	21840
17	88.38	23205
18	88.69	24570
19	88.98	25935
20	89.28	27300
21	89.50	28665
22	89.76	30030
23	90.01	31395
24	90.21	32760

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6.6 Clocks

6.6.1 Clock Sources

The table below lists the available clock sources on the device. Each of the clock sources can be enabled or disabled using the CSDISx registers in the system module. The clock source number in the table corresponds to the control bit in the CSDISx register for that clock source.

The table also shows the default state of each clock source.

Table 6-8. Available Clock Sources

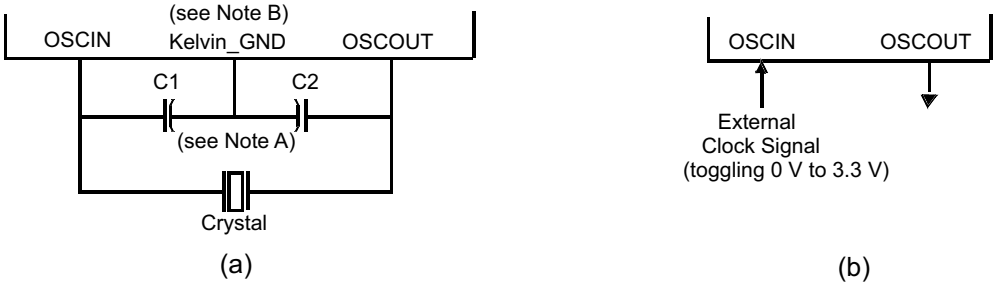
Clock Source #	Name	Description	Default State
0	OSCIN	Main Oscillator	Enabled
1	PLL1	Output From PLL1	Disabled
2	Reserved	Reserved	Disabled
3	EXTCLKIN1	External Clock Input #1	Disabled
4	LFLPO	Low Frequency Output of Internal Reference Oscillator	Enabled
5	HFLPO	High Frequency Output of Internal Reference Oscillator	Enabled
6	Reserved	Reserved	Disabled
7	EXTCLKIN2	External Clock Input #2	Disabled

6.6.1.1 Main Oscillator

The oscillator is enabled by connecting the appropriate fundamental resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 6-4. The oscillator is a single stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and low power modes.

TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 3.3V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in the figure below.



Note A: The values of C1 and C2 should be provided by the resonator/crystal vendor.
Note B: Kelvin_GND should not be connected to any other GND.

Figure 6-4. Recommended Crystal/Clock Connection

6.6.1.1.1 Timing Requirements for Main Oscillator

Table 6-9. Timing Requirements for Main Oscillator

Parameter		MIN	Type	MAX	Unit
tc(OSC)	Cycle time, OSCIN (when using a sine-wave input)	50		200	ns
tw(OSCIL)	Pulse duration, OSCIN low (when input to the OSCIN is a square wave)	15			ns
tw(OSCIH)	Pulse duration, OSCIN high (when input to the OSCIN is a square wave)	15			ns

6.6.1.2 Low Power Oscillator

The Low Power Oscillator (LPO) is comprised of two oscillators — HF LPO and LF LPO, in a single macro.

6.6.1.2.1 Features

The main features of the LPO are:

- Supplies a clock at extremely low power for power-saving modes. This is connected as clock source # 4 of the Global Clock Module.
- Supplies a high-frequency clock for non-timing-critical systems. This is connected as clock source # 5 of the Global Clock Module.
- Provides a comparison clock for the crystal oscillator failure detection circuit.

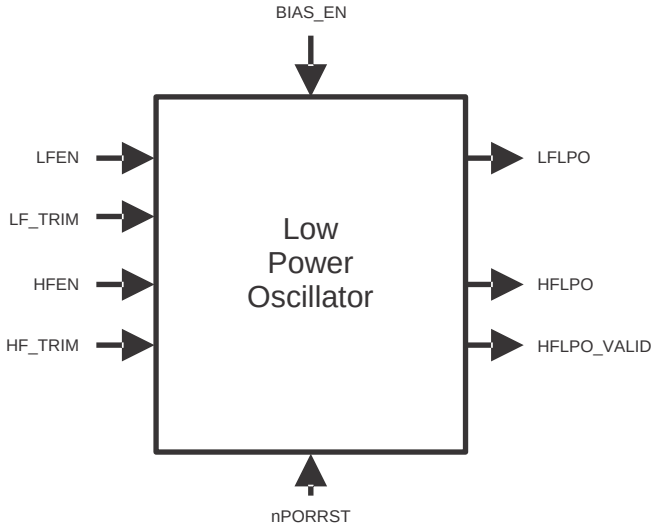


Figure 6-5. LPO Block Diagram

Figure 6-5 shows a block diagram of the internal reference oscillator. This is a low-power oscillator (LPO) and provides two clock sources: one nominally 80 KHz and one nominally 10 MHz.

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Table 6-10. LPO Specifications

PARAMETER		MIN	TYP	MAX	UNIT
Clock Detection	oscillator fail frequency - lower threshold, using untrimmed LPO output	1.375	2.4	4.875	MHz
	oscillator fail frequency - higher threshold, using untrimmed LPO output	22	38.4	78	MHz
LPO - HF oscillator	untrimmed frequency	5.5	9	19.5	MHz
	trimmed frequency	8	9.6	11	MHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900µs)			10	µs
	cold startup time			900	µs
LPO - LF oscillator	untrimmed frequency	36	85	180	kHz
	startup time from STANDBY (LPO BIAS_EN High for at least 900µs)			100	µs
	cold startup time			2000	µs

6.6.1.3 Phase Locked Loop (PLL) Clock Module

The PLL is used to multiply the input frequency to some higher frequency.

The main features of the PLL are:

- Frequency modulation can be optionally superimposed on the synthesized frequency of PLL1.
- Configurable frequency multipliers and dividers.
- Built-in PLL Slip monitoring circuit.
- Option to reset the device on a PLL slip detection.

6.6.1.3.1 Block Diagram

Figure 6-6 shows a high-level block diagram of the PLL macro on this microcontroller.

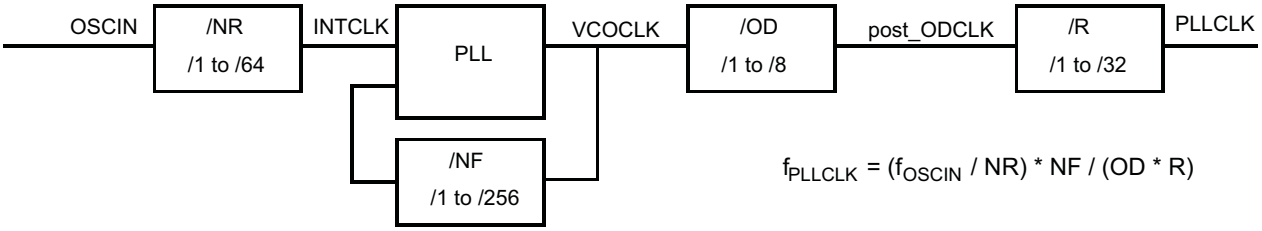


Figure 6-6. PLL Block Diagram

6.6.1.3.2 PLL Timing Specifications

Table 6-11. PLL Timing Specifications

PARAMETER		MIN	MAX	UNIT
f_{INTCLK}	PLL1 Reference Clock frequency	1	20	MHz
f_{post_ODCLK}	Post-ODCLK – PLL1 Post-divider input clock frequency		400	MHz
f_{VCOCLK}	VCOCLK – PLL1 Output Divider (OD) input clock frequency	150	550	MHz

6.6.1.4 External Clock Inputs

The device supports up to two external clock inputs. This clock input must be a square wave input. The electrical and timing requirements for these clock inputs are specified below. The external clock sources are not checked for validity. They are assumed valid when enabled.

Table 6-12. External Clock Timing and Electrical Specifications

Parameter	Description	Min	Max	Unit
$f_{EXTCLKx}$	External clock input frequency		80	MHz
$t_{w(EXTCLKIN)H}$	EXTCLK high-pulse duration	6		ns
$t_{w(EXTCLKIN)L}$	EXTCLK low-pulse duration	6		ns
$v_{iL(EXTCLKIN)}$	Low-level input voltage	-0.3	0.8	V
$v_{iH(EXTCLKIN)}$	High-level input voltage	2	VCCIO + 0.3	V

6.6.2 Clock Domains

6.6.2.1 Clock Domain Descriptions

The table below lists the device clock domains and their default clock sources. The table also shows the system module control register that is used to select an available clock source for each clock domain.

Table 6-13. Clock Domain Descriptions

Clock Domain Name	Default Clock Source	Clock Source Selection Register	Description
HCLK	OSCIN	GHVSRC	• Is disabled via the CDDISx registers bit 1 • Used for all system modules including DMA, ESM
GCLK	OSCIN	GHVSRC	• Always the same frequency as HCLK • In phase with HCLK • Is disabled separately from HCLK via the CDDISx registers bit 0 • Can be divided by 1up to 8 when running CPU self-test (LBIST) using the CLKDIV field of the STCCLKDIV register at address 0xFFFFE108
GCLK2	OSCIN	GHVSRC	• Always the same frequency as GCLK • 2 cycles delayed from GCLK • Is disabled along with GCLK • Gets divided by the same divider setting as that for GCLK when running CPU self-test (LBIST)
VCLK	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Is disabled separately from HCLK via the CDDISx registers bit 2
VCLK2	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Frequency must be an integer multiple of VCLK frequency • Is disabled separately from HCLK via the CDDISx registers bit 3
VCLK4	OSCIN	GHVSRC	• Divided down from HCLK • Can be HCLK/1, HCLK/2, ... or HCLK/16 • Is disabled separately from HCLK via the CDDISx registers bit 9
VCLKA1	VCLK	VCLKASRC	• Defaults to VCLK as the source • Is disabled via the CDDISx registers bit 4

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Table 6-13. Clock Domain Descriptions (continued)

Clock Domain Name	Default Clock Source	Clock Source Selection Register	Description
RTICLK	VCLK	RCLKSRC	• Defaults to VCLK as the source • If a clock source other than VCLK is selected for RTICLK, then the RTICLK frequency must be less than or equal to VCLK/3 – Application can ensure this by programming the RTI1DIV field of the RCLKSRC register, if necessary • Is disabled via the CDDISx registers bit 6

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6.6.2.2 Mapping of Clock Domains to Device Modules

Each clock domain has a dedicated functionality as shown in the figures below.

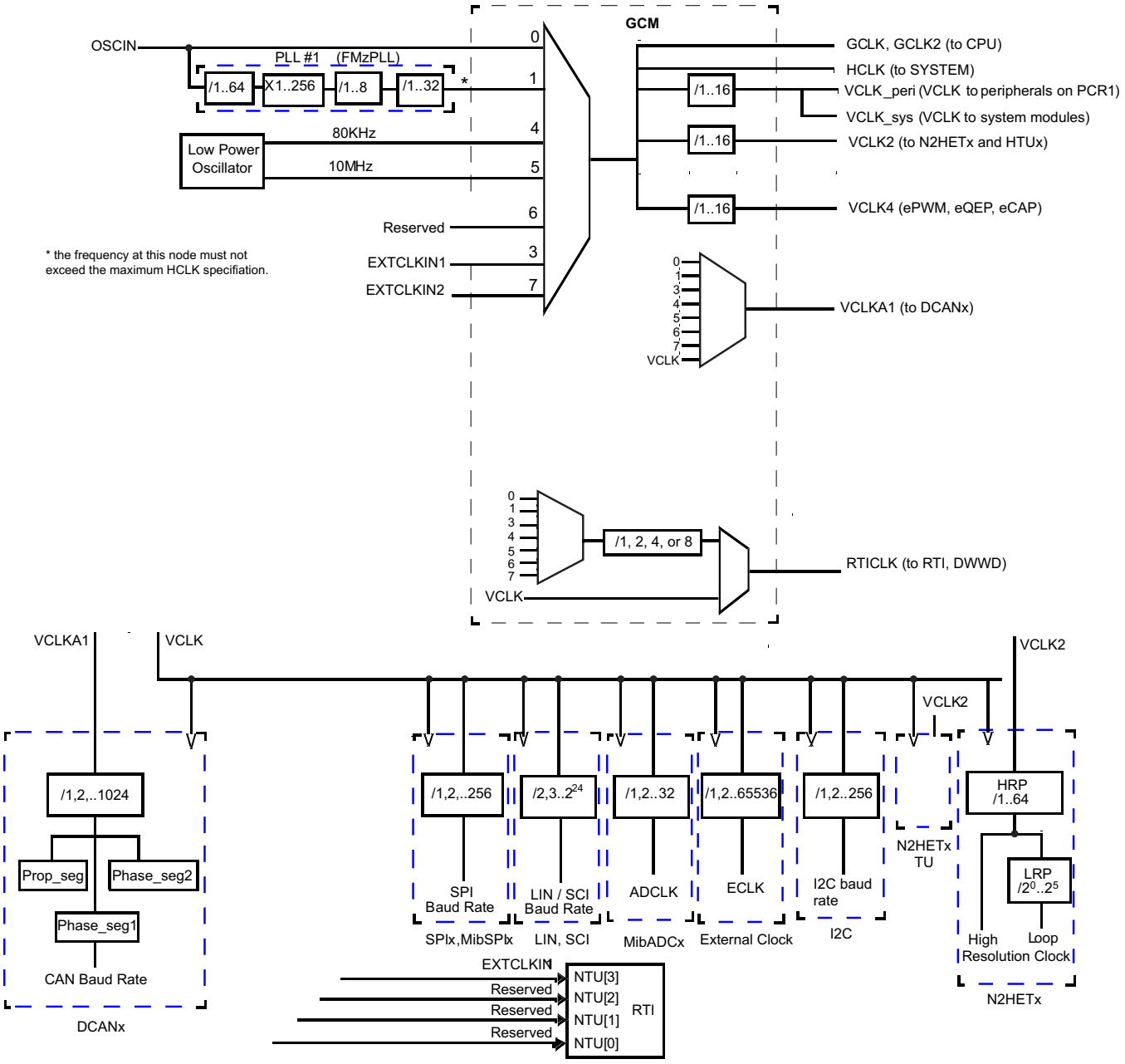


Figure 6-7. Device Clock Domains

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6.6.3 Clock Test Mode

The platform architecture defines a special mode that allows various clock signals to be brought out on to the ECLK pin and N2HET1[12] device outputs. This mode is called the Clock Test mode. It is very useful for debugging purposes and can be configured via the CLKTEST register in the system module.

Table 6-14. Clock Test Mode Options

SEL_ECP_PIN = CLKTEST[4-0]	SIGNAL ON ECLK		SEL_GIO_PIN = CLKTEST[11-8]	SIGNAL ON N2HET1[12]
00000	Oscillator		0000	Oscillator Valid Status
00001	Main PLL free-running clock output		0001	Main PLL Valid status
00010	Reserved		0010	Reserved
00011	EXTCLKIN1		0011	Reserved
00100	LFLPO		0100	Reserved
00101	HFLPO		0101	HFLPO Valid status
00110	Reserved		0110	Reserved
00111	EXTCLKIN2		0111	Reserved
01000	GCLK		1000	LFLPO
01001	RTI Base		1001	Oscillator Valid status
01010	Reserved		1010	Oscillator Valid status
01011	VCLKA1		1011	Oscillator Valid status
01100	VCLKA2		1100	Oscillator Valid status
01101	Reserved		1101	Reserved
01110	Reserved		1110	Reserved
01111	Reserved		1111	Oscillator Valid status
10000	Reserved			
10001	HCLK			
10010	VCLK			
10011	VCLK2			
10100	Reserved			
10101	VCLK4			
10110	Reserved			
10111	Reserved			
11000	Reserved			
Others	Reserved			

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6.7 Clock Monitoring

The LPO Clock Detect (LPOCLKDET) module consists of a clock monitor (CLKDET) and an internal low power oscillator (LPO).

The LPO provides two different clock sources – a low frequency (LFLPO) and a high frequency (HFLPO).

The CLKDET is a supervisor circuit for an externally supplied clock signal (OSCIN). In case the OSCIN frequency falls out of a frequency window, the CLKDET flags this condition in the global status register (GLBSTAT bit 0: OSC FAIL) and switches all clock domains sourced by OSCIN to the HFLPO clock (limp mode clock).

The valid OSCIN frequency range is defined as: $f_{HFLPO} / 4 < f_{OSCIN} < f_{HFLPO} * 4$.

6.7.1 Clock Monitor Timings

For more information on LPO and Clock detection, see the Table 6-10.

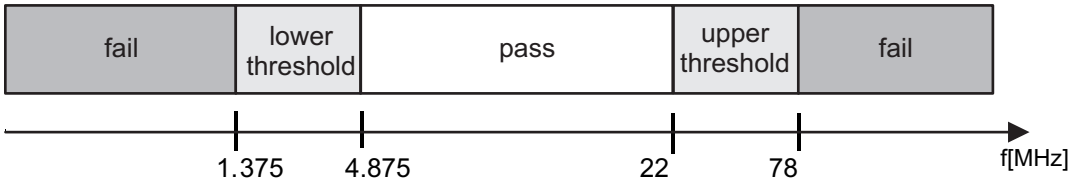


Figure 6-8. LPO and Clock Detection, Untrimmed HFLPO

6.7.2 External Clock (ECLK) Output Functionality

The ECLK pin can be configured to output a pre-scaled clock signal indicative of an internal device clock. This output can be externally monitored as a safety diagnostic.

6.7.3 Dual Clock Comparators

The Dual Clock Comparator (DCC) module determines the accuracy of selectable clock sources by counting the pulses of two independent clock sources (counter 0 and counter 1). If one clock is out of spec, an error signal is generated. For example, the DCC1 can be configured to use HFLPO as the reference clock (for counter 0) and VCLK as the "clock under test" (for counter 1). This configuration allows the DCC1 to monitor the PLL output clock when VCLK is using the PLL output as its source.

An additional use of this module is to measure the frequency of a selectable clock source, using the input clock as a reference, by counting the pulses of two independent clock sources. Counter 0 generates a fixed-width counting window after a preprogrammed number of pulses. Counter 1 generates a fixed-width pulse (1 cycle) after a pre-programmed number of pulses. This pulse sets as an error signal if counter 1 does not reach 0 within the counting window generated by counter 0.

6.7.3.1 Features

- Takes two different clock sources as input to two independent counter blocks.
- One of the clock sources is the known-good, or reference clock; the second clock source is the "clock under test."
- Each counter block is programmable with initial, or seed values.
- The counter blocks start counting down from their seed values at the same time; a mismatch from the expected frequency for the clock under test generates an error signal which is used to interrupt the CPU.

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6.7.3.2 Mapping of DCC Clock Source Inputs

Table 6-15. DCC1 Counter 0 Clock Sources

CLOCK SOURCE [3:0]	CLOCK NAME
others	oscillator (OSCIN)
0x5	high frequency LPO
0xA	test clock (TCK)

Table 6-16. DCC1 Counter 1 Clock Sources

KEY [3:0]	CLOCK SOURCE [3:0]	CLOCK NAME
others	-	N2HET1[31]
0xA	0x0	Main PLL free-running clock output
	0x1	Reserved
	0x2	low frequency LPO
	0x3	high frequency LPO
	0x4	reserved
	0x5	EXTCLKIN1
	0x6	EXTCLKIN2
	0x7	reserved
	0x8 - 0xF	VCLK

Table 6-17. DCC2 Counter 0 Clock Sources

CLOCK SOURCE [3:0]	CLOCK NAME
others	oscillator (OSCIN)
0xA	test clock (TCK)

Table 6-18. DCC2 Counter 1 Clock Sources

KEY [3:0]	CLOCK SOURCE [3:0]	CLOCK NAME
others	-	N2HET2[0]
0xA	00x0 - 0x7	Reserved
	0x8 - 0xF	VCLK

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6.8 Glitch Filters

A glitch filter is present on the following signals.

Table 6-19. Glitch Filter Timing Specifications

PIN	PARAMETER		MIN	MAX	UNIT
nPORRST	$t_{f(nPORRST)}$	Filter time nPORRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset(1)	475	2000	ns
nRST	$t_{f(nRST)}$	Filter time nRST pin; pulses less than MIN will be filtered out, pulses greater than MAX will generate a reset	475	2000	ns
TEST	$t_{f(TEST)}$	Filter time TEST pin; pulses less than MIN will be filtered out, pulses greater than MAX will pass through	475	2000	ns

(1) The glitch filter design on the nPORRST signal is designed such that no size pulse will reset any part of the microcontroller (flash pump, I/O pins, etc.) without also generating a valid reset signal to the CPU.

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6.9 Device Memory Map

6.9.1 Memory Map Diagram

The figure below shows the device memory map.

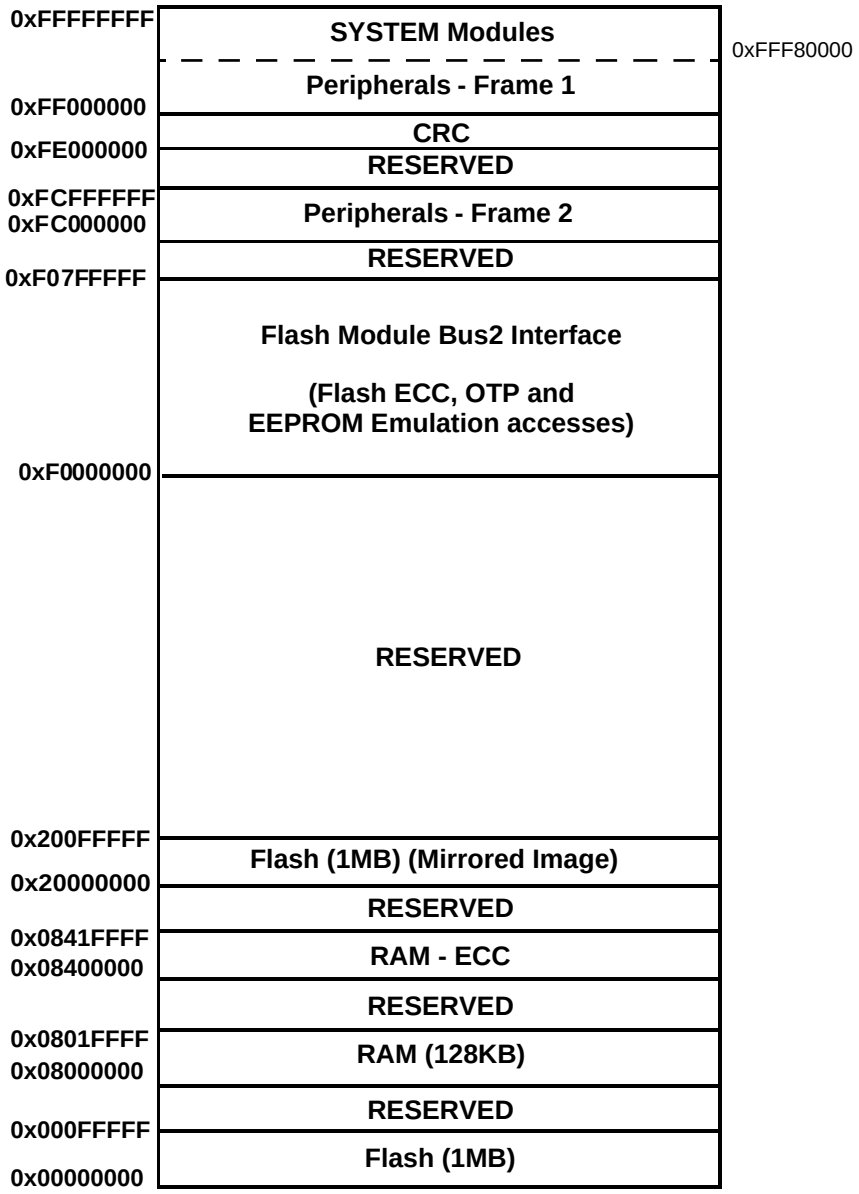


Figure 6-9. Memory Map

The Flash memory is mirrored to support ECC logic testing. The base address of the mirrored Flash image is 0x2000 0000.

6.9.2 Memory Map Table

See Figure 1-1 for block diagrams showing the devices interconnect.

Table 6-20. Device Memory Map

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
Memories tightly coupled to the ARM Cortex-R4F CPU						
TCM Flash	CS0	0x0000_0000	0x00FF_FFFF	16MB	1MB	Abort
TCM RAM + RAM ECC	CSRAM0	0x0800_0000	0x0BFF_FFFF	64MB	128KB	
Mirrored Flash	Flash mirror frame	0x2000_0000	0x20FF_FFFF	16MB	1MB	
Flash Module Bus2 Interface						
Customer OTP, TCM Flash Banks		0xF000_0000	0xF000_1FFF	8KB	4KB	Abort
Customer OTP, Bank 7		0xF000_E000	0xF000_FFFF	8KB	1KB	
Customer OTP–ECC, TCM Flash Banks		0xF004_0000	0xF004_03FF	1KB	512B	
Customer OTP–ECC, Bank 7		0xF004_1C00	0xF004_1FFF	1KB	128B	
TI OTP, TCM Flash Banks		0xF008_0000	0xF008_1FFF	8KB	4KB	
TI OTP, Bank 7		0xF008_E000	0xF008_FFFF	8KB	1KB	
TI OTP–ECC, TCM Flash Banks		0xF00C_0000	0xF00C_03FF	1KB	512B	
TI OTP–ECC, Bank 7		0xF00C_1C00	0xF00C_1FFF	1KB	128B	
Bank 7 – ECC		0xF010_0000	0xF013_FFFF	256KB	8KB	
Bank 7		0xF020_0000	0xF03F_FFFF	2MB	64KB	
Flash Data Space ECC		0xF040_0000	0xF04F_FFFF	1MB	128KB	
SCR5: Enhanced Timer Peripherals						
ePWM1		0xFCF7_8C00	0xFCF7_8CFF	256B	256B	Abort
ePWM2		0xFCF7_8D00	0xFCF7_8DFF	256B	256B	Abort
ePWM3		0xFCF7_8E00	0xFCF7_8EFF	256B	256B	Abort
ePWM4		0xFCF7_8F00	0xFCF7_8FFF	256B	256B	Abort
ePWM5		0xFCF7_9000	0xFCF7_90FF	256B	256B	Abort
ePWM6		0xFCF7_9100	0xFCF7_91FF	256B	256B	Abort
ePWM7		0xFCF7_9200	0xFCF7_92FF	256B	256B	Abort
eCAP1		0xFCF7_9300	0xFCF7_93FF	256B	256B	Abort
eCAP2		0xFCF7_9400	0xFCF7_94FF	256B	256B	Abort
eCAP3		0xFCF7_9500	0xFCF7_95FF	256B	256B	Abort
eCAP4		0xFCF7_9600	0xFCF7_96FF	256B	256B	Abort
eCAP5		0xFCF7_9700	0xFCF7_97FF	256B	256B	Abort
eCAP6		0xFCF7_9800	0xFCF7_98FF	256B	256B	Abort
eQEP1		0xFCF7_9900	0xFCF7_99FF	256B	256B	Abort
eQEP2		0xFCF7_9A00	0xFCF7_9AFF	256B	256B	Abort
Cyclic Redundancy Checker (CRC) Module Registers						
CRC	CRC frame	0xFE00_0000	0xFEFF_FFFF	16MB	512B	Accesses above 0x200 generate abort.
Peripheral Memories						
MIBSPI5 RAM	PCS[5]	0xFF0A_0000	0xFF0B_FFFF	128KB	2KB	Abort for accesses above 2KB
MIBSPI3 RAM	PCS[6]	0xFF0C_0000	0xFF0D_FFFF	128KB	2KB	Abort for accesses above 2KB
MIBSPI1 RAM	PCS[7]	0xFF0E_0000	0xFF0F_FFFF	128KB	2KB	Abort for accesses above 2KB
DCAN3 RAM	PCS[13]	0xFF1A_0000	0xFF1B_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.

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Table 6-20. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
DCAN2 RAM	PCS[14]	0xFF1C_0000	0xFF1D_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
DCAN1 RAM	PCS[15]	0xFF1E_0000	0xFF1F_FFFF	128KB	2KB	Wrap around for accesses to unimplemented address offsets lower than 0x7FF. Abort generated for accesses beyond offset 0x800.
MIBADC2 RAM	PCS[29]	0xFF3A_0000	0xFF3B_FFFF	128KB	8KB	Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF.
MIBADC2 Look-Up Table					384B	Look-Up Table for ADC2 wrapper. Starts at address offset 0x2000 and ends at address offset 0x217F. Wrap around for accesses between offsets 0x0180 and 0x3FFF. Abort generated for accesses beyond offset 0x4000.
MIBADC1 RAM	PCS[31]	0xFF3E_0000	0xFF3F_FFFF	128KB	8KB	Wrap around for accesses to unimplemented address offsets lower than 0x1FFF. Abort generated for accesses beyond 0x1FFF.
MibADC1 Look-Up Table					384B	Look-Up Table for ADC1 wrapper. Starts at address offset 0x2000 and ends at address offset 0x217F. Wrap around for accesses between offsets 0x0180 and 0x3FFF. Abort generated for accesses beyond offset 0x4000.
N2HET2 RAM	PCS[34]	0xFF44_0000	0xFF45_FFFF	128KB	16KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF.
N2HET1 RAM	PCS[35]	0xFF46_0000	0xFF47_FFFF	128KB	16KB	Wrap around for accesses to unimplemented address offsets lower than 0x3FFF. Abort generated for accesses beyond 0x3FFF.
N2HET2 TU2 RAM	PCS[38]	0xFF4C_0000	0xFF4D_FFFF	128KB	1KB	Abort
N2HET1 TU1 RAM	PCS[39]	0xFF4E_0000	0xFF4F_FFFF	128KB	1KB	Abort
Debug Components						
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4F Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect
Peripheral Control Registers						
HTU1	PS[22]	0xFFF7_A400	0xFFF7_A4FF	256B	256B	Reads return zeros, writes have no effect
HTU2	PS[22]	0xFFF7_A500	0xFFF7_A5FF	256B	256B	Reads return zeros, writes have no effect
N2HET1	PS[17]	0xFFF7_B800	0xFFF7_B8FF	256B	256B	Reads return zeros, writes have no effect
N2HET2	PS[17]	0xFFF7_B900	0xFFF7_B9FF	256B	256B	Reads return zeros, writes have no effect
GIO	PS[16]	0xFFF7_BC00	0xFFF7_BDFF	512B	256B	Reads return zeros, writes have no effect
MIBADC1	PS[15]	0xFFF7_C000	0xFFF7_C1FF	512B	512B	Reads return zeros, writes have no effect
MIBADC2	PS[15]	0xFFF7_C200	0xFFF7_C3FF	512B	512B	Reads return zeros, writes have no effect
I2C	PS[10]	0xFFF7_D400	0xFFF7_D4FF	256B	256B	Reads return zeros, writes have no effect
DCAN1	PS[8]	0xFFF7_DC00	0xFFF7_DDFF	512B	512B	Reads return zeros, writes have no effect
DCAN2	PS[8]	0xFFF7_DE00	0xFFF7_DFFF	512B	512B	Reads return zeros, writes have no effect
DCAN3	PS[7]	0xFFF7_E000	0xFFF7_E1FF	512B	512B	Reads return zeros, writes have no effect
LIN	PS[6]	0xFFF7_E400	0xFFF7_E4FF	256B	256B	Reads return zeros, writes have no effect
SCI	PS[6]	0xFFF7_E500	0xFFF7_E5FF	256B	256B	Reads return zeros, writes have no effect
MibSPI1	PS[2]	0xFFF7_F400	0xFFF7_F5FF	512B	512B	Reads return zeros, writes have no effect
SPI2	PS[2]	0xFFF7_F600	0xFFF7_F7FF	512B	512B	Reads return zeros, writes have no effect
MibSPI3	PS[1]	0xFFF7_F800	0xFFF7_F9FF	512B	512B	Reads return zeros, writes have no effect
SPI4	PS[1]	0xFFF7_FA00	0xFFF7_FBFF	512B	512B	Reads return zeros, writes have no effect
MibSPI5	PS[0]	0xFFF7_FC00	0xFFF7_FDFF	512B	512B	Reads return zeros, writes have no effect

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Table 6-20. Device Memory Map (continued)

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPONSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
System Modules Control Registers and Memories						
DMA RAM	PPCS0	0xFFF8_0000	0xFFF8_0FFF	4KB	4KB	Abort
VIM RAM	PPCS2	0xFFF8_2000	0xFFF8_2FFF	4KB	1KB	Wrap around for accesses to unimplemented address offsets between 1KB and 4KB.
Flash Module	PPCS7	0xFFF8_7000	0xFFF8_7FFF	4KB	4KB	Abort
eFuse Controller	PPCS12	0xFFF8_C000	0xFFF8_CFFF	4KB	4KB	Abort
Power Management Module (PMM)	PPSE0	0xFFFF_0000	0xFFFF_01FF	512B	512B	Abort
PCR registers	PPS0	0xFFFF_E000	0xFFFF_E0FF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 2 (see device TRM)	PPS0	0xFFFF_E100	0xFFFF_E1FF	256B	256B	Reads return zeros, writes have no effect
PBIST	PPS1	0xFFFF_E400	0xFFFF_E5FF	512B	512B	Reads return zeros, writes have no effect
STC	PPS1	0xFFFF_E600	0xFFFF_E6FF	256B	256B	Generates address error interrupt, if enabled
IOMM Multiplexing Control Module	PPS2	0xFFFF_EA00	0xFFFF_EBFF	512B	512B	Reads return zeros, writes have no effect
DCC1	PPS3	0xFFFF_EC00	0xFFFF_ECFF	256B	256B	Reads return zeros, writes have no effect
DMA	PPS4	0xFFFF_F000	0xFFFF_F3FF	1KB	1KB	Reads return zeros, writes have no effect
DCC2	PPS5	0xFFFF_F400	0xFFFF_F4FF	256B	256B	Reads return zeros, writes have no effect
ESM	PPS5	0xFFFF_F500	0xFFFF_F5FF	256B	256B	Reads return zeros, writes have no effect
CCMR4	PPS5	0xFFFF_F600	0xFFFF_F6FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC even	PPS6	0xFFFF_F800	0xFFFF_F8FF	256B	256B	Reads return zeros, writes have no effect
RAM ECC odd	PPS6	0xFFFF_F900	0xFFFF_F9FF	256B	256B	Reads return zeros, writes have no effect
RTI + DWWD	PPS7	0xFFFF_FC00	0xFFFF_FCFF	256B	256B	Reads return zeros, writes have no effect
VIM Parity	PPS7	0xFFFF_FD00	0xFFFF_FDFF	256B	256B	Reads return zeros, writes have no effect
VIM	PPS7	0xFFFF_FE00	0xFFFF_FEFF	256B	256B	Reads return zeros, writes have no effect
System Module - Frame 1 (see device TRM)	PPS7	0xFFFF_FF00	0xFFFF_FFFF	256B	256B	Reads return zeros, writes have no effect

6.9.3 Special Consideration for CPU Access Errors Resulting in Imprecise Aborts

Any CPU write access to a Normal or Device type memory, which generates a fault, will generate an imprecise abort. The imprecise abort exception is disabled by default and must be enabled for the CPU to handle this exception. The imprecise abort handling is enabled by clearing the "A" bit in the CPU's program status register (CPSR).

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6.9.4 Master/Slave Access Privileges

The table below lists the access permissions for each bus master on the device. A bus master is a module that can initiate a read or a write transaction on the device.

Each slave module on the main interconnect is listed in the table. A "Yes" indicates that the module listed in the "MASTERS" column can access that slave module.

Table 6-21. Master / Slave Access Matrix

MASTERS	ACCESS MODE	SLAVES ON MAIN SCR				
		Flash Module Bus2 Interface: OTP, ECC, Bank 7	Non-CPU Accesses to Program Flash and CPU Data RAM	CRC	Slave Interfaces	Peripheral Control Registers, All Peripheral Memories, And All System Module Control Registers And Memories
CPU READ	User/Privilege	Yes	Yes	Yes	Yes	Yes
CPU WRITE	User/Privilege	**No**	Yes	Yes	Yes	Yes
DMA	User	Yes	Yes	Yes	Yes	Yes
DAP	Privilege	Yes	Yes	Yes	Yes	Yes
HTU1	Privilege	**No**	Yes	Yes	Yes	Yes
HTU2	Privilege	**No**	Yes	Yes	Yes	Yes

6.9.5 Special Notes on Accesses to Certain Slaves

Write accesses to the Power Domain Management Module (PMM) control registers are limited to the CPU (master id = 1). The other masters can only read from these registers.

A debugger can also write to the PMM registers. The master-id check is disabled in debug mode.

The device contains dedicated logic to generate a bus error response on any access to a module that is in a power domain that has been turned OFF.

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6.10 Flash Memory

6.10.1 Flash Memory Configuration

Flash Bank: A separate block of logic consisting of 1 to 16 sectors. Each flash bank normally has a customer-OTP and a TI-OTP area. These flash sectors share input/output buffers, data paths, sense amplifiers, and control logic.

Flash Sector: A contiguous region of flash memory which must be erased simultaneously due to physical construction constraints.

Flash Pump: A charge pump which generates all the voltages required for reading, programming, or erasing the flash banks.

Flash Module: Interface circuitry required between the host CPU and the flash banks and pump module.

Table 6-22. Flash Memory Banks and Sectors

Memory Arrays (or Banks)	Sector No.	Segment	Low Address	High Address
BANK0 (1MBytes)(1)	0	16K Bytes	0x0000_0000	0x0000_3FFF
	1	16K Bytes	0x0000_4000	0x0000_7FFF
	2	16K Bytes	0x0000_8000	0x0000_BFFF
	3	16K Bytes	0x0000_C000	0x0000_FFFF
	4	16K Bytes	0x0001_0000	0x0001_3FFF
	5	16K Bytes	0x0001_4000	0x0001_7FFF
	6	32K Bytes	0x0001_8000	0x0001_FFFF
	7	128K Bytes	0x0002_0000	0x0003_FFFF
	8	128K Bytes	0x0004_0000	0x0005_FFFF
	9	128K Bytes	0x0006_0000	0x0007_FFFF
	10	128K Bytes	0x0008_0000	0x0009_FFFF
	11	128K Bytes	0x000A_0000	0x000B_FFFF
	12	128K Bytes	0x000C_0000	0x000D_FFFF
	13	128K Bytes	0x000E_0000	0x000F_FFFF
BANK7 (64KBytes) for EEPROM emulation(2)(3)(4)	0	4K Bytes	0xF020_0000	0xF020_0FFF
	1	4K Bytes	0xF020_1000	0xF020_1FFF
	2	4K Bytes	0xF020_2000	0xF020_2FFF
	3	4K Bytes	0xF020_3000	0xF020_3FFF
	4	4K Bytes	0xF020_4000	0xF020_4FFF
	5	4K Bytes	0xF020_5000	0xF020_5FFF
	6	4K Bytes	0xF020_6000	0xF020_6FFF
	7	4K Bytes	0xF020_7000	0xF020_7FFF
	8	4K Bytes	0xF020_8000	0xF020_8FFF
	9	4K Bytes	0xF020_9000	0xF020_9FFF
	10	4K Bytes	0xF020_A000	0xF020_AFFF
	11	4K Bytes	0xF020_B000	0xF020_BFFF
	12	4K Bytes	0xF020_C000	0xF020_CFFF
	13	4K Bytes	0xF020_D000	0xF020_DFFF
	14	4K Bytes	0xF020_E000	0xF020_EFFF
	15	4K Bytes	0xF020_F000	0xF020_FFFF

(1) Flash bank0 is a 144-bit-wide bank with ECC support.
(2) Flash bank7 is a 72-bit-wide bank with ECC support.
(3) The flash bank7 can be programmed while executing code from flash bank0.
(4) Code execution is not allowed from flash bank7.

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6.10.2 Main Features of Flash Module

- Support for multiple flash banks for program and/or data storage
- Simultaneous read access on a bank while performing program or erase operation on any other bank
- Integrated state machines to automate flash erase and program operations
- Pipelined mode operation to improve instruction access interface bandwidth
- Support for Single Error Correction Double Error Detection (SECDED) block inside Cortex-R4F CPU
  - Error address is captured for host system debugging
- Support for a rich set of diagnostic features

6.10.3 ECC Protection for Flash Accesses

All accesses to the program flash memory are protected by Single Error Correction Double Error Detection (SECDED) logic embedded inside the CPU. The flash module provides 8 bits of ECC code for 64 bits of instructions or data fetched from the flash memory. The CPU calculates the expected ECC code based on the 64 bits received and compares it with the ECC code returned by the flash module. A single-bit error is corrected and flagged by the CPU, while a multi-bit error is only flagged. The CPU signals an ECC error via its Event bus. This signaling mechanism is not enabled by default and must be enabled by setting the "X" bit of the Performance Monitor Control Register, c9.

```
MRC p15,#0,r1,c9,c12,#0    ;Enabling Event monitor states
ORR r1, r1, #0x00000010
MCR p15,#0,r1,c9,c12,#0    ;Set 4th bit (‘X’) of PMNC register
MRC p15,#0,r1,c9,c12,#0
```

The application must also explicitly enable the CPU's ECC checking for accesses on the CPU's ATCM and BTCM interfaces. These are connected to the program flash and data RAM respectively. ECC checking for these interfaces can be done by setting the B1TCMPCEN, B0TCMPCEN and ATCMPCEN bits of the System Control coprocessor's Auxiliary Control Register, c1.

```
MRC p15, #0, r1, c1, c0, #1
ORR r1, r1, #0x0e000000        ;Enable ECC checking for ATCM and BTCMs
DMB
MCR p15, #0, r1, c1, c0, #1
```

6.10.4 Flash Access Speeds

For information on flash memory access speeds and the relevant wait states required, see Section 5.8.1.2.

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6.10.5 Program Flash

Table 6-23. Timing Requirements for Program Flash

PARAMETER			MIN	NOM	MAX	UNIT
$t_{prog(144bit)}$	Wide Word (144bit) programming time			40	300	µs
$t_{prog(Total)}$	1MByte programming time(1)	-40°C to 125°C			11	s
		0°C to 60°C, for first 25 cycles		2.8	5.5	s
$t_{erase(bank0)}$	Sector/Bank erase time(2)	-40°C to 125°C		0.03	4	s
		0°C to 60°C, for first 25 cycles		16	100	ms
t_{wec}	Write/erase cycles with 15 year Data Retention requirement	-40°C to 125°C			1000	cycles

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 144 bits at a time at the maximum specified operating frequency.
(2) During bank erase, the selected sectors are erased simultaneously. The time to erase the bank is specified as equal to the time to erase a sector.

6.10.6 Data Flash

Table 6-24. Timing Requirements for Data Flash

Parameter			MIN	NOM	MAX	Unit
$t_{prog(144bit)}$	Wide Word (72bit) programming time			47	310	µs
$t_{prog(Total)}$	EEPROM Emulation (bank 7) 64KByte programming time(1)	-40°C to 125°C			2.6	s
		0°C to 60°C, for first 25 cycles		775	1435	ms
$t_{erase(bank7)}$	Sector/Bank erase time, EEPROM Emulation (bank 7)	-40°C to 125°C		0.2	8	s
		0°C to 60°C, for first 25 cycles		14	100	ms
t_{wec}	Write/erase cycles with 15 year Data Retention requirement	-40°C to 125°C			100000	cycles

(1) This programming time includes overhead of state machine, but does not include data transfer time. The programming time assumes programming 72 bits at a time at the maximum specified operating frequency.

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6.11 Tightly-Coupled RAM Interface Module

Figure 6-10 illustrates the connection of the Tightly Coupled RAM (TCRAM) to the Cortex-R4F™ CPU.

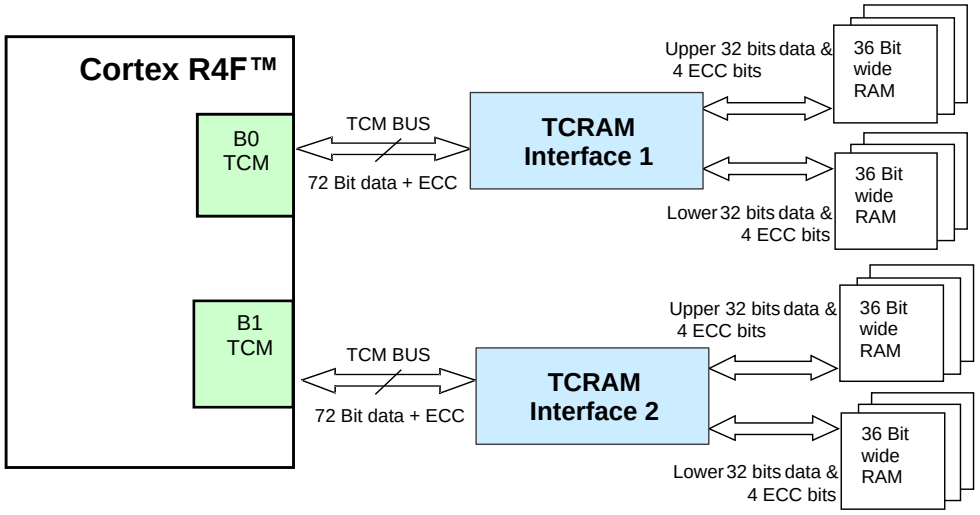


Figure 6-10. TCRAM Block Diagram

6.11.1 Features

The features of the Tightly Coupled RAM (TCRAM) Module are:

- Acts as slave to the Cortex-R4F CPU's BTCM interface
- Supports CPU's internal ECC scheme by providing 64-bit data and 8-bit ECC code
- Monitors CPU Event Bus and generates single or multi-bit error interrupts
- Stores addresses for single and multi-bit errors
- Supports RAM trace module
- Provides CPU address bus integrity checking by supporting parity checking on the address bus
- Performs redundant address decoding for the RAM bank chip select and ECC select generation logic
- Provides enhanced safety for the RAM addressing by implementing two 36-bit wide byte-interleaved RAM banks and generating independent RAM access control signals to the two banks
- Supports auto-initialization of the RAM banks along with the ECC bits

6.11.2 TCRAMW ECC Support

The TCRAMW passes on the ECC code for each data read by the Cortex-R4F CPU from the RAM. It also stores the CPU's ECC port contents in the ECC RAM when the CPU does a write to the RAM. The TCRAMW monitors the CPU's event bus and provides registers for indicating single/multi-bit errors and also for identifying the address that caused the single or multi-bit error. The event signaling and the ECC checking for the RAM accesses must be enabled inside the CPU.

For more information see the device Technical Reference Manual.

6.12 Parity Protection for Accesses to peripheral RAMs

Accesses to some peripheral RAMs are protected by odd/even parity checking. During a read access the parity is calculated based on the data read from the peripheral RAM and compared with the good parity value stored in the parity RAM for that peripheral. If any word fails the parity check, the module generates a parity error signal that is mapped to the Error Signaling Module. The module also captures the peripheral RAM address that caused the parity error.

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The parity protection for peripheral RAMs is not enabled by default and must be enabled by the application. Each individual peripheral contains control registers to enable the parity protection for accesses to its RAM.

NOTE

The CPU read access gets the actual data from the peripheral. The application can choose to generate an interrupt whenever a peripheral RAM parity error is detected.

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6.13 On-Chip SRAM Initialization and Testing

6.13.1 On-Chip SRAM Self-Test Using PBIST

6.13.1.1 Features

- Extensive instruction set to support various memory test algorithms
- ROM-based algorithms allow application to run TI production-level memory tests
- Independent testing of all on-chip SRAM

6.13.1.2 PBIST RAM Groups

Table 6-25. PBIST RAM Grouping

Memory	RAM Group	Test Clock	MEM Type	Test Pattern (Algorithm)			
				triple read slow read	triple read fast read	March 13N(1) two port (cycles)	March 13N(1) single port (cycles)
				ALGO MASK 0x1	ALGO MASK 0x2	ALGO MASK 0x4	ALGO MASK 0x8
PBIST_ROM	1	ROM CLK	ROM	24578	8194		
STC_ROM	2	ROM CLK	ROM	19586	6530		
DCAN1	3	VCLK	Dual Port			25200	
DCAN2	4	VCLK	Dual Port			25200	
DCAN3	5	VCLK	Dual Port			25200	
ESRAM1(2)	6	HCLK	Single Port				266280
MIBSPI1	7	VCLK	Dual Port			33440	
MIBSPI3	8	VCLK	Dual Port			33440	
MIBSPI5	9	VCLK	Dual Port			33440	
VIM	10	VCLK	Dual Port			12560	
MIBADC1	11	VCLK	Dual Port			4200	
DMA	12	HCLK	Dual Port			18960	
N2HET1	13	VCLK	Dual Port			31680	
HET TU1	14	VCLK	Dual Port			6480	
MIBADC2	18	VCLK	Dual Port			4200	
N2HET2	19	VCLK	Dual Port			31680	
HET TU2	20	VCLK	Dual Port			6480	
ESRAM5(3)	21	HCLK	Single Port				266280

(1) There are several memory testing algorithms stored in the PBIST ROM. However, TI recommends the March13N algorithm for application testing.
(2) ESRAM1: Address 0x08000000 - 0x0800FFFF
(3) ESRAM5: Address 0x08010000 - 0x0801FFFF

The PBIST ROM clock frequency is limited to 100MHz, if 100MHz < HCLK <= HCLKmax, or HCLK, if HCLK <= 100MHz.

The PBIST ROM clock is divided down from HCLK. The divider is selected by programming the ROM_DIV field of the Memory Self-Test Global Control Register (MSTGCR) at address 0xFFFFFF58.

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6.13.2 On-Chip SRAM Auto Initialization

This microcontroller allows some of the on-chip memories to be initialized via the Memory Hardware Initialization mechanism in the System module. This hardware mechanism allows an application to program the memory arrays with error detection capability to a known state based on their error detection scheme (odd/even parity or ECC).

The MINITGCR register enables the memory initialization sequence, and the MSINENA register selects the memories that are to be initialized.

For more information on these registers see the device Technical Reference Manual.

The mapping of the different on-chip memories to the specific bits of the MSINENA registers is shown in Table 6-26.

Table 6-26. Memory Initialization

CONNECTING MODULE	ADDRESS RANGE		MSINENA REGISTER BIT #
	BASE ADDRESS	ENDING ADDRESS	
RAM (PD#1)	0x08000000	0x0800FFFF	0 (1)
RAM (RAM_PD#1)	0x08010000	0x0801FFFF	0 (1)
MIBSPI5 RAM	0xFF0A0000	0xFF0BFFFF	12 (2)
MIBSPI3 RAM	0xFF0C0000	0xFF0DFFFF	11 (2)
MIBSPI1 RAM	0xFF0E0000	0xFF0FFFFF	7 (2)
DCAN3 RAM	0xFF1A0000	0xFF1BFFFF	10
DCAN2 RAM	0xFF1C0000	0xFF1DFFFF	6
DCAN1 RAM	0xFF1E0000	0xFF1FFFFF	5
MIBADC2 RAM	0xFF3A0000	0xFF3BFFFF	14
MIBADC1 RAM	0xFF3E0000	0xFF3FFFFF	8
N2HET2 RAM	0xFF440000	0xFF45FFFF	15
N2HET1 RAM	0xFF460000	0xFF47FFFF	3
HET TU2 RAM	0xFF4C0000	0xFF4DFFFF	16
HET TU1 RAM	0xFF4E0000	0xFF4FFFFF	4
DMA RAM	0xFFF80000	0xFFF80FFF	1
VIM RAM	0xFFF82000	0xFFF82FFF	2

(1) The TCM RAM wrapper has separate control bits to select the RAM power domain that is to be auto-initialized.
(2) The MibSPIx modules perform an initialization of the transmit and receive RAMs as soon as the module is released from its local reset.. This is independent of whether the application chooses to initialize the MibSPIx RAMs using the system module auto-initialization method. The MibSPIx module must be first brought out of its local reset in order to use the system module auto-initialization method.

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6.14 Vectored Interrupt Manager

The vectored interrupt manager (VIM) provides hardware assistance for prioritizing and controlling the many interrupt sources present on this device. Interrupts are caused by events outside of the normal flow of program execution. Normally, these events require a timely response from the central processing unit (CPU); therefore, when an interrupt occurs, the CPU switches execution from the normal program flow to an interrupt service routine (ISR).

6.14.1 VIM Features

The VIM module has the following features:

- Supports 128 interrupt channels.
  - Provides programmable priority and enable for interrupt request lines.
- Provides a direct hardware dispatch mechanism for fastest IRQ dispatch.
- Provides two software dispatch mechanisms when the CPU VIC port is not used.
  - Index interrupt
  - Register vectored interrupt
- Parity protected vector interrupt table against soft errors.

6.14.2 Interrupt Request Assignments

Table 6-27. Interrupt Request Assignments

Modules	Interrupt Sources	Default VIM Interrupt Channel
ESM	ESM High level interrupt (NMI)	0
Reserved	Reserved	1
RTI	RTI compare interrupt 0	2
RTI	RTI compare interrupt 1	3
RTI	RTI compare interrupt 2	4
RTI	RTI compare interrupt 3	5
RTI	RTI overflow interrupt 0	6
RTI	RTI overflow interrupt 1	7
RTI	RTI timebase interrupt	8
GIO	GIO interrupt A	9
N2HET1	N2HET1 level 0 interrupt	10
HET TU1	HET TU1 level 0 interrupt	11
MIBSPI1	MIBSPI1 level 0 interrupt	12
LIN	LIN level 0 interrupt	13
MIBADC1	MIBADC1 event group interrupt	14
MIBADC1	MIBADC1 sw group 1 interrupt	15
DCAN1	DCAN1 level 0 interrupt	16
SPI2	SPI2 level 0 interrupt	17
Reserved	Reserved	18
CRC	CRC Interrupt	19
ESM	ESM Low level interrupt	20
SYSTEM	Software interrupt (SSI)	21
CPU	PMU Interrupt	22
GIO	GIO interrupt B	23
N2HET1	N2HET1 level 1 interrupt	24
HET TU1	HET TU1 level 1 interrupt	25
MIBSPI1	MIBSPI1 level 1 interrupt	26

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Table 6-27. Interrupt Request Assignments (continued)

Modules	Interrupt Sources	Default VIM Interrupt Channel
LIN	LIN level 1 interrupt	27
MIBADC1	MIBADC1 sw group 2 interrupt	28
DCAN1	DCAN1 level 1 interrupt	29
SPI2	SPI2 level 1 interrupt	30
MIBADC1	MIBADC1 magnitude compare interrupt	31
Reserved	Reserved	32
DMA	FTCA interrupt	33
DMA	LFSA interrupt	34
DCAN2	DCAN2 level 0 interrupt	35
MIBSPI3	MIBSPI3 level 0 interrupt	37
MIBSPI3	MIBSPI3 level 1 interrupt	38
DMA	HBCA interrupt	39
DMA	BTCA interrupt	40
Reserved	Reserved	41
DCAN2	DCAN2 level 1 interrupt	42
DCAN1	DCAN1 IF3 interrupt	44
DCAN3	DCAN3 level 0 interrupt	45
DCAN2	DCAN2 IF3 interrupt	46
FPU	FPU interrupt	47
Reserved	Reserved	48
SPI4	SPI4 level 0 interrupt	49
MIBADC2	MibADC2 event group interrupt	50
MIBADC2	MibADC2 sw group1 interrupt	51
Reserved	Reserved	52
MIBSPI5	MIBSPI5 level 0 interrupt	53
SPI4	SPI4 level 1 interrupt	54
DCAN3	DCAN3 level 1 interrupt	55
MIBSPI5	MIBSPI5 level 1 interrupt	56
MIBADC2	MibADC2 sw group2 interrupt	57
Reserved	Reserved	58
MIBADC2	MibADC2 magnitude compare interrupt	59
DCAN3	DCAN3 IF3 interrupt	60
FMC	FSM_DONE interrupt	61
Reserved	Reserved	62
N2HET2	N2HET2 level 0 interrupt	63
SCI	SCI level 0 interrupt	64
HET TU2	HET TU2 level 0 interrupt	65
I2C	I2C level 0 interrupt	66
Reserved	Reserved	67-72
N2HET2	N2HET2 level 1 interrupt	73
SCI	SCI level 1 interrupt	74
HET TU2	HET TU2 level 1 interrupt	75
Reserved	Reserved	76-79
HWAG1	HWA_INT_REQ_H	80
HWAG2	HWA_INT_REQ_H	81
DCC1	DCC done interrupt	82
DCC2	DCC2 done interrupt	83

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Table 6-27. Interrupt Request Assignments (continued)

Modules	Interrupt Sources	Default VIM Interrupt Channel
Reserved	Reserved	84
PBIST Controller	PBIST Done Interrupt	85
Reserved	Reserved	86-87
HWAG1	HWA_INT_REQ_L	88
HWAG2	HWA_INT_REQ_L	89
ePWM1INTn	ePWM1 Interrupt	90
ePWM1TZINTn	ePWM1 Trip Zone Interrupt	91
ePWM2INTn	ePWM2 Interrupt	92
ePWM2TZINTn	ePWM2 Trip Zone Interrupt	93
ePWM3INTn	ePWM3 Interrupt	94
ePWM3TZINTn	ePWM3 Trip Zone Interrupt	95
ePWM4INTn	ePWM4 Interrupt	96
ePWM4TZINTn	ePWM4 Trip Zone Interrupt	97
ePWM5INTn	ePWM5 Interrupt	98
ePWM5TZINTn	ePWM5 Trip Zone Interrupt	99
ePWM6INTn	ePWM6 Interrupt	100
ePWM6TZINTn	ePWM6 Trip Zone Interrupt	101
ePWM7INTn	ePWM7 Interrupt	102
ePWM7TZINTn	ePWM7 Trip Zone Interrupt	103
eCAP1INTn	eCAP1 Interrupt	104
eCAP2INTn	eCAP2 Interrupt	105
eCAP3INTn	eCAP3 Interrupt	106
eCAP4INTn	eCAP4 Interrupt	107
eCAP5INTn	eCAP5 Interrupt	108
eCAP6INTn	eCAP6 Interrupt	109
eQEP1INTn	eQEP1 Interrupt	110
eQEP2INTn	eQEP2 Interrupt	111
Reserved	Reserved	112-127

NOTE

Address location 0x00000000 in the VIM RAM is reserved for the phantom interrupt ISR entry; therefore only request channels 0..126 can be used and are offset by 1 address in the VIM RAM.

NOTE

The lower-order interrupt channels are higher priority channels than the higher-order interrupt channels.

NOTE

The application can change the mapping of interrupt sources to the interrupt channels via the interrupt channel control registers (CHANCTRLx) inside the VIM module.

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6.15 DMA Controller

The DMA controller is used to transfer data between two locations in the memory map in the background of CPU operations. Typically, the DMA is used to:

- Transfer blocks of data between external and internal data memories
- Restructure portions of internal data memory
- Continually service a peripheral

6.15.1 DMA Features

- CPU independent data transfer
- One 64-bit master port that interfaces to the TMS570 Memory System.
- FIFO buffer(4 entries deep and each 64-bit wide)
- Channel control information is stored in RAM protected by parity
- 16 channels with individual enable
- Channel chaining capability
- 32 peripheral DMA requests
- Hardware and Software DMA requests
- 8, 16, 32 or 64-bit transactions supported
- Multiple addressing modes for source/destination (fixed, increment, offset)
- Auto-initiation
- Power-management mode
- Memory Protection with four configurable memory regions

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6.15.2 Default DMA Request Map

The DMA module on this microcontroller has 16 channels and up to 32 hardware DMA requests. The module contains DREQASIx registers which are used to map the DMA requests to the DMA channels. By default, channel 0 is mapped to request 0, channel 1 to request 1, and so on.

Some DMA requests have multiple sources, as shown in Table 6-28. The application must ensure that only one of these DMA request sources is enabled at any time.

Table 6-28. DMA Request Line Connection

Modules	DMA Request Sources	DMA Request
MIBSPI1	MIBSPI1[1](1)	DMAREQ[0]
MIBSPI1	MIBSPI1[0](2)	DMAREQ[1]
SPI2	SPI2 receive	DMAREQ[2]
SPI2	SPI2 transmit	DMAREQ[3]
MIBSPI1 / MIBSPI3 / DCAN2	MIBSPI1[2] / MIBSPI3[2] / DCAN2 IF3	DMAREQ[4]
MIBSPI1 / MIBSPI3 / DCAN2	MIBSPI1[3] / MIBSPI3[3] / DCAN2 IF2	DMAREQ[5]
DCAN1 / MIBSPI5	DCAN1 IF2 / MIBSPI5[2]	DMAREQ[6]
MIBADC1 / MIBSPI5	MIBADC1 event / MIBSPI5[3]	DMAREQ[7]
MIBSPI1 / MIBSPI3 / DCAN1	MIBSPI1[4] / MIBSPI3[4] / DCAN1 IF1	DMAREQ[8]
MIBSPI1 / MIBSPI3 / DCAN2	MIBSPI1[5] / MIBSPI3[5] / DCAN2 IF1	DMAREQ[9]
MIBADC1 / I2C / MIBSPI5	MIBADC1 G1 / I2C receive / MIBSPI5[4]	DMAREQ[10]
MIBADC1 / I2C / MIBSPI5	MIBADC1 G2 / I2C transmit / MIBSPI5[5]	DMAREQ[11]
RTI / MIBSPI1 / MIBSPI3	RTI DMAREQ0 / MIBSPI1[6] / MIBSPI3[6]	DMAREQ[12]
RTI / MIBSPI1 / MIBSPI3	RTI DMAREQ1 / MIBSPI1[7] / MIBSPI3[7]	DMAREQ[13]
MIBSPI3 / MibADC2 / MIBSPI5	MIBSPI3[1](1) / MibADC2 event / MIBSPI5[6]	DMAREQ[14]
MIBSPI3 / MIBSPI5	MIBSPI3[0](2) / MIBSPI5[7]	DMAREQ[15]
MIBSPI1 / MIBSPI3 / DCAN1 / MibADC2	MIBSPI1[8] / MIBSPI3[8] / DCAN1 IF3 / MibADC2 G1	DMAREQ[16]
MIBSPI1 / MIBSPI3 / DCAN3 / MibADC2	MIBSPI1[9] / MIBSPI3[9] / DCAN3 IF1 / MibADC2 G2	DMAREQ[17]
RTI / MIBSPI5	RTI DMAREQ2 / MIBSPI5[8]	DMAREQ[18]
RTI / MIBSPI5	RTI DMAREQ3 / MIBSPI5[9]	DMAREQ[19]
N2HET1 / N2HET2 / DCAN3	N2HET1 DMAREQ[4] / N2HET2 DMAREQ[4] / DCAN3 IF2	DMAREQ[20]
N2HET1 / N2HET2 / DCAN3	N2HET1 DMAREQ[5] / N2HET2 DMAREQ[5] / DCAN3 IF3	DMAREQ[21]
MIBSPI1 / MIBSPI3 / MIBSPI5	MIBSPI1[10] / MIBSPI3[10] / MIBSPI5[10]	DMAREQ[22]
MIBSPI1 / MIBSPI3 / MIBSPI5	MIBSPI1[11] / MIBSPI3[11] / MIBSPI5[11]	DMAREQ[23]
N2HET1 / N2HET2 / SPI4 / MIBSPI5	N2HET1 DMAREQ[6] / N2HET2 DMAREQ[6] / SPI4 receive / MIBSPI5[12]	DMAREQ[24]
N2HET1 / N2HET2 / SPI4 / MIBSPI5	N2HET1 DMAREQ[7] / N2HET2 DMAREQ[7] / SPI4 transmit / MIBSPI5[13]	DMAREQ[25]
CRC / MIBSPI1 / MIBSPI3	CRC DMAREQ[0] / MIBSPI1[12] / MIBSPI3[12]	DMAREQ[26]
CRC / MIBSPI1 / MIBSPI3	CRC DMAREQ[1] / MIBSPI1[13] / MIBSPI3[13]	DMAREQ[27]
LIN / MIBSPI5	LIN receive / MIBSPI5[14]	DMAREQ[28]
LIN / MIBSPI5	LIN transmit / MIBSPI5[15]	DMAREQ[29]
MIBSPI1 / MIBSPI3 / SCI / MIBSPI5	MIBSPI1[14] / MIBSPI3[14] / SCI receive / MIBSPI5[1](1)	DMAREQ[30]
MIBSPI1 / MIBSPI3 / SCI / MIBSPI5	MIBSPI1[15] / MIBSPI3[15] / SCI transmit / MIBSPI5[0](2)	DMAREQ[31]

(1) SPI1, SPI3, SPI5 receive when configured in standard SPI mode
(2) SPI1, SPI3, SPI5 transmit when configured in standard SPI mode

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6.16 Real Time Interrupt Module

The real-time interrupt (RTI) module provides timer functionality for operating systems and for benchmarking code. The RTI module can incorporate several counters that define the timebases needed for scheduling an operating system.

The timers also allow you to benchmark certain areas of code by reading the values of the counters at the beginning and the end of the desired code range and calculating the difference between the values.

6.16.1 Features

The RTI module has the following features:

- Two independent 64 bit counter blocks
- Four configurable compares for generating operating system ticks or DMA requests. Each event can be driven by either counter block 0 or counter block 1.
- Fast enabling/disabling of events
- Two time-stamp (capture) functions for system or peripheral interrupts, one for each counter block

6.16.2 Block Diagrams

Figure 6-11 shows a high-level block diagram for one of the two 64-bit counter blocks inside the RTI module. Both the counter blocks are identical except the Network Time Unit (NTUx) inputs are only available as time base inputs for the counter block 0.

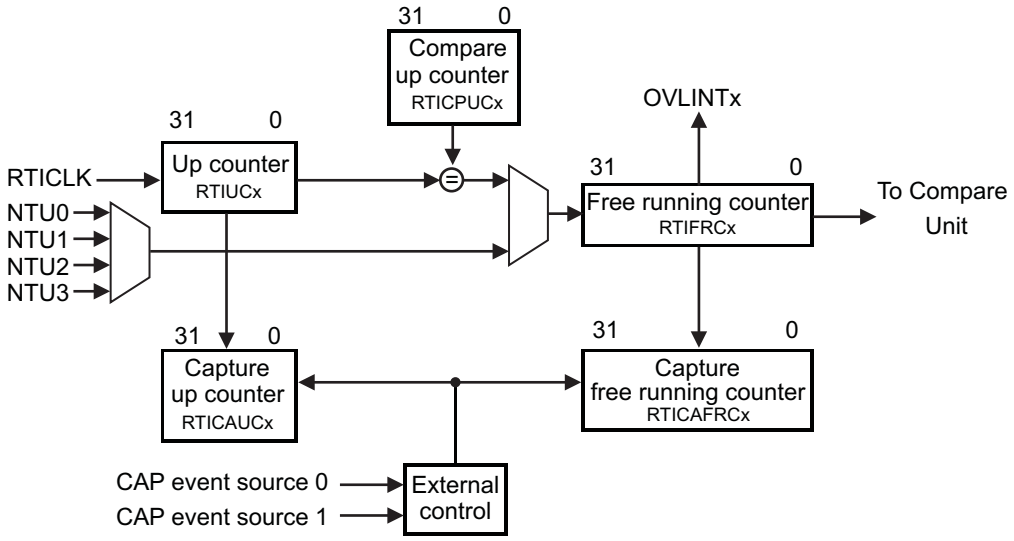


Figure 6-11. Counter Block Diagram

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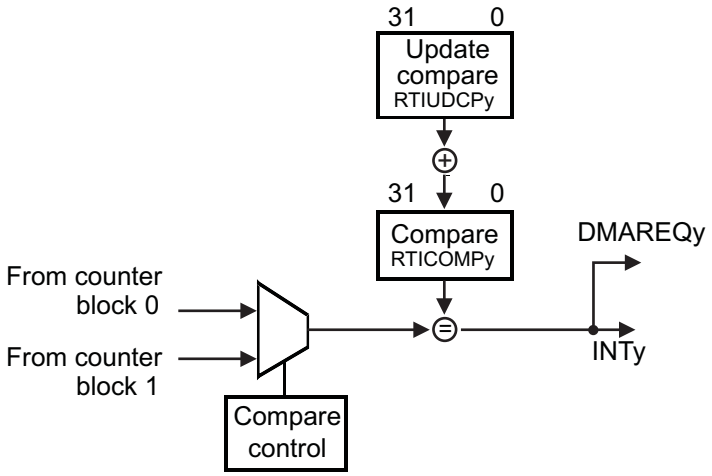


Figure 6-12. Compare Block Diagram

6.16.3 Clock Source Options

The RTI module uses the RTI1CLK clock domain for generating the RTI time bases.

The application can select the clock source for the RTI1CLK by configuring the RCLKSRC register in the System module at address 0xFFFFFF50. The default source for RTI1CLK is VCLK.

For more information on clock sources refer to Table 6-8 and Table 6-13.

6.16.4 Network Time Synchronization Inputs

The RTI module supports 4 Network Time Unit (NTU) inputs that signal internal system events, and which can be used to synchronize the time base used by the RTI module. On this device, these NTU inputs are connected as shown below.

Table 6-29. Network Time Synchronization Inputs

NTU Input	Source
0	Reserved
1	Reserved
2	Reserved
3	EXTCLKIN1 clock input

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6.17 Error Signaling Module

The Error Signaling Module (ESM) manages the various error conditions on the TMS570 microcontroller. The error condition is handled based on a fixed severity level assigned to it. Any severe error condition can be configured to drive a low level on a dedicated device terminal called nERROR. This can be used as an indicator to an external monitor circuit to put the system into a safe state.

6.17.1 Features

The features of the Error Signaling Module are:

- 128 interrupt/error channels are supported, divided into 3 different groups
  - 64 channels with maskable interrupt and configurable error pin behavior
  - 32 error channels with non-maskable interrupt and predefined error pin behavior
  - 32 channels with predefined error pin behavior only
- Error pin to signal severe device failure
- Configurable timebase for error signal
- Error forcing capability

6.17.2 ESM Channel Assignments

The Error Signaling Module (ESM) integrates all the device error conditions and groups them in the order of severity. Group1 is used for errors of the lowest severity while Group3 is used for errors of the highest severity. The device response to each error is determined by the severity group it is connected to. Table 6-31 shows the channel assignment for each group.

Table 6-30. ESM Groups

ERROR GROUP	INTERRUPT CHARACTERISTICS	INFLUENCE ON ERROR PIN
Group1	maskable, low or high priority	configurable
Group2	non-maskable, high priority	fixed
Group3	no interrupt generated	fixed

Table 6-31. ESM Channel Assignments

ERROR Condition	Group	Channels
Reserved	Group1	0
MibADC2 - RAM parity error	Group1	1
DMA - MPU configuration violation	Group1	2
DMA - control packet RAM parity error	Group1	3
Reserved	Group1	4
DMA - error on DMA read access, imprecise error	Group1	5
FMC - correctable ECC error: bus1 and bus2 interfaces (does not include accesses to Bank 7)	Group1	6
N2HET1 - RAM parity error	Group1	7
HET TU1/HET TU2 - dual-control packet RAM parity error	Group1	8
HET TU1/HET TU2 - MPU configuration violation	Group1	9
PLL1 - Slip	Group1	10
Clock Monitor - oscillator fail	Group1	11
Reserved	Group1	12
DMA - error on DMA write access, imprecise error	Group1	13
Reserved	Group1	14
VIM RAM - parity error	Group1	15
Reserved	Group1	16
MibSPI1 - RAM parity error	Group1	17
MibSPI3 - RAM parity error	Group1	18

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Table 6-31. ESM Channel Assignments (continued)

ERROR Condition	Group	Channels
MibADC1 - RAM parity error	Group1	19
Reserved	Group1	20
DCAN1 - RAM parity error	Group1	21
DCAN3 - RAM parity error	Group1	22
DCAN2 - RAM parity error	Group1	23
MibSPI5 - RAM parity error	Group1	24
Reserved	Group1	25
RAM even bank (B0TCM) - correctable ECC error	Group1	26
CPU - self-test failed	Group1	27
RAM odd bank (B1TCM) - correctable ECC error	Group1	28
Reserved	Group1	29
DCC1 - error	Group1	30
CCM-R4 - self-test failed	Group1	31
Reserved	Group1	32
Reserved	Group1	33
N2HET2 - RAM parity error	Group1	34
FMC - correctable ECC error (Bank 7 access)	Group1	35
FMC - uncorrectable ECC error (Bank 7 access)	Group1	36
IOMM - Access to unimplemented location in IOMM frame, or write access detected in unprivileged mode	Group1	37
Power domain controller compare error	Group1	38
Power domain controller self-test error	Group1	39
eFuse Controller Error – this error signal is generated when any bit in the eFuse controller error status register is set. The application can choose to generate an interrupt whenever this bit is set to service any eFuse controller error conditions.	Group1	40
eFuse Controller - Self Test Error. This error signal is generated only when a self test on the eFuse controller generates an error condition. When an ECC self test error is detected, group 1 channel 40 error signal will also be set.	Group1	41
Reserved	Group1	42
Reserved	Group1	43
Reserved	Group1	44
Reserved	Group1	45
Reserved	Group1	46
Reserved	Group1	47
Reserved	Group1	48
Reserved	Group1	49
Reserved	Group1	50
Reserved	Group1	51
Reserved	Group1	52
Reserved	Group1	53
Reserved	Group1	54
Reserved	Group1	55
Reserved	Group1	56
Reserved	Group1	57
Reserved	Group1	58
Reserved	Group1	59
Reserved	Group1	60
Reserved	Group1	61
DCC2 - error	Group1	62

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Table 6-31. ESM Channel Assignments (continued)

ERROR Condition	Group	Channels
Reserved	Group1	63
Reserved	Group2	0
Reserved	Group2	1
CCMR4 - dual-CPU lock-step error	Group2	2
Reserved	Group2	3
FMC - uncorrectable address parity error on accesses to main flash	Group2	4
Reserved	Group2	5
RAM even bank (B0TCM) - uncorrectable redundant address decode error	Group2	6
Reserved	Group2	7
RAM odd bank (B1TCM) - uncorrectable redundant address decode error	Group2	8
Reserved	Group2	9
RAM even bank (B0TCM) - address bus parity error	Group2	10
Reserved	Group2	11
RAM odd bank (B1TCM) - address bus parity error	Group2	12
Reserved	Group2	13
Reserved	Group2	14
Reserved	Group2	15
TCM - ECC live lock detect	Group2	16
Reserved	Group2	17
Reserved	Group2	18
Reserved	Group2	19
Reserved	Group2	20
Reserved	Group2	21
Reserved	Group2	22
Reserved	Group2	23
Windowed Watchdog (WWD) violation	Group2	24
Reserved	Group2	25
Reserved	Group2	26
Reserved	Group2	27
Reserved	Group2	28
Reserved	Group2	29
Reserved	Group2	30
Reserved	Group2	31
Reserved	Group3	0
eFuse Farm - autoload error	Group3	1
Reserved	Group3	2
RAM even bank (B0TCM) - ECC uncorrectable error	Group3	3
Reserved	Group3	4
RAM odd bank (B1TCM) - ECC uncorrectable error	Group3	5
Reserved	Group3	6
FMC - uncorrectable ECC error: bus1 and bus2 interfaces (does not include address parity error and errors on accesses to Bank 7)	Group3	7
Reserved	Group3	8
Reserved	Group3	9
Reserved	Group3	10
Reserved	Group3	11
Reserved	Group3	12
Reserved	Group3	13

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Table 6-31. ESM Channel Assignments (continued)

ERROR Condition	Group	Channels
Reserved	Group3	14
Reserved	Group3	15
Reserved	Group3	16
Reserved	Group3	17
Reserved	Group3	18
Reserved	Group3	19
Reserved	Group3	20
Reserved	Group3	21
Reserved	Group3	22
Reserved	Group3	23
Reserved	Group3	24
Reserved	Group3	25
Reserved	Group3	26
Reserved	Group3	27
Reserved	Group3	28
Reserved	Group3	29
Reserved	Group3	30
Reserved	Group3	31

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6.18 Reset/Abort/Error Sources

Table 6-32. Reset/Abort/Error Sources

ERROR SOURCE	CPUMODE	ERROR RESPONSE	ESM HOOKUP group.channel
CPU TRANSACTIONS			
Precise write error (NCNB/Strongly Ordered)	User/Privilege	Precise Abort (CPU)	n/a
Precise read error (NCB/Device or Normal)	User/Privilege	Precise Abort (CPU)	n/a
Imprecise write error (NCB/Device or Normal)	User/Privilege	Imprecise Abort (CPU)	n/a
Illegal instruction	User/Privilege	Undefined Instruction Trap (CPU)(1)	n/a
MPU access violation	User/Privilege	Abort (CPU)	n/a
SRAM			
B0 TCM (even) ECC single error (correctable)	User/Privilege	ESM	1.26
B0 TCM (even) ECC double error (non-correctable)	User/Privilege	Abort (CPU), ESM => nERROR	3.3
B0 TCM (even) uncorrectable error (i.e. redundant address decode)	User/Privilege	ESM => NMI => nERROR	2.6
B0 TCM (even) address bus parity error	User/Privilege	ESM => NMI => nERROR	2.10
B1 TCM (odd) ECC single error (correctable)	User/Privilege	ESM	1.28
B1 TCM (odd) ECC double error (non-correctable)	User/Privilege	Abort (CPU), ESM => nERROR	3.5
B1 TCM (odd) uncorrectable error (i.e. redundant address decode)	User/Privilege	ESM => NMI => nERROR	2.8
B1 TCM (odd) address bus parity error	User/Privilege	ESM => NMI => nERROR	2.12
FLASH WITH CPU BASED ECC			
FMC correctable error - Bus1 and Bus2 interfaces (does not include accesses to Bank 7)	User/Privilege	ESM	1.6
FMC uncorrectable error - Bus1 and Bus2 accesses (does not include address parity error)	User/Privilege	Abort (CPU), ESM => nERROR	3.7
FMC uncorrectable error - address parity error on Bus1 accesses	User/Privilege	ESM => NMI => nERROR	2.4
FMC correctable error - Accesses to Bank 7	User/Privilege	ESM	1.35
FMC uncorrectable error - Accesses to Bank 7	User/Privilege	ESM	1.36
DMA TRANSACTIONS			
External imprecise error on read (Illegal transaction with ok response)	User/Privilege	ESM	1.5
External imprecise error on write (Illegal transaction with ok response)	User/Privilege	ESM	1.13
Memory access permission violation	User/Privilege	ESM	1.2
Memory parity error	User/Privilege	ESM	1.3
HET TU1 (HTU1)			
NCNB (Strongly Ordered) transaction with slave error response	User/Privilege	Interrupt => VIM	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	Interrupt => VIM	n/a
Memory access permission violation	User/Privilege	ESM	1.9
Memory parity error	User/Privilege	ESM	1.8
HET TU2 (HTU2)			
NCNB (Strongly Ordered) transaction with slave error response	User/Privilege	Interrupt => VIM	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	Interrupt => VIM	n/a
Memory access permission violation	User/Privilege	ESM	1.9
Memory parity error	User/Privilege	ESM	1.8

(1) The Undefined Instruction TRAP is NOT detectable outside the CPU. The trap is taken only if the instruction reaches the execute stage of the CPU.

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Table 6-32. Reset/Abort/Error Sources (continued)

ERROR SOURCE	CPUMODE	ERROR RESPONSE	ESM HOOKUP group.channel
N2HET1			
Memory parity error	User/Privilege	ESM	1.7
N2HET2			
Memory parity error	User/Privilege	ESM	1.34
MIBSPI			
MibSPI1 memory parity error	User/Privilege	ESM	1.17
MibSPI3 memory parity error	User/Privilege	ESM	1.18
MibSPI5 memory parity error	User/Privilege	ESM	1.24
MIBADC			
MibADC1 Memory parity error	User/Privilege	ESM	1.19
MibADC2 Memory parity error	User/Privilege	ESM	1.1
DCAN			
DCAN1 memory parity error	User/Privilege	ESM	1.21
DCAN2 memory parity error	User/Privilege	ESM	1.23
DCAN3 memory parity error	User/Privilege	ESM	1.22
PLL			
PLL slip error	User/Privilege	ESM	1.10
CLOCK MONITOR			
Clock monitor interrupt	User/Privilege	ESM	1.11
DCC			
DCC1 error	User/Privilege	ESM	1.30
DCC2 error	User/Privilege	ESM	1.62
CCM-R4			
Self test failure	User/Privilege	ESM	1.31
Compare failure	User/Privilege	ESM => NMI => nERROR	2.2
VIM			
Memory parity error	User/Privilege	ESM	1.15
VOLTAGE MONITOR			
VMON out of voltage range	n/a	Reset	n/a
CPU SELFTEST (LBIST)			
CPU Selftest (LBIST) error	User/Privilege	ESM	1.27
PIN MULTIPLEXING CONTROL			
Mux configuration error	User/Privilege	ESM	1.37
POWER DOMAIN CONTROL			
PSCON compare error	User/Privilege	ESM	1.38
PSCON self-test error	User/Privilege	ESM	1.39
eFuse CONTROLLER			
eFuse Controller Autoload error	User/Privilege	ESM => nERROR	3.1
eFuse Controller - Any bit set in the error status register	User/Privilege	ESM	1.40
eFuse Controller self-test error	User/Privilege	ESM	1.41
WINDOWED WATCHDOG			
WWD Non-Maskable Interrupt exception	n/a	ESM => NMI => nERROR	2.24
ERRORS REFLECTED IN THE SYSESR REGISTER			
Power-Up Reset	n/a	Reset	n/a
Oscillator fail / PLL slip(2)	n/a	Reset	n/a
Watchdog exception	n/a	Reset	n/a

(2) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

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Table 6-32. Reset/Abort/Error Sources (continued)

ERROR SOURCE	CPUMODE	ERROR RESPONSE	ESM HOOKUP group.channel
CPU Reset (driven by the CPU STC)	n/a	Reset	n/a
Software Reset	n/a	Reset	n/a
External Reset	n/a	Reset	n/a

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6.19 Digital Windowed Watchdog

This device includes a digital windowed watchdog (DWWD) module that protects against runaway code execution.

The DWWD module allows the application to configure the time window within which the DWWD module expects the application to service the watchdog. A watchdog violation occurs if the application services the watchdog outside of this window, or fails to service the watchdog at all. The application can choose to generate a system reset or an ESM group2 error signal in case of a watchdog violation.

The watchdog is disabled by default and must be enabled by the application. Once enabled, the watchdog can only be disabled upon a system reset.

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6.20 Debug Subsystem

6.20.1 Block Diagram

The device contains an ICEPICK module to allow JTAG access to the scan chains.

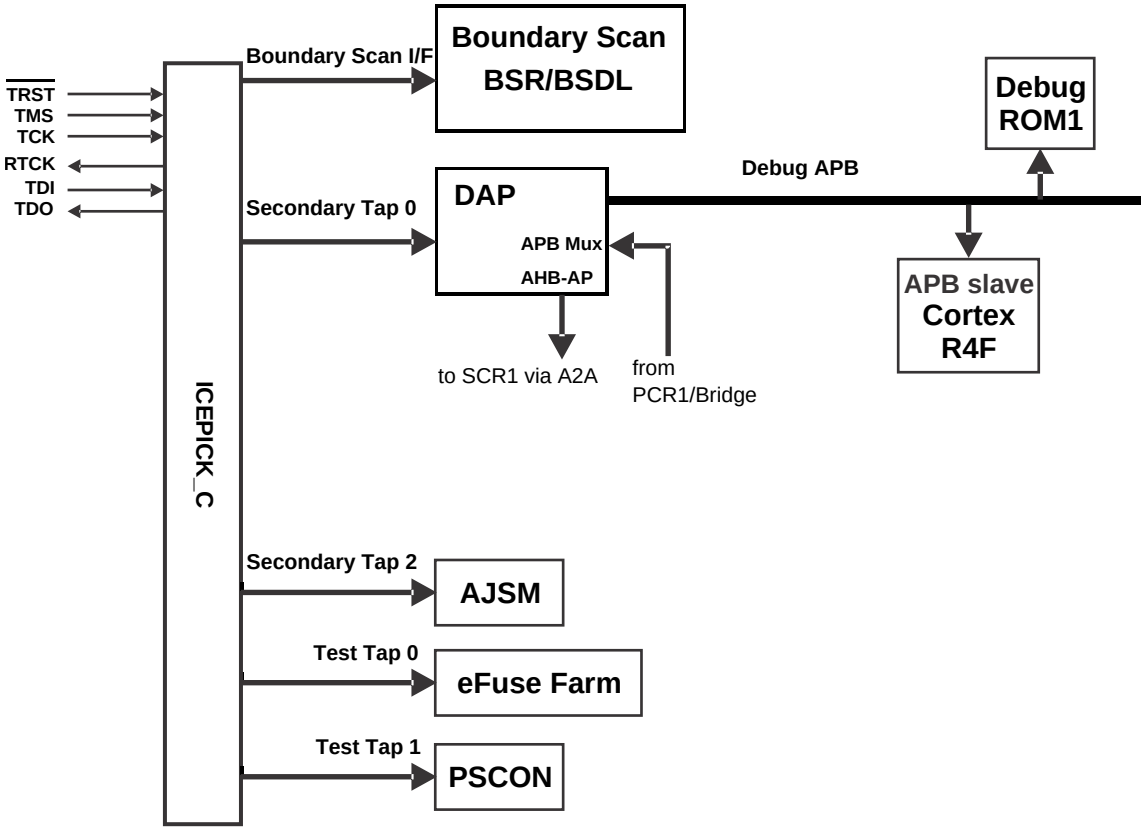


Figure 6-13. Debug Subsystem Block Diagram

6.20.2 Debug Components Memory Map

Table 6-33. Debug Components Memory Map

MODULE NAME	FRAME CHIP SELECT	FRAME ADDRESS RANGE		FRAME SIZE	ACTUAL SIZE	RESPNSE FOR ACCESS TO UNIMPLEMENTED LOCATIONS IN FRAME
		START	END			
CoreSight Debug ROM	CSCS0	0xFFA0_0000	0xFFA0_0FFF	4KB	4KB	Reads return zeros, writes have no effect
Cortex-R4F Debug	CSCS1	0xFFA0_1000	0xFFA0_1FFF	4KB	4KB	Reads return zeros, writes have no effect

6.20.3 JTAG Identification Code

The JTAG ID code for this device is the same as the device ICEPick Identification Code. For the JTAG ID Code per silicon revision, see Table 6-34.

Table 6-34. JTAG ID Code

SILICON REVISION	ID
Rev 0	0x0BB0302F
Rev A	0x1BB0302F

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6.20.4 Debug ROM

The Debug ROM stores the location of the components on the Debug APB bus:

Table 6-35. Debug ROM table

ADDRESS	DESCRIPTION	VALUE
0x000	pointer to Cortex-R4F	0x0000 1003
0x001	Reserved	0x0000 2002
0x002	Reserved	0x0000 3002
0x003	Reserved	0x0000 4003
0x004	end of table	0x0000 0000

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6.20.5 JTAG Scan Interface Timings

Table 6-36. JTAG Scan Interface Timing (1)

NO.	PARAMETER		MIN	MAX	UNIT
	fTCK	TCK frequency (at HCLKmax)		12	MHz
	fRTCK	RTCK frequency (at TCKmax and HCLKmax)	10		MHz
1	td(TCK -RTCK)	Delay time, TCK to RTCK		24	ns
2	tsu(TDI/TMS - RTCKr)	Setup time, TDI, TMS before RTCK rise (RTCKr)	26		ns
3	th(RTCKr -TDI/TMS)	Hold time, TDI, TMS after RTCKr	0		ns
4	th(RTCKr -TDO)	Hold time, TDO after RTCKf	0		ns
5	td(TCKf -TDO)	Delay time, TDO valid after RTCK fall (RTCKf)		12	ns

(1) Timings for TDO are specified for a maximum of 50pF load on TDO

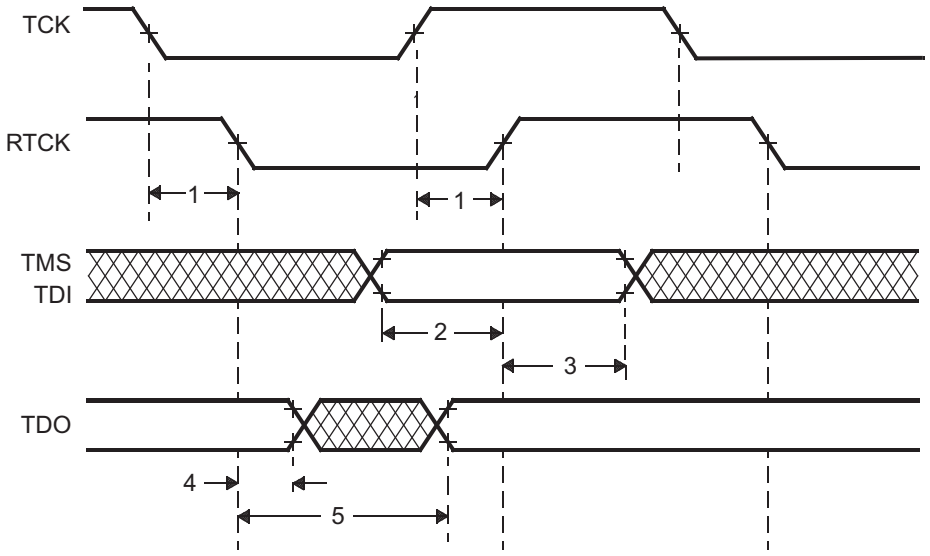


Figure 6-14. JTAG Timing

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6.20.6 Advanced JTAG Security Module

This device includes a an Advanced JTAG Security Module (AJSM). which provides maximum security to the device's memory content by allowing users to secure the device after programming.

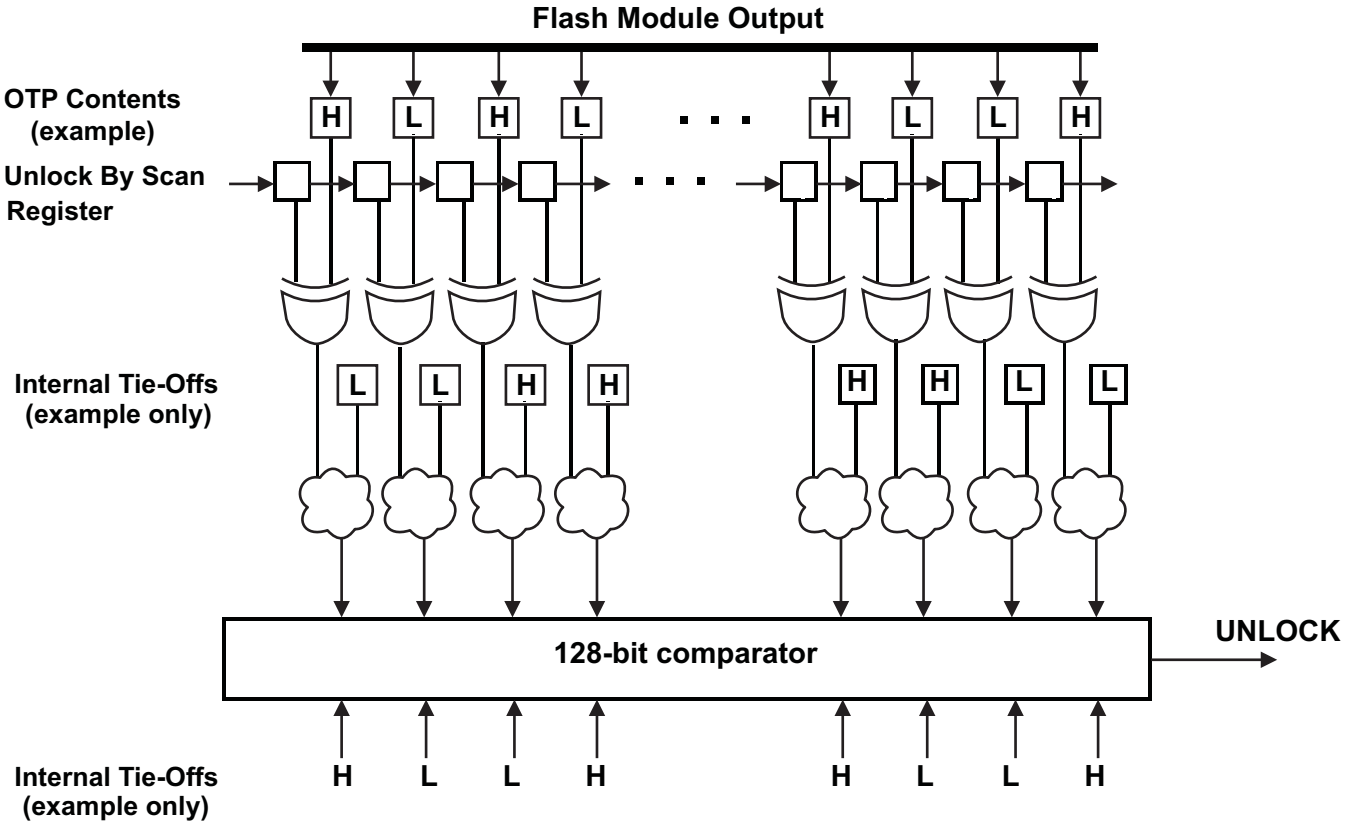


Figure 6-15. AJSM Unlock

The device is unsecure by default by virtue of a 128-bit visible unlock code programmed in the OTP address 0xF0000000.The OTP contents are XOR-ed with the "Unlock By Scan" register contents. The outputs of these XOR gates are again combined with a set of secret internal tie-offs. The output of this combinational logic is compared against a secret hard-wired 128-bit value. A match results in the UNLOCK signal being asserted, so that the device is now unsecure.

A user can secure the device by changing at least one bit in the visible unlock code from 1 to 0. Changing a 0 to 1 is not possible since the visible unlock code is stored in the One Time Programmable (OTP) flash region. Also, changing all the 128 bits to zeros is not a valid condition and will permanently secure the device.

Once secured, a user can unsecure the device by scanning an appropriate value into the "Unlock By Scan" register of the AJSM module. This register is accessible by configuring an IR value of 0b1011 on the AJSM TAP. The value to be scanned is such that the XOR of the OTP contents and the Unlock-By-Scan register contents results in the original visible unlock code.

The Unlock-By-Scan register is reset only upon asserting power-on reset (nPORRST).

A secure device only permits JTAG accesses to the AJSM scan chain via the Secondary Tap # 2 of the ICEPick module. All other secondary taps, test taps and the boundary scan interface are not accessible in this state.

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6.20.7 Boundary Scan Chain

The device supports BSDL-compliant boundary scan for testing pin-to-pin compatibility. The boundary scan chain is connected to the Boundary Scan Interface of the ICEPICK module.

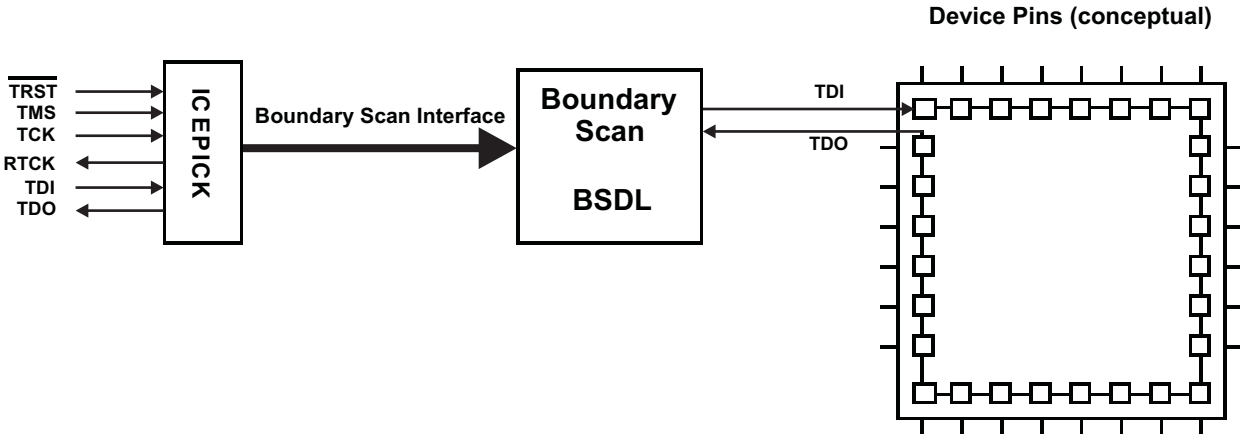


Figure 6-16. Boundary Scan Implementation (Conceptual Diagram)

Data is serially shifted into all boundary-scan buffers via TDI, and out via TDO.

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7 Peripheral Information and Electrical Specifications

7.1 I/O Timings

7.1.1 Input Timings



Figure 7-1. TTL-Level Inputs

Table 7-1. Timing Requirements for Inputs(1)

Parameter		MIN	MAX	Unit
t_{pw}	Input minimum pulse width	$t_{c(VCLK)}$ + 10(2)		ns
t_{in_slew}	Time for input signal to go from V_{IL} to V_{IH} or from V_{IH} to V_{IL}		1	ns

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$
(2) The timing shown above is only valid for pin used in general-purpose input mode.

7.1.2 Output Timings

Table 7-2. Switching Characteristics for Output Timings versus Load Capacitance (C_L)

Parameter			MIN	MAX	Unit
Rise time, t_r	8mA low EMI pins (see Table 4-40)	CL = 15 pF		2.5	ns
		CL = 50 pF		4	
		CL = 100 pF		7.2	
		CL = 150 pF		12.5	
Fall time, t_f		CL = 15 pF		2.5	ns
		CL = 50 pF		4	
		CL = 100 pF		7.2	
		CL = 150 pF		12.5	
Rise time, t_r	4mA low EMI pins (see Table 4-40)	CL = 15 pF		5.6	ns
		CL = 50 pF		10.4	
		CL = 100 pF		16.8	
		CL = 150 pF		23.2	
Fall time, t_f		CL = 15 pF		5.6	ns
		CL= 50 pF		10.4	
		CL = 100 pF		16.8	
		CL = 150 pF		23.2	
Rise time, t_r	2mA-z low EMI pins (see Table 4-40)	CL = 15 pF		8	ns
		CL = 50 pF		15	
		CL = 100 pF		23	
		CL = 150 pF		33	
Fall time, t_f		CL = 15 pF		8	ns
		CL = 50 pF		15	
		CL = 100 pF		23	
		CL = 150 pF		33	

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Table 7-2. Switching Characteristics for Output Timings versus Load Capacitance (C_L) (continued)

Parameter				MIN	MAX	Unit
Rise time, t_r	Selectable 8mA / 2mA-z pins (see Table 4-40)	8mA mode	CL = 15 pF		2.5	ns
			CL = 50 pF		4	
			CL = 100 pF		7.2	
			CL = 150 pF		12.5	
Fall time, t_f			CL = 15 pF		2.5	ns
			CL = 50 pF		4	
			CL = 100 pF		7.2	
			CL = 150 pF		12.5	
Rise time, t_r		2mA-z mode	CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	
Fall time, t_f			CL = 15 pF		8	ns
			CL = 50 pF		15	
			CL = 100 pF		23	
			CL = 150 pF		33	

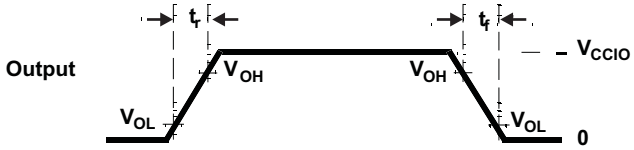


Figure 7-2. CMOS-Level Outputs

Table 7-3. Timing Requirements for Outputs (1)

Parameter		MIN	MAX	UNIT
$t_{d(parallel_out)}$	Delay between low to high, or high to low transition of general-purpose output signals that can be configured by an application in parallel, e.g. all signals in a GIOA port, or all N2HET1 signals, etc.		6	ns

(1) This specification does not account for any output buffer drive strength differences or any external capacitive loading differences. Check Table 4-40 for output buffer drive strength information on each signal.

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7.1.2.1 Low-EMI Output Buffers

The low-EMI output buffer has been designed explicitly to address the issue of decoupling sources of emissions from the pins which they drive. This is accomplished by adaptively controlling the impedance of the output buffer, and is particularly effective with capacitive loads.

This is not the default mode of operation of the low-EMI output buffers and must be enabled by setting the system module GPCR1 register for the desired module or signal, as shown in . The adaptive impedance control circuit monitors the DC bias point of the output signal. The buffer internally generates two reference levels, VREFLOW and VREFHIGH, which are set to approximately 10% and 90% of VCCIO, respectively.

Once the output buffer has driven the output to a low level, if the output voltage is below VREFLOW, then the output buffer's impedance will increase to hi-Z. A high degree of decoupling between the internal ground bus and the output pin will occur with capacitive loads, or any load in which no current is flowing, e.g. the buffer is driving low on a resistive path to ground. Current loads on the buffer which attempt to pull the output voltage above VREFLOW will be opposed by the buffer's output impedance so as to maintain the output voltage at or below VREFLOW.

Conversely, once the output buffer has driven the output to a high level, if the output voltage is above VREFHIGH then the output buffer's impedance will again increase to hi-Z. A high degree of decoupling between internal power bus ad output pin will occur with capacitive loads or any loads in which no current is flowing, e.g. buffer is driving high on a resistive path to VCCIO. Current loads on the buffer which attempt to pull the output voltage below VREFHIGH will be opposed by the buffer's output impedance so as to maintain the output voltage at or above VREFHIGH.

The bandwidth of the control circuitry is relatively low, so that the output buffer in adaptive impedance control mode cannot respond to high-frequency noise coupling into the buffer's power buses. In this manner, internal bus noise approaching 20% peak-to-peak of VCCIO can be rejected.

Unlike standard output buffers which clamp to the rails, an output buffer in impedance control mode will allow a positive current load to pull the output voltage up to VCCIO + 0.6V without opposition. Also, a negative current load will pull the output voltage down to VSSIO – 0.6V without opposition. This is not an issue since the actual clamp current capability is always greater than the IOH / IOL specifications.

The low-EMI output buffers are automatically configured to be in the standard buffer mode when the device enters a low-power mode.

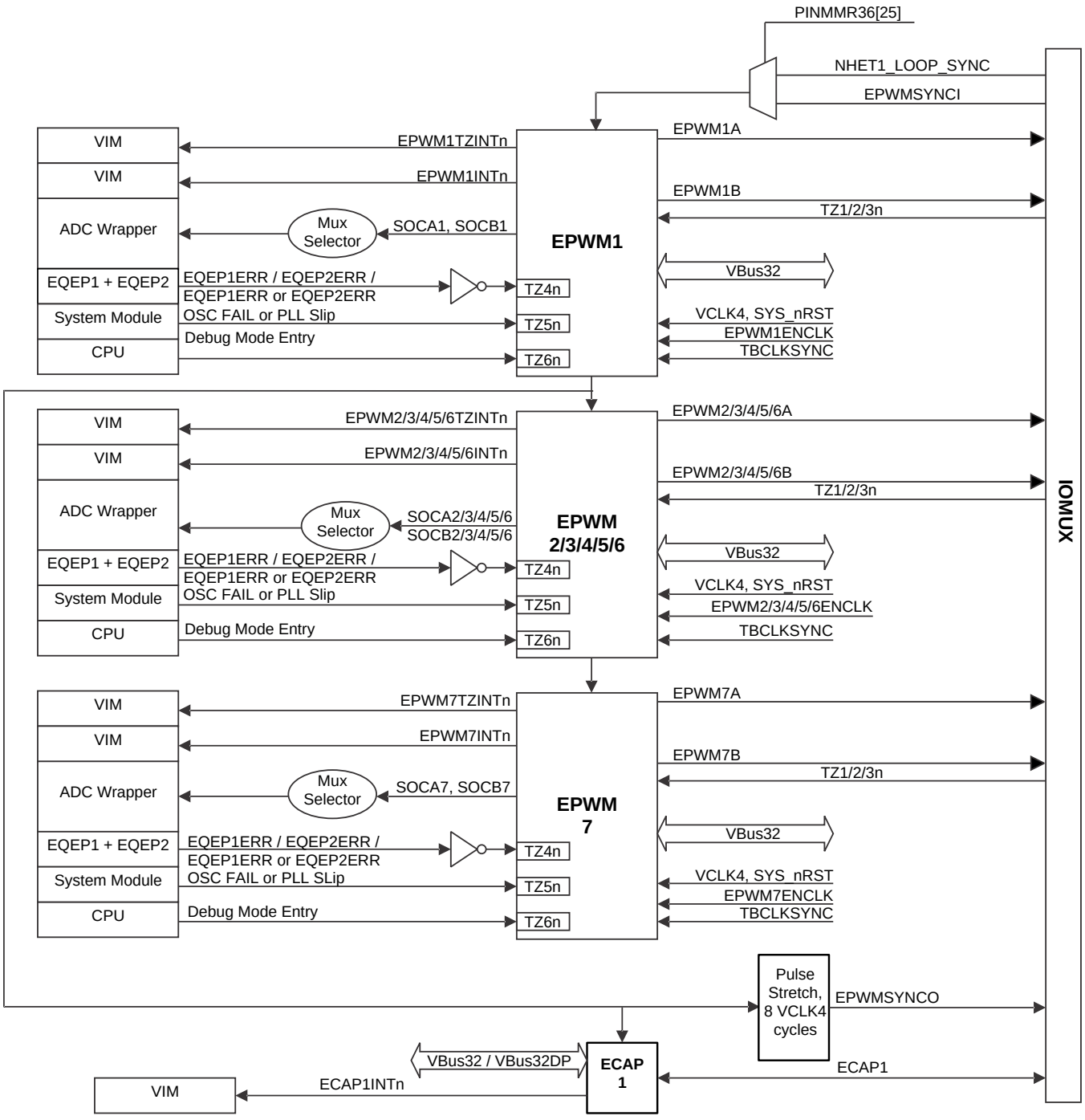
Table 7-4. Low-EMI Output Buffer Hookup

Module or Signal Name	Low-EMI Output Buffer Signal Hookup	
	Low Power Mode (LPM)	Standard Buffer Enable (SBEN)
Module: MibSPI1	LPM signal from SYS module	GPREG1.0
Reserved		GPREG1.1
Module: MibSPI3		GPREG1.2
Reserved		GPREG1.3
Module: MibSPI5		GPREG1.4
Reserved		GPREG1.5
Reserved		GPREG1.6
Reserved		GPREG1.7
Signal: TMS		GPREG1.8
Reserved		GPREG1.9
Signal: TDO		GPREG1.10
Signal: RTCK		GPREG1.11
Reserved		GPREG1.12
Signal: nERROR		GPREG1.13
Reserved		GPREG1.14

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7.2 Enhanced PWM Modules (ePWM)

Figure 7-3 illustrates the connections between the seven ePWM modules (ePWM1,2,3,4,5,6,7) on the device.



A. For more detail on the input synchronization selection of the TZ1/TZ2/TZ3n pins to each ePWMx module, see Figure 7-4.

Figure 7-3. ePWMx Module Interconnections

Figure 7-4 shows the detailed input synchronization selection (asynchronous, double-synchronous, or double-synchronous + filter width) for ePWMx.

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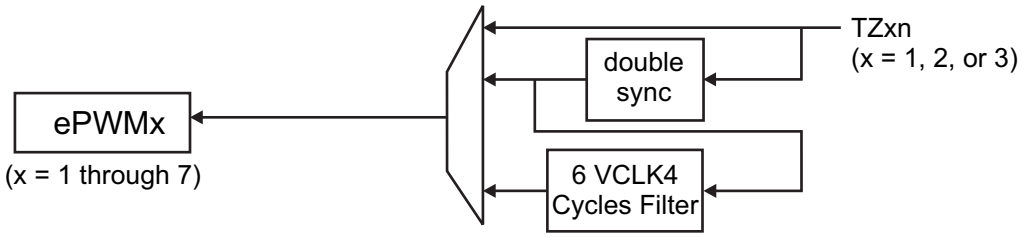


Figure 7-4. ePWMx Input Synchronization Selection Detail

7.2.1 ePWM Clocking and Reset

Each ePWM module has a clock enable (EPWMxENCLK). When SYS_nRST is active low, the clock enables are ignored and the ePWM logic is clocked so that it can reset to a proper state. When SYS_nRST goes in-active high, the state of clock enable is respected.

Table 7-5. ePWMx Clock Enable Control

ePWM Module Instance	Control Register to Enable Clock	Default Value
ePWM1	PINMMR37[8]	1
ePWM2	PINMMR37[16]	1
ePWM3	PINMMR37[24]	1
ePWM4	PINMMR38[0]	1
ePWM5	PINMMR38[8]	1
ePWM6	PINMMR38[16]	1
ePWM7	PINMMR38[24]	1

The default value of the control registers to enable the clocks to the ePWMx modules is 1. This means that the VCLK4 clock connections to the ePWMx modules are enabled by default. The application can choose to gate off the VCLK4 clock to any ePWMx module individually by clearing the respective control register bit.

7.2.2 Synchronization of ePWMx Time Base Counters

A time-base synchronization scheme connects all of the ePWM modules on a device. Each ePWM module has a synchronization input (EPWMxSYNCI) and a synchronization output (EPWMxSYNCO). The input synchronization for the first instance (ePWM1) comes from an external pin. Figure 7-3 shows the synchronization connections for all the ePWMx modules. Each ePWM module can be configured to use or ignore the synchronization input. Refer to the ePWM chapter in the device Technical Reference Manual for more information.

7.2.3 Synchronizing all ePWM Modules to the N2HET1 Module Time Base

The connection between the N2HET1_LOOP_SYNC and SYNCI input of ePWM1 module is implemented as shown in Figure 7-5.

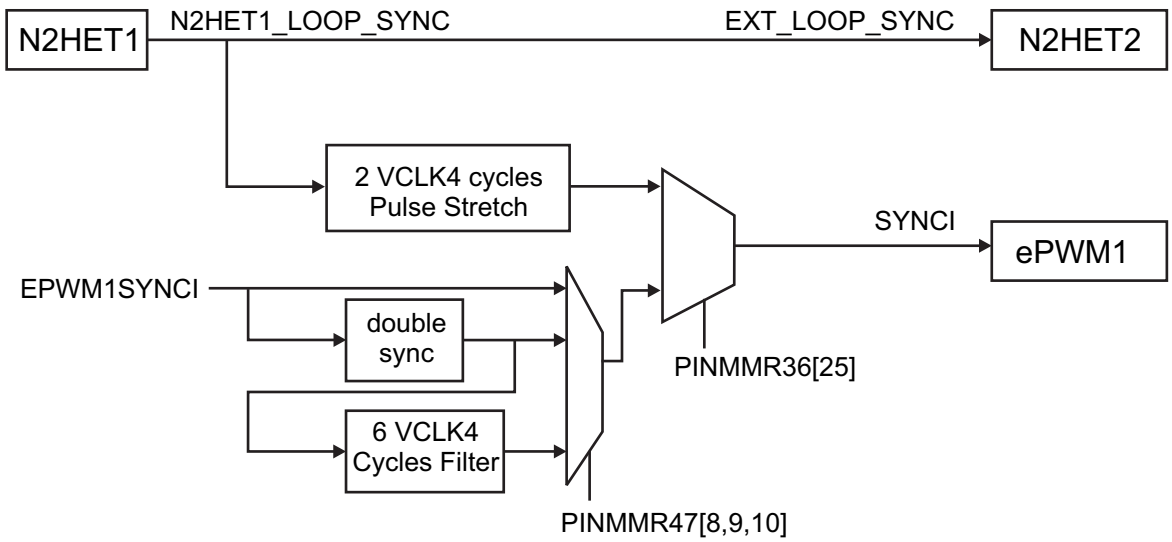


Figure 7-5. Synchronizing Time Bases Between N2HET1, N2HET2 and ePWMx Modules

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7.2.4 Phase-Locking the Time-Base Clocks of Multiple ePWM Modules

The TBCLKSYNC bit can be used to globally synchronize the time-base clocks of all enabled ePWM modules on a device. This bit is implemented as PINMMR37 register bit 1.

When TBCLKSYNC = 0, the time-base clock of all ePWM modules is stopped. This is the default condition.

When TBCLKSYNC = 1, all ePWM time-base clocks are started with the rising edge of TBCLK aligned.

For perfectly synchronized TBCLKs, the prescaler bits in the TBCTL register of each ePWM module must be set identically. The proper procedure for enabling the ePWM clocks is as follows:

1. Enable the individual ePWM module clocks (if disable) using the control registers shown in Table 7-5.
2. Configure TBCLKSYNC = 0. This will stop the time-base clock within any enabled ePWM module.
3. Configure the prescaler values and desired ePWM modes.
4. Configure TBCLKSYNC = 1.

7.2.5 ePWM Synchronization with External Devices

The output sync from ePWM1 Module is also exported to a device output terminal so that multiple devices can be synchronized together. The signal pulse is stretched by eight VCLK4 cycles before being exported on the terminal as the EPWM1SYNCO signal.

7.2.6 ePWM Trip Zones

7.2.6.1 Trip Zones TZ1n, TZ2n, TZ3n

These three trip zone inputs are driven by external circuits and are connected to device-level inputs. These signals are either connected asynchronously to the ePWMx trip zone inputs, or double-synchronized with VCLK4, or double-synchronized and then filtered with a 6-cycle VCLK4-based counter before connecting to the ePWMx. By default, the trip zone inputs are asynchronously connected to the ePWMx modules.

Table 7-6. Connection to ePWMx Modules for Device-Level Trip Zone Inputs

Trip Zone Input	Control for Asynchronous Connection to ePWMx	Control for Double-Synchronized Connection to ePWMx	Control for Double-Synchronized and Filtered Connection(1) to ePWMx
TZ1n	PINMMR46[16] = 1	PINMMR46[16] = 0 AND PINMMR46[17] = 1	PINMMR46[16] = 0 AND PINMMR46[17] = 0 AND PINMMR46[18] = 1
TZ2n	PINMMR46[24] = 1	PINMMR46[24] = 0 AND PINMMR46[25] = 1	PINMMR46[24] = 0 AND PINMMR46[25] = 0 AND PINMMR46[26] = 1
TZ3n	PINMMR47[0] = 1	PINMMR47[0] = 0 AND PINMMR47[1] = 1	PINMMR47[0] = 0 AND PINMMR47[1] = 0 AND PINMMR47[2] = 1

(1) The filter width is 6 VCLK4 cycles.

7.2.6.2 Trip Zone TZ4n

This trip zone input is dedicated to eQEPx error indications. There are two eQEP modules on this device. Each eQEP module indicates a phase error by driving its EQEPxERR output High. The following control registers allow the application to configure the trip zone input (TZ4n) to each ePWMx module based on the application's requirements.

Table 7-7. TZ4n Connections for ePWMx Modules

ePWMx	Control for TZ4n = not(EQEP1ERR OR EQEP2ERR)	Control for TZ4n = not(EQEP1ERR)	Control for TZ4n = not(EQEP2ERR)
ePWM1	PINMMR41[0] = 1	PINMMR41[0] = 0 AND PINMMR41[1] = 1	PINMMR41[0] = 1 AND PINMMR41[1] = 0 AND PINMMR41[2] = 1
ePWM2	PINMMR41[8]	PINMMR41[8] = 0 AND PINMMR41[9] = 1	PINMMR41[8] = 1 AND PINMMR41[9] = 0 AND PINMMR41[10] = 1
ePWM3	PINMMR41[16]	PINMMR41[16] = 0 AND PINMMR41[17] = 1	PINMMR41[16] = 1 AND PINMMR41[17] = 0 AND PINMMR41[18] = 1
ePWM4	PINMMR41[24]	PINMMR41[24] = 0 AND PINMMR41[25] = 1	PINMMR41[24] = 1 AND PINMMR41[25] = 0 AND PINMMR41[26] = 1
ePWM5	PINMMR42[0]	PINMMR42[0] = 0 AND PINMMR42[1] = 1	PINMMR42[0] = 1 AND PINMMR42[1] = 0 AND PINMMR42[2] = 1
ePWM6	PINMMR42[8]	PINMMR42[8] = 0 AND PINMMR42[9] = 1	PINMMR42[8] = 1 AND PINMMR42[9] = 0 AND PINMMR42[10] = 1
ePWM7	PINMMR42[16]	PINMMR42[16] = 0 AND PINMMR42[17] = 1	PINMMR42[16] = 1 AND PINMMR42[17] = 0 AND PINMMR42[18] = 1

7.2.6.3 Trip Zone TZ5n

This trip zone input is dedicated to a clock failure on the device. That is, this trip zone input is asserted whenever an oscillator failure or a PLL slip is detected on the device. The application can use this trip zone input for each ePWMx module in order to prevent the external system from going out of control when the device clocks are not within expected range (system running at limp clock).

The oscillator failure and PLL slip signals used for this trip zone input are taken from the status flags in the system module. These are level signals are set until cleared by the application.

7.2.6.4 Trip Zone TZ6n

This trip zone input to the ePWMx modules is dedicated to a debug mode entry of the CPU. If enabled, the user can force the PWM outputs to a known state when the emulator stops the CPU. This prevents the external system from going out of control when the CPU is stopped.

7.2.7 Triggering of ADC Start of Conversion Using ePWMx SOCA and SOCB Outputs

A special scheme is implemented in order to select the actual signal used for triggering the start of conversion on the two ADCs on this device. This scheme is defined in Section 7.5.2.3.

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7.2.8 Enhanced Translator-Pulse Width Modulator (ePWMx) Timings

Table 7-8. ePWMx Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Synchronization input pulse width	Asynchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK4)}$ + filter width(1)		cycles

(1) The filter width is 6 VCLK4 cycles

Table 7-9. ePWMx Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, ePWMx output high or low		33.33		ns
$t_{w(SYNCOUT)}$	Synchronization Output Pulse Width		8 $t_{c(VCLK4)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high, OR Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

Table 7-10. ePWMx Trip-Zone Timing Requirements

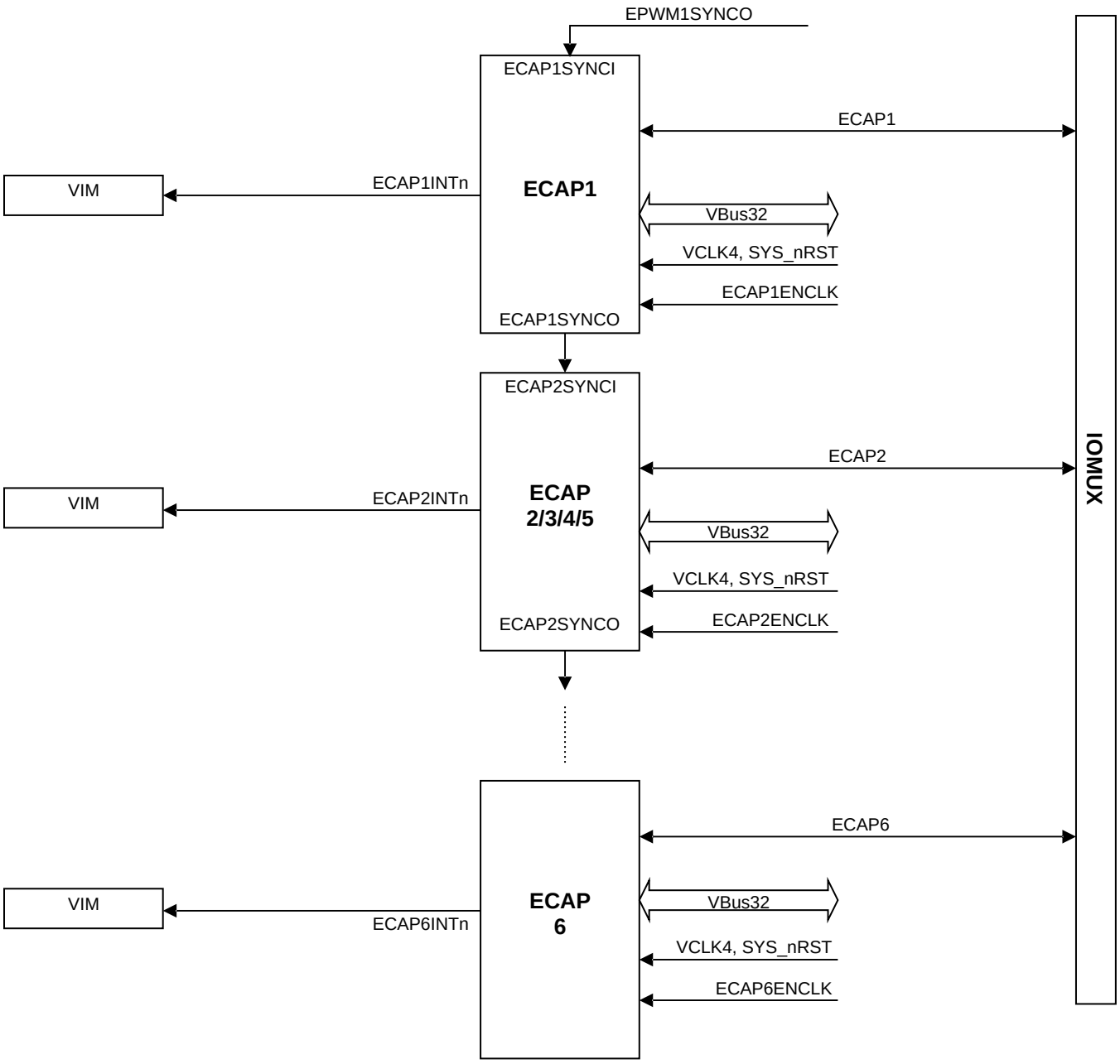
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, TZn input low	Asynchronous	2 * HSPCLKDIV * CLKDIV * $t_{c(VCLK4)}$ (1)		cycles
		Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 tc(VCLK4) + filter width		cycles

(1) For more information on the clock divider fields: HSPCLKDIV and CLKDIV, see the ePWM chapter of the device Technical Reference Manual.

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7.3 Enhanced Capture Modules (eCAP)

Figure 7-6 shows how the eCAP modules are interconnected on this microcontroller.



A. For more detail on the input synchronization selection of the ECAPx pins to each eCAPx module, see Figure 7-7.

Figure 7-6. eCAPx Module Connections

Figure 7-7 shows the detailed input synchronization selection (asynchronous, double-synchronous, or double-synchronous + filter width) for eCAPx.

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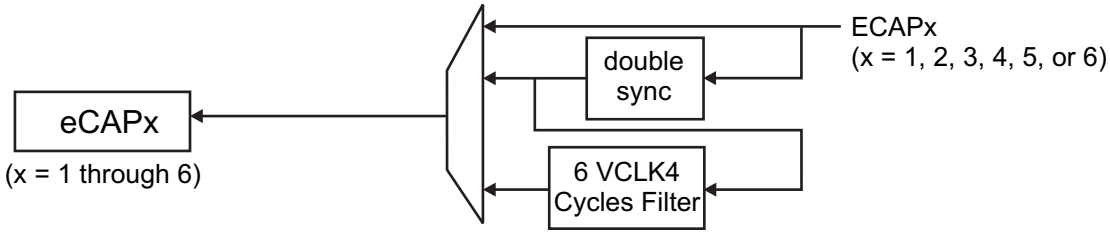


Figure 7-7. eCAPx Input Synchronization Selection Detail

7.3.1 Clock Enable Control for eCAPx Modules

Each of the ECAPx modules have a clock enable (ECAPxENCLK). These signals need to be generated from a device-level control register. When SYS_nRST is active low, the clock enables are ignored and the ECAPx logic is clocked so that it can reset to a proper state. When SYS_nRST goes in-active high, the state of clock enable is respected.

Table 7-11. eCAPx Clock Enable Control

ePWM Module Instance	Control Register to Enable Clock	Default Value
eCAP1	PINMMR39[0]	1
eCAP2	PINMMR39[8]	1
eCAP3	PINMMR39[16]	1
eCAP4	PINMMR39[24]	1
eCAP5	PINMMR40[0]	1
eCAP6	PINMMR40[8]	1

The default value of the control registers to enable the clocks to the eCAPx modules is 1. This means that the VCLK4 clock connections to the eCAPx modules are enabled by default. The application can choose to gate off the VCLK4 clock to any eCAPx module individually by clearing the respective control register bit.

7.3.2 PWM Output Capability of eCAPx

When not used in capture mode, each of the eCAPx modules can be used as a single-channel PWM output. This is called the auxiliary PWM (APWM) mode of operation of the eCAP modules. Refer to the eCAP chapter of the device Technical Reference Manual for more information.

7.3.3 Input Connection to eCAPx Modules

The input connection to each of the eCAP modules can be selected between a double-VCLK4-synchronized input or a double-VCLK4-synchronized and filtered input, as shown in Table 7-12.

Table 7-12. Device-Level Input Connection to eCAPx Modules

Input Signal	Control for Double-Synchronized Connection to eCAPx	Control for Double-Synchronized and Filtered Connection(1) to eCAPx
eCAP1	PINMMR43[0] = 1	PINMMR43[0] = 0 AND PINMMR43[1] = 1
eCAP2	PINMMR43[8] = 1	PINMMR43[8] = 0 AND PINMMR43[9] = 1
eCAP3	PINMMR43[16] = 1	PINMMR43[16] = 0 AND PINMMR43[17] = 1
eCAP4	PINMMR43[24] = 1	PINMMR43[24] = 0 AND PINMMR43[25] = 1
eCAP5	PINMMR44[0] = 1	PINMMR44[0] = 0 AND PINMMR44[1] = 1
eCAP6	PINMMR44[8] = 1	PINMMR44[8] = 0 AND PINMMR44[9] = 1

(1) The filter width is 6 VCLK4 cycles.

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7.3.4 Enhanced Capture Module (eCAP) Timings

Table 7-13. eCAPx Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK4)}$ + filter width(1)		cycles

(1) The filter width is 6 VCLK4 cycles.

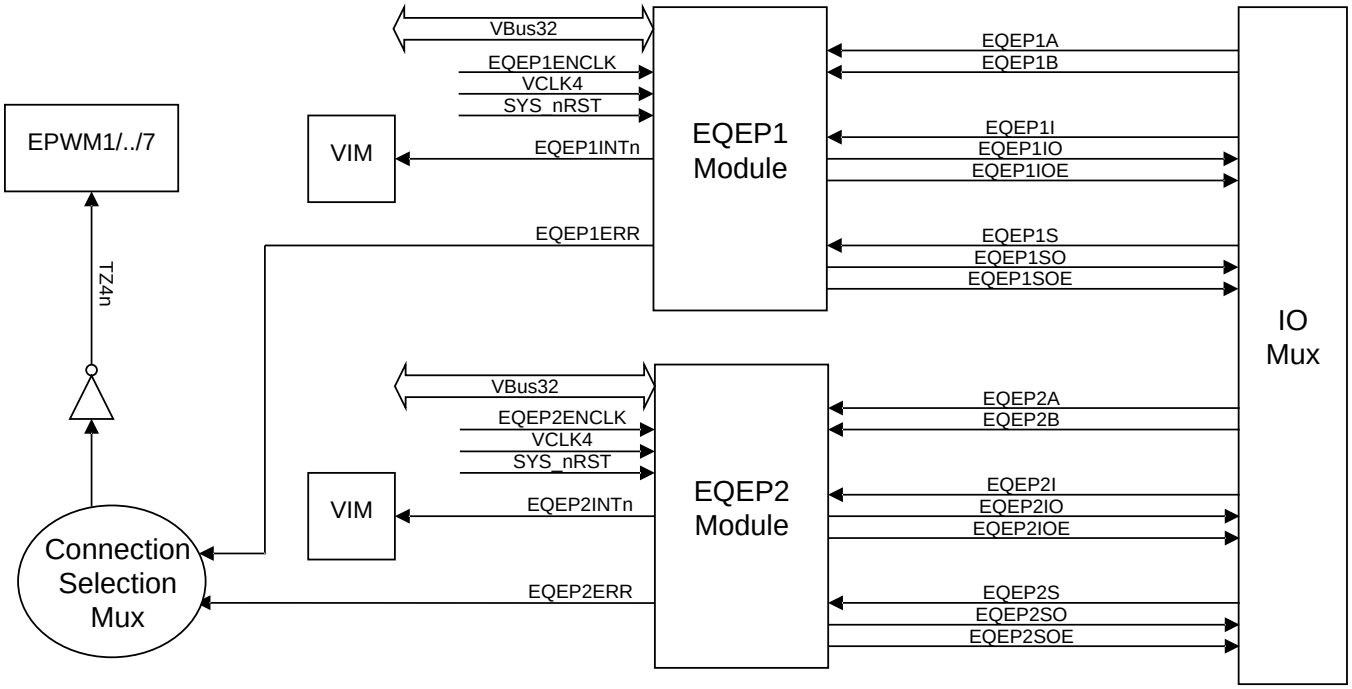
Table 7-14. eCAPx Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high or low		20		ns

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7.4 Enhanced Quadrature Encoder (eQEP)

Figure 7-8 shows the eQEP module interconnections on the device.



A. For more detail on the eQEP input synchronization selection of the EQEPxA/B pins to each eQEPx module, see Figure 7-9.

Figure 7-8. eQEP Module Interconnections

Figure 7-9 shows the detailed input synchronization selection (asynchronous, double-synchronous, or double-synchronous + filter width) for eQEPx.

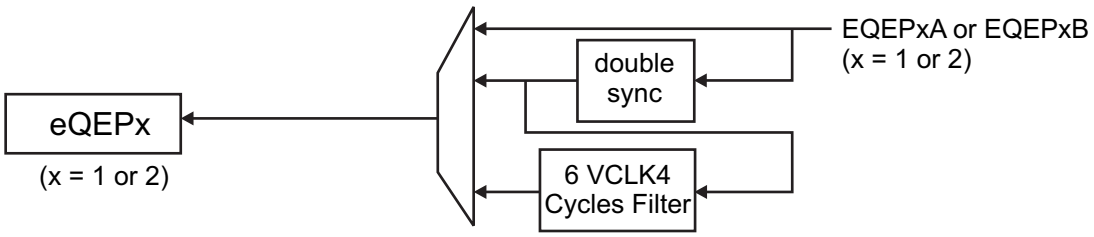


Figure 7-9. eQEPx Input Synchronization Selection Detail

7.4.1 Clock Enable Control for eQEPx Modules

Device-level control registers are implemented to generate the EQEPxENCLK signals. When SYS_nRST is active low, the clock enables are ignored and the eQEPx logic is clocked so that it can reset to a proper state. When SYS_nRST goes in-active high, the state of clock enable is respected.

Table 7-15. eQEPx Clock Enable Control

ePWM Module Instance	Control Register to Enable Clock	Default Value
eQEP1	PINMMR40[16]	1
eQEP2	PINMMR40[24]	1

The default value of the control registers to enable the clocks to the eQEPx modules is 1. This means that the VCLK4 clock connections to the eQEPx modules are enabled by default. The application can choose to gate off the VCLK4 clock to any eQEPx module individually by clearing the respective control register bit.

7.4.2 Using eQEPx Phase Error to Trip ePWMx Outputs

The eQEP module sets the EQEPERR signal output whenever a phase error is detected in its inputs EQEPxA and EQEPxB. This error signal from both the eQEP modules is input to the connection selection multiplexor. This multiplexor is defined in Table 7-7. As shown in Figure 7-3, the output of this selection multiplexor is inverted and connected to the TZ4n trip-zone input of all EPWMx modules. This connection allows the application to define the response of each ePWMx module on a phase error indicated by the eQEP modules.

7.4.3 Input Connections to eQEPx Modules

The input connections to each of the eQEP modules can be selected between a double-VCLK4-synchronized input or a double-VCLK4-synchronized and filtered input, as shown in Table 7-16.

Table 7-16. Device-Level Input Connection to eQEPx Modules

Input Signal	Control for Double-Synchronized Connection to eQEPx	Control for Double-Synchronized and Filtered Connection(1) to eQEPx
eQEP1A	PINMMR44[16] = 1	PINMMR44[16] = 0 and PINMMR44[17] = 1
eQEP1B	PINMMR44[24] = 1	PINMMR44[24] = 0 and PINMMR44[25] = 1
eQEP1I	PINMMR45[0] = 1	PINMMR45[0] = 0 and PINMMR45[1] = 1
eQEP1S	PINMMR45[8] = 1	PINMMR45[8] = 0 and PINMMR45[9] = 1
eQEP2A	PINMMR45[16] = 1	PINMMR45[16] = 0 and PINMMR45[17] = 1
eQEP2B	PINMMR45[24] = 1	PINMMR45[24] = 0 and PINMMR45[25] = 1
eQEP2I	PINMMR46[0] = 1	PINMMR46[0] = 0 and PINMMR46[1] = 1
eQEP2S	PINMMR46[8] = 1	PINMMR46[8] = 0 and PINMMR46[9] = 1

(1) The filter width is 6 VCLK4 cycles.

7.4.4 Enhanced Quadrature Encoder Pulse (eQEPx) Timing

Table 7-17. eQEPx Timing Requirements(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK4)}$ + filter width		cycles
$t_{w(INDEXH)}$	QEP Index Input High Time	Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK4)}$ + filter width		cycles
$t_{w(INDEXL)}$	QEP Index Input Low Time	Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK4)}$ + filter width		cycles
$t_{w(STROBH)}$	QEP Strobe Input High Time	Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK4)}$ + filter width		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low Time	Synchronous	2 $t_{c(VCLK4)}$		cycles
		Synchronous, with input filter	2 $t_{c(VCLK4)}$ + filter width		cycles

(1) The filter width is 6 VCLK4 cycles.

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Table 7-18. eQEPx Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		4 $t_{c(VCLK4)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		6 $t_{c(VCLK4)}$	cycles

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7.5 Multi-Buffered 12bit Analog-to-Digital Converter

The multibuffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on V_{SS} and V_{CC} from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to AD_{REFLO} unless otherwise noted.

Table 7-19. MibADC Overview

Description	Value
Resolution	12 bits
Monotonic	Assured
Output conversion code	00h to 3FFh [00 for $V_{AI} \le AD_{REFLO}$; 3FFh for $V_{AI} \ge AD_{REFHI}$]

7.5.1 Features

- 12-bit resolution
- AD_{REFHI} and AD_{REFLO} pins (high and low reference voltages)
- Total Sample/Hold/Convert time: 600ns Minimum at 30MHz ADCLK
- One memory region per conversion group is available (event, group 1, group 2)
- Allocation of channels to conversion groups is completely programmable
- Supports flexible channel conversion order
- Memory regions are serviced either by interrupt or by DMA
- Programmable interrupt threshold counter is available for each group
- Programmable magnitude threshold interrupt for each group for any one channel
- Option to read either 8-bit, 10-bit or 12-bit values from memory regions
- Single or continuous conversion modes
- Embedded self-test
- Embedded calibration logic
- Enhanced power-down mode
  - Optional feature to automatically power down ADC core when no conversion is in progress
- External event pin (ADxEVT) programmable as general-purpose I/O

7.5.2 Event Trigger Options

The ADC module supports 3 conversion groups: Event Group, Group1 and Group2. Each of these 3 groups can be configured to be hardware event-triggered. In that case, the application can select from among 8 event sources to be the trigger for a group's conversions.

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7.5.2.1 MibADC1 Event Trigger Hookup

Table 7-20. MibADC1 Event Trigger Hookup

Group Source Select, G1SRC, G2SRC or EVSRC	Event #	Trigger Event Signal				
		PINMMR30[0] = 1 (default)	PINMMR30[0] = 0 and PINMMR30[1] = 1			
			Option A	Control for Option A	Option B	Control for Option B
000	1	AD1EVT	AD1EVT	—	AD1EVT	—
001	2	N2HET1[8]	N2HET2[5]	PINMMR30[8] = 1	ePWM_B	PINMMR30[8] = 0 and PINMMR30[9] = 1
010	3	N2HET1[10]	N2HET1[27]	—	N2HET1[27]	—
011	4	RTI Compare 0 Interrupt	RTI Compare 0 Interrupt	PINMMR30[16] = 1	ePWM_A1	PINMMR30[16] = 0 and PINMMR30[17] = 1
100	5	N2HET1[12]	N2HET1[17]	—	N2HET1[17]	—
101	6	N2HET1[14]	N2HET1[19]	PINMMR30[24] = 1	N2HET2[1]	PINMMR30[24] = 0 and PINMMR30[25] = 1
110	7	GIOB[0]	N2HET1[11]	PINMMR31[0] = 1	ePWM_A2	PINMMR31[0] = 0 and PINMMR31[1] = 1
111	8	GIOB[1]	N2HET2[13]	PINMMR32[16] = 1	ePWM_AB	PINMMR31[8] = 0 and PINMMR31[9] = 1

NOTE

If ADEVT, N2HET1 or GIOB is used as a trigger source, the connection to the MibADC1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad (via the mux control), or by driving the function from an external trigger source as input. If the mux control module is used to select different functionality instead of the ADEVT, N2HET1[x] or GIOB[x] signals, then care must be taken to disable these signals from triggering conversions; there is no multiplexing on the input connections.

If ePWM_B, ePWM_A2, ePWM_AB, N2HET2[1], N2HET2[5], N2HET2[13], N2HET1[11], N2HET1[17] or N2HET1[19] is used to trigger the ADC the connection to the ADC is made directly from the N2HET or ePWM module outputs. As a result, the ADC can be triggered without having to enable the signal from being output on a device terminal.

NOTE

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

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7.5.2.2 MibADC2 Event Trigger Hookup

Table 7-21. MibADC2 Event Trigger Hookup

Group Source Select, G1SRC, G2SRC or EVSRC	Event #	Trigger Event Signal				
		PINMMR30[0] = 1 (default)	PINMMR30[0] = 0 and PINMMR30[1] = 1			
			Option A	Control for Option A	Option B	Control for Option B
000	1	AD2EVT	AD2EVT	—	AD2EVT	—
001	2	N2HET1[8]	N2HET2[5]	PINMMR31[16] = 1	ePWM_B	PINMMR31[16] = 0 and PINMMR31[17] = 1
010	3	N2HET1[10]	N2HET1[27]	—	N2HET1[27]	—
011	4	RTI Compare 0 Interrupt	RTI Compare 0 Interrupt	PINMMR31[24] = 1	ePWM_A1	PINMMR31[24] = 0 and PINMMR31[25] = 1
100	5	N2HET1[12]	N2HET1[17]	—	N2HET1[17]	—
101	6	N2HET1[14]	N2HET1[19]	PINMMR32[0] = 1	N2HET2[1]	PINMMR32[0] = 0 and PINMMR32[1] = 1
110	7	GIOB[0]	N2HET1[11]	PINMMR32[8] = 1	ePWM_A2	PINMMR32[8] = 0 and PINMMR32[9] = 1
111	8	GIOB[1]	N2HET2[13]	PINMMR32[16] = 1	ePWM_AB	PINMMR32[16] = 0 and PINMMR32[17] = 1

NOTE

If AD2EVT, N2HET1 or GIOB is used as a trigger source, the connection to the MibADC2 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by configuring the function as output onto the pad (via the mux control), or by driving the function from an external trigger source as input. If the mux control module is used to select different functionality instead of the AD2EVT, N2HET1[x] or GIOB[x] signals, then care must be taken to disable these signals from triggering conversions; there is no multiplexing on the input connections.

If ePWM_B, ePWM_A2, ePWM_AB, N2HET2[5], N2HET2[1], N2HET2[13], N2HET1[11], N2HET1[17] or N2HET1[19] is used to trigger the ADC the connection to the ADC is made directly from the N2HET or ePWM module outputs. As a result, the ADC can be triggered without having to enable the signal from being output on a device terminal.

NOTE

For the RTI compare 0 interrupt source, the connection is made directly from the output of the RTI module. That is, the interrupt condition can be used as a trigger source even if the actual interrupt is not signaled to the CPU.

7.5.2.3 Controlling ADC1 and ADC2 Event Trigger Options Using SOC Output from ePWM Modules

As shown in Figure 7-10, the ePWMxSOCA and ePWMxSOCB outputs from each ePWM module are used to generate 4 signals – ePWM_B, ePWM_A1, ePWM_A2 and ePWM_AB, that are available to trigger the ADC based on the application requirement.

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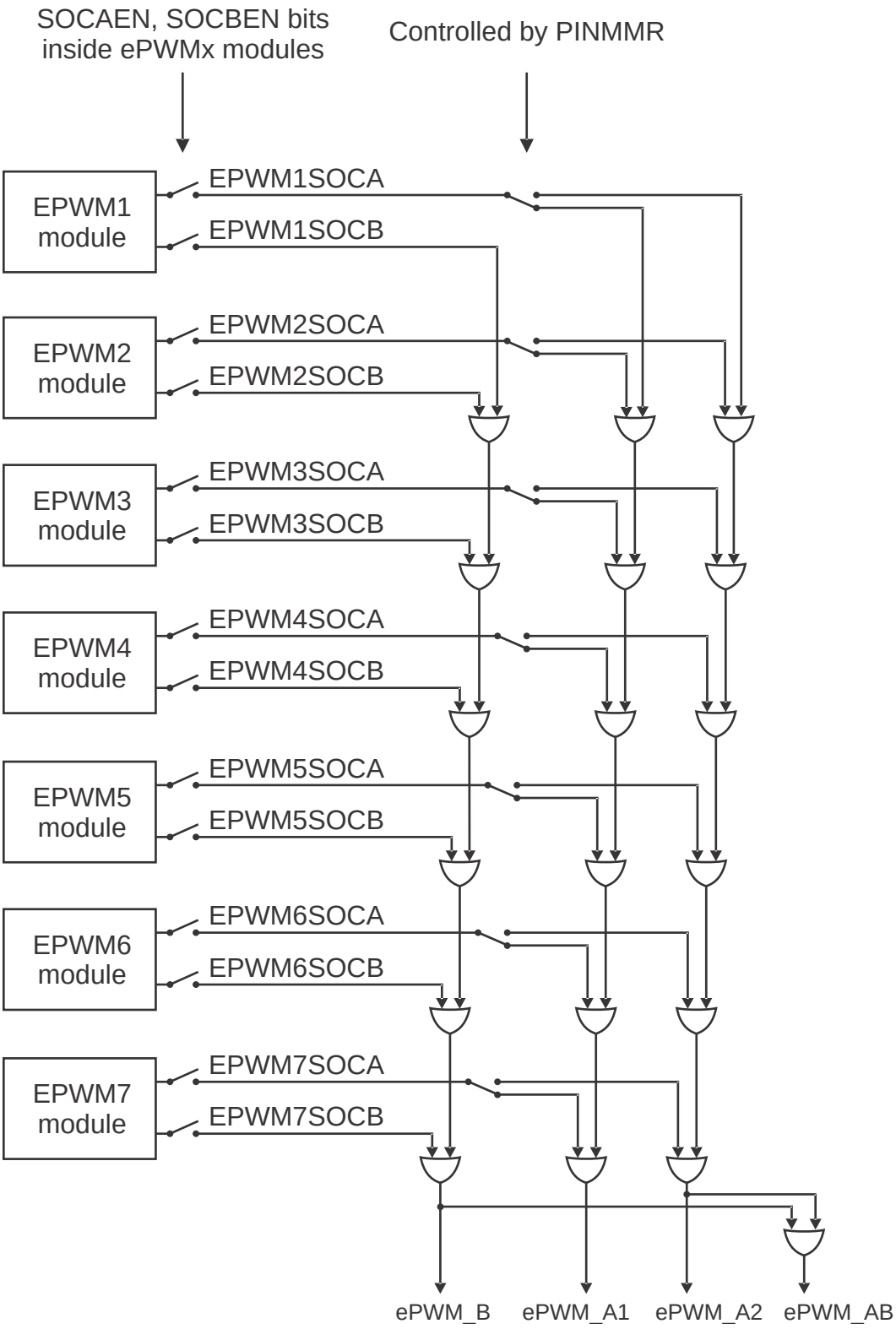


Figure 7-10. ADC Trigger Source Generation from ePWMx

Table 7-22. Control Bit to SOC Output

Control Bit	SOC Output
PINMMR35[0]	SOC1A_SEL
PINMMR35[8]	SOC2A_SEL
PINMMR35[16]	SOC3A_SEL
PINMMR35[24]	SOC4A_SEL
PINMMR36[0]	SOC5A_SEL
PINMMR36[8]	SOC6A_SEL
PINMMR36[16]	SOC7A_SEL

The SOCA output from each ePWM module is connected to a "switch" shown in Figure 7-10.

The logic equations for the 4 outputs from the combinational logic shown in Figure 7-10 are:

ePWM_B = SOC1B or SOC2B or SOC3B or SOC4B or SOC5B or SOC6B or SOC7B

ePWM_A1 = [SOC1A and not(SOC1A_SEL)] or [SOC2A and not(SOC2A_SEL)] or [SOC3A and not(SOC3A_SEL)] or [SOC4A and not(SOC4A_SEL)] or [SOC5A and not(SOC5A_SEL)] or [SOC6A and not(SOC6A_SEL)] or [SOC7A and not(SOC7A_SEL)]

ePWM_A2 = [SOC1A and SOC1A_SEL] or [SOC2A and SOC2A_SEL] or [SOC3A and SOC3A_SEL] or [SOC4A and SOC4A_SEL] or [SOC5A and SOC5A_SEL] or [SOC6A and SOC6A_SEL] or [SOC7A and SOC7A_SEL]

ePWM_AB = ePWM_B or ePWM_A2

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7.5.3 ADC Electrical and Timing Specifications

Table 7-23. MibADC Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high-voltage reference source	AD_{REFLO}	V_{CCAD} (1)	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD} (1)	AD_{REFHI}	V
V_{AI}	Analog input voltage	AD_{REFLO}	AD_{REFHI}	V
I_{AIC}	Analog input clamp current (2) (VAI < VSSAD – 0.3 or VAI > VCCAD + 0.3)	–2	2	mA

(1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see Table Section 5.4.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

Table 7-24. MibADC Electrical Characteristics Over Full Ranges of Recommended Operating Conditions

PARAMETER		DESCRIPTION/CONDITIONS		MIN	TYP	MAX	UNIT
R_{mux}	Analog input mux on-resistance	See Figure 7-11				250	Ω
R_{samp}	ADC sample switch on-resistance	See Figure 7-11				250	Ω
C_{mux}	Input mux capacitance	See Figure 7-11				16	pF
C_{samp}	ADC sample capacitance	See Figure 7-11				13	pF
I_{AIL}	Analog off-state input leakage current	V_{CCAD} = 3.6 V maximum	$V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100mV	–300		200	nA
			V_{SSAD} + 100mV ≤ $V_{IN} \le V_{CCAD}$ – 200mV	–200		200	nA
			V_{CCAD} – 200mV < $V_{IN} \le V_{CCAD}$	–200		500	nA
I_{AIL}	Analog off-state input leakage current	V_{CCAD} = 5.25 V maximum	$V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300mV	–1000		250	nA
			V_{SSAD} + 300mV ≤ $V_{IN} \le V_{CCAD}$ – 300mV	–250		250	nA
			V_{CCAD} – 300mV < $V_{IN} \le V_{CCAD}$	–250		1000	nA
I_{AOSB1} (1)	ADC1 Analog on-state input bias current	V_{CCAD} = 3.6 V maximum	$V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100mV	–8		2	µA
			V_{SSAD} + 100mV < V_{IN} < V_{CCAD} – 200mV	–4		2	µA
			V_{CCAD} – 200mV < V_{IN} < V_{CCAD}	–4		12	µA
I_{AOSB2} (1)	ADC2 Analog on-state input bias current	V_{CCAD} = 3.6 V maximum	$V_{SSAD} \le V_{IN} < V_{SSAD}$ + 100mV	–7		2	µA
			V_{SSAD} + 100mV ≤ $V_{IN} \le V_{CCAD}$ – 200mV	–4		2	µA
			V_{CCAD} - 200mV < $V_{IN} \le V_{CCAD}$	–4		10	µA
I_{AOSB1} (1)	ADC1 Analog on-state input bias current	V_{CCAD} = 5.25 V maximum	$V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300mV	–10		3	µA
			V_{SSAD} + 300mV ≤ $V_{IN} \le V_{CCAD}$ – 300mV	–5		3	µA
			V_{CCAD} – 300mV < $V_{IN} \le V_{CCAD}$	–5		14	µA
I_{AOSB2} (1)	ADC2 Analog on-state input bias current	V_{CCAD} = 5.25 V maximum	$V_{SSAD} \le V_{IN} < V_{SSAD}$ + 300mV	–8		3	µA
			V_{SSAD} + 300mV ≤ $V_{IN} \le V_{CCAD}$ – 300mV	–5		3	µA
			V_{CCAD} – 300mV < $V_{IN} \le V_{CCAD}$	–5		12	µA
$I_{ADREFHI}$	AD_{REFHI} input current	AD_{REFHI} = V_{CCAD}, AD_{REFLO} = V_{SSAD}				3	mA
I_{CCAD}	Static supply current	Normal operating mode				15	mA
		ADC core in power down mode				5	µA

(1) If a shared channel is being converted by both ADC converters at the same time, the on-state leakage is equal to I_{AOSB1} + I_{AOSB2}.

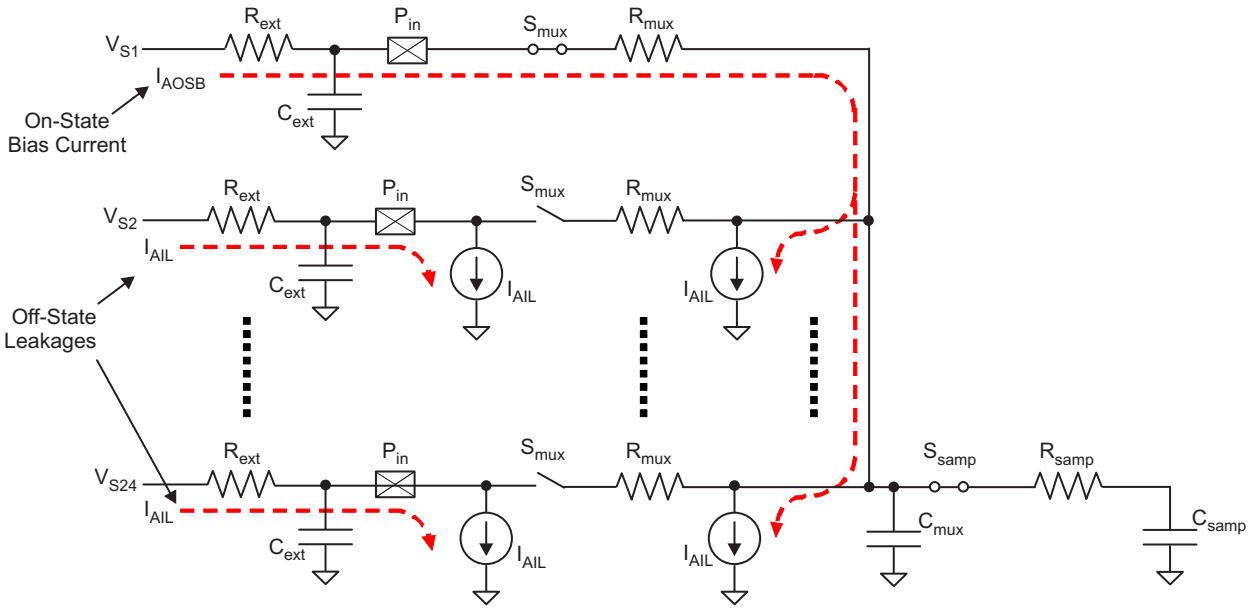


Figure 7-11. MibADC Input Equivalent Circuit

Table 7-25. MibADC Timing Specifications

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(ADCLK)}$ (1)	Cycle time, MibADC clock	0.033			µs
$t_{d(SH)}$ (2)	Delay time, sample and hold time	0.2			µs
$t_{d(PU-ADV)}$	Delay time from ADC power on until first input can be sampled	1			µs
12-Bit Mode					
$t_{d(C)}$	Delay time, conversion time	0.4			µs
$t_{d(SHC)}$ (3)	Delay time, total sample/hold and conversion time	0.6			µs
10-Bit Mode					
$t_{d(C)}$	Delay time, conversion time	0.33			µs
$t_{d(SHC)}$ (3)	Delay time, total sample/hold and conversion time	0.53			µs

(1) The MibADC clock is the ADCLK, generated by dividing down the VCLK by a prescale factor defined by the ADCLOCKCR register bits 4:0.
(2) The sample and hold time for the ADC conversions is defined by the ADCLK frequency and the AD<GP>SAMP register for each conversion group. The sample time needs to be determined by accounting for the external impedance connected to the input channel as well as the ADC's internal impedance.
(3) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors, for example, the prescale settings.

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Table 7-26. MibADC Operating Characteristics Over Full Ranges of Recommended Operating Conditions(1)(2)

PARAMETER		DESCRIPTION/CONDITIONS		MIN	MAX	UNIT
CR	Conversion range over which specified accuracy is maintained	$AD_{REFHI} - AD_{REFLO}$		3	5.25	V
Z_{SET}	Zero Scale Offset	Difference between the first ideal transition (from code 000h to 001h) and the actual transition	10-bit mode		1	LSB
			12-bit mode		2	LSB
F_{SET}	Full Scale Offset	Difference between the range of the measured code transitions (from first to last) and the range of the ideal code transitions	10-bit mode		2	LSB
			12-bit mode		3	LSB
E_{DNL}	Differential nonlinearity error	Difference between the actual step width and the ideal value. (see Figure 7-12)	10-bit mode		± 1.5	LSB
			12-bit mode		± 2	LSB
E_{INL}	Integral nonlinearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error.	10-bit mode		± 2	LSB
			12-bit mode		± 2	LSB
E_{TOT}	Total unadjusted error	Maximum value of the difference between an analog value and the ideal midstep value.	10-bit mode		± 2	LSB
			12-bit mode		± 4	LSB

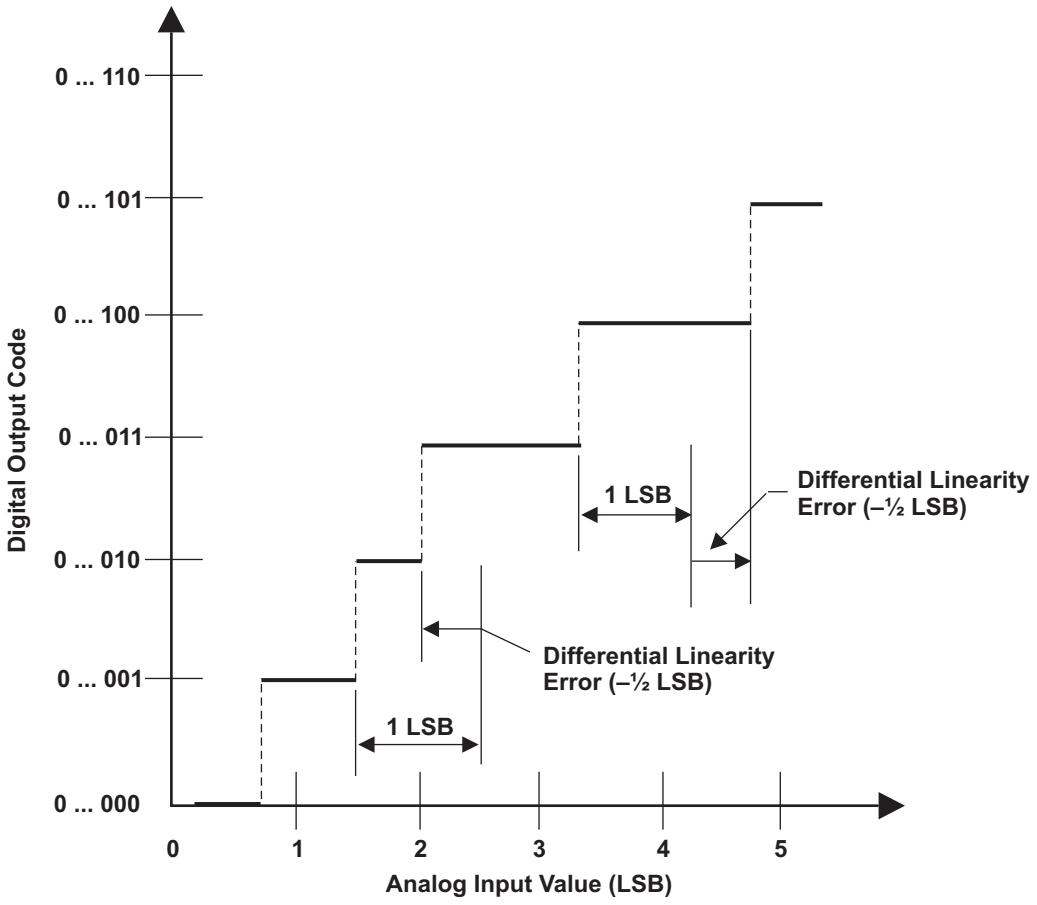
(1) 1 LSB = $(AD_{REFHI} - AD_{REFLO})/ 2^{12}$ for 12-bit mode
(2) 1 LSB = $(AD_{REFHI} - AD_{REFLO})/ 2^{10}$ for 10-bit mode

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7.5.4 Performance (Accuracy) Specifications

7.5.4.1 MibADC Nonlinearity Errors

The differential nonlinearity error shown in Figure 7-12 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.

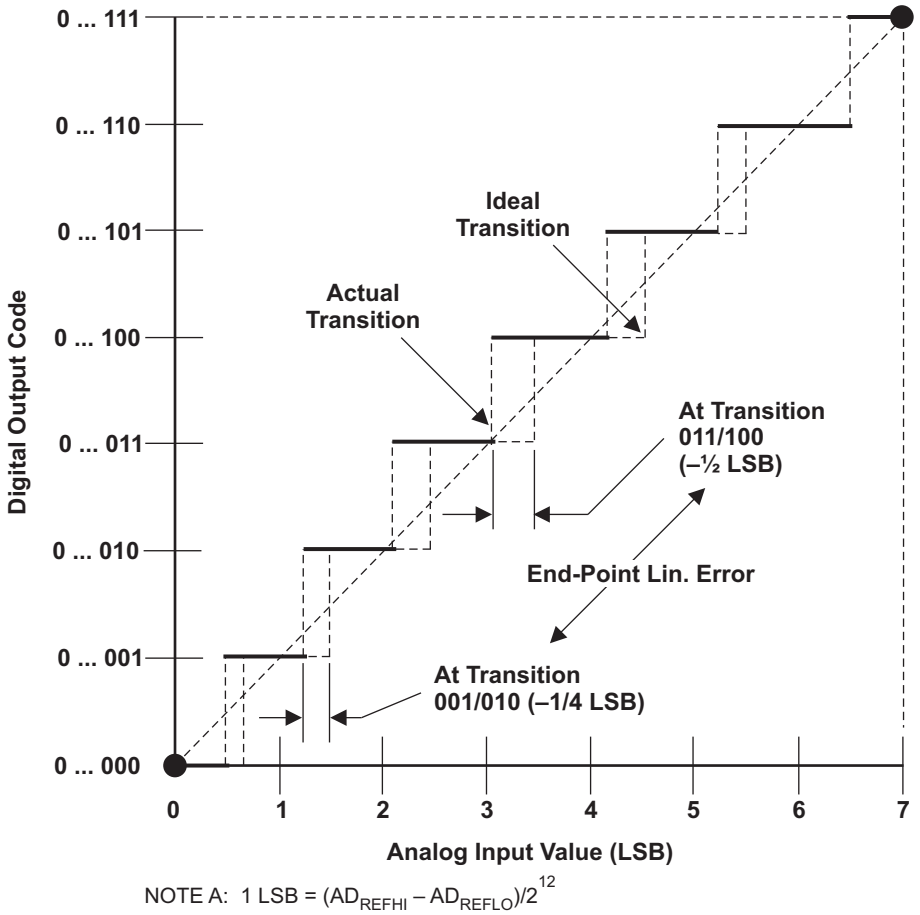


NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

Figure 7-12. Differential Nonlinearity (DNL) Error

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The integral nonlinearity error shown in Figure 7-13 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

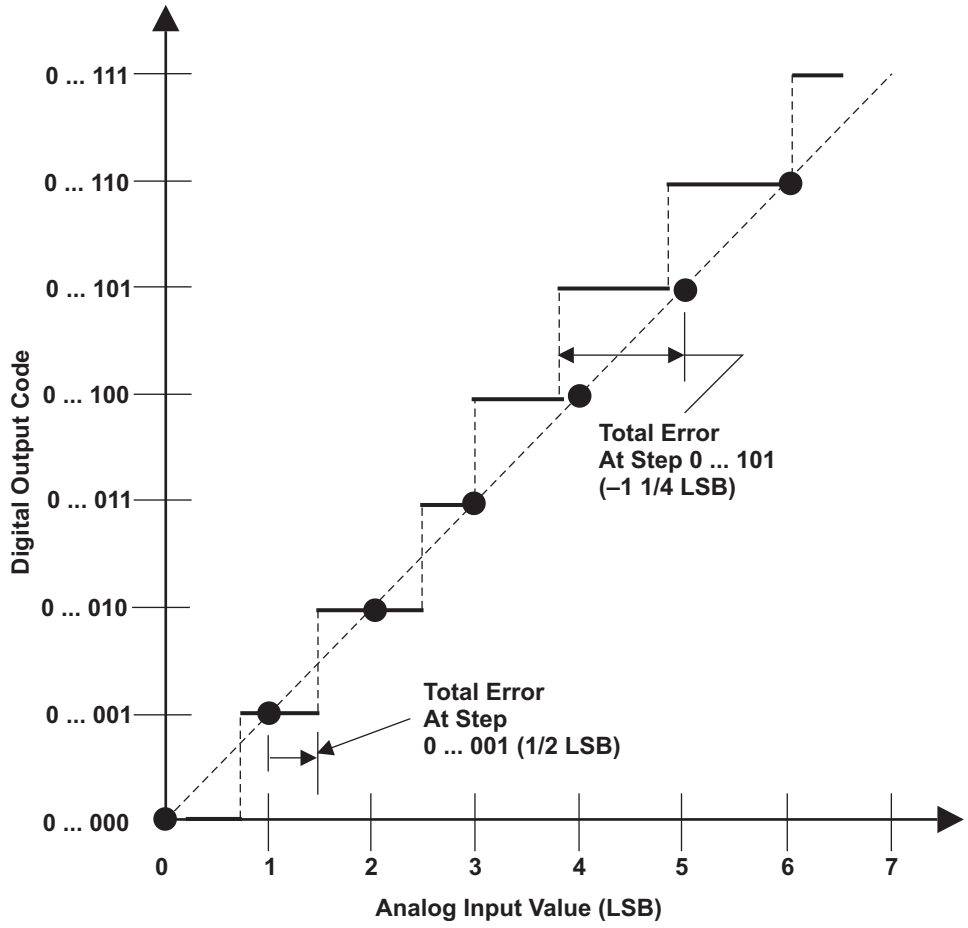


NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

Figure 7-13. Integral Nonlinearity (INL) Error

7.5.4.2 MibADC Total Error

The absolute accuracy or total error of an MibADC as shown in Figure 7-14 is the maximum value of the difference between an analog value and the ideal midstep value.



NOTE A: 1 LSB = $(AD_{REFHI} - AD_{REFLO})/2^{12}$

Figure 7-14. Absolute Accuracy (Total) Error

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7.6 General-Purpose Input/Output

The GPIO module on this device supports two ports, GIOA and GIOB. The I/O pins are bidirectional and bit-programmable. Both GIOA and GIOB support external interrupt capability.

7.6.1 Features

The GPIO module has the following features:

- Each IO pin can be configured as:
  - Input
  - Output
  - Open Drain
- The interrupts have the following characteristics:
  - Programmable interrupt detection either on both edges or on a single edge (set in GIOINTDET)
  - Programmable edge-detection polarity, either rising or falling edge (set in GIOPOL register)
  - Individual interrupt flags (set in GIOFLG register)
  - Individual interrupt enables, set and cleared through GIOENASET and GIOENACLR registers respectively
  - Programmable interrupt priority, set through GIOLVLSET and GIOLVLCLR registers
- Internal pullup/pulldown allows unused I/O pins to be left unconnected

For information on input and output timings see Section 7.1.1 and Section 7.1.2

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7.7 Enhanced High-End Timer (N2HET)

The N2HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The N2HET can be used for pulse width modulated outputs, capture or compare inputs, or general-purpose I/O.. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses.

7.7.1 Features

The N2HET module has the following features:

- Programmable timer for input and output timing functions
- Reduced instruction set (30 instructions) for dedicated time and angle functions
- 160 words of instruction RAM protected by parity
- User defined number of 25-bit virtual counters for timer, event counters and angle counters
- 7-bit hardware counters for each pin allow up to 32-bit resolution in conjunction with the 25-bit virtual counters
- Up to 32 pins usable for input signal measurements or output signal generation
- Programmable suppression filter for each input pin with adjustable limiting frequency
- Low CPU overhead and interrupt load
- Efficient data transfer to or from the CPU memory with dedicated High-End-Timer Transfer Unit (HTU) or DMA
- Diagnostic capabilities with different loopback mechanisms and pin status readback functionality

7.7.2 N2HET RAM Organization

The timer RAM uses 4 RAM banks, where each bank has two port access capability. This means that one RAM address may be written while another address is read. The RAM words are 96-bits wide, which are split into three 32-bit fields (program, control, and data).

7.7.3 Input Timing Specifications

The N2HET instructions PCNT and WCAP impose some timing constraints on the input signals.

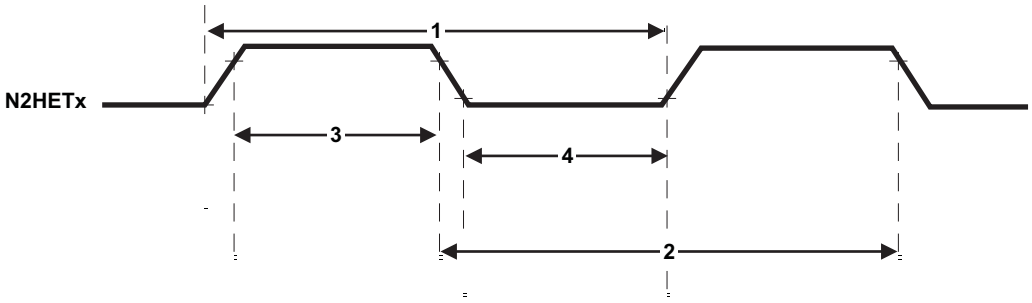


Figure 7-15. N2HET Input Capture Timings

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Table 7-27. Dynamic Characteristics for the N2HET Input Capture Functionality

	PARAMETER	MIN	MAX	UNIT
1	Input signal period, PCNT or WCAP for rising edge to rising edge	(HRP) (LRP) $tc_{(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $tc_{(VCLK2)}$ - 2	ns
2	Input signal period, PCNT or WCAP for falling edge to falling edge	(HRP) (LRP) $tc_{(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $tc_{(VCLK2)}$ - 2	ns
3	Input signal high phase, PCNT or WCAP for rising edge to falling edge	2 (HRP) $tc_{(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $tc_{(VCLK2)}$ - 2	ns
4	Input signal low phase, PCNT or WCAP for falling edge to rising edge	2 (HRP) $tc_{(VCLK2)}$ + 2	2^{25} (HRP) (LRP) $tc_{(VCLK2)}$ - 2	ns

7.7.4 N2HET1-N2HET2 Synchronization

In some applications the N2HET resolutions must be synchronized. Some other applications require a single time base to be used for all PWM outputs and input timing captures.

The N2HET provides such a synchronization mechanism. The Clk_master/slave (HETGCR.16) configures the N2HET in master or slave mode (default is slave mode). A N2HET in master mode provides a signal to synchronize the prescalers of the slave N2HET. The slave N2HET synchronizes its loop resolution to the loop resolution signal sent by the master. The slave does not require this signal after it receives the first synchronization signal. However, anytime the slave receives the re-synchronization signal from the master, the slave must synchronize itself again..

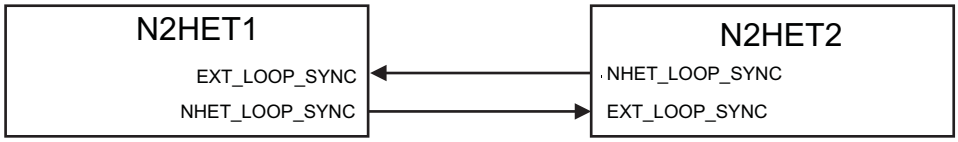


Figure 7-16. N2HET1 – N2HET2 Synchronization Hookup

7.7.5 N2HET Checking

7.7.5.1 Internal Monitoring

To assure correctness of the high-end timer operation and output signals, the two N2HET modules can be used to monitor each other's signals as shown in Figure 7-17. The direction of the monitoring is controlled by the I/O multiplexing control module.

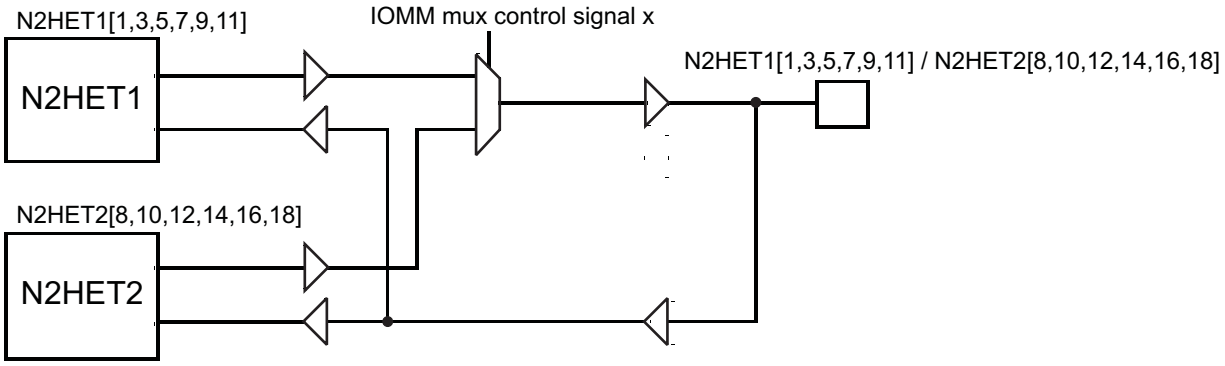


Figure 7-17. N2HET Monitoring

7.7.5.2 Output Monitoring using Dual Clock Comparator (DCC)

N2HET1[31] is connected as a clock source for counter 1 in DCC1. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET1[31].

Similarly, N2HET2[0] is connected as a clock source for counter 1 in DCC2. This allows the application to measure the frequency of the pulse-width modulated (PWM) signal on N2HET2[0].

Both N2HET1[31] and N2HET2[0] can be configured to be internal-only channels. That is, the connection to the DCC module is made directly from the output of the N2HETx module (from the input of the output buffer).

For more information on DCC see Section 6.7.3.

7.7.6 Disabling N2HET Outputs

Some applications require the N2HET outputs to be disabled under some fault condition. The N2HET module provides this capability via the "Pin Disable" input signal. This signal, when driven low, causes the N2HET outputs identified by a programmable register (HETPINDIS) to be tri-stated. Please refer to the device Terminal Reference Manual for more details on the "N2HET Pin Disable" feature.

GIOA[5] is connected to the "Pin Disable" input for N2HET1, and GIOB[2] is connected to the "Pin Disable" input for N2HET2.

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7.7.7 High-End Timer Transfer Unit (HET-TU)

A High End Timer Transfer Unit (HET-TU) can perform DMA type transactions to transfer N2HET data to or from main memory. A Memory Protection Unit (MPU) is built into the HET-TU.

7.7.7.1 Features

- CPU and DMA independent
- Master Port to access system memory
- 8 control packets supporting dual buffer configuration
- Control packet information is stored in RAM protected by parity
- Event synchronization (HET transfer requests)
- Supports 32 or 64 bit transactions
- Addressing modes for HET address (8 byte or 16 byte) and system memory address (fixed, 32 bit or 64bit)
- One shot, circular and auto switch buffer transfer modes
- Request lost detection

7.7.7.2 Trigger Connections

Table 7-28. HET TU1 Request Line Connection

Modules	Request Source	HET TU1 Request
N2HET1	HTUREQ[0]	HET TU1 DCP[0]
N2HET1	HTUREQ[1]	HET TU1 DCP[1]
N2HET1	HTUREQ[2]	HET TU1 DCP[2]
N2HET1	HTUREQ[3]	HET TU1 DCP[3]
N2HET1	HTUREQ[4]	HET TU1 DCP[4]
N2HET1	HTUREQ[5]	HET TU1 DCP[5]
N2HET1	HTUREQ[6]	HET TU1 DCP[6]
N2HET1	HTUREQ[7]	HET TU1 DCP[7]

Table 7-29. HET TU2 Request Line Connection

Modules	Request Source	HET TU2 Request
N2HET2	HTUREQ[0]	HET TU2 DCP[0]
N2HET2	HTUREQ[1]	HET TU2 DCP[1]
N2HET2	HTUREQ[2]	HET TU2 DCP[2]
N2HET2	HTUREQ[3]	HET TU2 DCP[3]
N2HET2	HTUREQ[4]	HET TU2 DCP[4]
N2HET2	HTUREQ[5]	HET TU2 DCP[5]
N2HET2	HTUREQ[6]	HET TU2 DCP[6]
N2HET2	HTUREQ[7]	HET TU2 DCP[7]

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7.8 Controller Area Network (DCAN)

The DCAN supports the CAN 2.0B protocol standard and uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring.

7.8.1 Features

Features of the DCAN module include:

- Supports CAN protocol version 2.0 part A, B
- Bit rates up to 1 MBit/s
- The CAN kernel can be clocked by the oscillator for baud-rate generation.
- 64 mailboxes on each DCAN
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Automatic bus on after Bus-Off state by a programmable 32-bit timer
- Message RAM protected by parity
- Direct access to Message RAM during test mode
- CAN Rx / Tx pins configurable as general purpose IO pins
- Message RAM Auto Initialization
- DMA support

For more information on the DCAN see the device Technical Reference Manual.

7.8.2 Electrical and Timing Specifications

Table 7-30. Dynamic Characteristics for the DCANx TX and RX pins

Parameter		MIN	MAX	Unit
$t_{d(CANnTX)}$	Delay time, transmit shift register to CANnTX pin (1)		15	ns
$t_{d(CANnRX)}$	Delay time, CANnRX pin to receive shift register		5	ns

(1) These values do not include rise/fall times of the output buffer.

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7.9 Local Interconnect Network Interface (LIN)

The SCI/LIN module can be programmed to work either as an SCI or as a LIN. The core of the module is an SCI. The SCI's hardware features are augmented to achieve LIN compatibility.

The SCI module is a universal asynchronous receiver-transmitter that implements the standard nonreturn to zero format. The SCI can be used to communicate, for example, through an RS-232 port or over a K-line.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-master/multiple-slave with a message identification for multi-cast transmission between any network nodes.

7.9.1 LIN Features

The following are features of the LIN module:

- Compatible to LIN 1.3, 2.0 and 2.1 protocols
- Multi-buffered receive and transmit units DMA capability for minimal CPU intervention
- Identification masks for message filtering
- Automatic Master Header Generation
  - Programmable Synch Break Field
  - Synch Field
  - Identifier Field
- Slave Automatic Synchronization
  - Synch break detection
  - Optional baudrate update
  - Synchronization Validation
- 2^{31} programmable transmission rates with 7 fractional bits
- Error detection
- 2 Interrupt lines with priority encoding

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7.10 Serial Communication Interface (SCI)

7.10.1 Features

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard nonreturn to zero (NRZ) format
- Double-buffered receive and transmit functions
- Configurable frame format of 3 to 13 bits per character based on the following:
  - Data word length programmable from one to eight bits
  - Additional address bit in address-bit mode
  - Parity programmable for zero or one parity bit, odd or even parity
  - Stop programmable for one or two stop bits
- Asynchronous or isosynchronous communication modes
- Two multiprocessor communication formats allow communication between more than two devices.
- Sleep mode is available to free CPU resources during multiprocessor communication.
- The 24-bit programmable baud rate supports 2^{24} different baud rates provide high accuracy baud rate selection.
- Four error flags and Five status flags provide detailed information regarding SCI events.
- Capability to use DMA for transmit and receive data.

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7.11 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module is a multimaster communication module providing an interface between the TMS570 microcontroller and devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I2C-bus. This module will support any slave or master I2C compatible device.

7.11.1 Features

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
  - Bit/Byte format transfer
  - 7-bit and 10-bit device addressing modes
  - General call
  - START byte
  - Multimaster transmitter/ slave receiver mode
  - Multimaster receiver/ slave transmitter mode
  - Combined master transmit/receive and receive/transmit mode
  - Transfer rates of 10 kbps up to 400 kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Seven interrupts that can be used by the CPU
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

NOTE

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the slave address second byte every time it sends the slave address first byte)

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7.11.2 I2C I/O Timing Specifications

Table 7-31. I2C Signals (SDA and SCL) Switching Characteristics(1)

Parameter		Standard Mode		Fast Mode		Unit
		MIN	MAX	MIN	MAX	
$t_{c(I2CCLK)}$	Cycle time, Internal Module clock for I2C, prescaled from VCLK	75.2	149	75.2	149	ns
$f_{(SCL)}$	SCL Clock frequency	0	100	0	400	kHz
$t_{c(SCL)}$	Cycle time, SCL	10		2.5		µs
$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7		0.6		µs
$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a repeated START condition)	4		0.6		µs
$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		1.3		µs
$t_{w(SCLH)}$	Pulse duration, SCL high	4		0.6		µs
$t_{su(SDA-SCLH)}$	Setup time, SDA valid before SCL high	250		100		ns
$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low (for I2C bus devices)	0	3.45(2)	0	0.9	µs
$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7		1.3		µs
$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4.0		0.6		µs
$t_{w(SP)}$	Pulse duration, spike (must be suppressed)			0	50	ns
C_b(3)	Capacitive load for each bus line		400		400	pF

(1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
(2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
(3) C_b = The total capacitance of one bus line in pF.

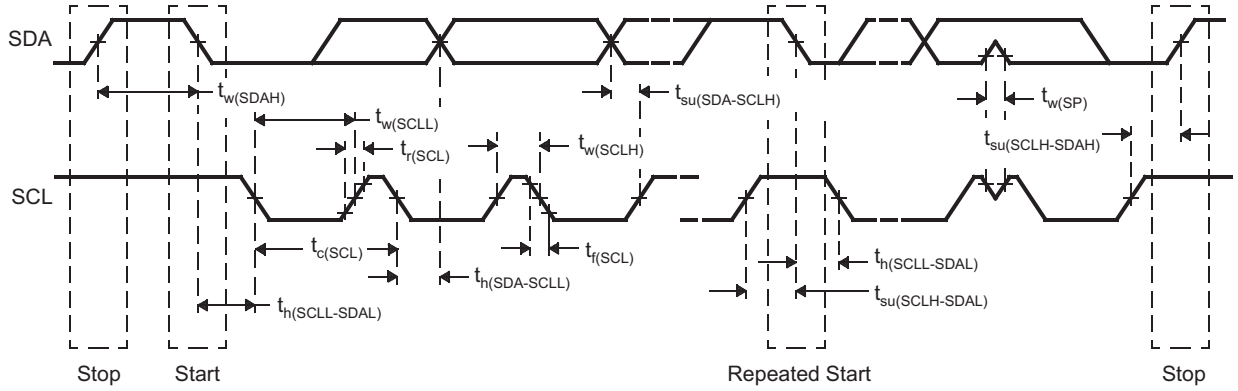


Figure 7-18. I2C Timings

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NOTE

- A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.
- A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-SCLH)}$.
- C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

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7.12 Multibuffered / Standard Serial Peripheral Interface

The MibSPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (2 to 16 bits) to be shifted in and out of the device at a programmed bit-transfer rate. Typical applications for the SPI include interfacing to external peripherals, such as I/Os, memories, display drivers, and analog-to-digital converters.

7.12.1 Features

Both Standard and MibSPI modules have the following features:

- 16-bit shift register
- Receive buffer register
- 11-bit baud clock generator
- SPICLK can be internally-generated (master mode) or received from an external clock source (slave mode)
- Each word transferred can have a unique format
- SPI I/Os not used in the communication can be used as digital input/output signals

Table 7-32. MibSPI/SPI Configurations

MibSPIx/SPIx	I/Os
MibSPI1	MIBSPI1SIMO[1:0], MIBSPI1SOMI[1:0], MIBSPI1CLK, MIBSPI1nCS[5:4,2:0], MIBSPI1nENA
MibSPI3	MIBSPI3SIMO, MIBSPI3SOMI, MIBSPI3CLK, MIBSPI3nCS[5:0], MIBSPI3nENA
MibSPI5	MIBSPI5SIMO[3:0], MIBSPI5SOMI[3:0], MIBSPI5CLK, MIBSPI5nCS[3:0], MIBSPI5nENA
SPI2	SPI2SIMO, SPI2SOMI, SPI2CLK, SPI2nCS[1:0], SPI2nENA
SPI4	SPI4SIMO, SPI4SOMI, SPI4CLK, SPI4nCS[0], SPI4nENA

7.12.2 MibSPI Transmit and Receive RAM Organization

The Multibuffer RAM is comprised of 128 buffers. Each entry in the Multibuffer RAM consists of 4 parts: a 16-bit transmit field, a 16-bit receive field, a 16-bit control field and a 16-bit status field. The Multibuffer RAM can be partitioned into multiple transfer group with variable number of buffers each. Each MibSPIx module supports 8 transfer groups.

7.12.3 MibSPI Transmit Trigger Events

Each of the transfer groups can be configured individually. For each of the transfer groups a trigger event and a trigger source can be chosen. A trigger event can be for example a rising edge or a permanent low level at a selectable trigger source. For example, up to 15 trigger sources are available which can be utilized by each transfer group. These trigger options are listed in Table 7-33 and Section 7.12.3.2 for MibSPI1 and MibSPi3 respectively.

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7.12.3.1 MibSPI1 Event Trigger Hookup

Table 7-33. MibSPI1 Event Trigger Hookup

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	N2HET1[8]
EVENT9	1010	N2HET1[10]
EVENT10	1011	N2HET1[12]
EVENT11	1100	N2HET1[14]
EVENT12	1101	N2HET1[16]
EVENT13	1110	N2HET1[18]
EVENT14	1111	Intern Tick counter

NOTE

For N2HET1 trigger sources, the connection to the MibSPI1 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

NOTE

For GIOx trigger sources, the connection to the MibSPI1 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin and selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI1 transfers; there is no multiplexing on the input connections.

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7.12.3.2 MibSPI3 Event Trigger Hookup

Table 7-34. MibSPI3 Event Trigger Hookup

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	N2HET1[8]
EVENT9	1010	N2HET1[10]
EVENT10	1011	N2HET1[12]
EVENT11	1100	N2HET1[14]
EVENT12	1101	N2HET1[16]
EVENT13	1110	N2HET1[18]
EVENT14	1111	Intern Tick counter

NOTE

For N2HET1 trigger sources, the connection to the MibSPI3 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

NOTE

For GIOx trigger sources, the connection to the MibSPI3 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin and selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI3 transfers; there is no multiplexing on the input connections.

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7.12.3.3 MibSPI5 Event Trigger Hookup

Table 7-35. MibSPI5 Event Trigger Hookup

Event #	TGxCTRL TRIGSRC[3:0]	Trigger
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0]
EVENT1	0010	GIOA[1]
EVENT2	0011	GIOA[2]
EVENT3	0100	GIOA[3]
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	GIOA[6]
EVENT7	1000	GIOA[7]
EVENT8	1001	N2HET1[8]
EVENT9	1010	N2HET1[10]
EVENT10	1011	N2HET1[12]
EVENT11	1100	N2HET1[14]
EVENT12	1101	N2HET1[16]
EVENT13	1110	N2HET1[18]
EVENT14	1111	Intern Tick counter

NOTE

For N2HET1 trigger sources, the connection to the MibSPI5 module trigger input is made from the input side of the output buffer (at the N2HET1 module boundary). This way, a trigger condition can be generated even if the N2HET1 signal is not selected to be output on the pad.

NOTE

For GIOx trigger sources, the connection to the MibSPI5 module trigger input is made from the output side of the input buffer. This way, a trigger condition can be generated either by selecting the GIOx pin as an output pin and selecting the pin to be a GIOx pin, or by driving the GIOx pin from an external trigger source. If the mux control module is used to select different functionality instead of the GIOx signal, then care must be taken to disable GIOx from triggering MibSPI5 transfers; there is no multiplexing on the input connections.

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7.12.4 MibSPI/SPI Master Mode I/O Timing Specifications

Table 7-36. SPI Master Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	Parameter			MIN	MAX	Unit
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)		40	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{d(SPCH-SIMO)M}$	Delay time, SPISIMO valid before SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - 6$		ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPISIMO valid before SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - 6$		
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 4$		ns
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 4$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)		$t_{f(SPC)} + 2.2$		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)		$t_{r(SPC)} + 2.2$		
7(5)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)		10		ns
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)		10		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$(C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	ns
			CSHOLD = 1	$C2TDELAY*t_{c(VCLK)} + 3*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$(C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low until CS inactive (clock polarity = 0)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + tr(SPICS) - 7$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	ns
10	t_{SPIENA}	SPIENAn Sample point		$(C2TDELAY+1) * t_{c(VCLK)} - t_{f(SPICS)} - 29$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see Table 7-2.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40$ns.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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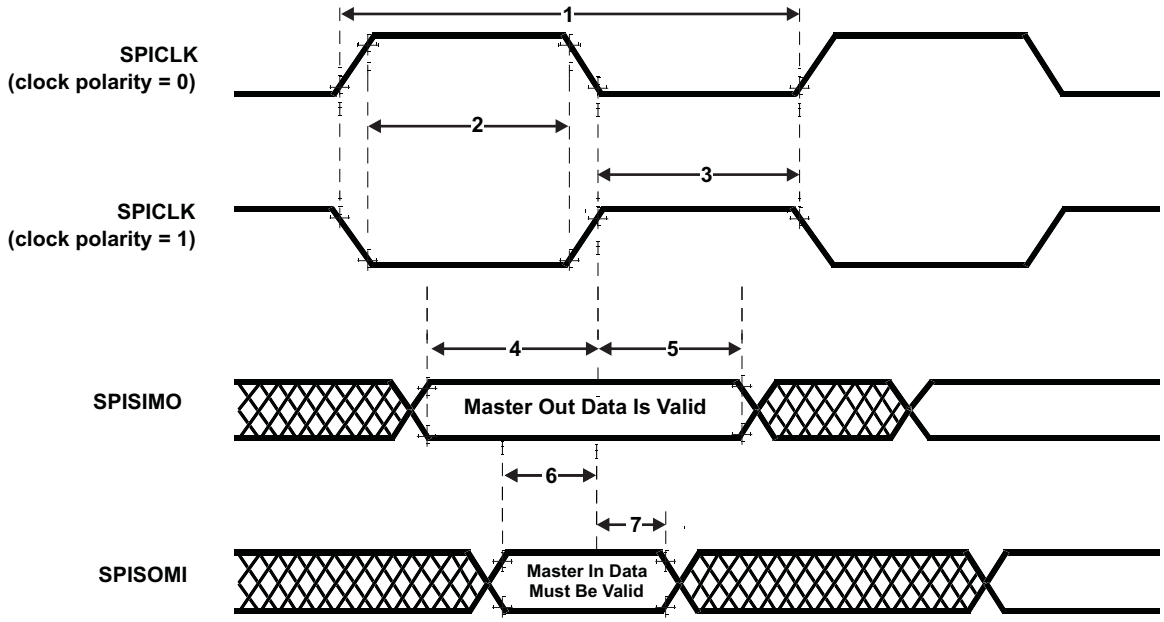


Figure 7-19. SPI Master Mode External Timing (CLOCK PHASE = 0)

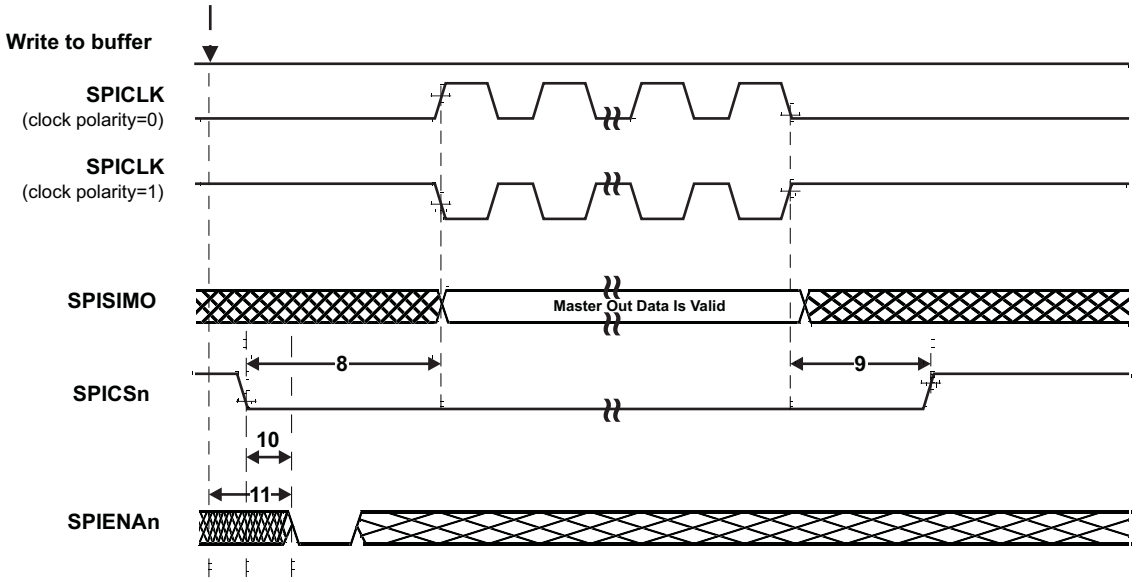


Figure 7-20. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

Table 7-37. SPI Master Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = output, SPISIMO = output, and SPISOMI = input)(1)(2)(3)

NO.	Parameter			MIN	MAX	Unit
1	$t_{c(SPC)M}$	Cycle time, SPICLK (4)		40	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{f(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{r(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	
4(5)	$t_{v(SIMO-SPCH)M}$	Valid time, SPICLK high after SPISIMO data valid (clock polarity = 0)		$0.5t_{c(SPC)M} - 6$		ns
	$t_{v(SIMO-SPCL)M}$	Valid time, SPICLK low after SPISIMO data valid (clock polarity = 1)		$0.5t_{c(SPC)M} - 6$		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)		$0.5t_{c(SPC)M} - t_{r(SPC)} - 4$		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)		$0.5t_{c(SPC)M} - t_{f(SPC)} - 4$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)		$t_{r(SPC)} + 2.2$		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)		$t_{f(SPC)} + 2.2$		
7(5)	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)		10		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)		10		
8(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPC)} + 5.5$	
		Setup time CS active until SPICLK low (clock polarity = 1)	CSHOLD = 0	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+2) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	ns
			CSHOLD = 1	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} - 7$	$0.5*t_{c(SPC)M} + (C2TDELAY+3) * t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPC)} + 5.5$	
9(6)	$t_{T2CDELAY}$	Hold time SPICLK low until CS inactive (clock polarity = 0)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} - 7$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPC)} + t_{r(SPICS)} + 11$	ns
		Hold time SPICLK high until CS inactive (clock polarity = 1)		$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} - 7$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPC)} + t_{r(SPICS)} + 11$	ns
10	t_{SPIENA}	SPIENAn Sample Point		$(C2TDELAY+1)* t_{c(VCLK)} - t_{f(SPICS)} - 29$	$(C2TDELAY+1)*t_{c(VCLK)}$	ns
11	$t_{SPIENAW}$	SPIENAn Sample point from write to buffer			$(C2TDELAY+2)*t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$
(3) For rise and fall timings, see Table 7-2.
(4) When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 40$ns.
The external load on the SPICLK pin must be less than 60pF.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register

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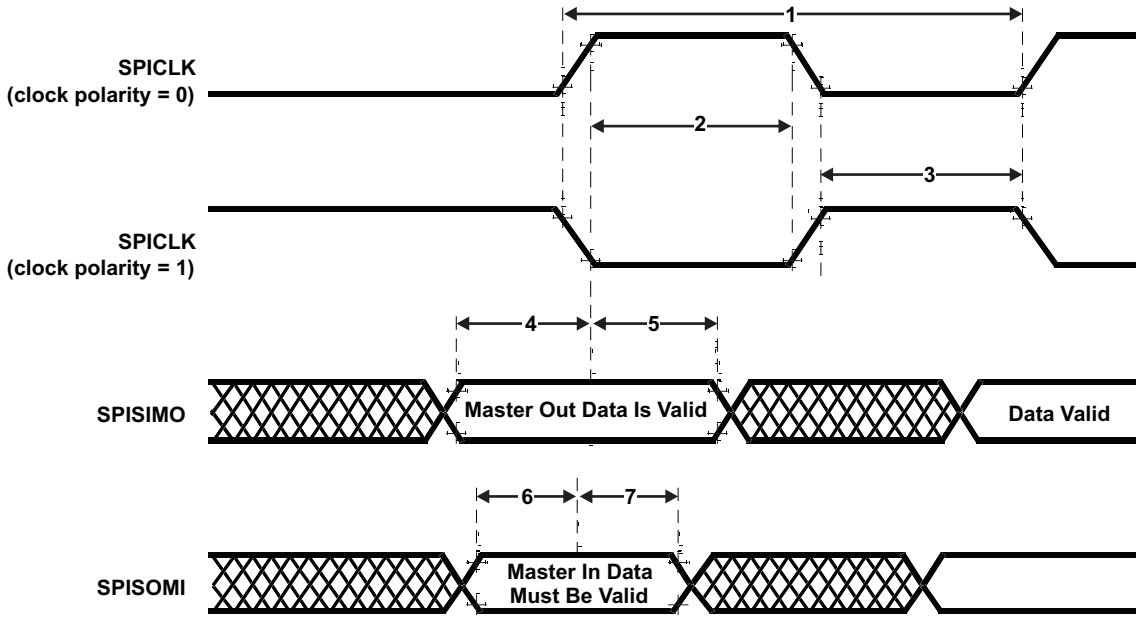


Figure 7-21. SPI Master Mode External Timing (CLOCK PHASE = 1)

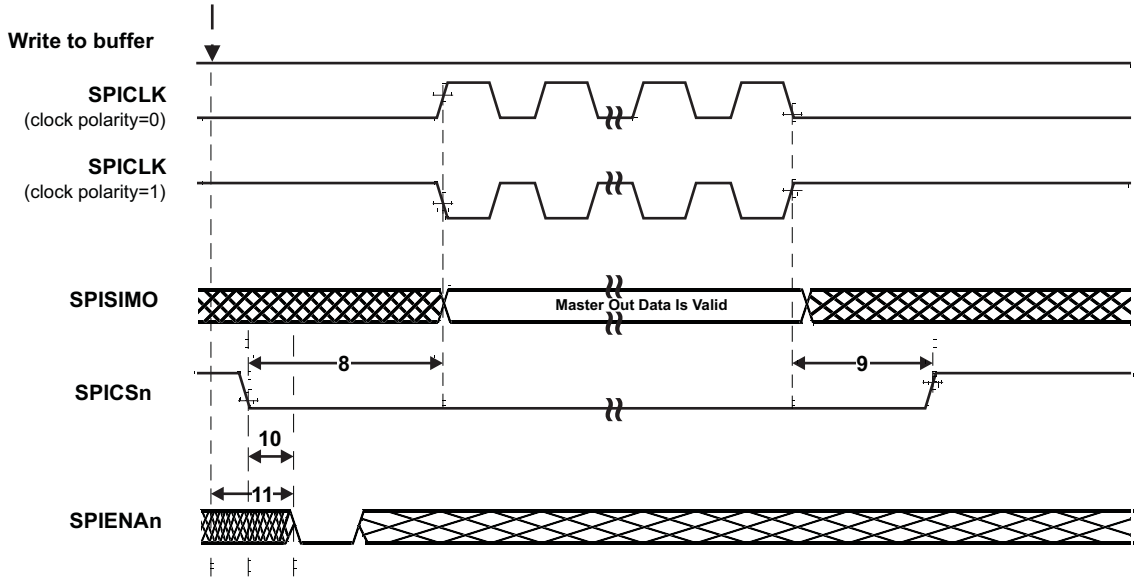


Figure 7-22. SPI Master Mode Chip Select Timing (CLOCK PHASE = 1)

7.12.5 SPI Slave Mode I/O Timings

Table 7-38. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	Parameter		MIN	MAX	Unit
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	40		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPISOMI valid after SPICLK high (clock polarity = 0)		$t_{rf(SOMI)}$ + 20	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPISOMI valid after SPICLK low (clock polarity = 1)		$t_{rf(SOMI)}$ + 20	
5(6)	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	4		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	4		
7(6)	$t_{h(SPCL-SIMO)S}$	Hold time, SPISIMO data valid after SPICLK low (clock polarity = 0)	2		ns
	$t_{h(SPCH-SIMO)S}$	Hold time, SPISIMO data valid after S PICLK high (clock polarity = 1)	2		
8	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$ +22	ns
	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}$ +22	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}$+27	ns

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is cleared.
(2) If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 7-2.
(4) $t_{c(VCLK)}$ = interface clock cycle time = $1 / f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS + 1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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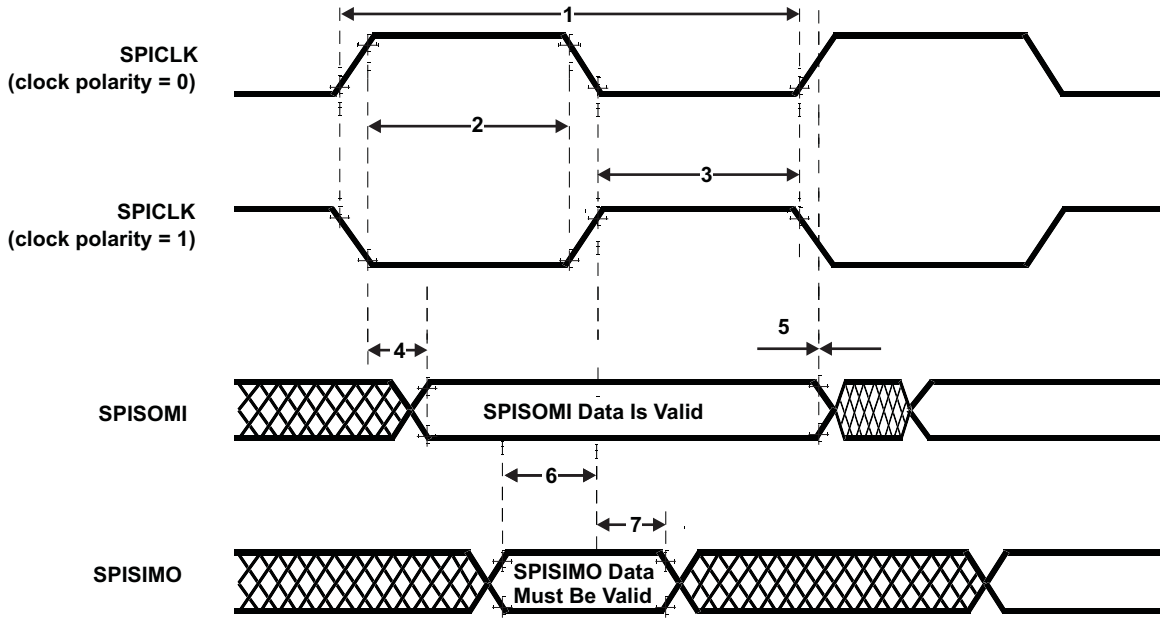


Figure 7-23. SPI Slave Mode External Timing (CLOCK PHASE = 0)

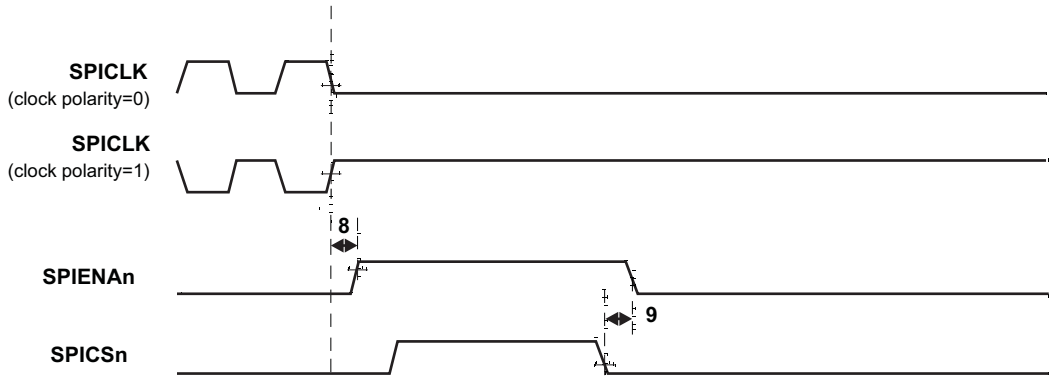


Figure 7-24. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)

Table 7-39. SPI Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPICLK = input, SPISIMO = input, and SPISOMI = output)(1)(2)(3)(4)

NO.	Parameter		MIN	MAX	Unit
1	$t_{c(SPC)S}$	Cycle time, SPICLK(5)	40		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	14		ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	14		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	14		ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	14		
4(6)	$t_{d(SOMI-SPCL)S}$	Delay time, SPISOMI data valid after SPICLK low (clock polarity = 0)		$t_{rf(SOMI)}$ + 20	ns
	$t_{d(SOMI-SPCH)S}$	Delay time, SPISOMI data valid after SPICLK high (clock polarity = 1)		$t_{rf(SOMI)}$ + 20	
5(6)	$t_{h(SPCL-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity =0)	2		ns
	$t_{h(SPCH-SOMI)S}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity =1)	2		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	4		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	4		
7(6)	$t_{v(SPCH-SIMO)S}$	High time, SPISIMO data valid after SPICLK high (clock polarity = 0)	2		ns
	$t_{v(SPCL-SIMO)S}$	High time, SPISIMO data valid after SPICLK low (clock polarity = 1)	2		
8	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}+22$	ns
	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}+t_{r(ENAn)}+22$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)	$t_{f(ENAn)}$	$t_{c(VCLK)}+t_{f(ENAn)}+27$	ns
10	$t_{d(SCSL-SOMI)S}$	Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer)	$t_{c(VCLK)}$	$2t_{c(VCLK)}+t_{rf(SOMI)}+28$	ns

(1) The MASTER bit (SPIGCR1.0) is cleared and the CLOCK PHASE bit (SPIFMTx.16) is set.
(2) If the SPI is in slave mode, the following must be true: tc(SPC)S ≤ (PS + 1) tc(VCLK), where PS = prescale value set in SPIFMTx.[15:8].
(3) For rise and fall timings, see Table 7-2.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /$f_{(VCLK)}$
(5) When the SPI is in Slave mode, the following must be true:
For PS values from 1 to 255: $t_{c(SPC)S} \geq (PS+1)t_{c(VCLK)} \geq 40$ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
For PS values of 0: $t_{c(SPC)S} = 2t_{c(VCLK)} \geq 40$ns.
(6) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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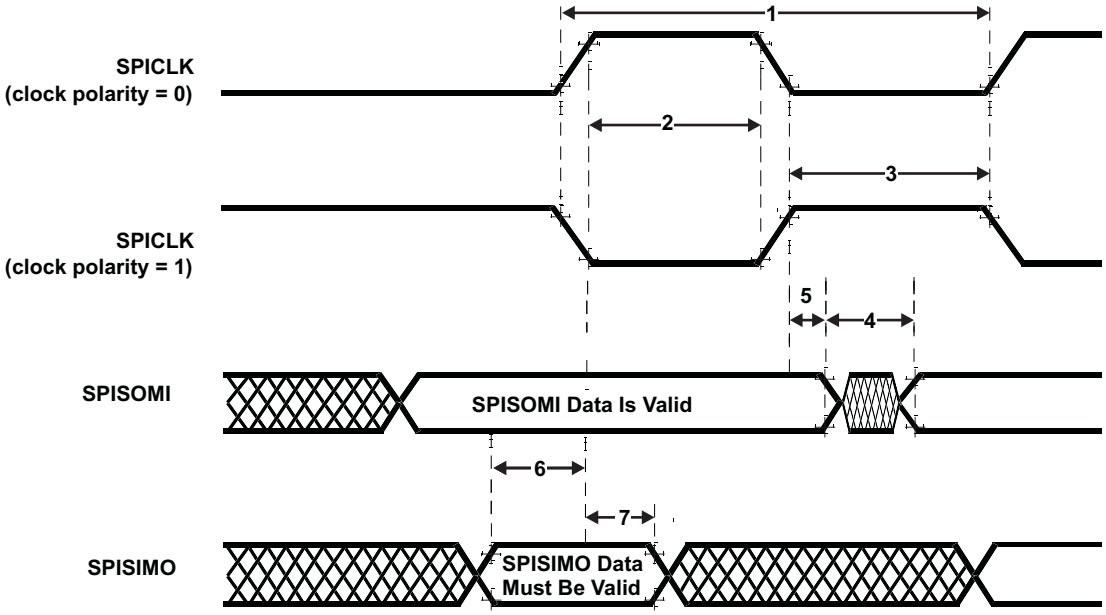


Figure 7-25. SPI Slave Mode External Timing (CLOCK PHASE = 1)

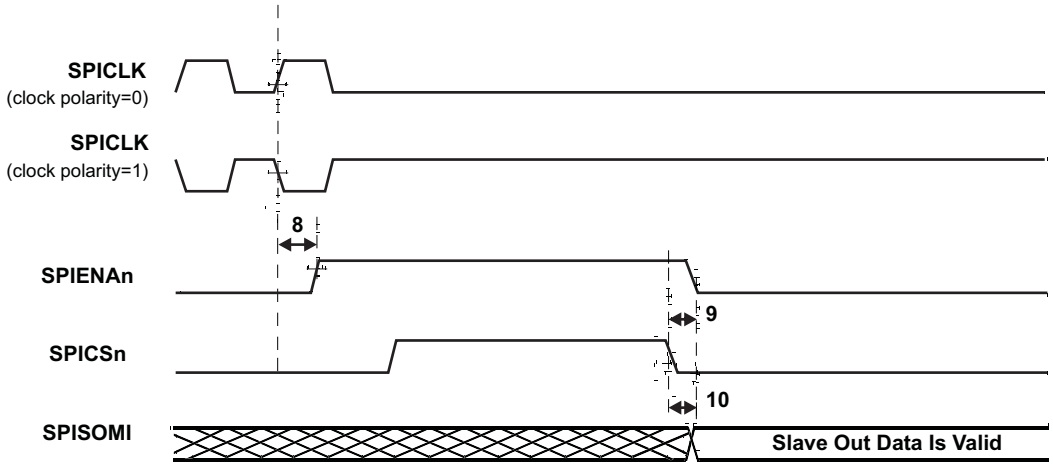


Figure 7-26. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)

8 Applications, Implementation, and Layout

NOTE

Information in the following sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Hercules™ TMS570LS12x LaunchPad™ Development Kit

LAUNCHXL2-TMS57012 — The Hercules TMS570LS12x LaunchPad development kit is a low-cost evaluation platform that helps users get started quickly in evaluating and developing with the Hercules microcontroller family, which is specifically designed for ISO 26262 and IEC 61508 functional safety automotive applications. The LaunchPad features onboard emulation for programming and debugging; push buttons; LEDs and ambient light sensor; and two standard 40-pin BoosterPack™ expansion connectors. Through the expansion connectors, the LaunchPad development kit can support a wide range of BoosterPack plug-in modules for added functionality (such as displays, wireless sensors, and so forth). LaunchPad development kits come preprogrammed with a demo code that lets the user easily learn the key safety, data acquisition, and control features of the Hercules MCU platform. For additional software downloads and other resources, visit the Hercules LaunchPads wiki.

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9 Device and Documentation Support

9.1 Development Support

Texas Instruments (TI) offers an extensive line of development tools for the Hercules™ Safety generation of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of Hercules™-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators - XDS100 v2, XDS200, XDS560™ v2 emulator
- Flash programming tools
- Power supply
- Documentation and cables

9.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices and support tools. Each commercial family member has one of three prefixes: TMX, TMP, or TMS (for example,TMS570LS0914). These prefixes represent evolutionary stages of product development from engineering prototypes (TMX) through fully qualified production devices/tools (TMS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

TMX and TMP devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

Figure 9-1 shows the numbering and symbol nomenclature for the TMS570LS0914 devices.

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Full Part #	TMS	570	LS	09	1	4	A	PGE	Q	Q1	R
Orderable Part #	TMS	570		09	1	4	A	PGE	Q	Q1	R

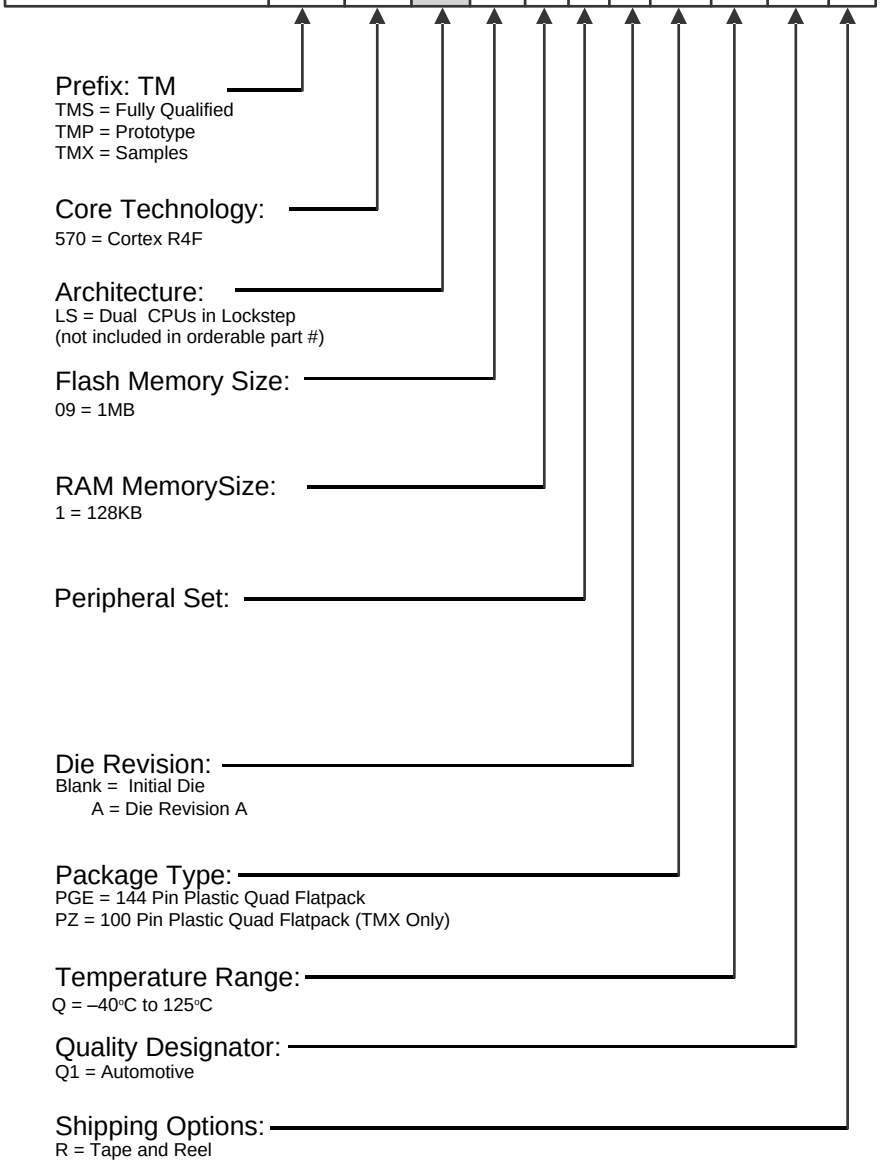


Figure 9-1. TMS570LS0914 Device Numbering Conventions

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9.3 Documentation Support

9.3.1 Related Documentation from Texas Instruments

The following documents describe the *TMS570LS0914* microcontroller.

SPNU607 ***TMS570LS09x/07x 16/32-Bit RISC Flash Microcontroller Technical Reference Manual*** details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

SPNZ215 ***TMS570LS09xx/07xx 16/32-Bit RISC Flash Microcontroller Silicon Errata (Silicon Revision 0)*** describes the known exceptions to the functional specifications for the device.

SPNA204 ***Compatibility Considerations: Migrating From TMS570LS31x/21x or TMS570LS12x/11x to TMS570LS0914/0714 Safety Microcontrollers*** provides a summary of the differences between the TMS570LS0914/0714 versus the TMS570LS31x/21x and TMS570LS12x/11x series of microcontrollers.

9.3.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

9.4 Trademarks

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All other trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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9.7 Device Identification

9.7.1 Device Identification Code Register

The device identification code register identifies several aspects of the device including the silicon version. The details of the device identification code register are shown in Table 9-1. The device identification code register value for this device is:

- Rev 0 = 0x8052AD05
- Rev A = 0x8052AD0D

Figure 9-2. Device ID Bit Allocation Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CP-15	UNIQUE ID														TECH
R-1	R-00000000101001														R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TECH			I/O VOLTAGE	PERIPH PARITY	FLASH ECC		RAM ECC	VERSION					1	0	1
R-101			R-0	R-1	R-10		R-1	R-00000					R-1	R-0	R-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9-1. Device ID Bit Allocation Register Field Descriptions

Bit	Field	Value	Description
31	CP15		Indicates the presence of coprocessor 15
		1	CP15 present
30-17	UNIQUE ID	101001	Unique device identification number This bitfield holds a unique number for a dedicated device configuration (die).
16-13	TECH		Process technology on which the device is manufactured.
		0101	F021
12	I/O VOLTAGE		I/O voltage of the device.
		0	I/O are 3.3v
11	PERIPHERAL PARITY	1	Peripheral Parity Parity on peripheral memories
10-9	FLASH ECC		Flash ECC
		10	Program memory with ECC
8	RAM ECC		Indicates if RAM memory ECC is present.
		1	ECC implemented
7-3	REVISION		Revision of the Device.
2-0	101		The platform family ID is always 0b101

9.7.2 Die Identification Registers

The two die ID registers at addresses 0xFFFFFF7C and 0xFFFFFF80 form a 64-bit dieid with the information as shown in Table 9-2.

Table 9-2. Die-ID Registers

Item	# of Bits	Bit Location
X Coord. on Wafer	12	0xFFFFFF7C[11:0]
Y Coord. on Wafer	12	0xFFFFFF7C[23:12]
Wafer #	8	0xFFFFFF7C[31:24]
Lot #	24	0xFFFFFF80[23:0]
Reserved	8	0xFFFFFF80[31:24]

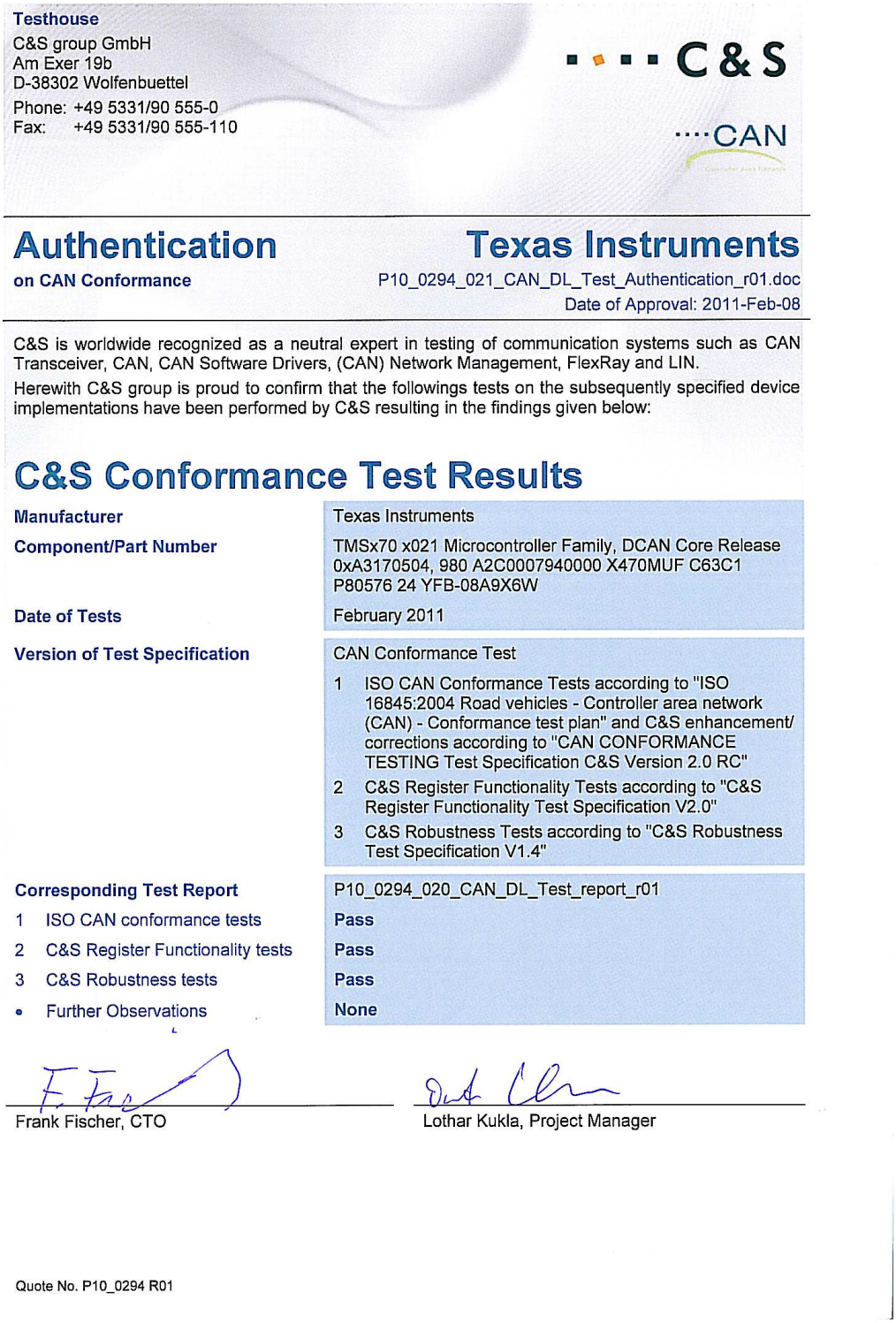
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9.8 Module Certifications

The following communications modules have received certification of adherence to a standard.

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9.8.1 DCAN Certification



Testhouse
C&S group GmbH
Am Exer 19b
D-38302 Wolfenbuettel
Phone: +49 5331/90 555-0
Fax: +49 5331/90 555-110

C&S
CAN

Authentication
on CAN Conformance

Texas Instruments
P10_0294_021_CAN_DL_Test_Authentication_r01.doc
Date of Approval: 2011-Feb-08

C&S is worldwide recognized as a neutral expert in testing of communication systems such as CAN Transceiver, CAN, CAN Software Drivers, (CAN) Network Management, FlexRay and LIN.

Herewith C&S group is proud to confirm that the followings tests on the subsequently specified device implementations have been performed by C&S resulting in the findings given below:

C&S Conformance Test Results

Manufacturer	Texas Instruments
Component/Part Number	TMSx70 x021 Microcontroller Family, DCAN Core Release 0xA3170504, 980 A2C0007940000 X470MUF C63C1 P80576 24 YFB-08A9X6W
Date of Tests	February 2011
Version of Test Specification	CAN Conformance Test 1 ISO CAN Conformance Tests according to "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan" and C&S enhancement/ corrections according to "CAN CONFORMANCE TESTING Test Specification C&S Version 2.0 RC" 2 C&S Register Functionality Tests according to "C&S Register Functionality Test Specification V2.0" 3 C&S Robustness Tests according to "C&S Robustness Test Specification V1.4"
Corresponding Test Report	P10_0294_020_CAN_DL_Test_report_r01
1 ISO CAN conformance tests	**Pass**
2 C&S Register Functionality tests	**Pass**
3 C&S Robustness tests	**Pass**
• Further Observations	**None**

Frank Fischer, CTO

Lothar Kukla, Project Manager

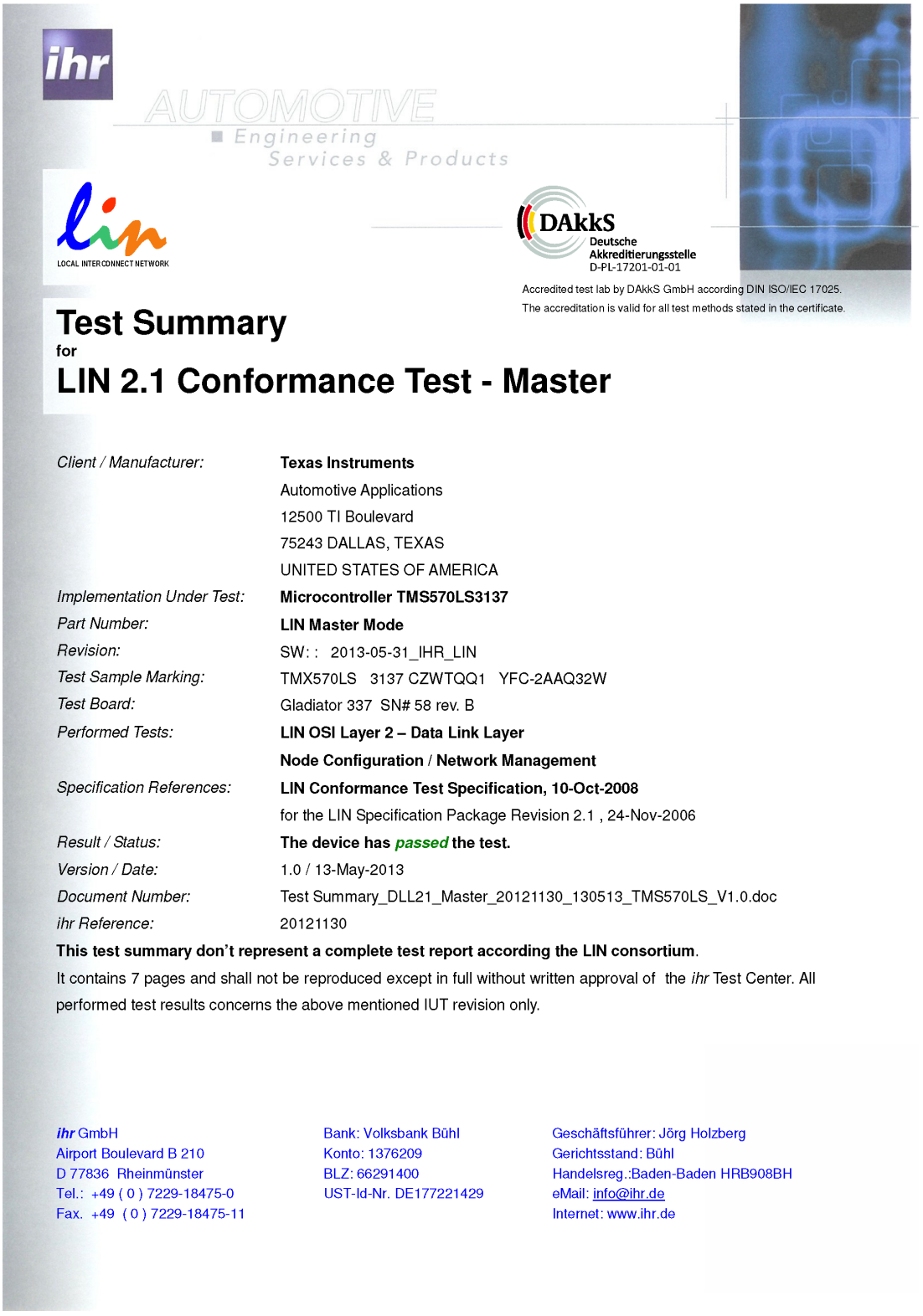
Quote No. P10_0294 R01

Figure 9-3. DCAN Certification

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9.8.2 LIN Certification

9.8.2.1 LIN Master Mode



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DAkkS
Deutsche
Akkreditierungsstelle
D-PL-17201-01-01

Accredited test lab by DAkkS GmbH according DIN ISO/IEC 17025.
The accreditation is valid for all test methods stated in the certificate.

Test Summary
for
LIN 2.1 Conformance Test - Master

Client / Manufacturer:	**Texas Instruments**
	Automotive Applications
	12500 TI Boulevard
	75243 DALLAS, TEXAS
	UNITED STATES OF AMERICA
Implementation Under Test:	**Microcontroller TMS570LS3137**
Part Number:	**LIN Master Mode**
Revision:	SW: : 2013-05-31_IHR_LIN
Test Sample Marking:	TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W
Test Board:	Gladiator 337 SN# 58 rev. B
Performed Tests:	**LIN OSI Layer 2 – Data Link Layer**
	Node Configuration / Network Management
Specification References:	**LIN Conformance Test Specification, 10-Oct-2008**
	for the LIN Specification Package Revision 2.1 , 24-Nov-2006
Result / Status:	**The device has *passed* the test.**
Version / Date:	1.0 / 13-May-2013
Document Number:	Test Summary_DLL21_Master_20121130_130513_TMS570LS_V1.0.doc
ihr Reference:	20121130

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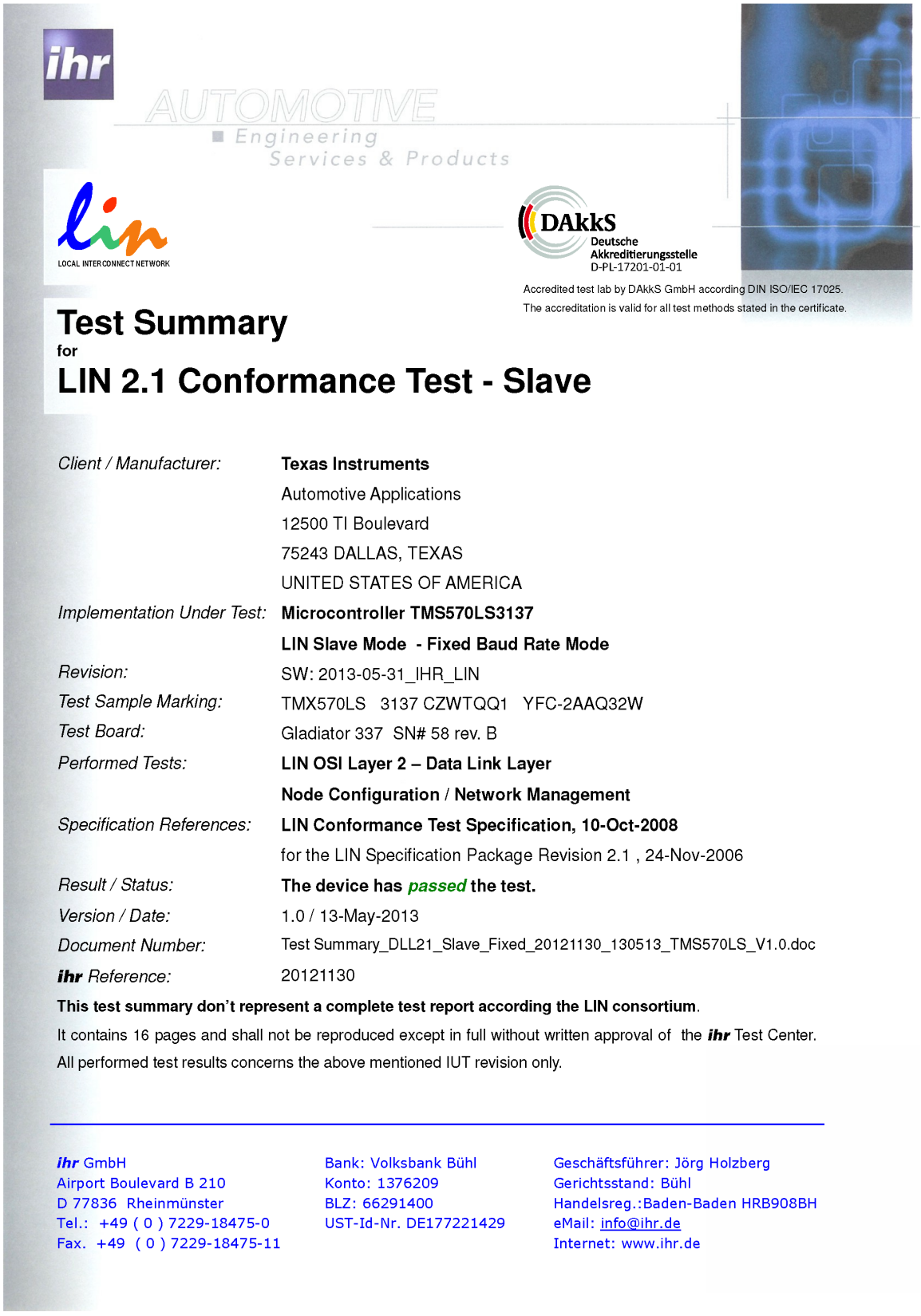
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Figure 9-4. LIN Certification - Master Mode

9.8.2.2 LIN Slave Mode - Fixed Baud Rate



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Test Summary
for
LIN 2.1 Conformance Test - Slave

Client / Manufacturer:	**Texas Instruments**
	Automotive Applications
	12500 TI Boulevard
	75243 DALLAS, TEXAS
	UNITED STATES OF AMERICA
Implementation Under Test:	**Microcontroller TMS570LS3137**
	LIN Slave Mode - Fixed Baud Rate Mode
Revision:	SW: 2013-05-31_IHR_LIN
Test Sample Marking:	TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W
Test Board:	Gladiator 337 SN# 58 rev. B
Performed Tests:	**LIN OSI Layer 2 – Data Link Layer**
	Node Configuration / Network Management
Specification References:	**LIN Conformance Test Specification, 10-Oct-2008**
	for the LIN Specification Package Revision 2.1 , 24-Nov-2006
Result / Status:	**The device has *passed* the test.**
Version / Date:	1.0 / 13-May-2013
Document Number:	Test Summary_DLL21_Slave_Fixed_20121130_130513_TMS570LS_V1.0.doc
***ihr** Reference:*	20121130

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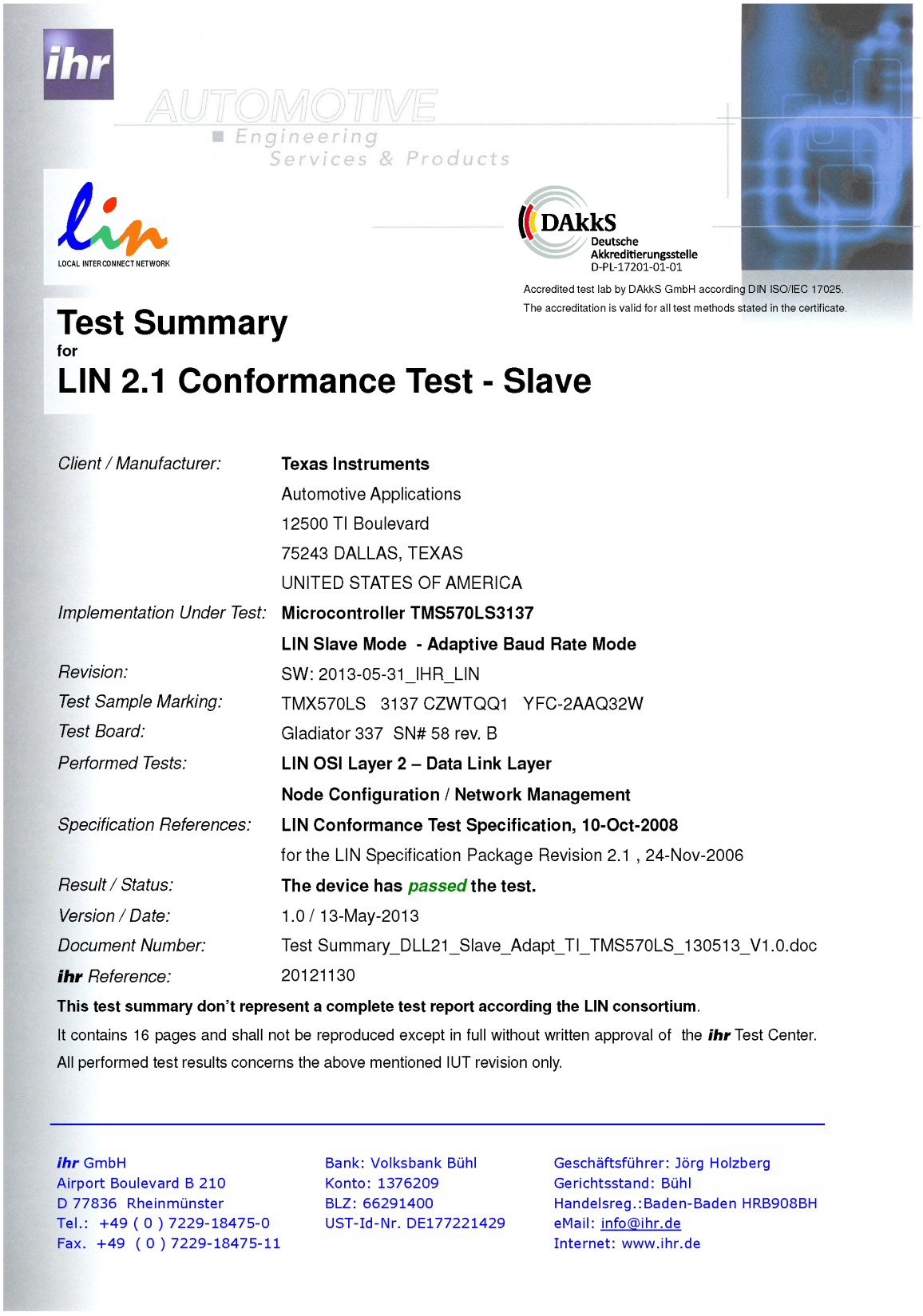
Bank: Volksbank Bühl
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UST-Id-Nr. DE177221429

Geschäftsführer: Jörg Holzberg
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Figure 9-5. LIN Certification - Slave Mode - Fixed Baud Rate

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9.8.2.3 LIN Slave Mode - Adaptive Baud Rate



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Test Summary
for
LIN 2.1 Conformance Test - Slave

Client / Manufacturer:	**Texas Instruments**
	Automotive Applications
	12500 TI Boulevard
	75243 DALLAS, TEXAS
	UNITED STATES OF AMERICA
Implementation Under Test:	**Microcontroller TMS570LS3137**
	LIN Slave Mode - Adaptive Baud Rate Mode
Revision:	SW: 2013-05-31_IHR_LIN
Test Sample Marking:	TMX570LS 3137 CZWTQQ1 YFC-2AAQ32W
Test Board:	Gladiator 337 SN# 58 rev. B
Performed Tests:	**LIN OSI Layer 2 – Data Link Layer**
	Node Configuration / Network Management
Specification References:	**LIN Conformance Test Specification, 10-Oct-2008**
	for the LIN Specification Package Revision 2.1 , 24-Nov-2006
Result / Status:	**The device has *passed* the test.**
Version / Date:	1.0 / 13-May-2013
Document Number:	Test Summary_DLL21_Slave_Adapt_TI_TMS570LS_130513_V1.0.doc
***ihr** Reference:*	20121130

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Figure 9-6. LIN Certification - Slave Mode - Adaptive Baud Rate

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10 Mechanical Packaging and Orderable Information

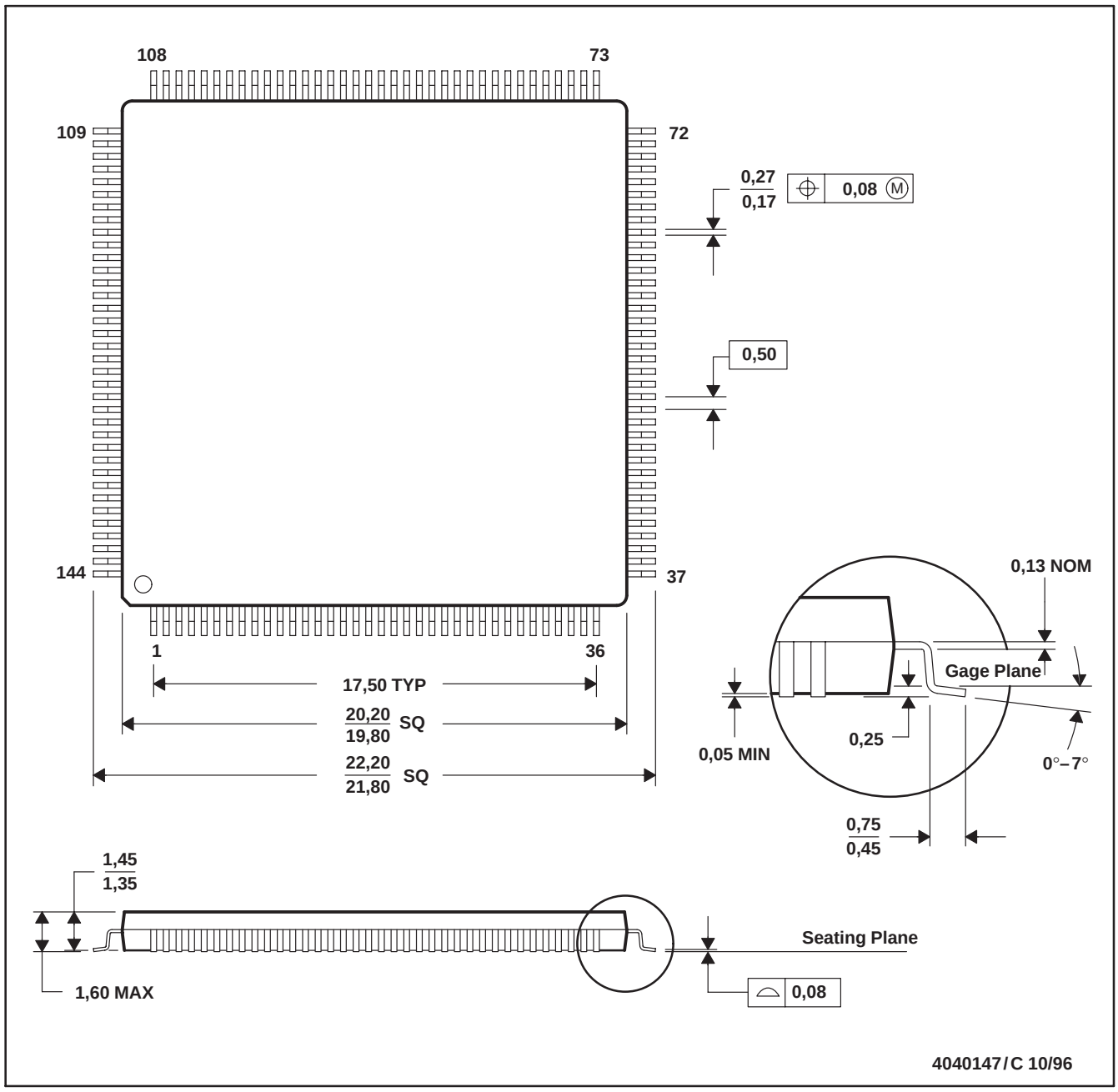
10.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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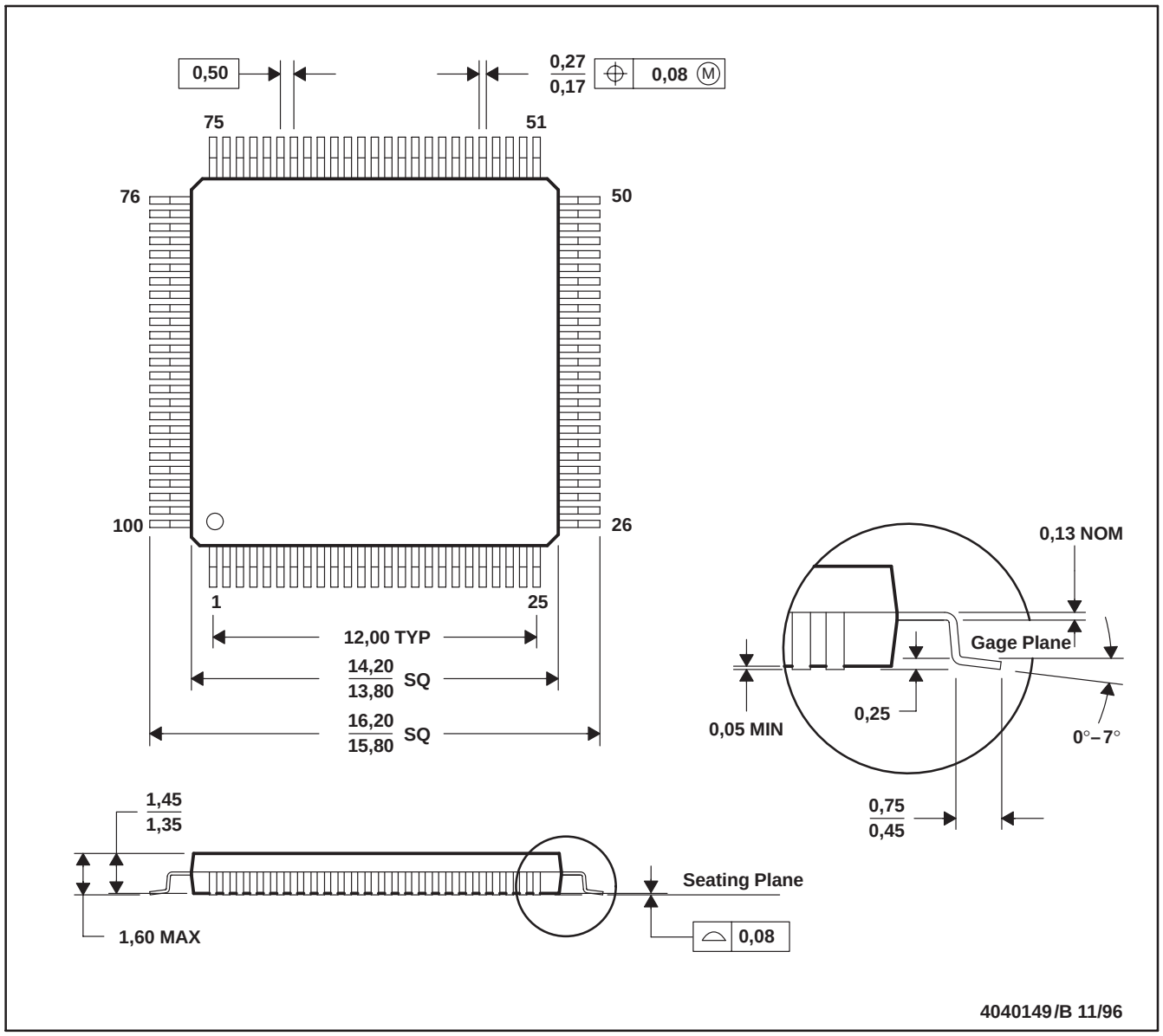
PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS5700914APGEQQ1	ACTIVE	LQFP	PGE	144	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS570LS 0914APGEQQ1	Samples
TMX5700914APZQQ1	PREVIEW	LQFP	PZ	100	1	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

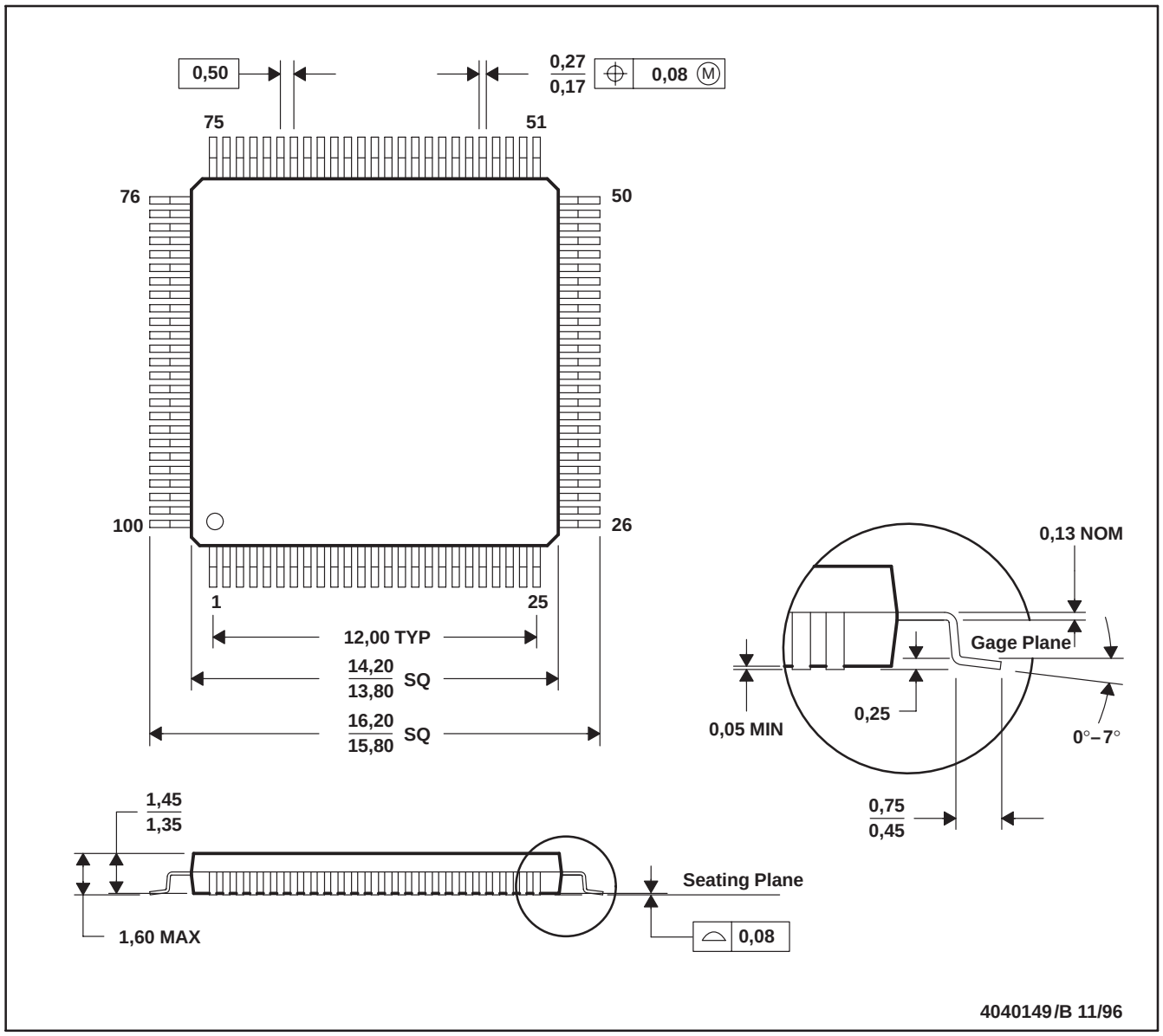
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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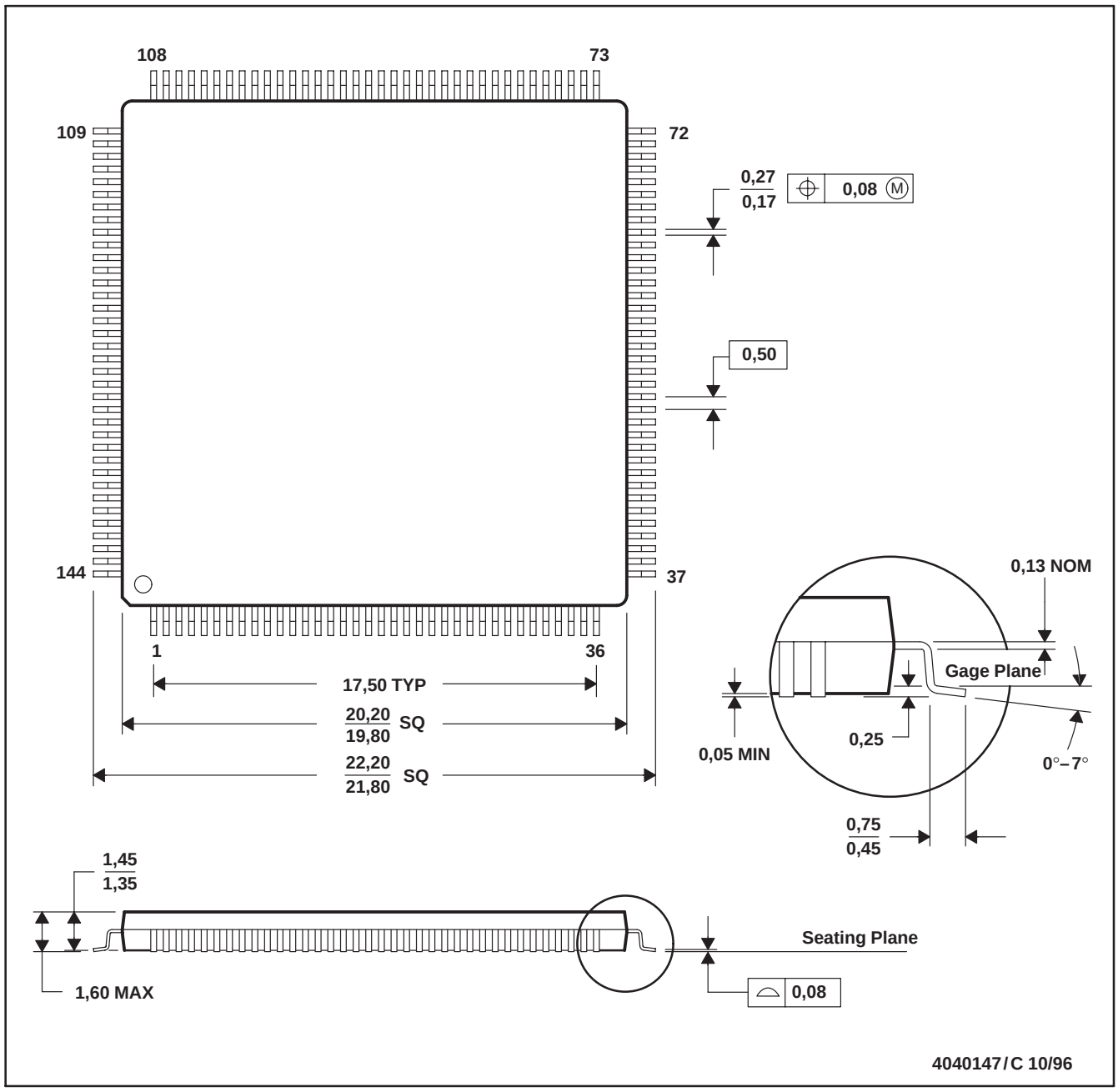
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
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PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
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