TMS470MF06607 16/32-Bit RISC Flash Microcontroller

Check for Samples: TMS470MF06607

1 Features

- High-Performance Automotive Grade Microcontroller with Safety Features
  - Full Automotive Temperature Range
  - ECC on Flash and SRAM
  - CPU and Memory BIST (Built-In Self Test)
- ARM Cortex™-M3 32-Bit RISC CPU
  - Efficient 1.2 DMIPS/MHz
  - Optimized Thumb2 Instruction Set
  - Memory Protection Unit (MPU)
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
- Operating Features
  - Up to 80MHz System Clock
  - Single 3.3V Supply Voltage
- Integrated Memory
  - 640KB Total Program Flash with ECC
  - Support for Flash EEPROM Emulation
  - 64K-Byte Static RAM (SRAM) with ECC
- Key Peripherals
  - High-End Timer, MibADC, CAN, MibSPI
- Common TMS470M/570 Platform Architecture
  - Consistent Memory Map across the family
  - Real-Time Interrupt Timer (RTI)
  - Digital Watchdog
  - Vectored Interrupt Module (VIM)
  - Cyclic Redundancy Checker (CRC)
- Frequency-Modulated Zero-Pin Phase-Locked Loop (FMzPLL)-Based Clock Module
  - Oscillator and PLL clock monitor
- Up to 51 Peripheral IO pins
  - 4 Dedicated GIO - w/ External Interrupts
  - Programmable External Clock (ECLK)
- Communication Interfaces
  - Two CAN Controllers
    - One with 32 mailboxes, one with 16
    - Parity on mailbox RAM
  - Two Multi-buffered Serial Peripheral Interface (MibSPI)
    - 12 total chip selects
    - 64 buffers with parity on each
  - Two UART (SCI) interfaces
    - H/W Support for Local Interconnect Network (LIN 2.1 master mode)
- High-End Timer (HET)
  - Up to 18 Programmable I/O Channels
  - 64 Word Instruction RAM with parity
- 10-Bit Multi-Buffered ADCs (MibADC)
  - Up to 16 ADC Input channels
  - 64 Result FIFO Buffer with parity
  - 1.55uS total conversion time
  - Calibration and Self Test features
- On-Chip Scan-Base Emulation Logic
  - IEEE Standard 1149.1 (JTAG) Test-Access Port and Boundary Scan
- Packages supported
  - 100-Pin Plastic Quad Flatpack (PZ Suffix)
  - Green/Lead-Free
- Development Tools Available
  - Development Boards
  - Code Composer Studio™ Integrated Development Environment (IDE)
  - HET Assembler and Simulator
  - nowFlash™ Flash Programming Tool
- Community Resources
  - TI E2E Community

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1.1 PZ Package View

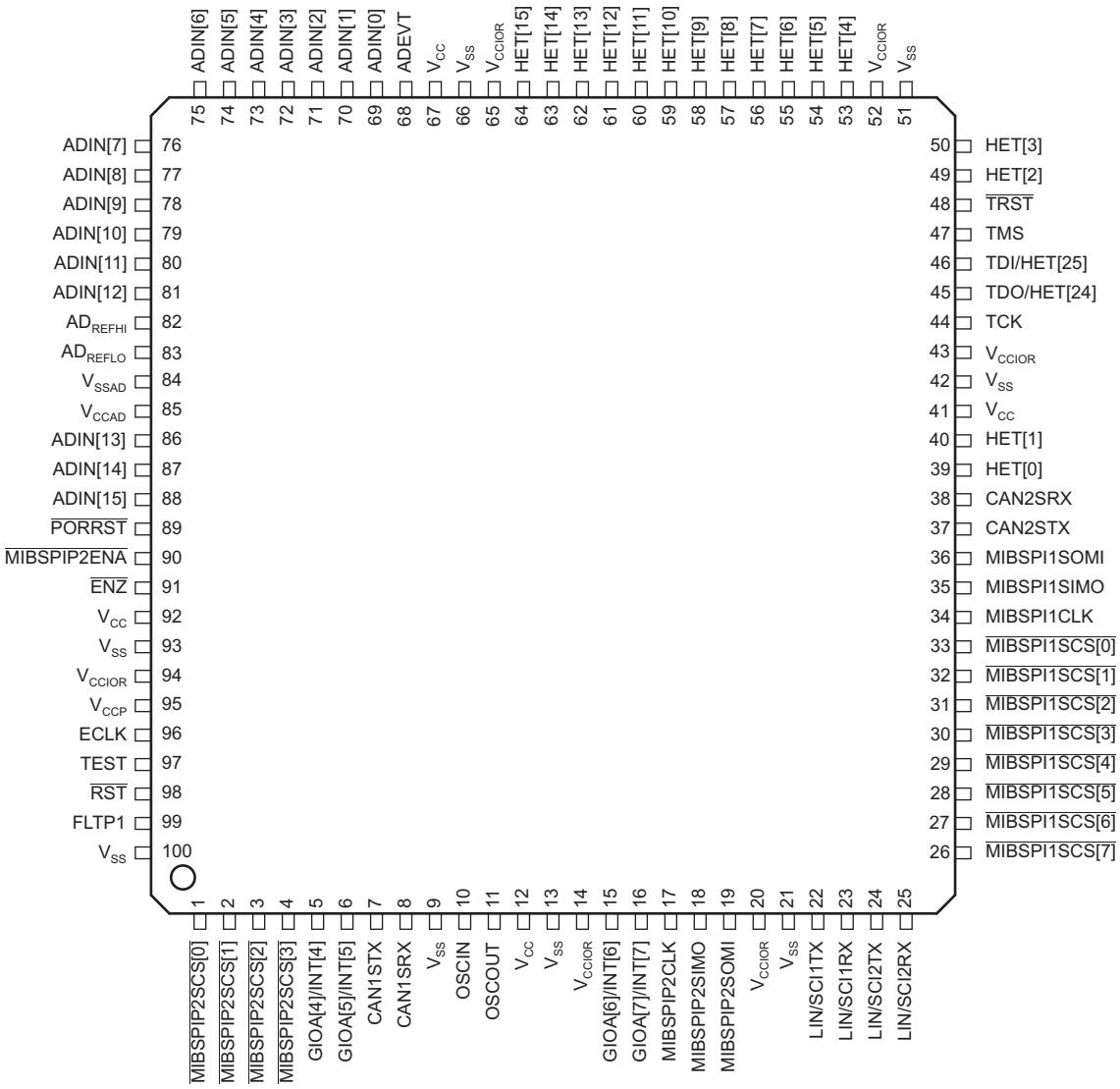


Figure 1-1. TMS470MF06607 100-Pin PZ Package (Top View)

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1.2 Description

The TMS470MF06607 device is a member of the Texas Instruments TMS470M family of Automotive Grade 16/32-bit reduced instruction set computer (RISC) microcontrollers. The TMS470M microcontrollers offer high performance utilizing the high efficiency ARM Cortex™-M3 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The TMS470M microcontroller architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The TMS470MF06607 device contains the following:

- 16/32-Bit RISC CPU Core
- 640K-Byte Total Flash with SECDED ECC
  - 512K-Byte Program Flash
  - 128K- Byte Flash for additional program space or EEPROM Emulation
- 64K-Byte Static RAM (SRAM) with SECDED ECC
- Real-Time Interrupt Timer (RTI)
- Vectored Interrupt Module (VIM)
- Hardware built-in self-test (BIST) checkers for SRAM (MBIST) and CPU (LBIST)
- 64-bit Cyclic Redundancy Checker (CRC)
- Frequency-Modulated Zero-Pin Phase-Locked Loop (FMzPLL)-Based Clock Module With Prescaler
- Two Multi-buffered Serial Peripheral Interfaces (MibSPI)
- Two UARTs (SCI) with Local Interconnect Network Interfaces (LIN)
- Two CAN Controller (DCAN)
- High-End Timer (HET)
- External Clock Prescale (ECP) Module
- One 16-Channel 10-Bit Multi-Buffered ADC (MibADC)
- Error Signaling Module (ESM)
- Four Dedicated General-Purpose I/O (GIO) Pins and 47 (2 of them are muxed with JTAG pins) Additional Peripheral I/Os (100-Pin Package)

The TMS470M memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes. The SRAM on the TMS470M devices can be protected by means of ECC. This feature utilizes a single error correction and double error detection circuit (SECDED circuit) to detect and optionally correct single bit errors as well as detect all dual bit and some multi-bit errors. This is achieved by maintaining an 8-bit ECC checksum/code for each 64-bit double-word of memory space in a separate ECC RAM memory space.

The flash memory on this device is a nonvolatile, electrically erasable and programmable memory. It is implemented with a 144-bit wide data word (128-bit without ECC) and a 64-bit wide flash module interface. The flash operates with a system clock frequency of up to 28 MHz. Pipeline mode, which allows linear prefetching of flash data, enables a system clock of up to 80 MHz.

The enhanced real-time interrupt (RTI) module on the TMS470M devices has the option to be driven by the oscillator clock. The digital watchdog (DWD) is a 25-bit resetable decrementing counter that provides a system reset when the watchdog counter expires.

The TMS470M devices have six communication interfaces: two LIN/SCIs, two DCANs and two MibSPIs. The LIN is the Local Interconnect Network standard and also supports an SCI mode. SCI can be used in a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The DCAN uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication

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rates of up to 1 megabit per second (Mbps). The DCAN is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring. The MibSPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The MibSPI provides the standard SOMI, SIMO, and SPI clock interface as well as up to eight chip select lines.

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. The TMS470M HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high- resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET.

The TMS470M devices have one 10-bit-resolution, sample-and-hold MibADC. Each of the MibADC channels can be grouped by software for sequential conversion sequences. There are three separate groupings, all three of which can be triggered by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode.

The frequency-modulated zero-pin phase-locked loop (FMzPLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler. The function of the FMzPLL is to multiply the external frequency reference to a higher frequency for internal use. The FMzPLL provides the input to the global clock module (GCM). The GCM module subsequently provides system clock (HCLK), real-time interrupt clock (RTICLK), CPU clock (GCLK), HET clock (VCLK2), DCAN clock (AVCLK1), and peripheral interface clock (VCLK) to all other TMS470M device modules.

The TMS470M devices also have an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK). The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency.

An error signaling module (ESM) provides a common location within the device for error reporting allowing efficient error checking and identification.

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1.3 Functional Block Diagram

Figure 1-2 shows the functional block diagram of the TMS470M devices.

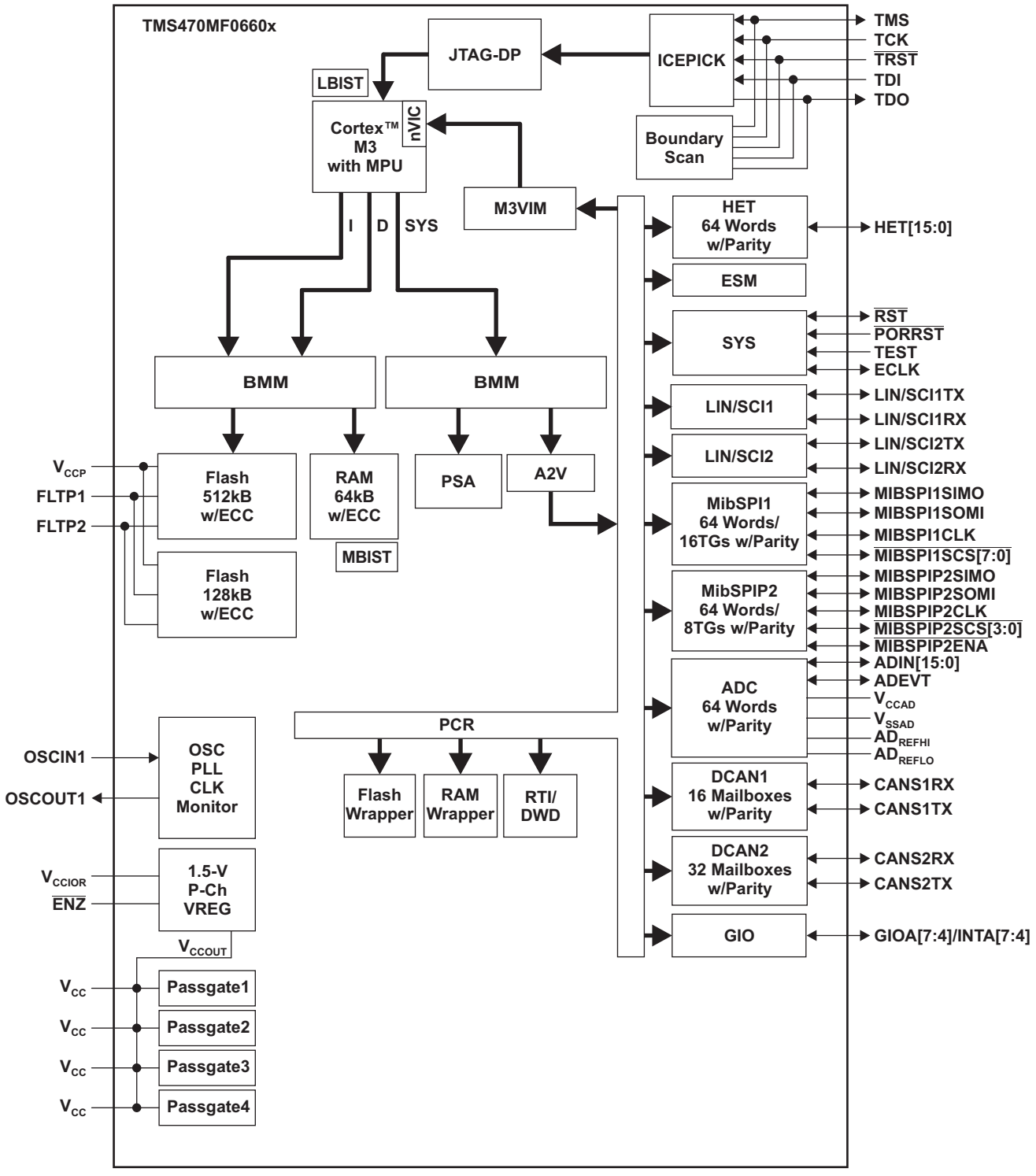


Figure 1-2. TMS470M Functional Block Diagram

1.4 Terms and Acronyms

Table 1-1. Terms and Acronyms

Terms and Acronyms	Description	Comments
A2V	AHB to VBUSP Bridge	The A2V bridge provides the memory interface between the proprietary TI VBUSP and the ARM AHB bus in the TMS470 platform devices.
ADC	Analog To Digital Converter	
AHB	Advanced High-performance Bus	Part of the M3 core
BMM	Bus Matrix Master	The BMM provides connectivity between different bus slave modules to different bus master modules. Accesses from different master modules are executed in parallel if no resource conflict occurs or if the master modules are kept in series through arbitration
CRC	Cyclic Redundancy Check Controller	
DAP	Debug Access Port	DAP is an implementation of an ARM Debug Interface.
DCAN	Controller Area Network	
DWD	Digital Watchdog	
ECC	Error Correction Code	
ESM	Error Signaling Module	
GIO	General-Purpose Input/Output	
HET	High-End Timer	
ICEPICK	In Circuit Emulation TAP (Test Access Port) Selection Module	ICEPick can connect or isolate a module level TAP to or from a higher level chip TAP. ICEPick was designed with both emulation and test requirements in mind.
JTAG	Joint Test Access Group	IEEE Committee responsible for Test Access Ports
JTAG-DP	JTAG Debug Port	JTAG-DP contains a debug port state machine (JTAG) that controls the JTAG-DP operation, including controlling the scan chain interface that provides the external physical interface to the JTAG-DP. It is based closely on the JTAG TAP State Machine, see IEEE Std 1149.1-2001.
LBIST	Logic Built-In Self Test	Test the integrity of M3 CPU
LIN	Local Interconnect Network	
M3VIM	Cortex-M3 Vectored Interrupt Manager	
MBIST	Memory Built-In Self Test	Test the integrity of SRAM
MibSPI	Multi-Buffered Serial Peripheral Interface	
MPU	Protection Unit	
NVIC	Nested Vectored Interrupt Controller	Part of the M3 core
OSC	Oscillator	
PCR	Peripheral Central Resource	
PLL	Phase-Locked Loop	
PSA	Parallel Signature Analysis	
RTI	Real-Time Interrupt	
SCI	Serial Communication Interface	
SECDED	Single Error Correction and Double Error Detection	
STC	Self Test Controller	
SYS	System Module	
VBUS	Virtual Bus	One of the protocols that comprises CBA (Common Bus Architecture)
VBUSP	Virtual Bus-Pipelined	One of the protocols that comprises CBA (Common Bus Architecture)
VREG	Voltage Regulator	

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2 Device Overview

The TMS470MF06607 device is a TMS470M Platform Architecture implemented in F035 130-nm TI technology. Table 2-1 identifies all the characteristics of the TMS470MF06607 device except the SYSTEM and CPU, which are generic.

Table 2-1. Device Characteristics

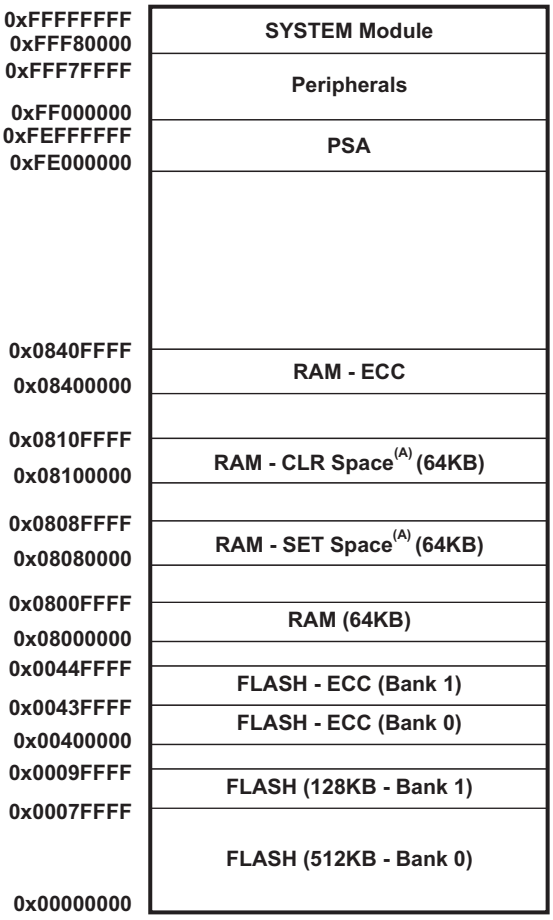
CHARACTERISTICS	DEVICE DESCRIPTION TMS470MF06607	COMMENTS FOR TMS470MF06607
MEMORY		
INTERNAL MEMORY	Pipeline/Non-Pipeline 2 Bank 640K-Byte Flash with ECC 64K-Byte SRAM with ECC CRC, 1-channel	Flash is pipeline-capable
PERIPHERALS		
For the device-specific interrupt priority configurations, see Table 3-4. For the peripheral address ranges and their peripheral selects, see Table 2-6.		
CLOCK	FMzPLL	Frequency-modulated zero-pin PLL has no external loop filter pins.
GENERAL-PURPOSE I/Os	4 I/O	The GIOA port has up to four (4) external pins with external interrupt capability.
LIN/SCI	2 LIN/SCI	
DCAN	2 DCAN	Each with 16/32 mailboxes, respectively.
MibSPI	2 MibSPI	One MibSPI with eight chip select pins, 16 transfer groups, and a 64 word buffer with parity. A second MibSPI with four chip select pins, 1 enable pin, 8 transfer groups, and a 64 word buffer with parity.
HET with XOR Share	18 I/O	The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. HET RAM with parity checking capability.
HET RAM	64-Instruction Capacity	
MibADC	10-bit, 16-channel 64-word FIFO	MibADC RAM includes parity support.
CORE VOLTAGE	1.5 V	
I/O VOLTAGE	3.3 V	
PINS	100	Available in 100-pin package.
PACKAGE	PZ (100 pin)	The 100-pin package designator is PZ.

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2.1 Memory Map Summary

2.1.1 Memory Map

Figure 2-1 shows the TMS470MF06607 memory map.



A. The RAM supports bit access operation which allows set/clear to dedicated bits without disturbing the other bits; for detailed description see the Architecture Specification.

Figure 2-1. TMS470MF06607 Memory Map

2.1.2 Memory Selects

Memories in the TMS470M devices are located at fixed addresses. Table 2-2 through Table 2-6 detail the mapping of the memory regions.

Table 2-2. TMS470MF06607-Specific Memory Frame Assignment

MEMORY FRAME NAME	START ADDRESS	ENDING ADDRESS	MEMORY TYPE	ACTUAL MEMORY
nCS0(1)	0x0000 0000	0x0009 FFFF	Flash	640K Bytes
RAM-CLR	0x0810 0000	0x0810 FFFF	Internal RAM	64K Bytes
RAM-SET	0x0808 0000	0x0808 FFFF	Internal RAM	64K Bytes
CSRAM0(1)	0x0800 0000	0x0800 FFFF	Internal RAM	64K Bytes
CSRAM0(1)	0x0840 0000	0x0840 FFFF	Internal RAM-ECC	64K Bytes

(1) Additional address mirroring could be present resulting in invalid but addressable locations beyond those listed above. The device may generate an abort when accessing the unimplemented memory regions of peripheral memories. TI recommends the use of the MPU for protecting access to addresses outside the intended range of use.

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Table 2-3. Memory Initialization and MBIST

CONNECTING MODULE	ADDRESS RANGE		MEMORY INITIALIZATION CHANNEL	MBIST CONTROLLER ENABLE CHANNEL
	BASE ADDRESS	ENDING ADDRESS		
System RAM	0x08000000	0x0800FFFF	0	0
MibSPI1 RAM	0xFF0E0000	0xFF0FFFFF	1	1 or 2 (1)
MibSPIP2 RAM	0xFF0C0000	0xFF0DFFFF	2	
DCAN1 RAM	0xFF1E0000	0xFF1FFFFF	3	3 or 4 (1)
DCAN2 RAM	0xFF1C0000	0xFF1DFFFF	4	
ADC RAM	0xFF3E0000	0xFF3FFFFF	5	5
HET RAM	0xFF460000	0xFF47FFFF	Not Available	6
STC ROM	Not Applicable	Not Applicable	Not Applicable	7

(1) There are single MBIST controllers for both MibSPI RAMs and both DCAN RAMs. The MBIST controller for both MibSPI RAMs is mapped to channels 1 and 2 and the MBIST controller for both DCAN RAMs is mapped to channels 3 and 4. MBIST on these modules can be initiated by selecting one of the 2 channels or both.

Table 2-4. Peripheral Memory Chip Select Assignment

CONNECTING MODULE	ADDRESS RANGE		PERIPHERAL SELECTS
	BASE ADDRESS	ENDING ADDRESS	
MibSPI1 RAM	0xFF0E0000	0xFF0FFFFF	PCS[7]
MibSPIP2 RAM	0xFF0C0000	0xFF0DFFFF	PCS[6]
DCAN1 RAM	0xFF1E0000	0xFF1FFFFF	PCS[14]
DCAN2 RAM	0xFF1C0000	0xFF1DFFFF	PCS[15]
ADC RAM	0xFF3E0000	0xFF3FFFFF	PCS[31]
HET RAM	0xFF460000	0xFF47FFFF	PCS[35]

NOTE

All used peripheral memory chip selects should decode down to the smallest possible address for this particular peripheral configuration, starting from 4kB upwards. Unused addresses should generate an illegal address error when accessed.

Table 2-5. System Peripheral Registers

FRAME NAME	ADDRESS RANGE	
	FRAME START ADDRESS	FRAME ENDING ADDRESS
PSA	0xFE00_0000	0xFEFF_FFFF
Flash Wrapper Registers	0xFFF8_7000	0xFFF8_7FFF
PCR Register	0xFFFF_E000	0xFFFF_E0FF
System Frame 2 Registers	0xFFFF_E100	0xFFFF_E1FF
CPU STC (LBIST)	0xFFFF_E400	0xFFFF_E4FF
ESM Register	0xFFFF_F500	0xFFFF_F5FF
RAM ECC Register	0xFFFF_F900	0xFFFF_F9FF
RTI Register	0xFFFF_FC00	0xFFFF_FCFF
VIM Register	0xFFFF_FE00	0xFFFF_FEFF
System Registers	0xFFFF_FF00	0xFFFF_FFFF

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Table 2-6. Peripheral Select Map with Address Range

CONNECTING MODULE	BASE ADDRESS	END ADDRESS	PERIPHERAL SELECTS
MibSPIP2	0xFFF7_F600	0xFFF7_F7FF	PS[2]
MibSPI1	0xFFF7_F400	0xFFF7_F5FF	
LIN/SCI1	0xFFF7_E500	0xFFF7_E5FF	PS[6]
LIN/SCI2	0xFFF7_E400	0xFFF7_E4FF	
DCAN2	0xFFF7_DE00	0xFFF7_DFFF	PS[8]
DCAN1	0xFFF7_DC00	0xFFF7_DDFF	
ADC	0xFFF7_C000	0xFFF7_C1FF	PS[15]
GIO	0xFFF7_BC00	0xFFF7_BCFF	PS[16]
HET	0xFFF7_B800	0xFFF7_B8FF	PS[17]

2.1.3 Flash Memory

When in pipeline mode, the Flash operates with a system clock frequency of up to 80 MHz (versus a system clock in non-pipeline mode of up to 28 MHz). Flash in pipeline mode is capable of accessing 128-bit words and provides four 32-bit pipelined words to the CPU.

NOTE

1. After a system reset, pipeline mode is **disabled** [FRDCNTL[2:0] is 000b, see the Flash chapter in the *TMS470M Series Technical Reference Manual* (SPNU495). In other words, the device powers up and comes out of reset in **non-pipeline mode**.
2. **The flash external pump voltage (V_{CCP}) is required for all operations (program, erase, and read).**

2.1.4 Flash Program and Erase

The TMS470MF06607 device flash contains one 512K-byte memory array (or bank) and one 128K-byte bank for a total of 15 sectors. These 15 sectors are sized as shown in Table 2-7.

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

Table 2-7. Flash Memory Banks and Sectors

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
0	16k	0x0000_0000	0x0000_3FFF	BANK 0 (512K Bytes)
1	16k	0x0000_4000	0x0000_7FFF	
2	32k	0x0000_8000	0x0000_FFFF	
3	64k	0x0001_0000	0x0001_FFFF	
4	64k	0x0002_0000	0x0002_FFFF	
5	64k	0x0003_0000	0x0003_FFFF	
6	64k	0x0004_0000	0x0004_FFFF	
7	64k	0x0005_0000	0x0005_FFFF	
8	64k	0x0006_0000	0x0006_FFFF	
9	64k	0x0007_0000	0x0007_FFFF	

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Table 2-7. Flash Memory Banks and Sectors (continued)

SECTOR NO.	SEGMENT	LOW ADDRESS	HIGH ADDRESS	MEMORY ARRAYS (OR BANKS)
0	16k	0x0008_0000	0x0008_3FFF	BANK 1 (1) (128K Bytes)
1	16k	0x0008_4000	0x0008_7FFF	
2	16k	0x0008_8000	0x0008_BFFF	
3	16k	0x0008_C000	0x0008_FFFF	
4	64k	0x0009_0000	0x0009_FFFF	

(1) Bank 1 can be used as either EEPROM emulation space or as program space.

2.2 Terminal Functions

The terminal functions table (Table 2-8) identifies the pin names, the associated pin numbers, input voltage, output voltage, whether the pin has any internal pullup/pulldown resistors and a functional pin description.

Table 2-8. Terminal Functions

TERMINAL		INPUT VOLTAGE (1) (2)	OUTPUT CURRENT (3)	IPU/IPD (4)	DESCRIPTION
NAME	100 PIN				
HIGH-END TIMER (HET)					
HET[0]	39	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	Timer input capture or output compare. The HET[15:0] applicable pins can be programmed as general-purpose input/output (GIO) pins. All are high-resolution pins. The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and shared, then the odd pin can only be used as a general-purpose I/O. NOTE: HET[24] and HET[25] channels are muxed with TDO/TDI pins. During debug, their respective input buffers will reflect the state of TDI and TDO.
HET[1]	40				
HET[2]	49				
HET[3]	50				
HET[4]	53				
HET[5]	54				
HET[6]	55				
HET[7]	56				
HET[8]	57				
HET[9]	58				
HET[10]	59				
HET[11]	60				
HET[12]	61				
HET[13]	62				
HET[14]	63				
HET[15]	64				
HET[24]	45				
HET[25]	46				
CAN CONTROLLER 1 (DCAN1)					
CAN1STX	7	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	DCAN1 transmit pin or GIO pin.
CAN1SRX	8				DCAN1 receive pin or GIO pin.
CAN CONTROLLER 2 (DCAN2)					
CAN2STX	37	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	DCAN2 transmit pin or GIO pin
CAN2SRX	38				DCAN2 receive pin or GIO pin

(1) PWR = power, GND = ground, REF = reference voltage, NC = no connect
(2) All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
(3) The TMS470M device utilizes adaptive impedance 4 mA buffers that default to the adaptive impedance mode of operation. As a fail-safe, the adaptive impedance features of the buffer may be disabled and revert the buffer to a standard buffer mode.
(4) IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are inactive on input pins when $\overline{\text{PORRST}}$ is asserted)

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Table 2-8. Terminal Functions (continued)

TERMINAL		INPUT VOLTAGE (1) (2)	OUTPUT CURRENT (3)	IPU/IPD (4)	DESCRIPTION
NAME	100 PIN				
GENERAL-PURPOSE I/O (GIO)					
GIOA[4]/INT[4]	5	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	General-purpose input/output pins. 100 pin - GIOA[7:4]/INT[7:4] are interrupt-capable pins.
GIOA[5]/INT[5]	6				
GIOA[6]/INT[6]	15				
GIOA[7]/INT[7]	16				
MULTI-BUFFERED SERIAL PERIPHERAL INTERFACE 1 (MIBSPI1)					
MIBSPI1CLK	34	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	MIBSPI1 clock. MIBSPI1CLK can be programmed as a GIO pin.
MIBSPI1SCS[0]	33				MIBSPI1 slave chip select. MIBSPI1SCS[7:0] can be programmed as a GIO pins.
MIBSPI1sCS[1]	32				
MIBSPI1SCS[2]	31				
MIBSPI1SCS[3]	30				
MIBSPI1SCS[4]	29				
MIBSPI1SCS[5]	28				
MIBSPI1SCS[6]	27				
MIBSPI1SCS[7]	26				
MIBSPI1SIMO	35				MIBSPI1 data stream. Slave in/master out. MIBSPI1SIMO can be programmed as a GIO pin.
MIBSPI1SOMI	36				MIBSPI1 data stream. Slave out/master in. MIBSPI1SOMI can be programmed as a GIO pin.
MULTI-BUFFERED SERIAL PERIPHERAL INTERFACE 2 (MIBSPIP2)					
MIBSPIP2CLK	17	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	MIBSPIP2 clock. MIBSPIP2CLK can be programmed as a GIO pin.
$\overline{\text{MIBSPIP2SCS[0]}}$	1				MIBSPIP2 slave chip select $\overline{\text{MIBSPIP2SCS[3:0]}}$ can be programmed as GIO pins.
$\overline{\text{MIBSPIP2SCS[1]}}$	2				
$\overline{\text{MIBSPIP2SCS[2]}}$	3				
$\overline{\text{MIBSPIP2SCS[3]}}$	4				
$\overline{\text{MIBSPIP2ENA}}$	90				MIBSPIP2 enable pin. $\overline{\text{MIBSPIP2ENA}}$ can be programmed as a GIO pin.
MIBSPIP2SIMO	18				MIBSPIP2 data stream. Slave in/master out. MIBSPIP2SIMO pins can be programmed as a GIO pins.
MIBSPIP2SOMI	19				MIBSPIP2 data stream. Slave out/master in. MIBSPIP2SOMI pins can be programmed as GIO pins.
LOCAL INTERCONNECT NETWORK 1/SERIAL COMMUNICATIONS INTERFACE 1 (LIN1/SCI1)					
LIN1/SCI1RX	23	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	LIN/SCI1 data receive. Can be programmed as a GIO pin.
LIN1/SCI1TX	22				LIN/SCI1 data transmit. Can be programmed as a GIO pin.
LOCAL INTERCONNECT NETWORK 2/SERIAL COMMUNICATIONS INTERFACE 2 (LIN2/SCI2)					
LIN2/SCI2RX	25	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPU (100 µA)	LIN/SCI2 data receive. Can be programmed as a GIO pin.
LIN2/SCI2TX	24				LIN/SCI2 data transmit. Can be programmed as a GIO pin.
MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MIBADC)					
ADEVT	68	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	MibADC event input. Can be programmed as a GIO pin.

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Table 2-8. Terminal Functions (continued)

TERMINAL		INPUT VOLTAGE (1) (2)	OUTPUT CURRENT (3)	IPU/IPD (4)	DESCRIPTION
NAME	100 PIN				
ADIN[0]	69	3.3 V			MibADC analog input pins.
ADIN[1]	70				
ADIN[2]	71				
ADIN[3]	72				
ADIN[4]	73				
ADIN[5]	74				
ADIN[6]	75				
ADIN[7]	76				
ADIN[8]	77				
ADIN[9]	78				
ADIN[10]	79				
ADIN[11]	80				
ADIN[12]	81				
ADIN[13]	86				
ADIN[14]	87				
ADIN[15]	88				
AD_{REFHI}	82	3.3-V REF			MibADC module high-voltage reference input.
AD_{REFLO}	83	GND REF			MibADC module low-voltage reference input.
V_{CCAD}	85	3.3-V PWR			MibADC analog supply voltage.
V_{SSAD}	84	GND			MibADC analog ground reference.
OSCILLATOR (OSC)					
OSCIN	10	1.5-V I			Crystal connection pin or external clock input.
OSCOUT	11	1.5-V O			External crystal connection pin.
SYSTEM MODULE (SYS)					
$\overline{\text{PORRST}}$	89	3.3-V I		IPD (100 µA)	Input master chip power-up reset. External V_{CC} monitor circuitry must assert a power-on reset.
$\overline{\text{RST}}$	98	3.3-V I/O	Adaptive impedance 4 mA	IPU (100 µA)	Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset. On this pin, the output buffer is implemented as an open drain (drives low only). To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin.
ECLK	96	3.3-V I/O	Adaptive impedance 4 mA	Programmable IPD (100 µA)	Bidirectional pin. ECLK can be programmed as a GIO pin.
TEST/DEBUG (T/D)					
TCK	44	3.3-V I		IPD (100 µA)	Test clock. TCK controls the test hardware (JTAG).
TDI	46	3.3-V I/O	Adaptive impedance 4 mA	IPU (100 µA)	Test data in pin. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG). **Note: This pin is muxed with the HET channel 25.**
TDO	45			IPD (100 µA)	Test data out pin. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG). **Note: This pin is muxed with the HET channel 24.**
TMS	47			IPU (100 µA)	Serial input pin for controlling the state of the CPU test access port (TAP) controller (JTAG).
$\overline{\text{TRST}}$	48	3.3-V I		IPD (100 µA)	Test hardware reset to TAP. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic.

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Table 2-8. Terminal Functions (continued)

TERMINAL		INPUT VOLTAGE (1) (2)	OUTPUT CURRENT (3)	IPU/IPD (4)	DESCRIPTION
NAME	100 PIN				
TEST	97	3.3-V I		IPD (100 µA)	Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.
$\overline{ENZ}$	91	3.3-V I		IPD (100 µA)	Enables/disables the internal voltage regulator. 0V - Enables internal voltage regulator. 3.3V-Disables internal voltage regulator.
FLASH					
FLTP1	99				Flash Test Pad 1 pin. **For proper operation, this pin must connect only to a test pad or not be connected at all [no connect (NC)]. The test pad must not be exposed in the final product where it might be subjected to an ESD event.**
V_{CCP1}	95	3.3-V PWR			Flash external pump voltage (3.3 V). This pin is required for both Flash read and Flash program and erase operations. **V_{CCP1} and V_{CCP2} are double bonded to the same pin.**
V_{CCP2}	95				
SUPPLY VOLTAGE CORE (1.5 V)					
V_{CC}	12	1.5-V PWR			Vreg output voltage when Vreg is enabled. V_{CC} input when Vreg is disabled.
	41				
	67				
	92				
SUPPLY VOLTAGE DIGITAL I/O AND REGULATOR (3.3 V)					
V_{CCIOR}	14	3.3-V PWR			Digital I/O and internal regulator supply voltage.
	20				
	43				
	52				
	65				
	94				
SUPPLY GROUND					
V_{SS}	9	GND			Digital I/O and core supply ground reference.
	13				
	21				
	42				
	51				
	66				
	93				
	100				

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2.3 Device Support

2.3.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices and support tools. Each commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g.,TMS470MF06607). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZ), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz.

Figure 2-2 illustrates the numbering and symbol nomenclature for the TMS470M family.

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Full Part Number	TMS	470	MF	06	6	07	B	S	PZ	Q	Q1	R
Orderable Part Number	S	4	MF	06	6	07	B	S	PZ	Q	Q1	R

Prefix: TM
S = TMS Qualified
P = TMP Prototype
X = TMX Samples

Core Technology:
4 = 470 Cortex M3

Architecture:
MF = M3 Flash

Flash Memory Size:
06 = 640 KBytes

RAM Memory Size:
6 = 64 KBytes

Package Option:
07 = 100-pin package

Die Revision:
Blank = Initial Die
A = First Die Revision
B = Second Die Revision

Technology/Core Voltage:
S = F035 (130 nm), 1.5-V Nominal Core Voltage

Package Type:
PZ = 100-Pin QFP Package (Green)

Temperature Range:
I = -40°C to +85°C
T = -40°C to +105°C
Q = -40°C to +125°C

Quality Designator:
Q1 = Automotive

Shipping Options:
R = Tape and Reel

NOTE: The part number given above is for illustrative purposes only and does not represent the specific part number or silicon revision to which this document applies.

Figure 2-2. TMS470M Device Numbering Conventions

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3 Device Configuration

3.1 Reset/Abort Sources

Resets/aborts are handled as shown in Table 3-1.

Table 3-1. Reset/Abort Sources

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP, GROUP.CHANNEL
1) CPU TRANSACTIONS			
Precise write error (NCNB/Strongly Ordered)	User/Privilege	Precise Abort (CPU)	n/a
Precise read error (NCB/Device or Normal)	User/Privilege	Precise Abort (CPU)	n/a
Imprecise write error (NCB/Device or Normal)	User/Privilege	Imprecise Abort (CPU)	n/a
External imprecise error (Illegal transaction with ok response)	User/Privilege	ESM	2.17
Illegal instruction	User/Privilege	Undefined Instruction Trap (CPU)(1)	n/a
M3 Lockup	User/Privilege	ESM => NMI	2.16
MPU access violation	User/Privilege	Abort (CPU)	n/a
2) SRAM			
ECC single error (correctable)	User/Privilege	ESM	1.26
ECC double error (uncorrectable)	User/Privilege	ESM => NMI	2.6
3) FLASH WITH ECC			
ECC single error (correctable)	User/Privilege	ESM	1.6
ECC double error (uncorrectable)	User/Privilege	ESM => NMI	2.4
8) HET			
HET Memory parity error	User/Privilege	ESM	1.7
9) MIBSPI			
MibSPI1 memory parity error	User/Privilege	ESM	1.17
MibSPI2 memory parity error	User/Privilege	ESM	1.18
10) MIBADC			
Memory parity error	User/Privilege	ESM	1.19
11) DCAN/CAN			
DCAN1 memory parity error	User/Privilege	ESM	1.21
DCAN2 memory parity error	User/Privilege	ESM	1.23
13) PLL			
PLL slip error	User/Privilege	ESM	1.10
14) CLOCK MONITOR			
Clock monitor interrupt	User/Privilege	ESM	1.11
19) VOLTAGE REGULATOR			
Vcc out of range	n/a	Reset	n/a
20) CPU SELFTEST (LBIST)			
CPU Selftest (LogicBIST) error	User/Privilege	ESM	1.27
21) ERRORS REFLECTED IN THE SYSESR REGISTER			
Power-Up Reset/Vreg out of voltage(2)	n/a	Reset	n/a

(1) The undefined instruction trap is NOT detected outside of the CPU. The trap is taken only if the code reaches the execute stage of the CPU.
(2) Both a power-on reset and Vreg out-of-range reset are indicated by the PORST bit in the SYSESR register.

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Table 3-1. Reset/Abort Sources (continued)

ERROR SOURCE	SYSTEM MODE	ERROR RESPONSE	ESM HOOKUP, GROUP.CHANNEL
Oscillator fail / PLL slip(3)	n/a	Reset	n/a
M3 Lockup/LRM	n/a	Reset	n/a
Watchdog time limit exceeded	n/a	Reset	n/a
CPU Reset	n/a	Reset	n/a
Software Reset	n/a	Reset	n/a
External Reset	n/a	Reset	n/a

(3) Oscillator fail/PLL slip can be configured in the system register (SYS.PLLCTL1) to generate a reset.

3.2 Lockup Reset Module

The lockup reset module (LRM) is implemented to communicate a lockup condition by the core. The LRM provides a small watchdog timer which can generate a system reset in case a lockup condition that is identified by the core cannot be cleared by software.

3.3 ESM Assignments

The ESM module is intended for the communication critical system failures in a central location. The error indication is by an error interrupt when the failure is recognized from any detection unit. The ESM module consist of three error groups with 32 inputs each. The generation of the interrupts is shown in Table 3-2. ESM assignments are listed in Table 3-3.

Table 3-2. ESM Groups

ERROR GROUP	INTERRUPT, LEVEL
Group1	maskable, low/high
Group2	non-maskable, high
Group3	Not Used

Table 3-3. ESM Assignments

ERROR SOURCES	CHANNEL
GROUP 1	
Reserved	0 - 5
Flash - ECC Single Bit	6
HET memory parity error	7
Reserved	8-9
PLL Slip Error	10
Clock Monitor interrupt	11
Reserved	12-16
MibSPI1 memory parity error	17
MibSPIP2 memory parity error	18
MibADC memory parity error	19
Reserved	20
DCAN1 memory parity error	21
Reserved	22
DCAN2 memory parity error	23
Reserved	24-25
SRAM - single bit	26
CPU LBIST - selftest error	27

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Table 3-3. ESM Assignments (continued)

ERROR SOURCES	CHANNEL
Reserved	28-31
GROUP 2	
Reserved	0-3
Flash - Double-Bit Error (uncorrectable)	4
Reserved	5
SRAM - Double-Bit Error (uncorrectable)	6
Reserved	7-15
M3 Lockup	16
M3 External Imprecise Abort	17
Reserved	18-31

3.4 Interrupt Priority (M3VIM)

The TMS470M platform interrupt architecture includes a vectored interrupt manager (M3VIM) that provides hardware assistance for prioritizing and controlling the many interrupt sources present on a device. Table 3-4 communicates the default interrupt request assignments.

Table 3-4. Interrupt Request Assignments

MODULES	INTERRUPT SOURCES	DEFAULT VIM INTERRUPT REQUEST
ESM	ESM High level interrupt (NMI)	0
Reserved	(NMI)	1
ESM	ESM Low level interrupt	2
SYSTEM	Software interrupt (SSI)	3
RTI	RTI compare interrupt 0	4
RTI	RTI compare interrupt 1	5
RTI	RTI compare interrupt 2	6
RTI	RTI compare interrupt 3	7
RTI	RTI overflow interrupt 0	8
RTI	RTI overflow interrupt 1	9
Reserved	Reserved	10
GIO	GIO Interrupt A	11
GIO	GIO Interrupt B	12
HET	HET level 0 interrupt	13
HET	HET level 1 interrupt	14
MibSPI1	MibSPI1 level 0 interrupt	15
MibSPI1	MibSPI1 level 1 interrupt	16
Reserved	Reserved	17
LIN2/SCI2	LIN2/SCI2 level 0 interrupt	18
LIN2/SCI2	LIN2/SCI2 level 1 Interrupt	19
LIN1/SCI1	LIN1/SCI1 level 0 interrupt	20
LIN1/SCI1	LIN1/SCI1 level 1 Interrupt	21
DCAN1	DCAN1 level 0 Interrupt	22
DCAN1	DCAN1 level 1 Interrupt	23
ADC	ADC event group interrupt	24
ADC	ADC sw group 1 interrupt	25
ADC	ADC sw group 2 interrupt	26

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Table 3-4. Interrupt Request Assignments (continued)

MODULES	INTERRUPT SOURCES	DEFAULT VIM INTERRUPT REQUEST
MibSPIP2	MibSPIP2 level 0 interrupt	27
MibSPIP2	MibSPIP2 level 1 interrupt	28
DCAN2	DCAN2 level 0 interrupt	29
DCAN2	DCAN2 level 1 interrupt	30
ADC	ADC magnitude threshold interrupt	31
Reserved	Reserved	32
Reserved	Reserved	33
DCAN1	DCAN1 IF3 interrupt	34
DCAN2	DCAN2 IF3 interrupt	35
Reserved	Reserved	36-47

3.5 MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The TMS470M MibADC module stores its digital results in one of three FIFO buffers. There is one FIFO buffer for each conversion group [event, group1 (G1), and group2 (G2)], and the total MibADC FIFO on the device is divided amongst these three regions. The size of the individual group buffers are software programmable. MibADC buffers can be serviced by interrupts.

3.5.1 MIBADC Event Triggers

All three conversion groups can be configured for event-triggered operation, providing up to three event-triggered groups.

The trigger source and polarity can be selected individually for group 1, group 2 and the event group from the options identified in Table 3-5.

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Table 3-5. MibADC Event Hookup Configuration

EVENT NO.	SOURCE SELECT BITS for G1 or EVENT (G1SRC[2:0] or EVSRC[2:0])	SIGNAL PIN NAME
1	000	ADEVT
2	001	HET[1]
3	010	HET[3]
4	011	HET[16](1)
5	100	HET[18](1)
6	101	HET[24](2)
7	110	HET[26](1)
8	111	HET[28](1)

(1) These channels are available as internal signals even if they are not included as pins (Figure 1-1).
(2) During debug modes, the state of TDO will affect the state of the HET[24] input buffer.

3.6 MibSPI

The multi-buffered serial peripheral interface module allows CPU independent SPI communications with system peripherals.

The MibSPI1 module can support up to 16 transfer groups and 8 chip selects. In addition, up to 4 data formats can be supported allowing assignment of various formats to each transfer group.

The MiBSPIP2 module can support up to 8 transfer groups, 4 chip selects, and up to 4 data formats.

3.6.1 MIBSPI Event Trigger

The MibSPI module has the ability to automatically trigger SPI events based on internal and external event triggers.

The trigger sources can be selected individually for each transfer group from the options identified in Table 3-6.

Table 3-6. MibSPI1 and MibSPIP2 Event Hookup Configuration

EVENT NO.	SOURCE SELECT BITS FOR MIBSPI EVENTS TGXCTRL TRIGSRC[3:0]	SIGNAL PIN NAME
Disabled	0000	No trigger source
EVENT0	0001	GIOA[0](1)
EVENT1	0010	GIOA[1](1)
EVENT2	0011	GIOA[2](1)
EVENT3	0100	GIOA[3](1)
EVENT4	0101	GIOA[4]
EVENT5	0110	GIOA[5]
EVENT6	0111	HET[20](1)
EVENT7	1000	HET[21](1)
EVENT8	1001	HET[22](1)
EVENT9	1010	HET[23](1)
EVENT10	1011	HET[28](1)
EVENT11	1100	HET[29](1)
EVENT12	1101	HET[30](1)
EVENT13	1110	HET[31](1)
EVENT14	1111	Internal Tick Counter

(1) These channels are available as internal signals even if they are not included as pins (Figure 1-1).

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3.7 JTAG ID

The 32-bit JTAG ID code for this device is 0x0B7E202F.

3.8 Scan Chains

The device contains an ICEPICK module to access the debug scan chains; see Figure 3-1. Debug scan chain #0 handles the access to the CPU. The ICEPICK scan ID is 0x00246D15, which is the same as the device ID.

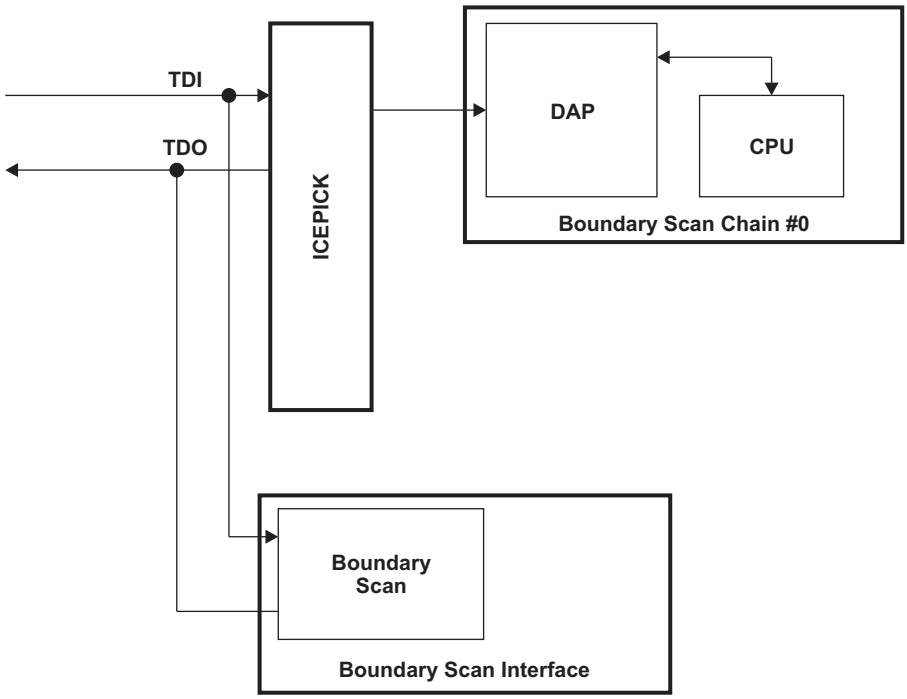


Figure 3-1. Debug Scan Chains

3.9 Low-Power Modes

TMS470M devices support multiple low-power modes. These different modes allow the user to trade-off the amount of current consumption during low power mode versus functionality and wake-up time.

Supported low-power modes on the TMS470MF06607 are Doze and Sleep; for a detailed description see the *TMS470M Series Technical Reference Manual* (SPNU495).

3.10 Adaptive Impedance 4 mA IO Buffer

The adaptive impedance 4 mA buffer is a buffer that has been explicitly designed to address the issue of decoupling EMI sources from the pins which they drive. This is accomplished by adaptively controlling the impedance of the output buffer and should be particularly effective with capacitive loads.

The adaptive impedance 4 mA buffer features two modes of operation: Impedance Control Mode, and Low-Power Mode/Standard Buffer Mode as defined below:

- **Impedance Control Mode** is enabled in the design by default. This mode adaptively controls the impedance of the output buffer.
- **Low-Power Mode** is functionally identical to **Standard Buffer Mode** and is used to configure the buffer back into a generic configuration. This buffer mode is used during low-power device modes, when it is necessary to drive the output at very high speeds, or when EMI reduction is not a concern.

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Table 3-7. Adaptive Impedance 4 mA Buffer Mode Availability

MODULE OR PIN NAME	ADAPTIVE IMPEDANCE 4 mA BUFFER SIGNAL REGISTER HOOKUP	
	LOW-POWER MODE (LPM)	STANDARD BUFFER ENABLE (SBEN)(1)
SYS.ECLK	SYS.VRCTL.VLPMENA	GPREG1.0
SYS.nRST	SYS.VRCTL.VLPMENA	GPREG1.1
SYS.TDI/TDO	SYS.VRCTL.VLPMENA	Standard Buffer Enabled
SYS.TMSC	SYS.VRCTL.VLPMENA	Standard Buffer Enabled
HET	SYS.VRCTL.VLPMENA	GPREG1.2
SCI1	SYS.VRCTL.VLPMENA	GPREG1.3
LIN/SCI2	SYS.VRCTL.VLPMENA	GPREG1.4
MIBSPI1	SYS.VRCTL.VLPMENA	GPREG1.5
MIBSPIP2	SYS.VRCTL.VLPMENA	GPREG1.6
Reserved	SYS.VRCTL.VLPMENA	GPREG1.7
MIBADC.ADEVT	SYS.VRCTL.VLPMENA	GPREG1.8
DCAN1	SYS.VRCTL.VLPMENA	GPREG1.9
DCAN2	SYS.VRCTL.VLPMENA	GPREG1.10
GIOA	SYS.VRCTL.VLPMENA	GPREG1.11

(1) SBEN configuration can be achieved using the GPREG register within the system frame (0xFFFFFFA0).

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3.10.1 Standard Buffer Enable Register (GPREG1)

A general purpose register with the system frame has been utilized to control the enabling of standard buffer mode. This register is shown in Figure 3-2 and described in Table 3-8

31							16
Reserved							
R-0							
15			12	11	10	9	8
Reserved				GIOA_SBEN	DCAN2_SBEN	DCAN1_SBEN	ADC.ADEVT_SBEN
R-0				RW-0	RW-0	RW-0	RW-0
7	6	5	4	3	2	1	0
Reserved	MIBSPIP2_SBEN	MIBSPI1_SBEN	LIN2SCI2_SBEN	LIN1SCI1_SBEN	HET_SBEN	$\overline{\text{RST}}$_SBEN	ECLK_SBEN
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-2. General-Purpose Register 1 (GPREG1)

Table 3-8. General-Purpose Register 1 (GPREG1) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved		These bits are reserved. Reads return 0 and writes have no effect.
11	GIOA_SBEN		GIOA port standard buffer enable bit. This bit enables/disables standard buffer mode for all GIOA pins
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
10	DCAN2_SBEN		DCAN2 standard buffer enable bit. This bit enables/disables standard buffer mode for all DCAN2 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
9	DCAN1_SBEN		DCAN1 standard buffer enable bit. This bit enables/disables standard buffer mode for all DCAN1 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
8	ADC.ADEVT_SBEN		ADC.ADEVT standard buffer enable bit. This bit enables/disables standard buffer mode for the ADC.ADEVT pin.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for the ADEVT pin.
7	Reserved		Reserved
		0	Reserved
		1	Reserved
6	MIBSPIP2_SBEN		MIBSPIP2 standard buffer enable bit. This bit enables/disables standard buffer mode for all MIBSPIP2 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
5	MIBSPI1		MIBSPI1 standard buffer enable bit. This bit enables/disables standard buffer mode for all MIBSPI1 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
4	LIN2SCI2_SBEN		LINSCI2 standard buffer enable bit. This bit enables/disables standard buffer mode for all LINSCI2 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.

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Table 3-8. General-Purpose Register 1 (GPREG1) Field Descriptions (continued)

Bit	Field	Value	Description
3	LIN1SCI1_SBEN		SCI1 standard buffer enable bit. This bit enables/disables standard buffer mode for all SCI1 pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
2	HET_SBEN		HET standard buffer enable bit. This bit enables/disables standard buffer mode for all HET pins.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for all associated module pins.
1	$\overline{\text{RST}}$_SBEN		$\overline{\text{RST}}$ standard buffer enable bit. This bit enables/disables standard buffer mode for the $\overline{\text{RST}}$ pin.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for the $\overline{\text{RST}}$ pin.
0	ECLK_SBEN		ECLK standard buffer enable bit. This bit enables/disables standard buffer mode for the ECLK pin.
		0	Standard buffer mode is not enabled.
		1	Standard buffer mode is enabled for the ECLK pin.

3.10.2 Coresight Components/Debug ROM

Coresight registers are memory-mapped and accessible via the CPU and JTAG.

Table 3-9. Debug Component Memory Map

COMPONENT	FRAME START ADDRESS	FRAME END ADDRESS	FRAME SIZE	MEMORY TYPE
M3 INTEGRATION FRAME				
ITM(1)	0xE000_0000	0xE000_0FFF	4K	Control Registers for debug and trace modules
DWT	0xE000_1000	0xE000_1FFF	4K	
FPB	0xE000_2000	0xE000_2FFF	4K	
NVIC	0xE000_E000	0xE000_EFFF	4K	
Debug ROM 1	0xE00F_F000	0xE00F_FFFF	4K	
PLATFORM DEBUG FRAME				
Debug ROM 2	0xFFA0_0000	0xFFA0_0FFF	4K	Control Registers for debug and trace modules
ETM-M3(1)	0xFFA0_1000	0xFFA0_1FFF	4K	
HTM(1)	0xFFA0_2000	0xFFA0_2FFF	4K	
Trace Funnel	0xFFA0_3000	0xFFA0_3FFF	4K	
TPIU	0xFFA0_4000	0xFFA0_4FFF	4K	

(1) Availability of trace components, although present in the design, are not externally available in the PZ packaged devices. A suitable emulation capable package is available from TI if a need for trace capability exists.

Table 3-10. Debug ROM contents for Debug ROM 1 (M3 ROM)

ADDRESS OFFSET (see Table 3-9)	DESCRIPTION	VALUE
0x000	NVIC	0xFFF0_F003
0x004	DWT	0xFFF0_2003
0x008	FPB	0xFFF0_3003
0x00C	ITM	0xFFF0_1003

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Table 3-10. Debug ROM contents for Debug ROM 1 (M3 ROM) (continued)

ADDRESS OFFSET (see Table 3-9)	DESCRIPTION	VALUE
0x010	TPIU(1)	0xFFF4_1002
0x014	ETM(1)	0xFFF4_2002
0x018	Debug ROM 2 (CoreSight ROM)	0x1F90_1003
0x01C	End of Table	0x0000_0000
0x020 - 0xEFC	Unused	0x0000_0000
0xF00 - 0xFC8	Reserved	0x0000_0000
0xFCC	MEMTYPE	0x0000_0001
0xFD0	PID4	0x0000_0000
0xFD4	PID5	0x0000_0000
0xFD8	PID6	0x0000_0000
0xFDC	PID7	0x0000_0000
0xFE0	PID0	0x0000_0000
0xFE4	PID1	0x0000_0000
0xFE8	PID2	0x0000_0000
0xFEC	PID3	0x0000_0000
0xFF0	CID0	0x0000_000D
0xFF4	CID1	0x0000_0010
0xFF8	CID2	0x0000_0005
0xFFC	CID3	0x0000_00B1

(1) Cortex™-M3 debug ROM always will have entries for optional components TPIU and ETM. Whether or not these components are present is determined by bit number 0 of the entry value.

Table 3-11. Debug ROM contents for Debug ROM 2 (CoreSight ROM)

ADDRESS OFFSET (see Table 3-9)	DESCRIPTION	VALUE
0x000	ETM-M3	0x0000_1003
0x004	HTM	0x0000_2003
0x008	Trace Funnel	0x0000_3003
0x00C	TPIU	0x0000_4003
0x010	End of Table	0x0000_0000
0x014 - 0xEFC	Unused	0x0000_0000
0xF00 - 0xFCC	Reserved	0x0000_0000
0xFD0	PID4	0x0000_0000
0xFD4	PID5	0x0000_0000
0xFD8	PID6	0x0000_0000
0xFDC	PID7	0x0000_0000
0xFE0	PID0	0x0000_0000
0xFE4	PID1	0x0000_0007
0xFE8	PID2	0x0000_0009
0xFEC	PID3	0x0000_0000
0xFF0	CID0	0x0000_000D
0xFF4	CID1	0x0000_0010
0xFF8	CID2	0x0000_0005
0xFFC	CID3	0x0000_00B1

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3.11 Built-In Self Test (BIST) Features

3.11.1 STC/LBIST

The TMS470M family supports a logic built-in self test (LBIST or CPUBIST) of the M3 CPU.

LBIST testing can be performed in two modes of operation:

- **Full Execution.** In this mode, the full suite of test patterns is run without interruption. This test is started via CPU control and is well suited for use at device start up.
- **Cyclic Execution.** During cyclic execution, a small percentage of time will be dedicated to running a subset of the self-test (STC Intervals). This mode is well suited for executing on a periodic basis to minimize the bandwidth use. After all STC intervals are executed, all test patterns will have been run.

NOTE

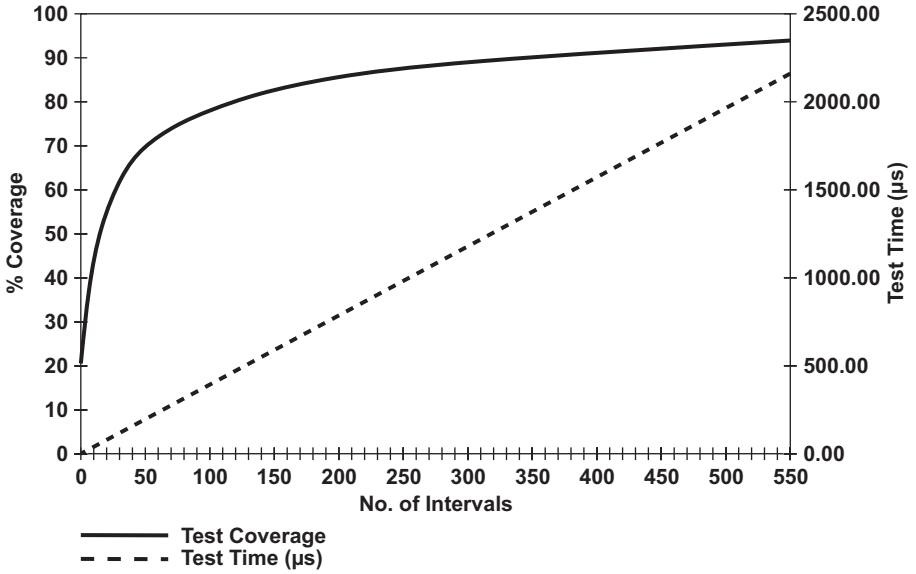
1. The application will need to disable peripherals and or interrupts to avoid missing interrupts.
2. No debugger interaction is possible with the CPU during self test. This includes access to memory and registers since access is through the CPU.

The default value of the LBIST clock prescaler (STCDIV) is *divide-by-1*; however, the maximum STC CLK is limited by the current consumption and supply capability of the Vreg. For specified maximum STC clock rates for specified operating frequencies, see Table 3-12.

Table 3-12. Maximum STC Clock Frequencies vs HCLK(1)

HCLK FREQUENCY (MHz)	STC DIVIDER (STC_DIV+1)	STC CLOCK FREQUENCY (MHz)
80	2	40
72	2	36
56	2	28
28	1	28

(1) The maximum LBIST STC clock frequency is limited to 40MHz.



A. A single LBIST interval is 158 STC CLK cycles in duration, excluding clock transition timing of 20 cycles.
B. This device has 550 total intervals.

Figure 3-3. CPU BIST Intervals vs Coverage

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3.11.2 MBIST

The TMS470M family supports memory built-in self test (MBIST) of the system and peripheral SRAM. The MBIST is accessible via the application in order to facilitate memory self test by the application by enabling the MBIST controllers associated with the specific RAMs to be tested. (For device-specific MBIST controller assignments, see Table 2-3.)

The MBIST controller:

- Supports testing of all system and peripheral RAM.
- Captures the MBIST results in the MBIST status register (MSTFAIL).
- Supports execution of each Memory BIST controller in parallel (MSINENA).
  For MSIENA bit assignments, see Table 2-3
- Supports execution of each Memory BIST controller individually (MSINENA).
  For MSIENA bit assignments, see Table 2-3

The MBIST controller selection is mapped to the MBIST controller/memory initialization enable register (MSIENA) within the SYS register frame. Each MBIST controller is enabled by setting the corresponding bit within this register and then enabling memory self-test via the memory self-test global enable within the global control register (MSTGCR.MSTGENA[3:0]).

The MBIST controllers support execution of the following tests:

- March13N, background 0
- March11N, background A
- Checkerboard and Inverse Checkerboard
- March13N, background 3, 0F, and 69
- PMOS Address decoder Algorithm
- ROM2 algorithm for STC

NOTE

The algorithm to be applied is selectable via the memory self-test global control register algo selection field (MSTGCR.MBIST_ALGSEL[7:0]).

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3.12 Device Identification Code Register

The device identification code register identifies the coprocessor status, an assigned device-specific part number, the technology family (TF), the I/O voltage, whether or not parity is supported, the levels of flash and RAM error detection, and the device version. The TMS470M device identification code base register value is 0X00246D15 and is subject to change based on the silicon version.

31	30														17	16
CP15	PART NUMBER															TF
R-0	R-00000000010010															R-0

15	13	12	11	10	9	8
TF		I/O VOLT	PP	FLASHECC		RAMECC
R-011		R-0	R-1	R-10		R-1

7	3	2	1	0
VERSION		1	0	1
R-0010		R-1	R-0	R-1

LEGEND: R = Read only; -*n* = value after reset

Figure 3-4. TMS470M Device ID Bit Allocation Register

Table 3-13. TMS470M Device ID Bit Allocation Register Field Descriptions

Bit	Field	Value	Description
31	CP15		This bit indicates the presence of coprocessor (CP15).
		0	No coprocessor present in the device.
		1	Coprocessor present in the device.
30-17	PART NUMBER		These bits indicate the assigned device-specific part number. The assigned device-specific part number for the TMS470M device is 00000000010010.
16-13	TF		Technology family bit. These bits indicate the technology family (C05, F05, F035, C035).
		0011	F035
12	I/O VOLT		I/O voltage bit. This bit identifies the I/O power supply.
		0	3.3 V
		1	5 V
11	PP		Peripheral parity bit. This bit indicates whether parity is supported.
		0	No parity on peripheral.
		1	Parity on peripheral.
10	FLASHECC		Flash ECC bits. These bits indicate the level of error detection and correction on the flash memory.
		00	No error detection/correction.
		01	Program memory with parity.
		10	Program memory with ECC.
		11	Reserved
8	RAMECC		RAM ECC bits. This bit indicates the presence of error detection and correction on the CPU RAM.
		0	RAM ECC not present.
		1	RAM ECC present.
7-3	VERSION		These bits identify the silicon version of the device.
2-0	101		Bits 2:0 are set to 101 by default to indicate a platform device.

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3.13 Device Part Numbers

Table 3-14 lists all the available TMS470MF06607 device configurations.

Table 3-14. Device Part Numbers

DEVICE PART NUMBER	SAP PART NUMBER	PROGRAM MEMORY	PACKAGE TYPE	TEMPERATURE RANGE	PbFREE/ GREEN(1)
		FLASH EEPROM	100-PIN LQFP	-40°C to 125°C	
TMS470MF06607BPZQ	S4MF06607BSPZQQ1	X	X	X	X

(1) RoHS compliant products are compatible with the current RoHS requirements for all six substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials, unless exempt. Pb-Free products are RoHS Compliant, plus suitable for use in higher temperature lead-free solder processes (typically 245 to 260°C). Green products are RoHS and Pb-Free, plus also free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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4 Device Operating Conditions

4.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range, Q Version(1)

Supply voltage range:	V_{CC} (2)	-0.5 V to 2.1 V
	V_{CCIOR}, V_{CCAD}, V_{CC} (Flash pump) (2)	-0.5 V to 4.1 V
Input voltage range:	All input pins	-0.5 V to 4.1 V
Input clamp current:	I_{IK} (V_I < 0 or V_I > V_{CCIOR}) All pins, except ADIN[0:15]	±20 mA
	I_{IK} (V_I < 0 or V_I > V_{CCIOR}) ADIN[0:15]	±10 mA
Operating free-air temperature range, T_A:	Q version	-40°C to 125°C
Operating junction temperature range, T_J:	Standard	-40°C to 150°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated grounds.

4.2 Device Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
V_{CCIOR}	Digital I/O and internal regulator supply voltage		3	3.3	3.6	V
V_{CC}	Voltage regulator output voltage		1.40	1.55	1.70	V
V_{CCAD}	MibADC supply voltage		3	3.3	3.6	V
V_{CCP}	Flash pump supply voltage		3	3.3	3.6	V
V_{SS}	Digital logic supply ground			0		V
V_{SSAD}	MibADC supply ground		-0.1		0.1	V
T_A	Operating free-air temperature	Q version	-40		125	°C
T_J	Operating junction temperature		-40		150	°C

(1) All voltages are with respect to V_{SS}, except V_{CCAD}, which is with respect to V_{SSAD}.

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4.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, Q Version[1][2]

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Input hysteresis			150			mV
V_{IL}	Low-level input voltage	All inputs[3]		-0.3		0.8	V
		OSCIN				0.2 V_{CC}	V
V_{IH}	High-level input voltage	All inputs[3]		2		V_{CCIOR} + 0.3	V
		OSCIN		0.8 V_{CC}			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.2 V_{CCIOR}	V
			I_{OL} = 50 µA Standard mode			0.2	
			I_{OL} = 50 µA Impedance Control mode			0.2 V_{CCIOR}	
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MAX	0.8 V_{CCIOR}			V
			I_{OH} = 50 µA Standard mode	V_{CCIOR} -0.2			
			I_{OH} = 50 µA Impedance Control mode	0.8 V_{CCIOR}			
I_{IC}	Input clamp current (I/O pins)[4]		V_I < V_{SSIO} - 0.3 or V_I > V_{CCIOR} + 0.3	-2		2	mA
I_I	Input current (I/O pins)	I_{IH} Pulldown	V_I = V_{CCIOR}	45		190	µA
		I_{IL} Pullup	V_I = V_{SS}	-190		-45	
		All other pins	No pullup or pulldown	-1		1	
I_{OL}	Low-level output tcurrent	Adaptive Impedance 4 mA Buffer	V_{OL} = V_{OL} MAX			4	mA
I_{OH}	High-level output current	Adaptive Impedance 4 mA Buffer	V_{OH} = V_{OH} MIN	-4			mA
I_{CC}	V_{CC} digital supply current (operating mode, internal regulator disabled)		HCLK = 80 MHz, VCLK = 80 MHz, V_{CC} = 1.70 V[5]			115	mA

(1) Source currents (out of the device) are negative while sink currents (into the device) are positive.
(2) "All frequencies" will include all specified device configuration frequencies.
(3) The V_{IL} here does not apply to the OSCIN, and $\overline{PORRST}$ pins; the V_{IH} here does not apply to the OSCIN, and $\overline{RST}$ pins; For $\overline{RST}$ and $\overline{PORRST}$ exceptions, see Section 5.1.
(4) Parameter does not apply to input-only or output-only pins.
(5) Maximum currents are measured using a system-level test case. This test case exercises all of the device peripherals concurrently (excluding MBIST and STC LBIST).

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Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, Q Version[1][2] *(continued)*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCIOR}	V_{CCIOR} IO and digital supply current (operating mode, internal regulator enabled)	HCLK = 80 MHz, VCLK = 80 MHz, No DC load, V_{CCIOR} = 3.6 V[5][6]			120	mA
	V_{CCIOR} IO and digital supply current (LBIST execution, internal regulator enabled)[7]	HCLK = 80 MHz, VCLK = 80 MHz, STCCLK = 40 MHz, No DC load, V_{CCIOR} = 3.6 V[6]			170	
	V_{CCIOR} IO and digital supply current (MBIST execution, internal regulator enabled)[8]	HCLK = 80 MHz, VCLK = 80 MHz, No DC load, V_{CCIOR} = 3.6 V[6]			180	
	V_{CCIOR} IO and digital supply current (doze mode, internal regulator enabled)	No DC load, V_{CCIOR} = 3.6 V[6][9]		2[10]		
	V_{CCIOR} IO and digital supply current (sleep mode, internal regulator enabled)	No DC load, V_{CCIOR} = 3.6 V[6][9]		200[10]		µA
I_{CCAD}	V_{CCAD} supply current (operating mode)	All frequencies, V_{CCAD} = 3.6 V[11]			8	mA
I_{CCP}	V_{CCP} pump supply current	V_{CCP} = 3.6 V read operation[5]			10	mA
		V_{CCP} = 3.6 V program[11]			75	
		V_{CCP} = 3.6 V erase			75	
$I_{CCTOTAL}$[12]	V_{CCIOR} + V_{CCAD} + V_{CCP} total digital supply current (operating mode, internal regulator enabled)	HCLK = 80 MHz, VCLK = 80 MHz, No DC load, V_{CCIOR} = 3.6 V[5][6]			135	mA
	V_{CCIOR} + V_{CCAD} + V_{CCP} total digital supply current (doze mode, internal regulator enabled)	No DC load, V_{CCIOR} = 3.6 V[6][9]		2[10]		
	V_{CCIOR} + V_{CCAD} + V_{CCP} total digital supply current (sleep mode, internal regulator enabled)	No DC load, V_{CCIOR} = 3.6 V[6][9]		200[10]		µA
C_I	Input capacitance			6		pF
C_O	Output capacitance			7		pF

(6) I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ V_{CCIO} - 0.2 V. ECLK output ≤ 2 MHz.
(7) LBIST current specified is peak current for the maximum supported operating clock (HCLK = 80 MHz) and STC CLK = HCLK/2. Lower current consumption can be achieved by configuring a slower STC Clock frequency. The current peak duration can last for the duration of 1 LBIST test interval.
(8) MBIST currents specified are for execution of MBIST on all RAMs in parallel. Lower current consumption can be achieved by sequenced execution of MBIST on each of the RAM spaces available.
(9) For Flash banks/pumps in sleep mode.
(10) Typical doze and sleep currents represent measurements under nominal conditions (baseline/nominal material, 30°C, 3.3 V).
(11) Assumes reading from one bank while programming the same bank.
(12) Total device operating current is derived from the total I_{CCIOR}, I_{CCAD}, and I_{CCP} in normal operating mode excluding MBIST and LBIST execution. It is expected that the total will be less than the sums of the values of the individual components due to statistical calculations involved in producing the specification values.

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5 Peripheral Information and Electrical Specifications

5.1 $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ Timings(13)

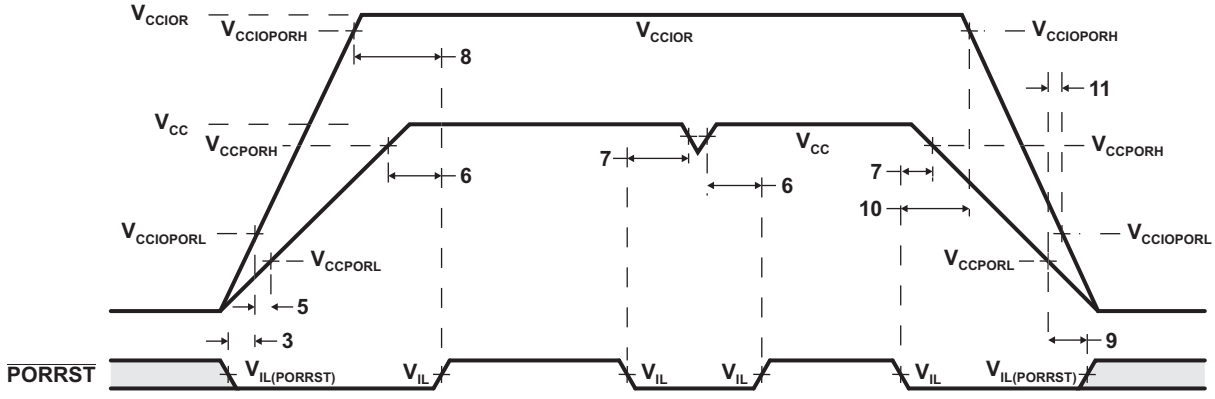
(13) When the V_{CC} timing requirements for $\overline{\text{PORRST}}$ are satisfied, there are no timing requirements for V_{CCP}.

Table 5-1. Timing Requirements for $\overline{\text{PORRST}}$

(see Figure 5-1)

NO.			MIN	MAX	UNIT
	V_{CCPORL}	V_{CC} low supply level when $\overline{\text{RST}}$ becomes active	1.30		V
	V_{CCPORH}	V_{CC} high supply level when $\overline{\text{RST}}$ becomes active		1.80	V
	$V_{CCIOPORL}$	V_{CCIO} low supply level when $\overline{\text{PORRST}}$ must be active during power up		1.1	V
	$V_{CCIOPORH}$	V_{CCIO} high supply level when $\overline{\text{PORRST}}$ must remain active during power up and become active during power down	3.0		V
	V_{IL} (1)	Low-level input voltage after $V_{CCIOR} > V_{CCIOPORH}$		0.2 V_{CCIOR}	V
	V_{OH} (2)	High-level output voltage after $V_{CCIOR} > V_{CCIOPORH}$	0.8 V_{CCIOR}		V
	$V_{IL(PORRST)}$	Low-level input voltage of $\overline{\text{PORRST}}$ before $V_{CCIOR} > V_{CCIOPORL}$		0.5	V
3	$t_{su(PORRST)r}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CCIOR} > V_{CCIOPORL}$ during power up	0		ms
5	$t_{su(VCCIOR)r}$	Setup time, $V_{CCIOR} > V_{CCIOPORL}$ before $V_{CC} > V_{CCPORL}$	0		ms
6	$t_{h(PORRST)r}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CC} > V_{CCPORH}$	1		ms
7	$t_{su(PORRST)f}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \le V_{CCPORH}$ during power down	8		µs
8	$t_{h(PORRST)rio}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CCIOR} > V_{CCIOPORH}$	1		ms
9	$t_{h(PORRST)d}$	Hold time, $\overline{\text{PORRST}}$ active after $V_{CCIOR} < V_{CCIORPORL}$	0		ms
10	$t_{su(PORRST)fio}$	Setup time, $\overline{\text{PORRST}}$ active before $V_{CC} \le V_{CCIOPORH}$ during power down	0		ns
11	$t_{su(VCCIO)f}$	Setup time, $V_{CC} <$ $_{VCCPORE}$ before $V_{CCIO} < V_{CCIOPORL}$	0		ns
	$t_{f(PORRST)}$	Filter time $\overline{\text{PORRST}}$, pulses less than MIN get filtered out; pulses greater than MAX generate a reset.	30	150	ns
	$t_{f(RST)}$	Filter time $\overline{\text{RST}}$, pulses less than MIN get filtered out; pulses greater than MAX generate a reset.	40	150	ns

(1) Corresponds to $\overline{\text{PORRST}}$.
(2) Corresponds to $\overline{\text{RST}}$.



V_{CC} (1.55 V)
V_{CCP}/V_{CCIOR} (3.3 V)

Note: V_{CC} is provided by the on-chip voltage regulator during normal application run time. It is not recommended to use the device in an application with the Vreg disabled due to potential glitching issues; however, if used in this mode, the application should ensure that the specified voltage ranges for V_{CC} are maintained.

Figure 5-1. $\overline{\text{PORRST}}$ Timing Diagram

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Table 5-2. Switching Characteristics Over Recommended Operating Conditions for $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$(1)

PARAMETER		MIN	MAX	UNIT
$t_{v(RST)}$	Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive	$1024t_{c(OSC)}$		ns
	Valid time, $\overline{\text{RST}}$ active (all others)	$8t_{c(VCLK)}$		
$V_{CCIOPORL}$	Vccio low supply level when $\overline{\text{PORRST}}$ must be active during power-up and power-down		1.1	V

(1) Specified values do NOT include rise/fall times. For rise and fall timings, see Table 5-13.

Table 5-3. Internal Voltage Regulator Specifications

PARAMETER		MIN	MAX	UNIT
$t_{D(VCCIOR)0-3}$	Delay time, input supply to ramp from 0 V to 3 V	12		µs
$t_{V(PORRST)L}$	Valid time, $\overline{\text{PORRST}}$ active after input supply becomes ≥ 3.0 V	1		ms
$V_{CCIORmin(PORRST)f}$	Minimum input voltage, when $\overline{\text{PORRST}}$ must be made active during power down or brown out	3.0		V
$C_{(VCC)core}$	Capacitance distributed over core V_{CC} pins for voltage regulator stability	1.2	6.0	µF
$ESR_{(max)core}$	Total combined ESR of stabilization capacitors on core V_{CC} pins	0	0.75	Ω

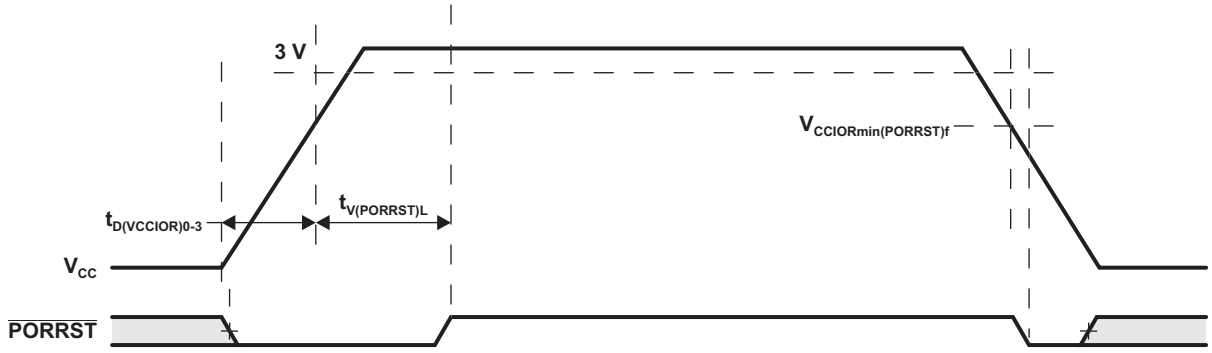


Figure 5-2. $\overline{\text{PORRST}}$ Timing Requirements

Table 5-4. VREG Recommended Operation Conditions

PARAMETER		CONDITIONS	MIN	MAX	UNIT
I_{CC}	V_{CC} Load Rating	Normal mode, regulator active	0	200	mA
		Sleep mode, regulator active		5	mA
		Off, enable forced off	-	-	µA

Table 5-5. VREG Sleep-Mode Timing Characteristics(1)

PARAMETER		MIN	MAX	UNIT
$t_{normal-sleep}$	Transition time between normal mode and sleep mode		70	ns
$t_{sleep-normal}$	Transition time between sleep mode and normal mode		3.5	µs

(1) These times only reflect VREG transition times. Times for other components are not included.

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5.1.1 Sequence to Wake Up from Doze Mode

In doze mode, the HCLK, GCLK, VCLK, and VCLK2 are all turned off. Also, the main oscillator is the only clock source running while in doze mode. For more details on the doze mode, see the *TMS470M Series Technical Reference Manual* (SPNU495). Doze mode is not supported if the internal voltage regulator is disabled.

The RTICLK is still active, which allows the RTI module to generate periodic wake up interrupts, if required. The other wake-up options are: external interrupts via GIO pins, CAN message, and SCI/LIN. The sequence for waking up from doze mode is described below:

1. Wake-up request is received/generated. Figure 5-3 shows the CAN module generating the wakeup interrupt.
2. This wake-up event causes the core VREG to wake up.
3. Since the main oscillator is running already it is used as the clock source upon wake up.
4. The software runs using the main oscillator as the clock source. Also, the PLL can now be enabled.
5. Once the PLL has acquired LOCK, the software can switch over to using the PLL output clock for normal operation.

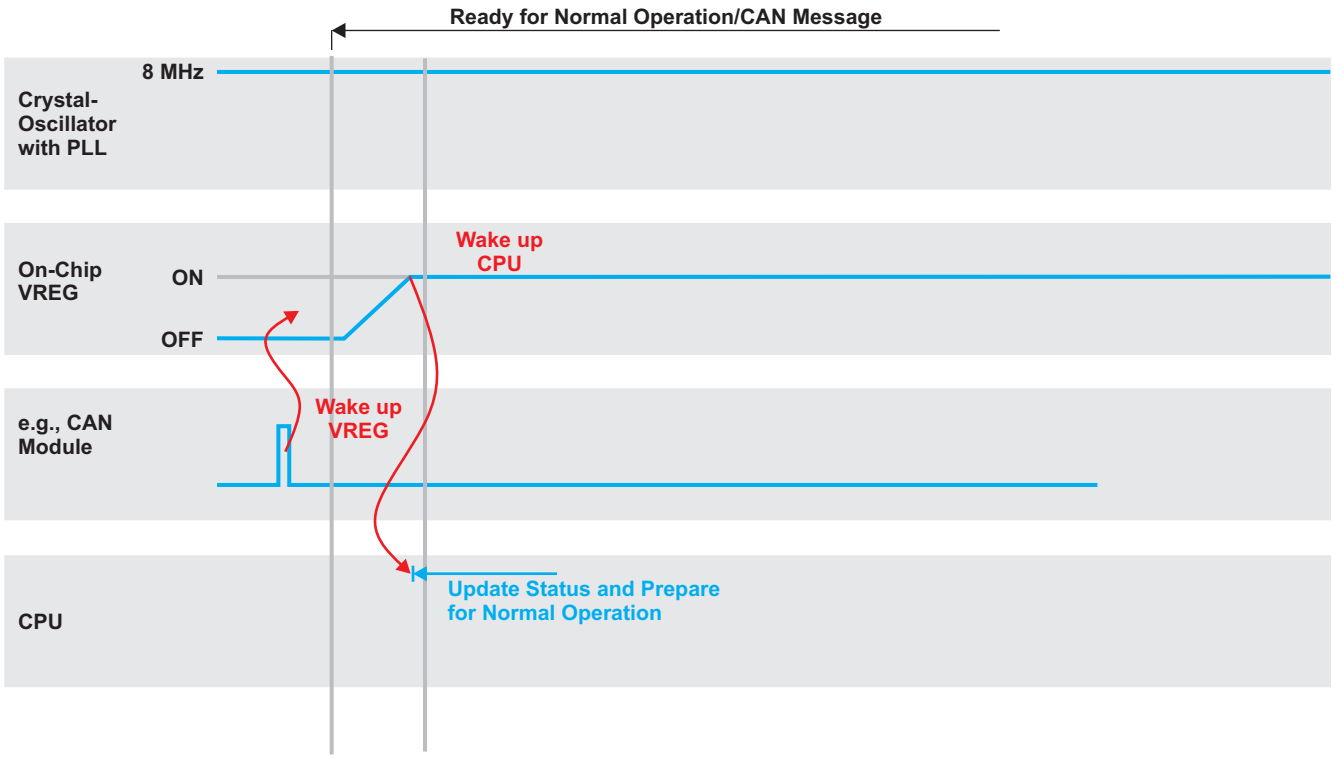


Figure 5-3. Wake Up From Doze Mode

5.1.2 Sequence to Wake Up from Sleep Mode

In sleep mode, ***all*** the clocks are turned off: HCLK, GCLK, VCLK, VCLK2, and RTICLK. All the clock sources are also disabled. For more details on sleep mode, see the *TMS470M Series Technical Reference Manual* (SPNU495). Sleep mode is not supported if the internal voltage regulator is disabled.

The wake-up options are: external interrupts via GIO pins, CAN, and SCI/LIN. The sequence for waking up from the sleep mode is described below:

1. Wake-up request is received/generated. Figure 5-4 shows the CAN module generating the wake-up interrupt based on a message received.
2. This wake-up event causes the on-chip VREG to wake up.
3. Once the on-chip VREG wakes up, the CPU and the main oscillator start to wake up.
4. Once the main oscillator output is valid, the software runs using the main oscillator as the clock source. The software can prepare for normal operation. Also, now the PLL can be enabled.
5. Once the PLL has acquired LOCK, the software can switch over to using the PLL output clock for normal operation.

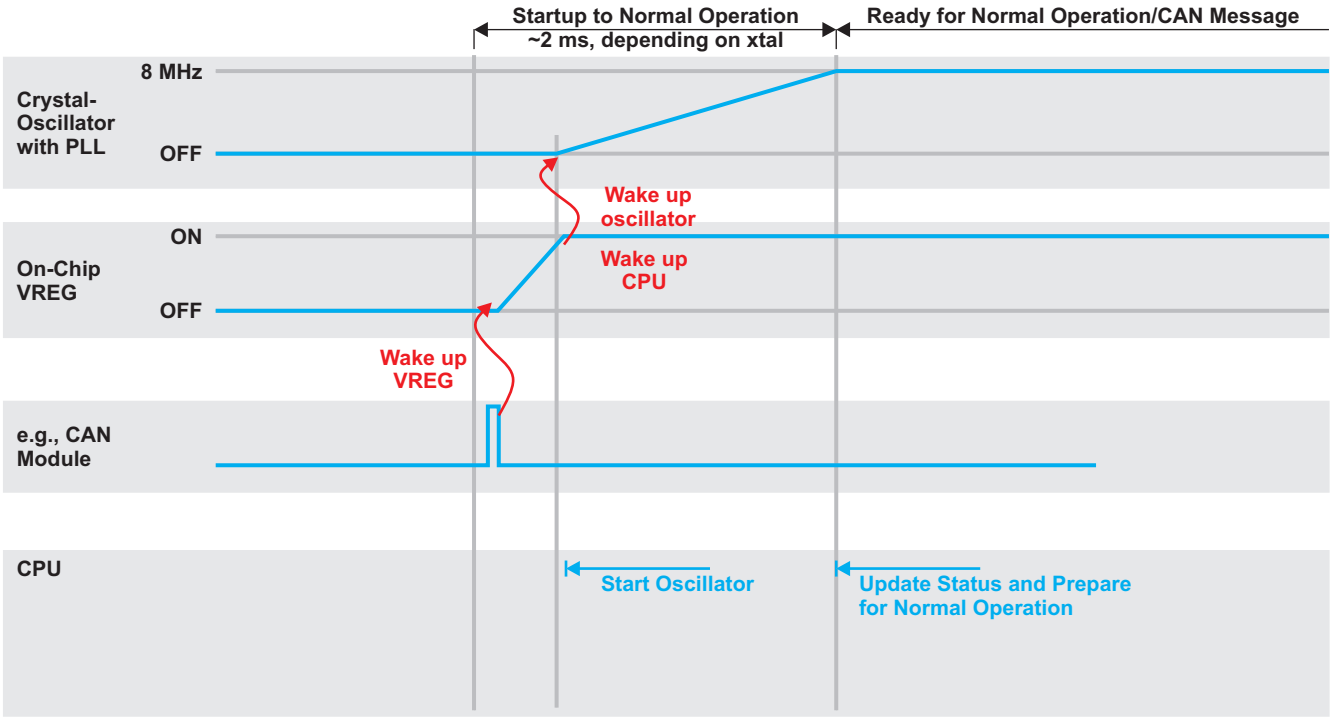


Figure 5-4. Wake Up From Sleep Mode

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Table 5-6. Summary of Wake Up from Low-Power Modes(1)

MODE	CLOCK SOURCE ACTIVE	ACTIVE CLOCKS	WAKE-UP OPTIONS	WAKE-UP CLOCK SOURCE	WAKE-UP TIMES
Doze	Oscillator	RTICLK1	GIO interrupts, CAN Rx, SCI/LIN Rx, RTI	Oscillator	VREG wake up(2) + flash pump sleep(3) + flash pump standby(4)
Sleep	None	None	GIO interrupts, CAN Rx, SCI/LIN Rx	Oscillator	VREG wakeup + Osc. startup + 1024 Osc. cycles + flash pump sleep + flash pump standby

(1) Low-power modes are not supported if the internal voltage regulator is disabled.
(2) VREG wake up = $t_{halt\text{-}normal}$ (see Table 5-4).
(3) Flash pump sleep = minimum time for which the flash pump is in sleep mode before it enters standby mode = 20 µs. The flash pump sleep to standby counter must be programmed such that the (counter value X wake-up clock source period) is at least 20 µs.
(4) Flash pump standby = minimum time for which the flash pump is in standby mode before it enters active mode = 1 µs. The flash pump standby2active counter must be programmed such that the (counter value X wake-up clock source period) is at least 1 µs.

NOTE

The flash banks will wake up in parallel with the flash pump. The flash banks can wake up faster than the flash pump and therefore the overall flash module wake-up time is determined by the pump wake-up time.

5.2 PLL and Clock Specifications

Table 5-7. Timing Requirements for PLL Circuits Enabled or Disabled

PARAMETER		MIN	MAX	UNIT
$f_{(OSC)}$	Input clock frequency	5	20	MHz
$t_{c(OSC)}$	Cycle time, OSCIN	50		ns
$t_{w(OSCIL)}$	Pulse duration, OSCIN low	15		ns
$t_{w(OSCIH)}$	Pulse duration, OSCIN high	15		ns

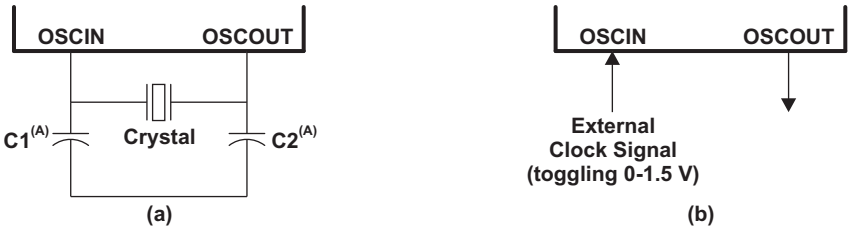
5.2.1 External Reference Resonator/Crystal Oscillator Clock Option

The oscillator is enabled by connecting the appropriate fundamental 5-20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 5-5(a). The oscillator is a single stage inverter held in bias by an integrated bias resistor.

TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. Vendors are equipped to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

5.2.2 External Clock Source

An external oscillator source can be used by connecting a 1.5-V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 5-5(b).



A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

Figure 5-5. Recommended Crystal/Clock Connection

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5.2.3 LPO and Clock Detection

The LPOCLKDET module consists of a clock monitor (CLKDET) and 2 low-power oscillators (LPO): a low-frequency (LF) and a high-frequency (HF) oscillator. The CLKDET is a supervisor circuit for an externally supplied clock signal. In case the externally supplied clock frequency falls out of a frequency window, the clock detector flags this condition and switches to the HF LPO clock (limp mode). The OSCFAIL flag and clock switch-over remain, regardless of the behavior of the oscillator clock signal. The only way OSCFAIL can be cleared (and OSCIN be again the driving clock) is a power-on reset.

Table 5-8. LPO and Clock Detection

PARAMETER		MIN	TYP	MAX	UNIT
invalid frequency	Lower threshold	1.5		5.0	MHz
	Higher threshold	20.0		50.0	MHz
limp mode frequency (HFosc)		9.0	12	14.0	MHz
LFosc frequency		79	90	110	kHz
HFosc frequency		9.0	12	14.0	MHz

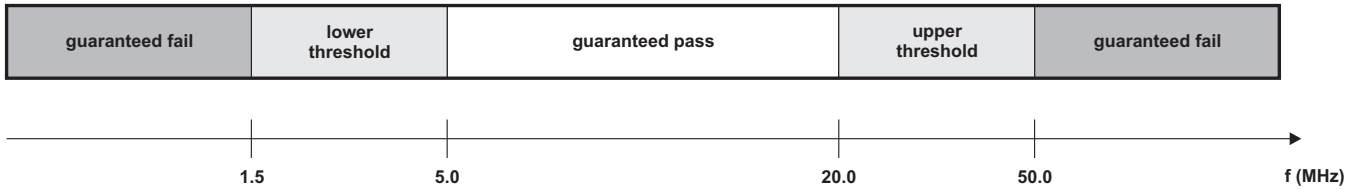
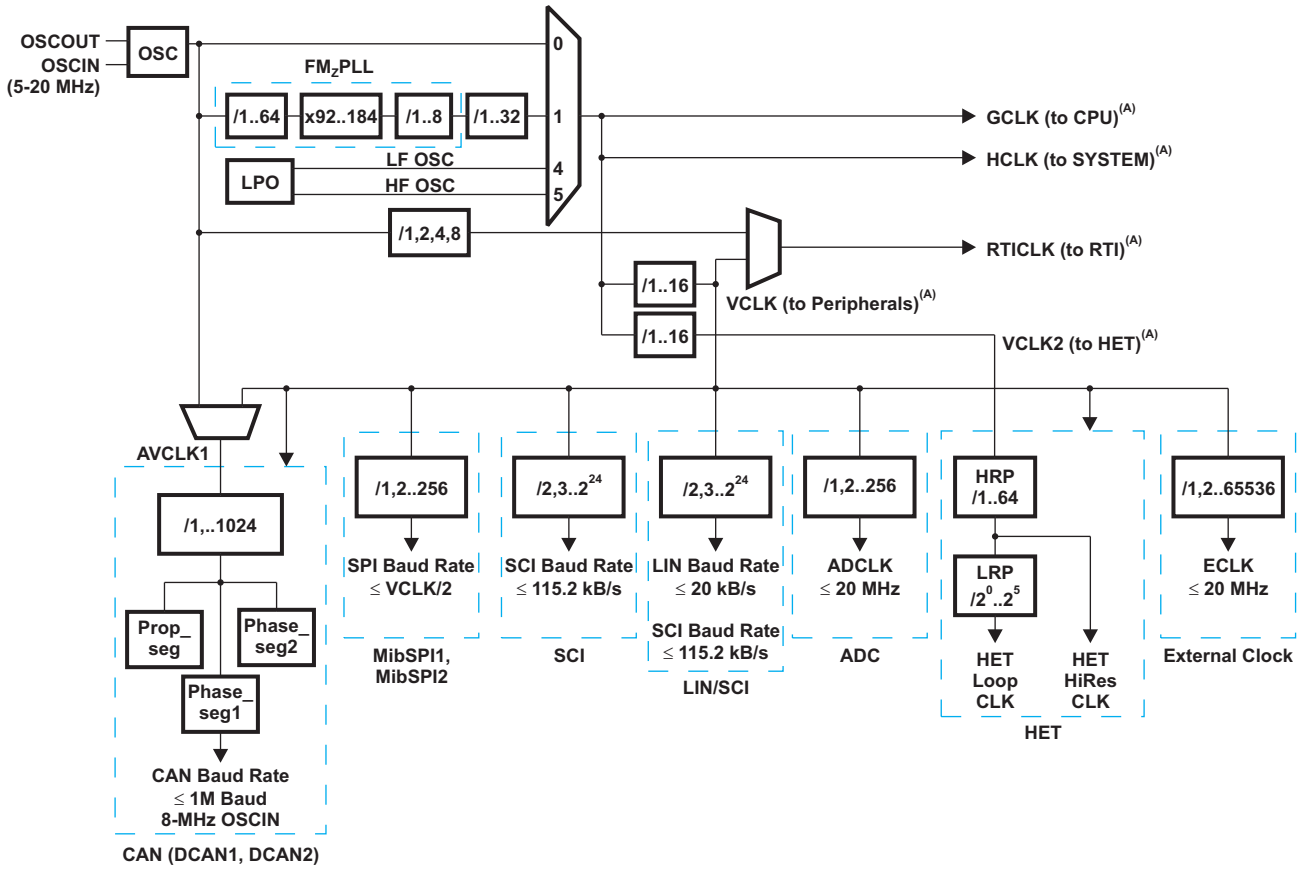


Figure 5-6. LPO and Clock Detection

5.2.4 Device Clock Domains Block Diagram

The clock domains block diagram and GCM clock source assignments are given in and Table 5-9.



A. See Table 5-10.

Figure 5-7. Device Clock Domains Block Diagram

Table 5-9. GCM Clock Source Assignments

GCM SOURCE NUMBER	CLOCK SOURCE
0	OSCIN
1	F035 FMzPLL
2	Reserved(1)
3	Reserved(1)
4	LF OSC
5	HF OSC
6	Reserved(1)
7	Reserved(1)

(1) 'Reserved' clock sources should not be enabled or used.

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Table 5-10. Switching Characteristics Over Recommended Operating Conditions for Clocks (1)(2)(3)(4)(5)

PARAMETER		TEST CONDITIONS (6)	MIN	MAX	UNIT
$f_{(HCLK)}$	System clock frequency	Pipeline mode enabled		80	MHz
		Pipeline mode disabled, 0 flash wait states		28	
$f_{(PROG/ERASE)}$	System clock frequency Flash programming/erase			80	MHz
$f_{(VCLK/VCLK2)}$	Peripheral VBUS clock frequency			$f_{(HCLK)}$	MHz
$f_{(ECLK)}$	External clock output frequency for ECP Module			20	MHz
$f_{(RCLK)}$	RCLK - Frequency out of PLL macro into R-divider			180	MHz
$t_{c(HCLK)}$	Cycle time, system clock	Pipeline mode enabled	12.50		ns
		Pipeline mode disabled, 0 flash wait states	35.71		
$t_{c(PROG/ERASE)}$	Cycle time, system clock - Flash programming/erase		12.50		ns
$t_{c(VCLK/VCLK2)}$	Cycle time, peripheral clock		$t_{c(HCLK)}$		ns
$t_{c(ECLK)}$	Cycle time, ECP module external clock output		50.0		ns
$t_{c(RCLK)}$	Cycle time, minimum input cycle time for the R- divider (RCLK)		5.56		ns

(1) $f_{(HCLK)} = f_{(OSC)}$ / NR *NF /ODPLL/PLLDIV; for details, see the PLL documentation. TI strongly recommends selection of NR and NF parameters such that NF ≤ 120 and ($f_{(OSC)}$ / NR *NF) ≤ 400.
$f_{(VCLK)} = f_{(HCLK)}$ / X, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the peripheral VBUS clock divider ratio determined by the VCLKR[3:0] bits in the SYS module.
(2) Enabling FM mode can reduce maximum rated operating frequencies. The degree of impact is application-specific and the specific settings, as well as the impact of the settings, should be discussed and agreed upon prior to using FM modes. Use of FM modes do not impact the maximum rated external clock output, $f_{(ECLK)}$, for the ECP module.
(3) Pipeline mode enabled or disabled is determined by FRDCNTL[2:0].
(4) $f_{(ECLK)} = f_{(VCLK)}$ / N, where N = {1 to 65536}. N is the ECP prescale value defined by the ECPCTRL.[15:0] register bits in the ECP module.
(5) ECLK output will increase radiated emissions within the system that is used. Rated emissions at the device level do not include emissions due to ECLK output.
(6) All test conditions assume FM Mode disabled and RAM ECC enabled with 0 waitstates for RAM.

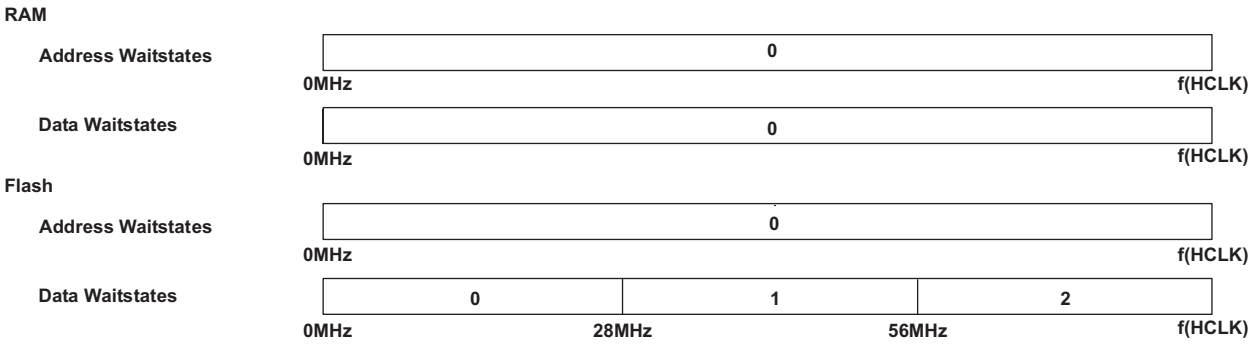


Figure 5-8. Timing - Wait States

NOTE

If FMzPLL frequency modulation is enabled, special care must be taken to ensure that the maximum system clock frequency f(HCLK) and peripheral clock frequency f(VCLK) are not exceeded. The speed of the device clocks may need be derated to accommodate the modulation depth when FMzPLL frequency modulation is enabled.

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5.2.4.1 ECLK Specification

Table 5-11. Switching Characteristics Over Recommended Operating Conditions for External Clocks(1)(2)

(see Figure 5-9)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
1	$t_{w(EOL)}$	Pulse duration, ECLK low	Under all prescale factor combinations (X and N)	$0.5t_{c(ECLK)} - t_f$		ns
2	$t_{w(EOH)}$	Pulse duration, ECLK high	Under all prescale factor combinations (X and N)	$0.5t_{c(ECLK)} - t_r$		ns

(1) X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the VBUS interface clock divider ratio determined by the CLKCNTL.[19:16] bits in the SYS module.
(2) N = {1 to 65536}. N is the ECP prescale value defined by the ECPCNTL.[15:0] register bits in the SYS module.

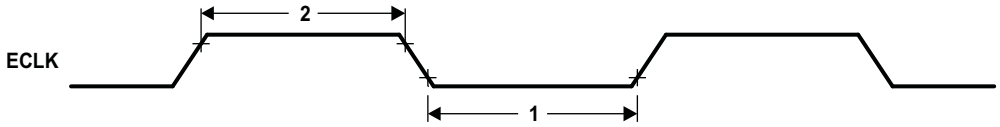


Figure 5-9. ECLK Timing Diagram

5.2.5 JTAG Timing

Table 5-12. JTAG Scan Interface Timing (JTAG Clock specification 10-MHz and 50-pF Load on TDO Output)

(see Figure 5-10

NO.			MIN	MAX	UNIT
1	$t_{c(JTAG)}$	Cycle time, JTAG low and high period	50		ns
2	$t_{su(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	5		ns
3	$t_{h(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	5		ns
4	$t_{h(TCKf -TDO)}$	Hold time, TDO after TCKf	5		ns
5	$t_{d(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)		45	ns

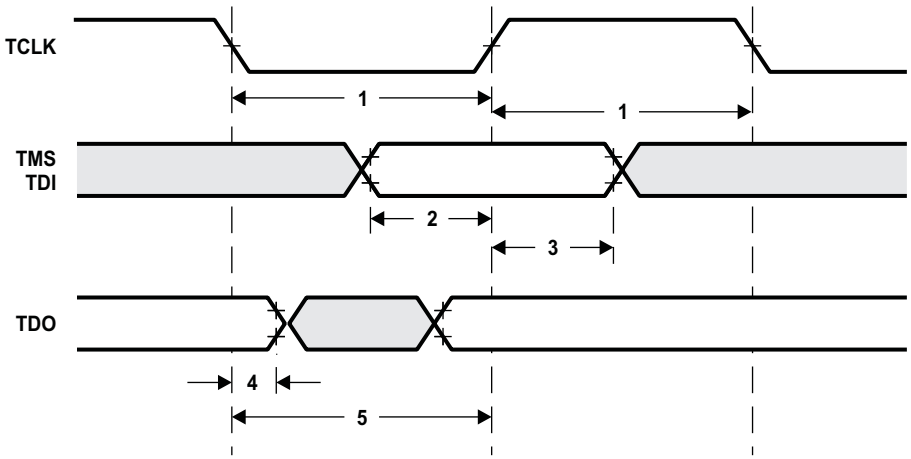


Figure 5-10. JTAG Scan Timings

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5.2.6 Output Timings

Table 5-13. Switching Characteristics for Output Timings Versus Load Capacitance (C_L)(1)

(see Figure 5-11)

PARAMETER			MAX	UNIT
t_r	Adaptive impedance 4 mA pins	C_L = 15 pF	4	ns
		C_L = 50 pF	8	
		C_L = 100 pF	15	
		C_L = 150 pF	21	
t_f	Adaptive impedance 4 mA pins	C_L = 15 pF	5	ns
		C_L = 50 pF	8	
		C_L = 100 pF	12	
		C_L = 150 pF	17	

(1) Peripheral output timings given within this document are measured in either standard buffer or impedance control mode.

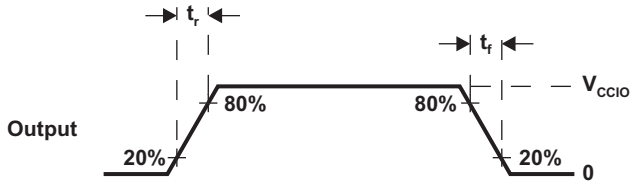


Figure 5-11. CMOS-Level Outputs

5.2.7 Input Timings

Table 5-14. Timing Requirements for Input Timings(1)

(see Figure 5-12)

		MIN	MAX	UNIT
t_{pw}	Input minimum pulse width	$t_{c(VCLK)}$ + 10		ns

(1) $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = 1 / $f_{(VCLK)}$.

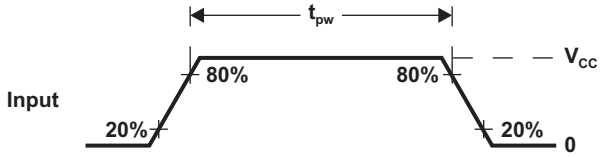


Figure 5-12. CMOS-Level Inputs

5.2.8 Flash Timings

Table 5-15. Timing Requirements for Program Flash

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{acc_delay}	Flash pump stabilization time	From Sleep Mode to Standby Mode	20			µs
		From Standby Mode to Active Mode	1			
	Flash bank stabilization time	From Sleep Mode to Standby Mode	1.9			
		From Standby Mode to Active Mode	0.1			
$t_{prog(16\text{-}bit)}$	Half-word (16-bit) programming time			37.5	300	µs
$t_{prog(Total)}$	512k-byte programming time(1)			10	78.7	s
	640-k-byte programming time(1)			12.5	98.4	
$t_{erase(sector)}$	Sector erase time			1.5	15	s
N_{wec}	Write/erase cycles at TA = -40 to125°C with 15-year Data Retention requirement				1000(2)	cycles
	Write/erase cycles at TA = -40 to 125°C EEPROM emulation requirement for 16k flash sectors in Bank 1				25000(2)(3)	cycles

(1) $t_{prog(Total)}$ programming time includes overhead of state machine, but does not include data transfer time.
(2) Flash write/erase cycles and data retention specifications are based on a validated implementation of the TI flash API. Non-TI flash API implementation is not supported. For detailed description see the *F035 Flash Validation Procedure (SPNA127)*.
(3) Flash write/erase cycle and data retention specifications are based on an assumed distribution of write/erase cycles over the life of the product including and even distribution over the rated temperature range and time between cycles. The EEPROM emulation bank has been qualified as outlined in the JEDEC specification JESD22-A117C.

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5.3 SPIn Master Mode Timing Parameters

Table 5-16. SPIn Master Mode External Timing Parameters (CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3)

(see Figure 5-13 and Figure 5-14)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)	90	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{d(SIMO-SPCL)M}$	Delay time, SPISIMO data valid before SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - 15$		
	$t_{d(SIMO-SPCH)M}$	Delay time, SPISIMO data valid before SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - 15$		
5(5)	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid (clock polarity = 0)	$0.5t_{c(SPC)M} - t_{f(SPC)}$		
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid (clock polarity = 1)	$0.5t_{c(SPC)M} - t_{r(SPC)}$		
6(5)	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	4		
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	4		
7(5)	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 0)	8		
	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 1)	8		
8(5)(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPICLK)}-6$	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPICLK)}+38$	
		Setup time CS active until SPICLK low (clock polarity = 1)	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPICLK)}-6$	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPICLK)}+38$	
9(5)(6)	$t_{T2CDELAY}$	Hold time SPICLK low until CS inactive (clock polarity = 0)	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPICLK)} + t_{r(SPICS)}-28$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPICLK)} + t_{r(SPICS)}+8$	
		Hold time SPICLK high until CS inactive (clock polarity = 1)	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPICLK)} + t_{r(SPICS)}-28$	$0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPICLK)} + t_{r(SPICS)}+8$	
10(6)	t_{SPIENA}	SPIENAn sample point	$C2TDELAY * t_{c(VCLK)} - t_{f(SPICS)}$	$C2TDELAY *t_{c(VCLK)}$	ns

(1) The MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is clear.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$.
(3) For rise and fall timings, see Table 5-13.
(4) When the SPI is in Master mode, the following must be true:
- For PS values from 1 to 255: t ≥ (PS +1)$t_{c(VCLK)}$ ≥ 90 ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
- For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)}$ ≥ 90 ns.

(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY are programmed in the SPIDELAY register.

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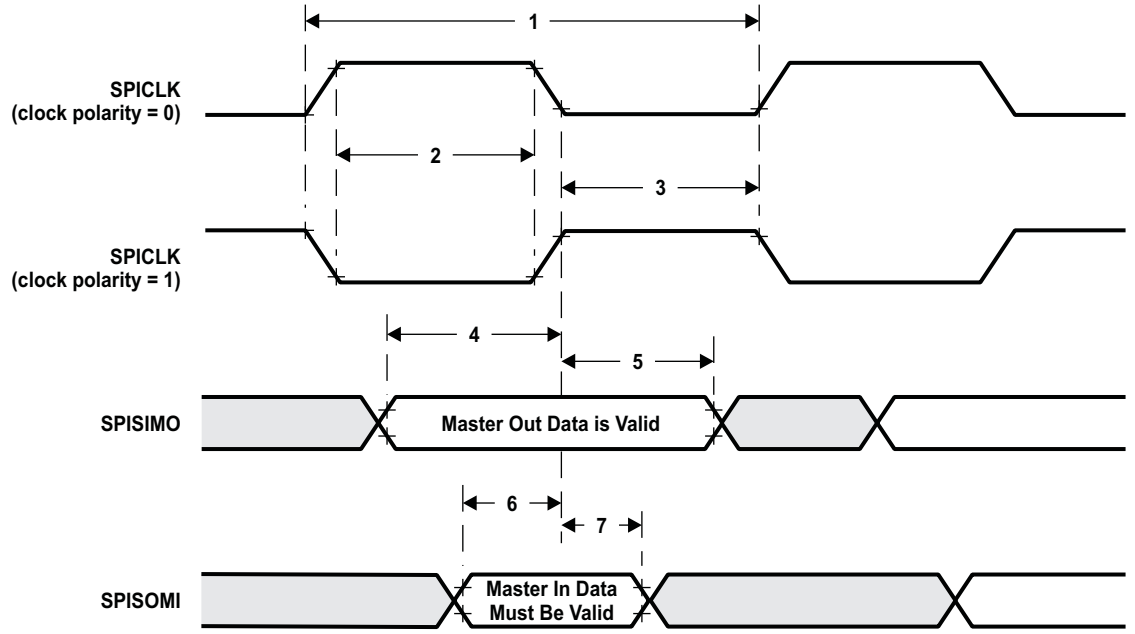


Figure 5-13. SPI Master Mode External Timing (CLOCK PHASE = 0)

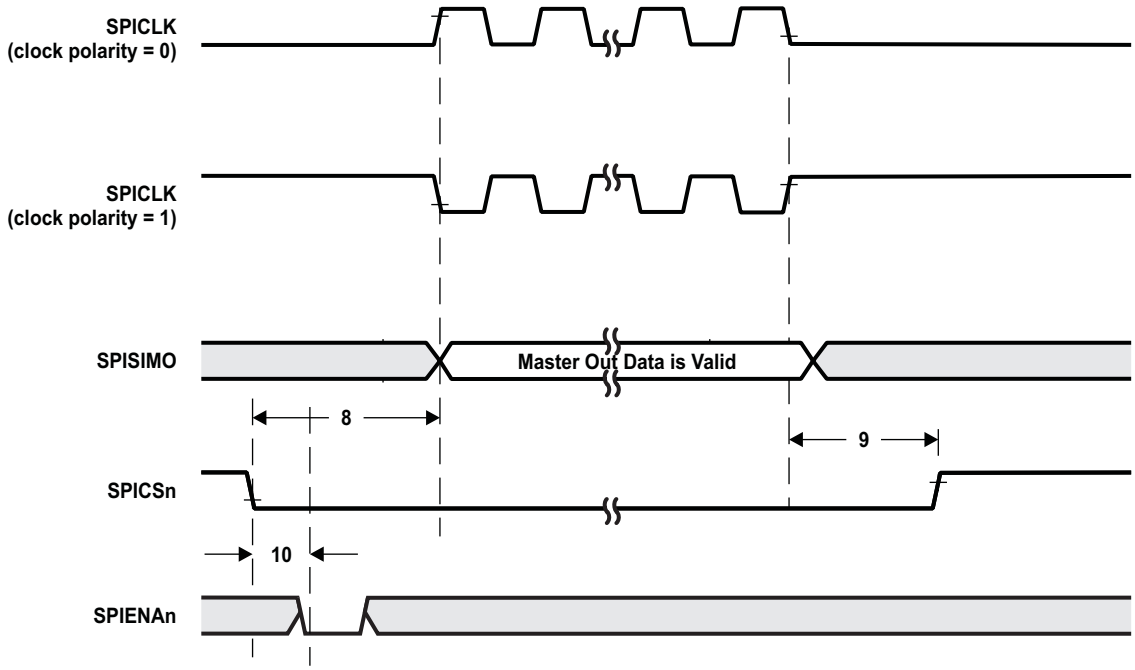


Figure 5-14. SPI Master Mode Chip Select Timing (CLOCK PHASE = 0)

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Table 5-17. SPIn Master Mode External Timing Parameters (CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3)

(see Figure 5-15 and Figure 5-16)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle time, SPICLK(4)	90	$256t_{c(VCLK)}$	ns
2(5)	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
3(5)	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M} - t_f$	$0.5t_{c(SPC)M} + 5$	
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M} - t_r$	$0.5t_{c(SPC)M} + 5$	
4(5)	$t_{d(SIMO-SPCH)M}$	Delay time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - 15$		
	$t_{d(SIMO-SPCL)M}$	Delay time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - 15$		
5(5)	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M} - t_{r(SPC)}$		
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M} - t_{f(SPC)}$		
6(5)	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	4		
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	4		
7(5)	$t_{h(SPCH-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK high (clock polarity = 0)	8		
	$t_{h(SPCL-SOMI)M}$	Hold time, SPISOMI data valid after SPICLK low (clock polarity = 1)	8		
8(5)(6)	$t_{C2TDELAY}$	Setup time CS active until SPICLK high (clock polarity = 0)	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)}+0.5*t_{c(SPC)M} - t_{f(SPICS)} + t_{r(SPICLK)}-6$	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)}+0.5*t_{c(SPC)M} - t_{f(SPICS)} + t_{f(SPICLK)}+38$	
		Setup time CS active until SPICLK low (clock polarity = 1)	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)}+0.5*t_{c(SPC)M} - t_{f(SPICS)} + t_{f(SPICLK)}-6$	$(C2TDELAY+CSHOLD+2)*t_{c(VCLK)}+0.5*t_{c(SPC)M} - t_{f(SPICS)} + t_{f(SPICLK)}+38$	
9(5)(6)	$t_{T2CDELAY}$	Hold time SPICLK low until CS inactive (clock polarity = 0)	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPICLK)} + t_{r(SPICS)}-28$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPICLK)} + t_{r(SPICS)}+8$	
		Hold time SPICLK high until CS inactive (clock polarity = 1)	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPICLK)} + t_{r(SPICS)}-28$	$T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPICLK)} + t_{r(SPICS)}+8$	
10(7)	t_{SPIENA}	SPIENAn Sample Point	$C2TDELAY * t_{c(VCLK)} - t_{f(SPICS)}$	$C2TDELAY * t_{c(VCLK)}$	ns

(1) he MASTER bit (SPIGCR1.0) is set and the CLOCK PHASE bit (SPIFMTx.16) is clear.
(2) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$.
(3) For rise and fall timings, see Table 5-13.
(4) When the SPI is in Master mode, the following must be true:
- For PS values from 1 to 255: $t_{c(SPC)M} \geq (PS+1)t_{c(VCLK)} \geq 90$ ns, where PS is the prescale value set in the SPIFMTx.[15:8] register bits.
- For PS values of 0: $t_{c(SPC)M} = 2t_{c(VCLK)} \geq 90$ ns.

(5) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).
(6) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register.
(7) C2TDELAY and T2CDELAY is programmed in the SPIDELAY register.

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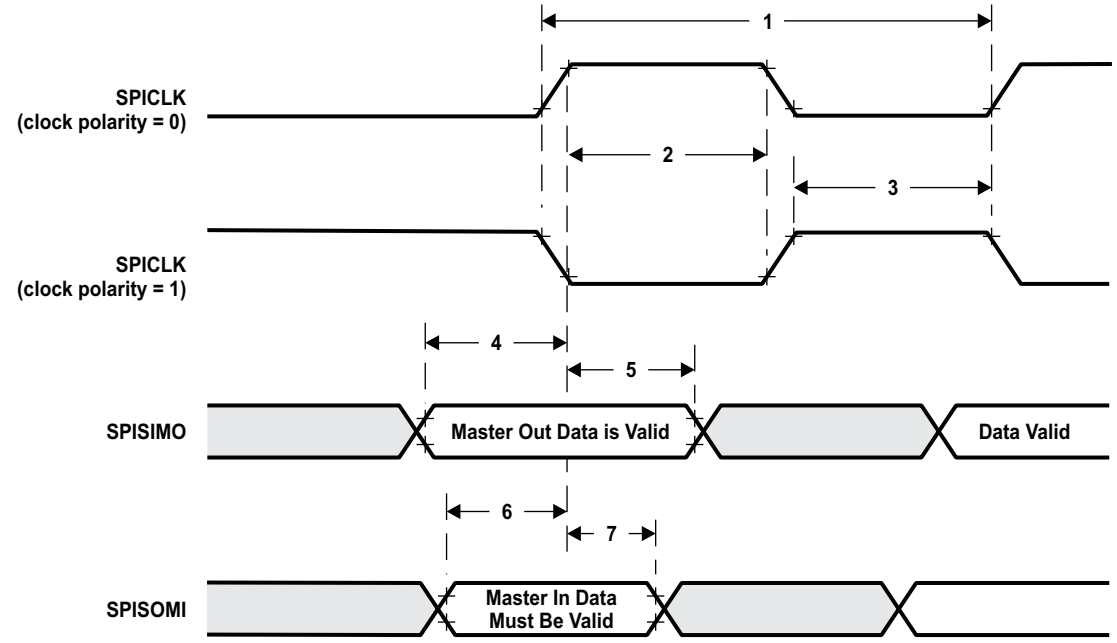


Figure 5-15. SPI Master Mode External Timing (CLOCK PHASE = 1)

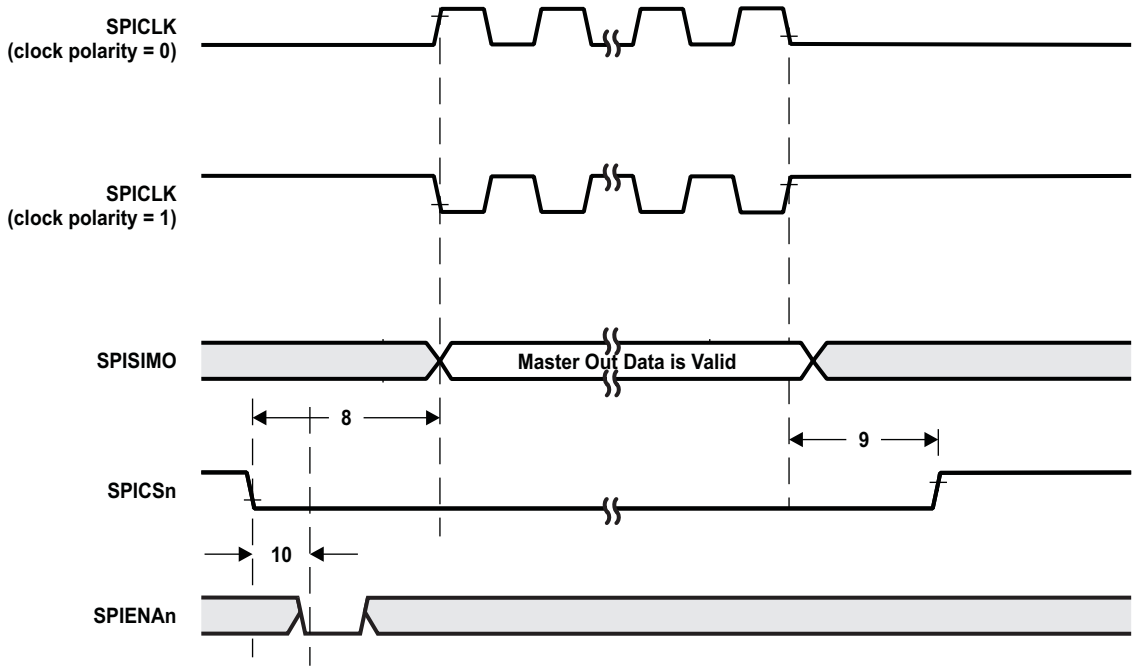


Figure 5-16. SPI Master Mode Chip Select timing (CLOCK PHASE = 1)

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5.4 SPIn Slave Mode Timing Parameters

Table 5-18. SPIn Slave Mode External Timing Parameters (CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4)

(see Figure 5-17 and Figure 5-18)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	90		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	30		
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	30		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	30		
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	30		
4(6)	$t_{d(SPCH-SOMI)S}$	Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0)		$t_{rf(SOMI)}$+15	
	$t_{d(SPCL-SOMI)S}$	Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1)		$t_{rf(SOMI)}$+15	
5(6)	$t_{v(SPCH-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)	0		
	$t_{v(SPCL-SOMI)S}$	Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)	0		
6(6)	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 0)	4		
	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 1)	4		
7(6)	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0)	6		
	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1)	6		
8	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ $t_{r(ENAn)}$	ns
	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ $t_{r(ENAn)}$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)		$t_{f(ENAn)}$+6	ns

(1) The MASTER bit (SPIGCR1.0) is clear and the CLOCK PHASE bit (SPIFMTx.16) is clear.
(2) When the SPI is in Slave mode, the following must be true: $t_{c(SPC)S} > 2t_{c(VCLK)}$ and $t_{c(SPC)S} \geq 90$ ns.
(3) For rise and fall timings, see Table 5-13.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 / $f_{(VCLK)}$.
(5) When the SPI is in Slave mode, the following must be true: $t_{w(SPCL)S} > t_{c(VCLK)}$, $t_{w(SPCL)S} \geq 30$, $t_{w(SPCH)S} > t_{c(VCLK)}$ ns and $t_{w(SPCH)S} \geq 30$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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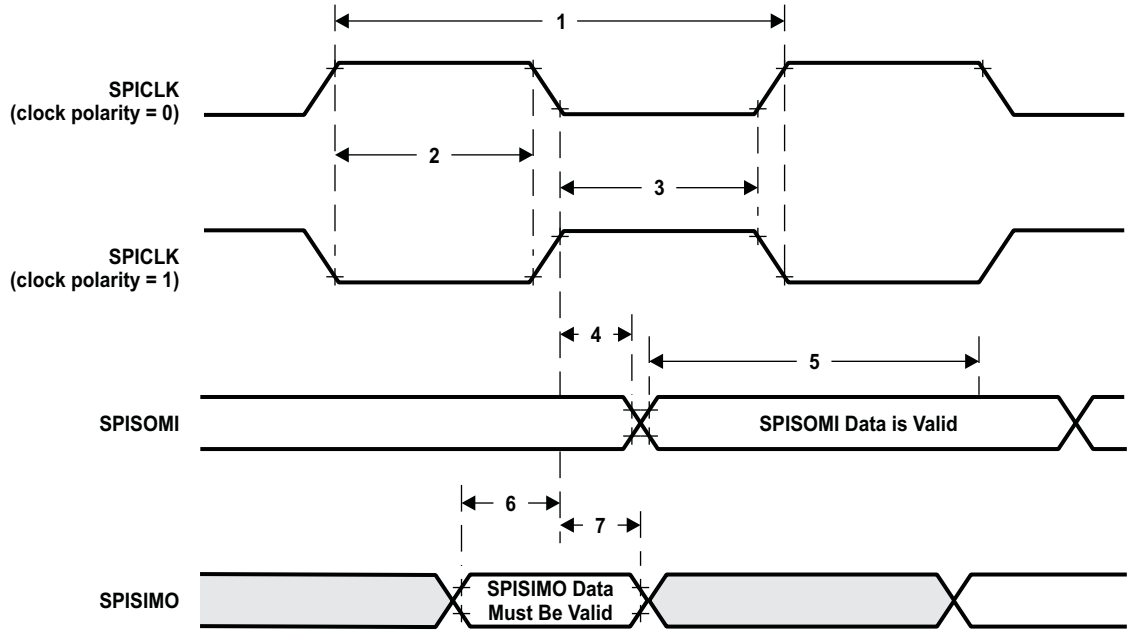


Figure 5-17. SPI Slave Mode External Timing (CLOCK PHASE = 0)

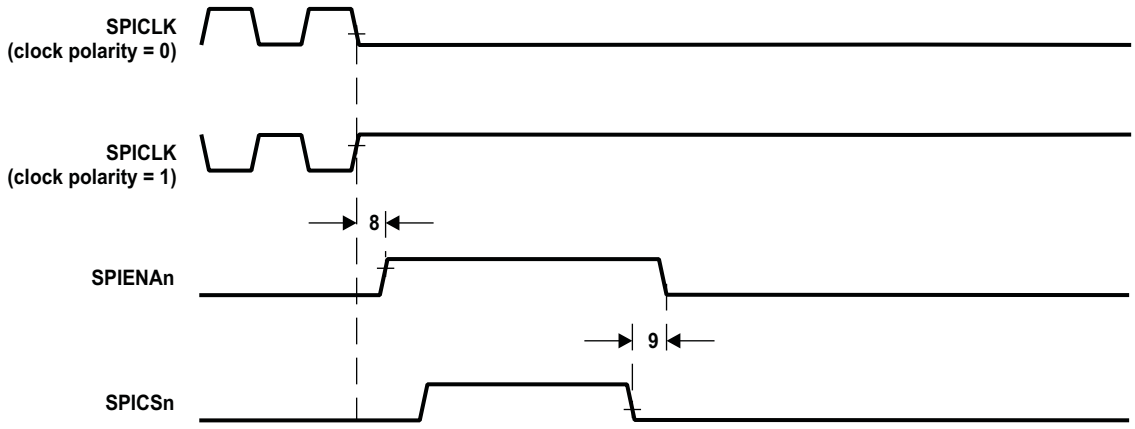


Figure 5-18. SPI Slave Mode Enable Timing (CLOCK PHASE = 0)

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Table 5-19. SPIn Slave Mode External Timing Parameters (CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4)

(see Figure 5-19 and Figure 5-20)

NO.			MIN	MAX	UNIT
1	$t_{c(SPC)S}$	Cycle time, SPInCLK(5)	90		ns
2(6)	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 0)	30		
	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 1)	30		
3(6)	$t_{w(SPCL)S}$	Pulse duration, SPInCLK low (clock polarity = 0)	30		
	$t_{w(SPCH)S}$	Pulse duration, SPInCLK high (clock polarity = 1)	30		
4(6)	$t_{v(SPCH-SOMI)S}$	Delay time, SPInSOMI data valid after SPInCLK high (clock polarity = 0)		$t_{rf(SOMI)}$+15	
	$t_{v(SPCL-SOMI)S}$	Delay time, SPInSOMI data valid after SPInCLK low (clock polarity = 1)		$t_{rf(SOMI)}$+15	
5(6)	$t_{v(SOMI-SPCH)S}$	Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0)	0		
	$t_{v(SOMI-SPCL)S}$	Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1)	0		
6(6)	$t_{su(SIMO-SPCH)S}$	Setup time, SPInSIMO before SPInCLK high (clock polarity = 0)	4		
	$t_{su(SIMO-SPCL)S}$	Setup time, SPInSIMO before SPInCLK low (clock polarity = 1)	4		
7(6)	$t_{v(SPCH-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0)	6		
	$t_{v(SPCL-SIMO)S}$	Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1)	6		
8	$t_{d(SPCH-SENAH)S}$	Delay time, SPIENAn high after last SPICLK high (clock polarity = 0)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ tr(ENAn)	ns
	$t_{d(SPCL-SENAH)S}$	Delay time, SPIENAn high after last SPICLK low (clock polarity = 1)	$1.5t_{c(VCLK)}$	$2.5t_{c(VCLK)}$+ $t_{r(ENAn)}$	
9	$t_{d(SCSL-SENAL)S}$	Delay time, SPIENAn low after SPICSn low (if new data has been written to the SPI buffer)		$t_{f(ENAn)}$+6	ns
10	$t_{d(SCSL-SOMI)S}$	Delay time, SOMI valid after SPICSn low (if new data has been written to the SPI buffer)		$t_{rf(SOMI)}$+6	ns

(1) The MASTER bit (SPInCTRL2.3) is cleared and the CLOCK PHASE bit (SPInCTRL2.0) is set.
(2) When the SPI is in Slave mode, the following must be true: $t_{c(SPC)S} > 2t_{c(VCLK)}$ and $t_{c(SPC)S} \geq 90$ ns.
(3) For rise and fall timings, see Table 5-13.
(4) $t_{c(VCLK)}$ = interface clock cycle time = 1 /f(VCLK).
(5) When the SPI is in Slave mode, the following must be true: $t_{w(SPCL)S} > t_{c(VCLK)}$, $t_{w(SPCL)S} \geq 30$ ns, $t_{w(SPCH)S} > t_{c(VCLK)}$ and $t_{w(SPCH)S} \geq 30$ ns.
(6) The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit (SPIFMTx.17).

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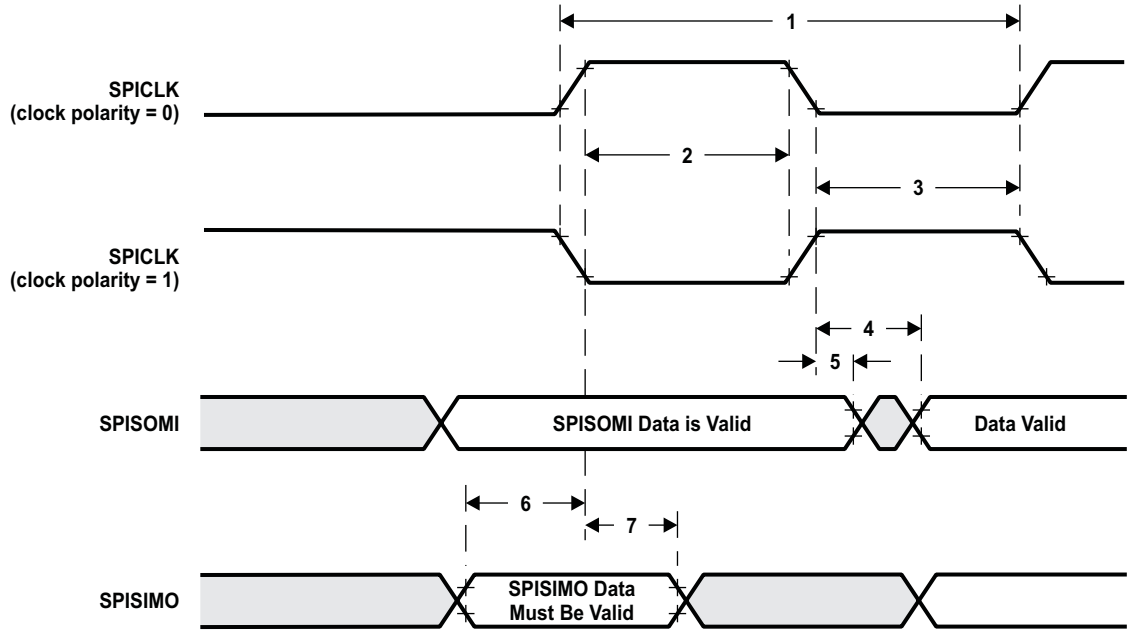


Figure 5-19. SPI Slave Mode External Timing (CLOCK PHASE = 1)

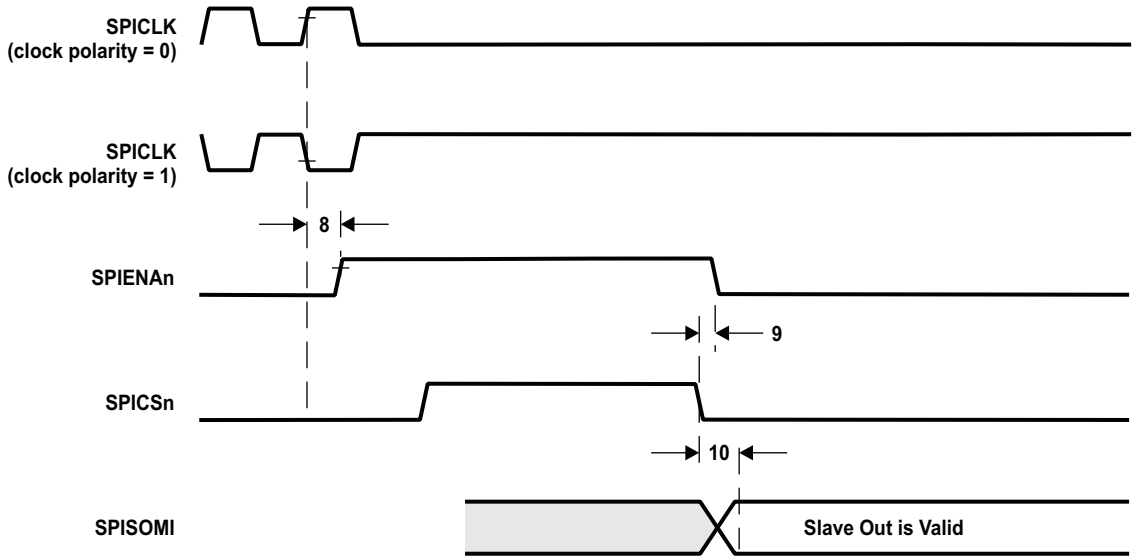


Figure 5-20. SPI Slave Mode Enable Timing (CLOCK PHASE = 1)

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5.5 CAN Controller (DCANn) Mode Timings

Table 5-20. Dynamic Characteristics for the CANnSTX and CANnSRX Pins

PARAMETER		MIN	MAX	UNIT
$t_{d(CANnSTX)}$	Delay time, transmit shift register to CANnSTX pin (1)		15	ns
$t_{d(CANnSRX)}$	Delay time, CANnSRX pin to receive shift register		6	ns

(1) These values do not include rise/fall times of the output buffer.

5.6 High-End Timer (HET) Timings

Table 5-21. Dynamic Characteristics for the HET Pins

PARAMETER		MIN	MAX	UNIT
$t_{opw}(HET)$	Output pulse width, this is the minimum pulse width that can be generated (1)	$1/f_{(VCLK2)}$		ns
$t_{ipw}(HET)$	Input pulse width, this is the minimum pulse width that can be captured (2)	$1/f_{(VCLK2)}$		ns

(1) $t_{opw}(HET)_{min} = HRP_{(min)} = hr_{(min)}$ / VCLK2.
(2) $t_{ipw}(HET) = LRP_{(min)} = hr_{(min)} * lr_{(min)}$ / VCLK2.

5.7 Multi-Buffered A-to-D Converter (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on VSS and VCC from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to ADREFLO unless otherwise noted.

Resolution	10 bits (1024 values)
Monotonic	Assured
Output conversion code	00h to 3FFh [00 for $V_{AI} \le AD_{REFLO}$; 3FF for $V_{AI} \ge A_{DREFHI}$]

Table 5-22. MibADC Recommended Operating Conditions(1)

		MIN	MAX	UNIT
AD_{REFHI}	A-to-D high -voltage reference source	3.0	V_{CCAD}	V
AD_{REFLO}	A-to-D low-voltage reference source	V_{SSAD}	0.3	V
V_{AI}	Analog input voltage	AD_{REFLO}	AD_{REFHI}	V
I_{AIC}	Analog input clamp current(2) ($V_{AI} < V_{SSAD}$ - 0.3 or $V_{AI} > V_{CCAD}$ + 0.3)	- 2	2	mA

(1) For V_{CCAD} and V_{SSAD} recommended operating conditions, see Section 4.2.
(2) Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

Table 5-23. MibADC Operating Characteristics Over Full Range of Recommended Operating Conditions(1)

PARAMETER		DESCRIPTION/CONDITIONS	MIN	NOM	MAX	UNIT
R_{mux}	Analog input mux on-resistance	See Figure 5-21		125	1.5K	Ω
R_{samp}	ADC sample switch on-resistance	See Figure 5-21		150	1.5K	Ω
C_{mux}	Input mux capacitance	See Figure 5-21			16	pF
C_{samp}	ADC sample capacitance	See Figure 5-21			8	pF
I_{AIL}	Analog input leakage current	Input leakage per ADC input pin	-200		200	nA
$I_{ADREFHI}$	AD_{REFHI} input current	AD_{REFHI} = 3.6 V, AD_{REFLO} = V_{SSAD}			5	mA
CR	Conversion range over which specified accuracy is maintained	ADREFHI - ADREFLO	3		3.6	V
E_{DNL}	Differential non-linearity error	Difference between the actual step width and the ideal value (see Figure 5-22).			± 2	LSB
E_{INL}	Integral non-linearity error	Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error (see Figure 5-23).			± 2	LSB
E_{TOT}	Total error/Absolute accuracy	Maximum value of the difference between an analog value and the ideal midstep value (see Figure 5-24).			± 2	LSB

(1) 1 - LSB = $(AD_{REFHI} – AD_{REFLO})/ 2^{10}$ for the MibADC.

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5.7.1 MibADC Input Model

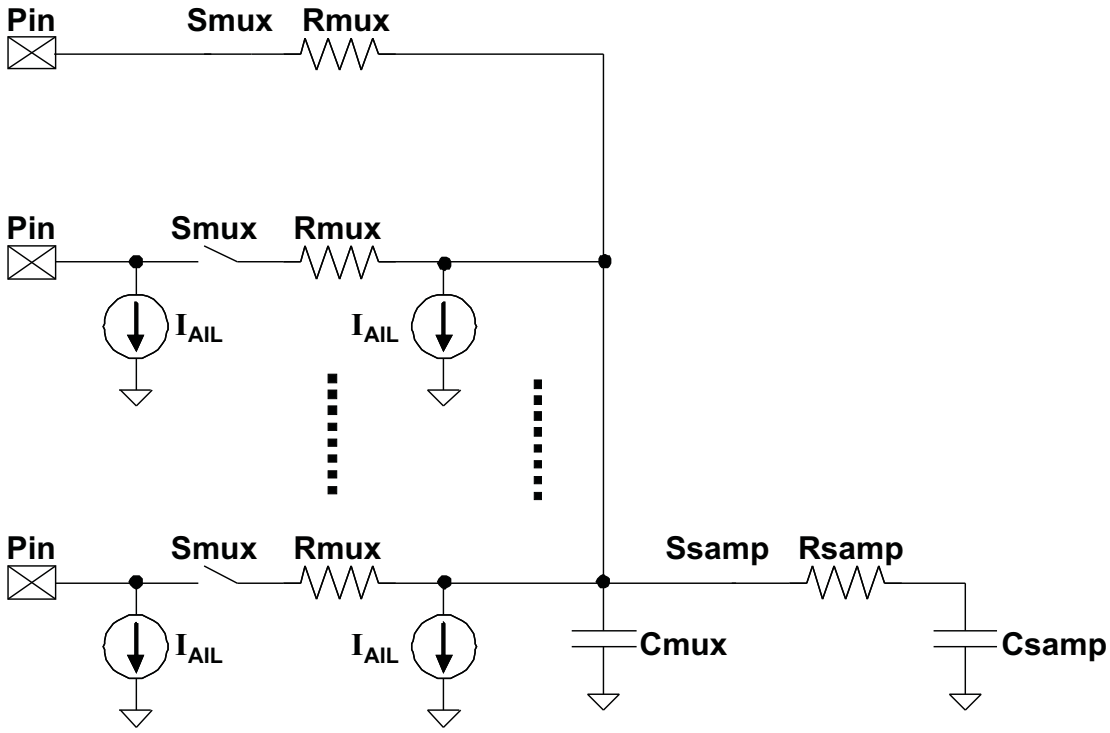


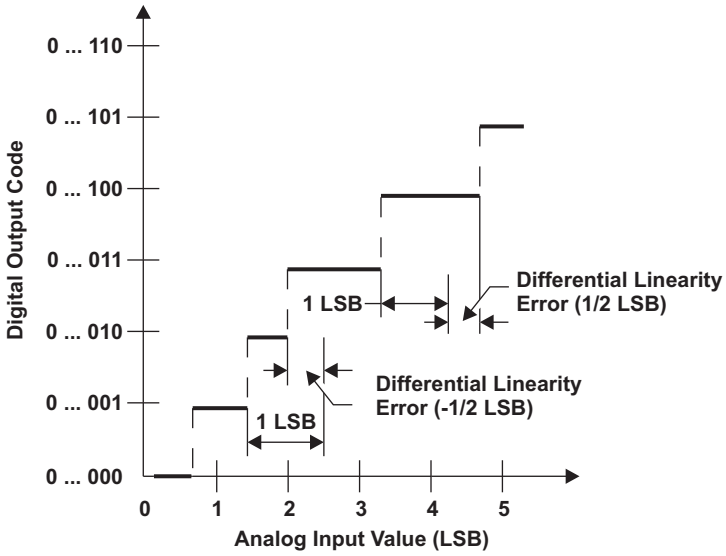
Figure 5-21. MibADC Input Equivalent Circuit

Table 5-24. Multi-Buffer ADC Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
$t_{c(ADCLK)}$	Cycle time, MibADC clock	0.05			µs
$t_{d(SH)}$	Delay time, sample and hold time	1			µs
$t_{d(C)}$	Delay time, conversion time	0.55			µs
$t_{d(SHC)}$ (1)	Delay time, total sample/hold and conversion time	1.55			µs

(1) This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors.

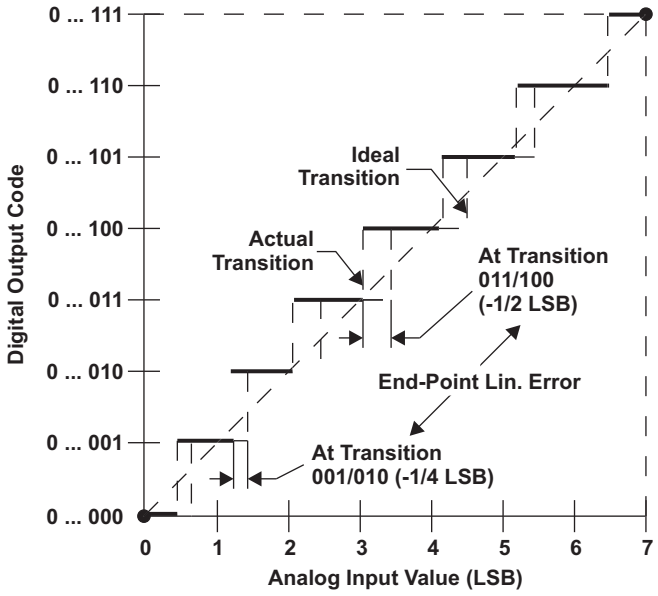
The differential non-linearity error shown in Figure 5-22 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.



A. 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 5-22. Differential Non-linearity (DNL)

The integral non-linearity error shown in Figure 5-23 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

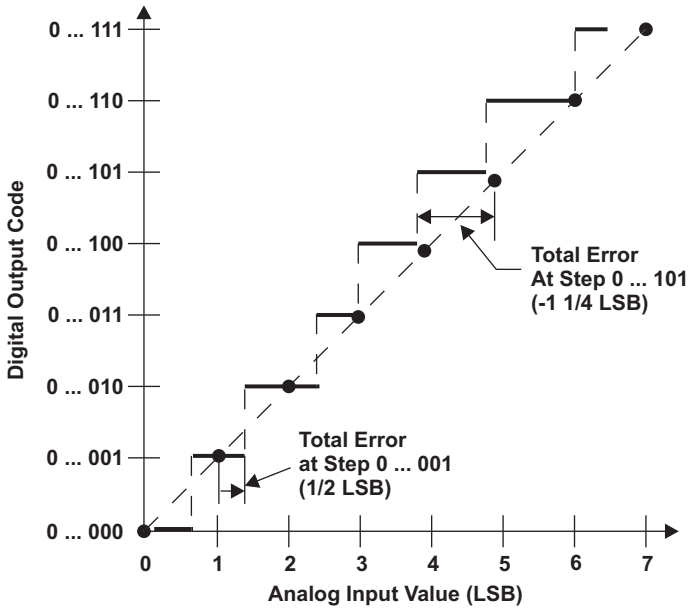


A. 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

Figure 5-23. Integral Non-linearity (INL) Error

The absolute accuracy or total error of an MibADC as shown in Figure 5-24 is the maximum value of the difference between an analog value and the ideal midstep value.

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A. 1 LSB = $(AD_{REFHI\mu} - AD_{REFLO})/2^{10}$

Figure 5-24. Absolute Accuracy (Total) Error

6 Revision History

This data sheet revision history highlights the technical changes made to the device or the datasheet.

Date	Additions, Deletions, And Modifications	Revision
October 2010	Updated the MibADC Input Equivalent Circuit illustration. Renamed $f_{(PLLDIV)}$ to $f_{(RCLK)}$. Fixed the formulas in SPI timing, including item 4,5,8,9,10 in master mode, and item 1,2,3 and footnotes in slave mode. Removed slew rate control description, renamed low EMI buffer to adaptive impedance 4 mA buffer. Swapped DCAN1 and DCAN0 RAM Map. Removed VIH of PORRST pin from section 5.1 RST and PORRST timings. Changed the footnotes in the Electrical characterization section so that the VIH of general IO pins also applies to PORRST pin. Added a new section "Terms and Acronyms".	A
August 2011	Fixed the Device ID in . Added descriptions for the ENZ pin.	B
January 2012	Added maximum programming time specifications to Flash Timings table. Added note to clarify application use and qualification methodology of EEPROM emulation bank in Flash Timings table.	C

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7 Mechanical Data

7.1 Thermal Data

Table 7-1 show the thermal resistance characteristics for the PQFP - PZ mechanical packages.

Table 7-1. Thermal Resistance Characteristics (S-PQFP Package) [PZ]

PARAMETER	°C/W
$R_{\theta JA}$	48
$R_{\theta JC}$	5

7.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device. This data is subject to change without notice and without revision of this document.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
S4MF06607BSPZQQ1	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	S4MF06607BSPZ TMS470	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

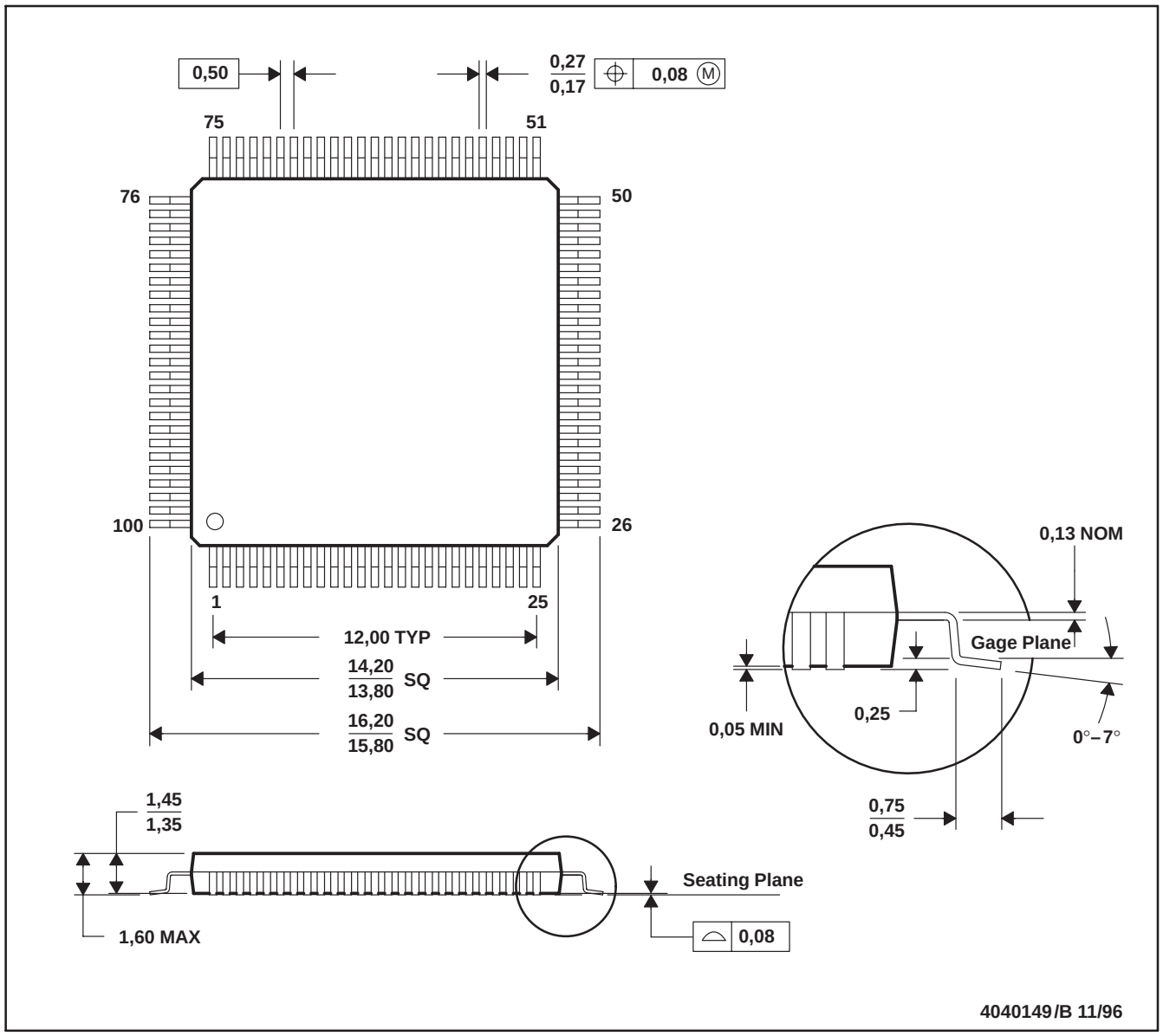
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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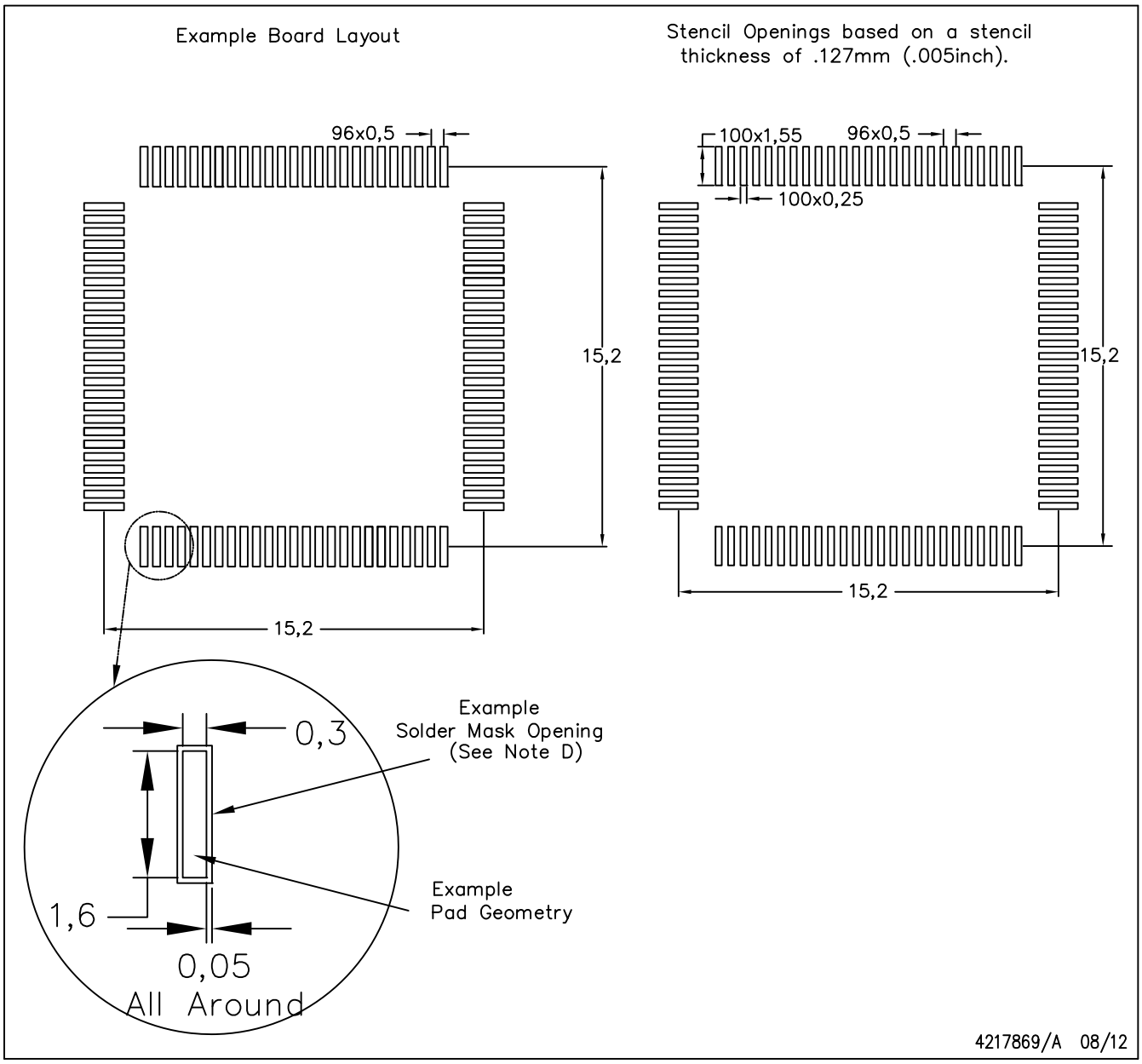
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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