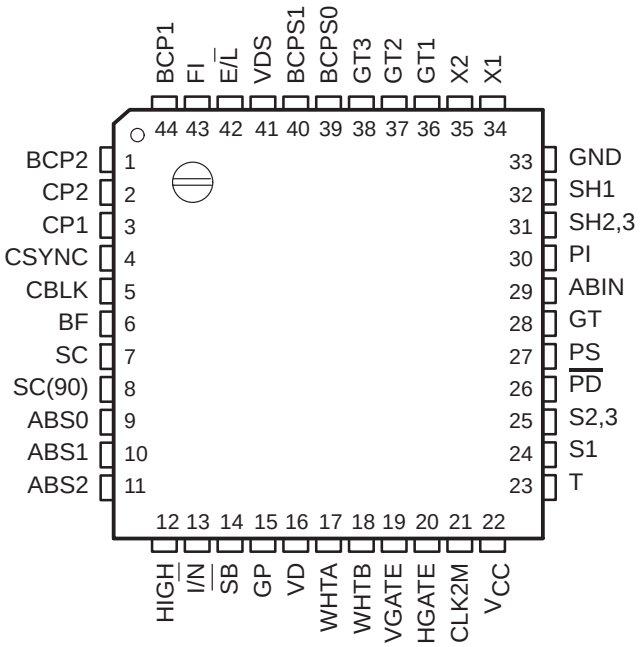
- **NTSC-Timing Operation**
- **Solid-State Reliability**
- **Monochrome Operation**
- **Eight Selectable-Antiblooming Modes**
- **Surface-Mount Package**
- **Clamp-Pulse Select Option**

FS PACKAGE
(TOP VIEW)



description

The TMS3471C is a monolithic integrated circuit designed to supply timing signals for the Texas Instruments (TI™) 11-mm diagonal TC241 monochrome CCD image sensor. The TMS3471C supplies both CCD drive signals and NTSC television synchronization signals at standard video rates. It requires a single 5-V supply voltage and a 14.318-MHz crystal-oscillator input. The TMS3471C provides several options, including multiple antiblooming modes, clamp-pulse selection, and delayed horizontal transfer.

The TMS3471C is used in conjunction with level-shifting devices such as the TI TMS3473B parallel driver and the TI TMS3472A serial driver. It also supplies sample-and-hold signals for the TI TL1593 three-channel sample-and-hold and multiplex signals for the TI TL1051 video preprocessor. The TMS3471C NTSC synchronization-signal outputs include composite sync, composite blank, clamp, subcarrier, subcarrier delayed by 90 degrees, and burst flag.

The TMS3471C is supplied in a 44-pin plastic flat package and is characterized for operation from –20°C to 45°C.

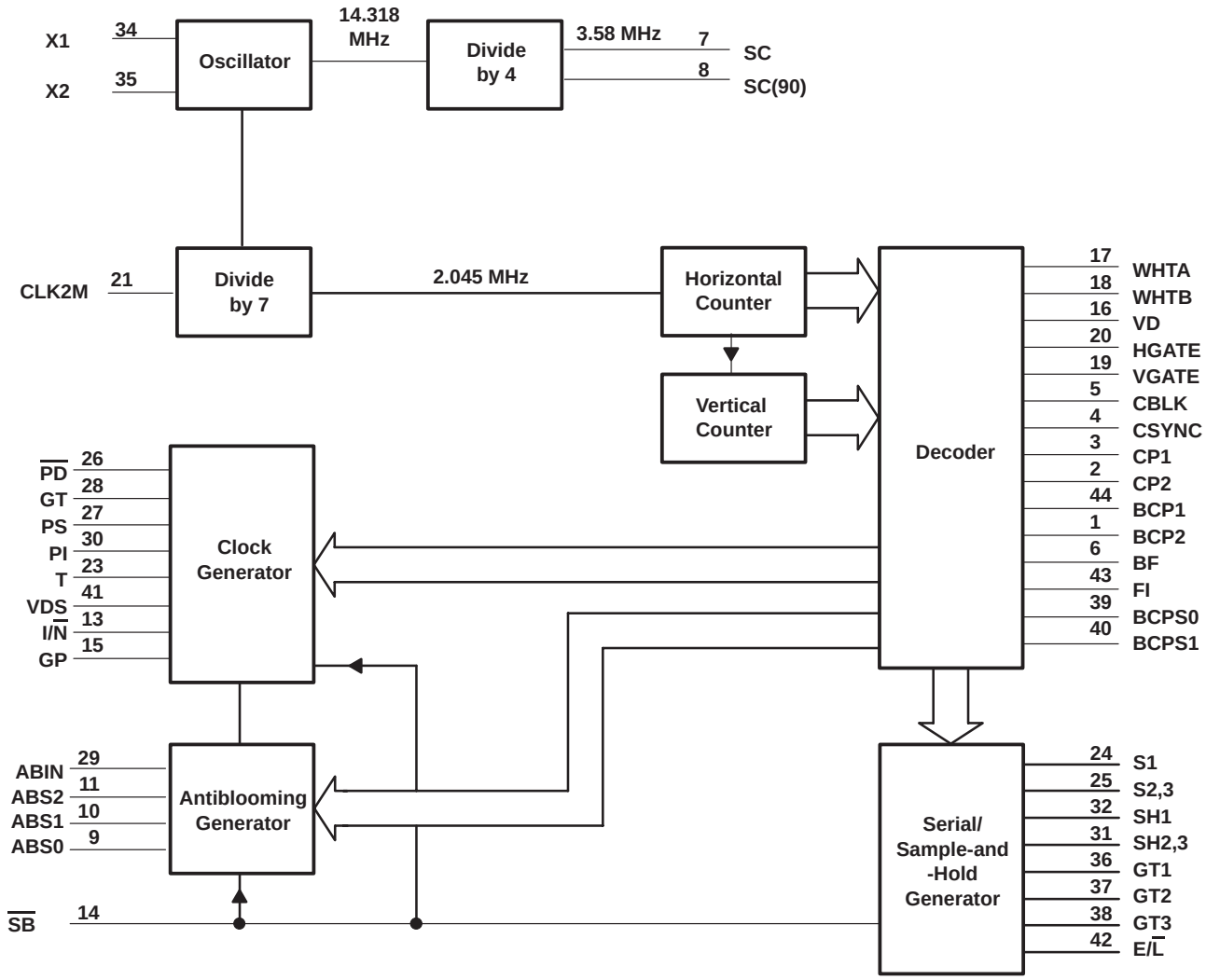
This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

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functional block diagram

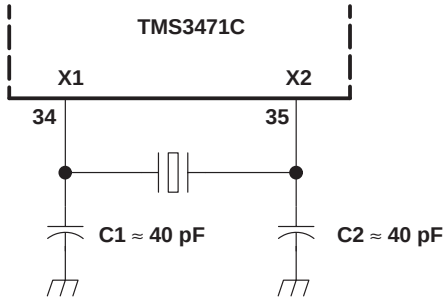


Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABIN	29	O	Antiblooming in. ABIN drives the ABG input of the TC240/TC241 CCD image sensors.
ABS0	9	I	The levels on these three terminals determine which of the eight antiblooming modes is selected: MODE ABS2 ABS1 ABS0 Operation 0 L L L No ABG pulses 1 L L H 250-kHz clocking during flyback only 2 L H L 1-MHz clocking during flyback only 3 L H H 2.2-MHz clocking during flyback only 4 H L L 250-kHz continuous clocking 5 H L H 500-kHz continuous clocking 6 H H L 1-MHz continuous clocking 7 H H H 2.2-MHz continuous clocking
ABS1	10	I	
ABS2	11	I	
BCP1	44	O	Optical black clamp pulse 1
BCP2	1	O	Optical black clamp pulse 2
BCPS0	39	I	The levels on BCPS0 and BCPS1 determine the placement and duration of the BCP1 and BCP2 pulses relative to the horizontal scan timing (see Figure 4 for the truth table for BCPS0 and BCPS1 and for the corresponding BCP1 and BCP2 pulse placements).
BCPS1	40	I	
BF	6	O	Burst flag
CBLK	5	O	Composite blank
CLK2M	21	O	2-MHz clock
CP1	3	O	Clamp
CP2	2	O	Clamp
CSYNC	4	O	Composite sync
E/$\overline{L}$	42	I	Delay select for S1 and S2,3. When E/$\overline{L}$ is high, the two serial-transfer pulses occur early relative to the sample-and-hold pulses SH1 and SH2,3. When E/$\overline{L}$ is low, the two serial-transfer pulses occur late relative to the sample-and-hold pulses.
FI	43	O	Field index
GND	33		Ground
GP	15	I	Exposure control: GP gates PS and PI
GT	28	O	TMS3473B parallel-driver MIDSEL input switch
GT1	36	O	Y gate 1
GT2	37	O	Y gate 2
GT3	38	O	Y gate 3
HGATE	20	O	Decoded H count signal. HGATE is a test point and is not used in normal operation.
HIGH	12	I	Not used (tie high)
I/$\overline{N}$	13	I	Interlace select. If high, interlace mode is selected; if low, noninterlace mode is selected.
$\overline{PD}$	26	O	Power down. A low-logic level on $\overline{PD}$ causes the device to enter a low power-consumption mode.
PI	30	O	Parallel-image-area gate clock
PS	27	O	Parallel-storage-area gate clock
$\overline{SB}$	14	I	Standby-mode select. When $\overline{SB}$ is high, normal operation is selected; when $\overline{SB}$ is low, the power-down mode is selected.
SC	7	O	Subcarrier (3.58 MHz)
SC(90)	8	O	Subcarrier phase shifted by 90 degrees
SH1	32	O	Sample-and-hold pulse 1
SH2,3	31	O	Sample-and-hold pulse 2, 3

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
S1	24	O	Serial clock 1
S2,3	25	O	Serial clock 2, 3
T	23	O	Transfer-gate clock
V_{CC}	22		DC power
VD	16	O	Vertical drive
VDS	41	I	Vertical-dump speed. When VDS is high, the vertical-dump frequency is 2 MHz; when VDS is low, the vertical-dump frequency is 1 MHz. VDS can also function as a timer reset by dropping the voltage on VDS from V_{CC} to $V_{CC}/2$ and then raising it back to V_{CC}.
VGATE	19	O	Decoded V count signal. VGATE is a test point and is not used in normal operation.
WHTA	17	O	WHTA is a test point and is not used in normal operation.
WHTB	18	O	WHTB is a test point and is not used in normal operation.
X1	34		Crystal oscillator (see Figure 1)
X2	35		



NOTE: The TMS3471C is designed for use with a crystal oscillator. The X1 and X2 terminals should not connect directly to external driver outputs.

Figure 1. Connection of an External Crystal Oscillator to the TMS3471C

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range, V_I . . . . . –0.3 V to V_{CC} + 0.3 V
Output voltage range, V_O . . . . . –0.3 V to V_{CC} + 0.3 V
Continuous total power dissipation: T_A = 25°C . . . . . 550 mW
T_A = 45°C . . . . . 440 mW
T_A = 75°C . . . . . 275 mW
Operating free-air temperature range, T_A . . . . . –20°C to 45°C
Storage temperature range . . . . . –55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 3 seconds . . . . . 350°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}				V
Low-level input voltage, V_{IL}			0.8	V
Operating frequency		14.31818		MHz
Power-up time		300		μs
Operating free-air temperature, T_A	–20		45	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{CC} = 5 V (unless otherwise noted)†

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$\lvert I_{OH} \rvert$ < 1 μA	4.95			V
V_{OL}	Low-level output voltage		$\lvert I_{OL} \rvert$ < 1 μA			0.05	V
I_{IH}‡	High-level input current		V_{CC} = 5 V	75			μA
			V_{CC} = 4.5 V	65			
I_{IL}	Low-level input current		V_{CC} = 5.5 V			225	μA
			V_{CC} = 5 V			200	
I_{OH}	High-level output current	S1, T, ABIN, PS, PI, GT	V_{OH} = 3.5 V			–0.1	mA
		S2,3, $\overline{PD}$				–0.2	
		SH1, GT1, GT2, GT3				–2.5	
		SH2,3				–5	
		BCP1, BCP2				–1	
		SC, SC(90)				–3	
		CP2				–0.6	
		CLK2M				–0.3	
		All other outputs	V_{OH} = 4.6 V			–0.5	
I_{OL}	Low-level output current	S1, T, ABIN, PS, PI, GT	V_{OL} = 0.4 V			0.1	mA
		S2,3, $\overline{PD}$				0.2	
		SH1, GT1, GT2, GT3				2.5	
		SH2,3				5	
		BCP1, BCP2				1	
		SC, SC(90)				0.3	
		CP2				0.6	
		CLK2M				0.3	
		All other outputs				0.5	
$I_{CC(AV)}$	Average supply current				40		mA
$I_{CC(S)}$	Standby supply current				15		mA

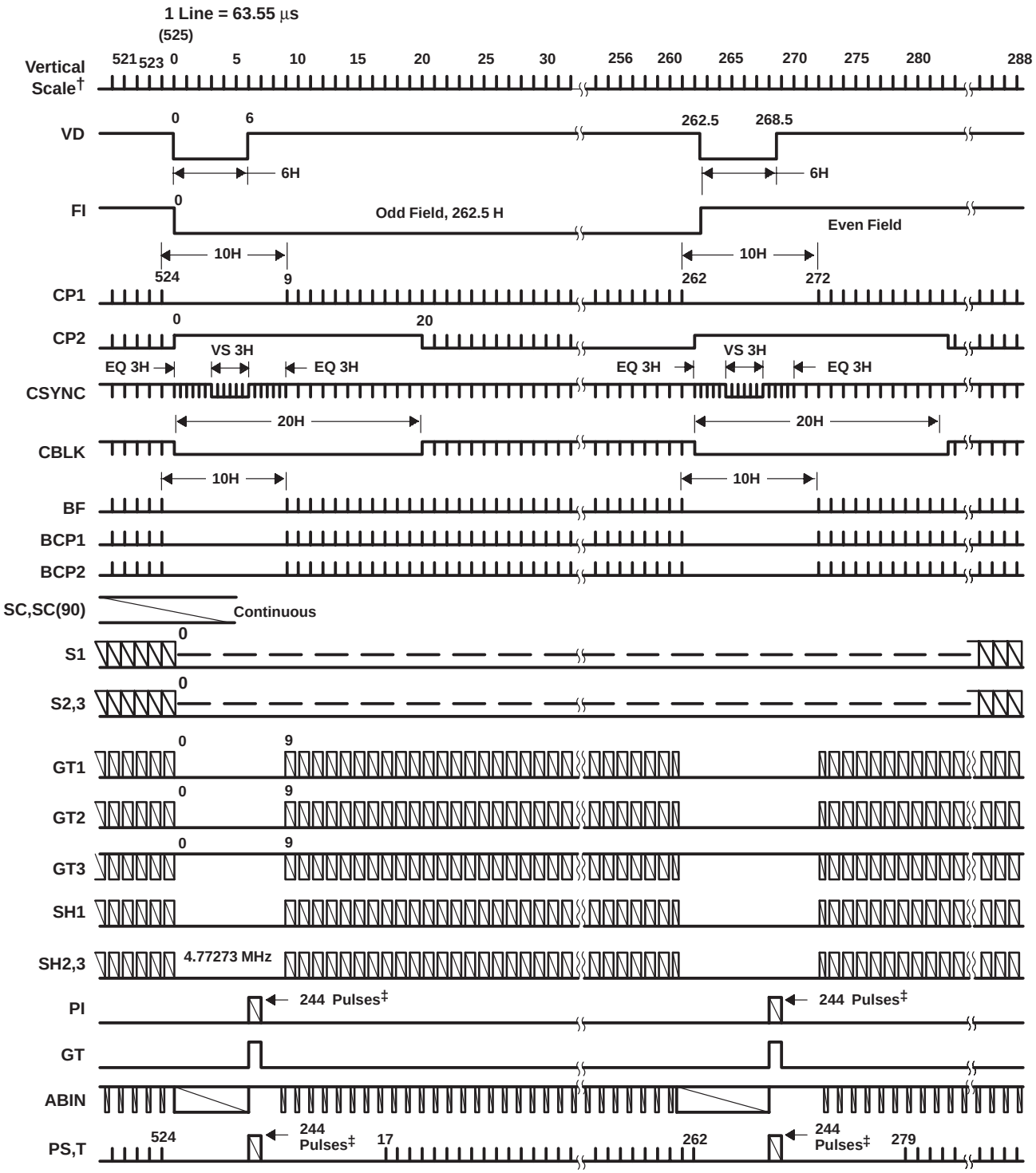
† The $\overline{SB}$ input is a Schmitt-trigger input with 0.5-V to 1-V hysteresis.
‡ All inputs have pullup-current sources.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	S1	C_L = 20 pF		10		ns
		S2,3	C_L = 40 pF		10		
		ABIN, GT, $\overline{PD}$, PI, PS, T	C_L = 20 pF		30		
		GT1, GT2, GT3, SH1			10		
		SH2,3	C_L = 40 pF		10		
		BCP1, BCP2	C_L = 50 pF		100		
		SC, SC(90)	C_L = 15 pF		30		
		CLK2M	C_L = 50 pF		50		
		All other outputs			200		
t_f	Fall time	S1	C_L = 20 pF		8		ns
		S2,3	C_L = 40 pF		8		
		ABIN, GT, $\overline{PD}$, PI, PS, T	C_L = 20 pF		30		
		GT1, GT2, GT3, SH1			8		
		SH2,3	C_L = 40 pF		8		
		BCP1, BCP2	C_L = 50 pF		100		
		SC, SC(90)	C_L = 15 pF		30		
		CLK2M	C_L = 50 pF		50		
		All other outputs			100		
$t_{sk(o)}$	Skew time	S1 rising edge to S2,3 rising edge				±5	ns
		S1 falling edge to SH1 falling edge		–3	–8	–13	
		S1 rising edge to GT1 falling edge		–3	–8	–13	
		SH2,3 rising edge to GT1 rising edge				±5	
		S2,3 falling edge to SH2,3 falling edge		–3	–8	–13	
		S2,3 falling edge to GT2 rising edge		–3	–8	–13	
		SH2,3 falling edge to GT2 rising edge				±5	
		SH2,3 rising edge to GT3 falling edge				±5	
$t_w - t_c/2$	Pulse duration compared to pulse duration at 50% duty cycle†	S1 or S2, 3				±5	ns

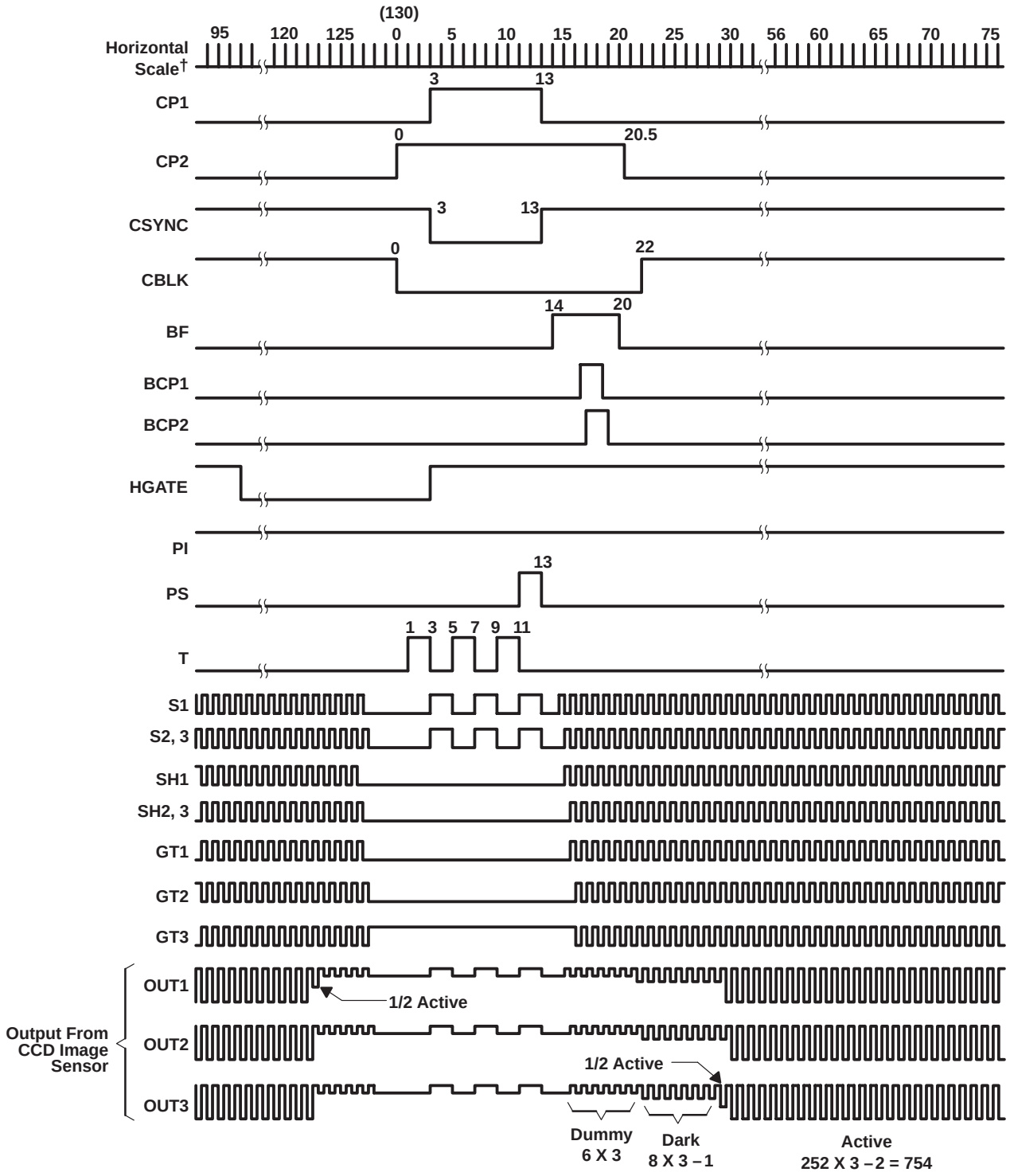
† The S1 and S2,3 outputs ideally exhibit a 50% duty cycle. This parameter indicates how much the duty cycle may shift while a constant cycle time is maintained. For example, for a 210-ns cycle time, $t_{w(H)}$ = 110 ns and $t_{w(L)}$ = 100 ns are possible.

PARAMETER MEASUREMENT INFORMATION



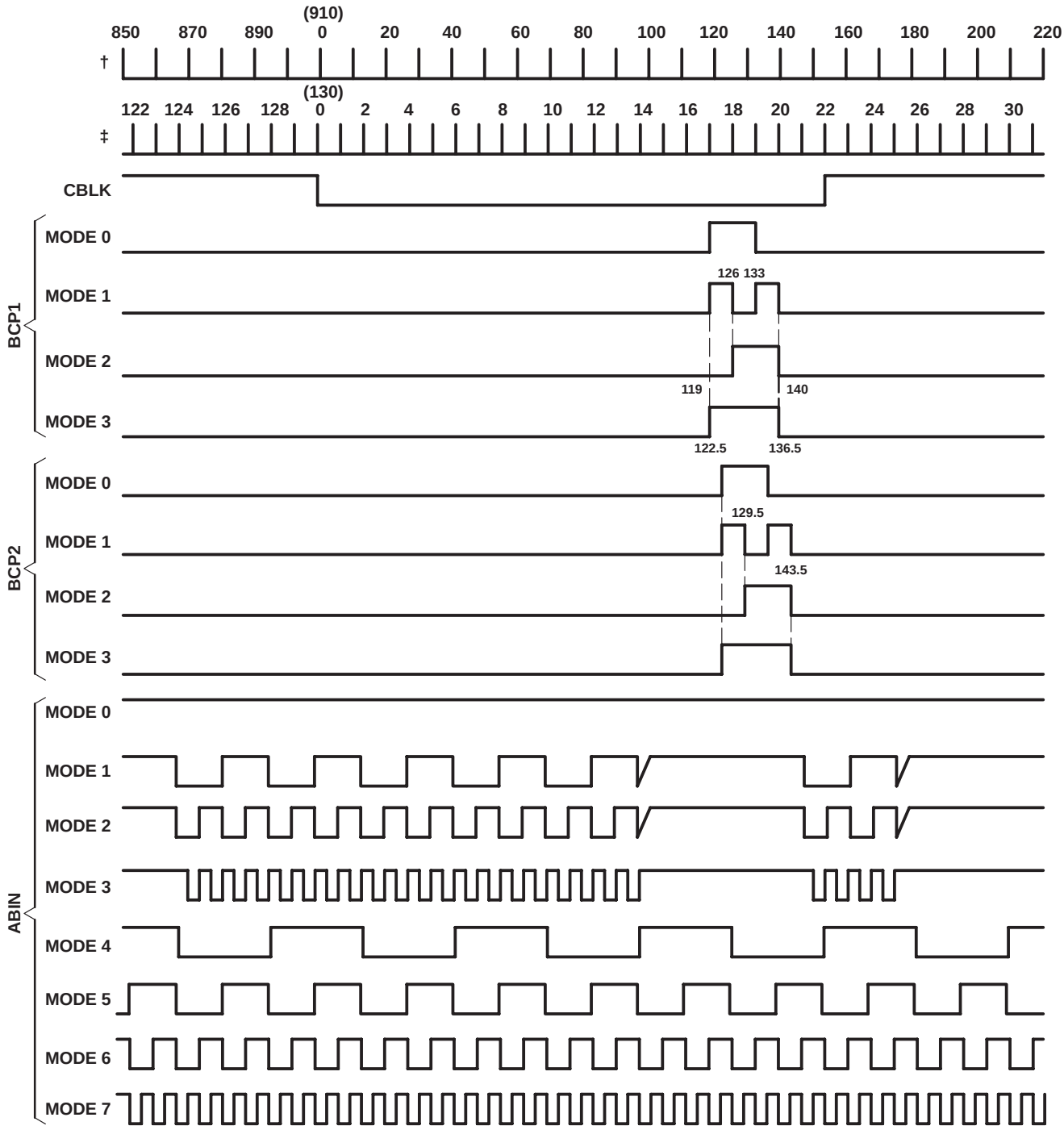
† 525 intervals equal 33.3 ms equals 1 TV frame
‡ The frequency of these pulses is either 2.04545 MHz or 1.02273 MHz and is determined by the logic level on the VDS input.

Figure 2. Vertical Timing



† 130 intervals equal 63.55 μs equals one horizontal-scan line

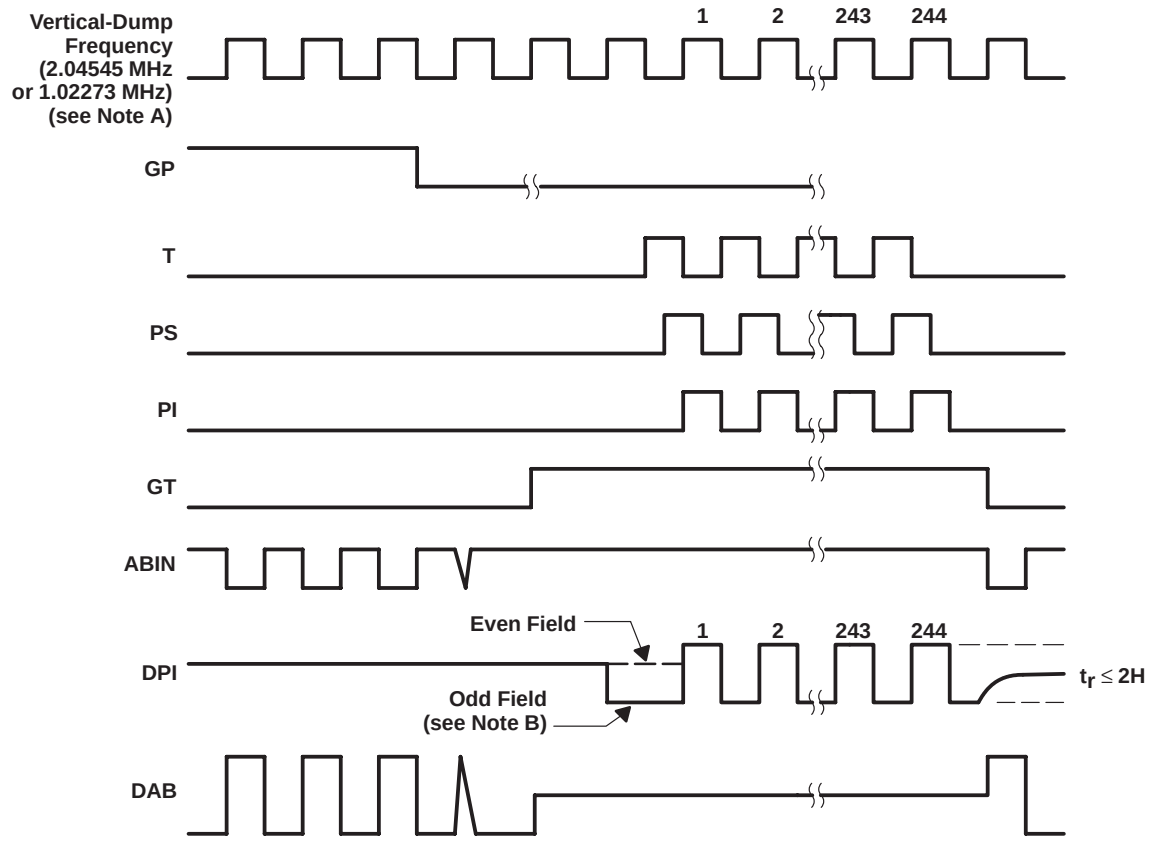
Figure 3. Horizontal Timing



† 910 intervals equal 63.55 μs equals one horizontal-scan line
‡ 130 intervals equal 63.55 μs equals one horizontal-scan line

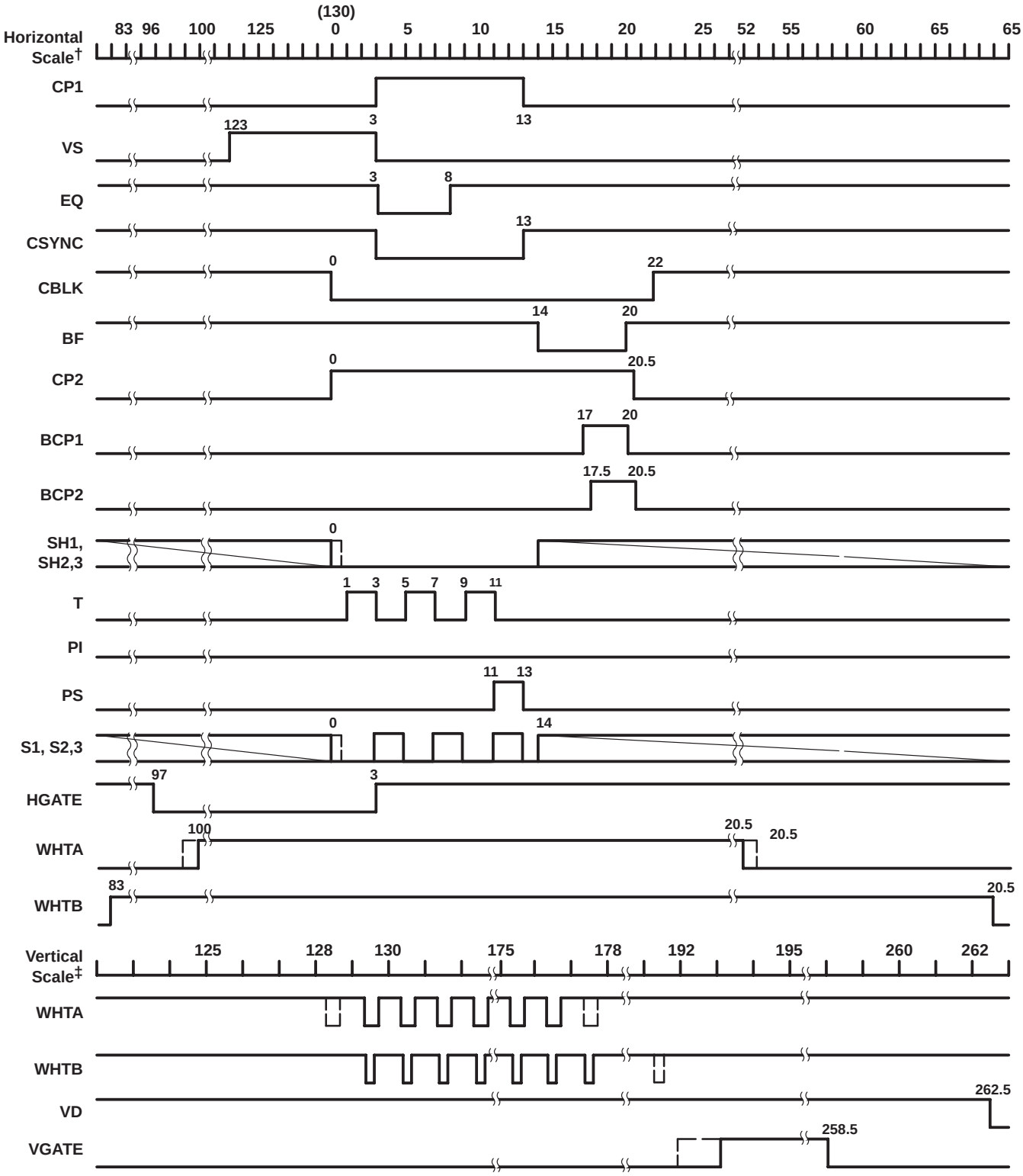
MODE	0	1	2	3		MODE	0	1	2	3	4	5	6	7
BCPS1	L	L	H	H		ABS2	L	L	L	L	H	H	H	H
BCPS0	L	H	L	H		ABS1	L	L	H	H	L	L	H	H
						ABS0	L	H	L	H	L	H	L	H

Figure 4. ABIN, BCP1, BCP2 Timing at the Start of H



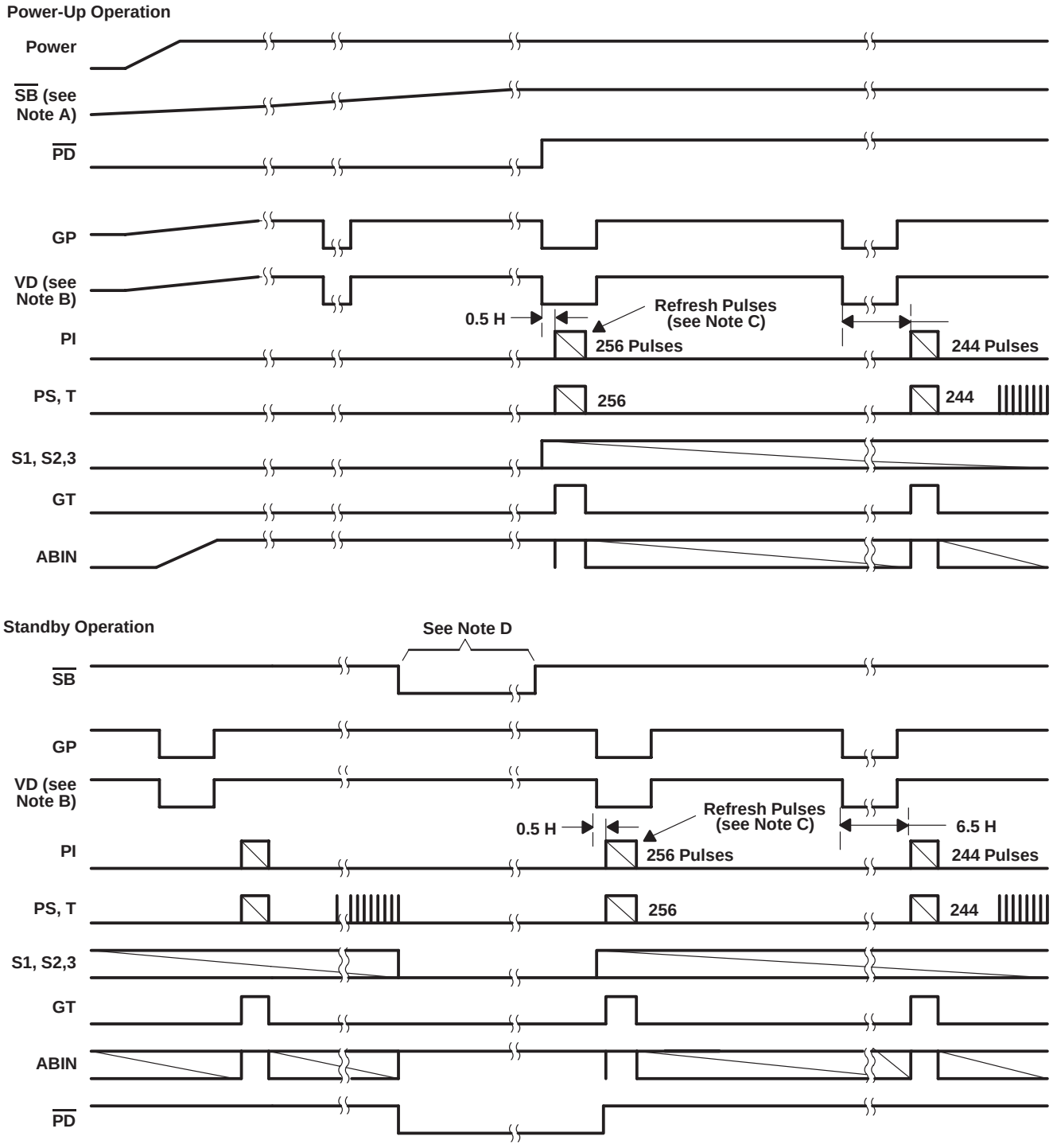
NOTES: A. When the vertical-dump frequency is 1.02273 MHz, PI, PS, and T have a 50% duty cycle.
B. If I/$\overline{N}$ is low, the DPI waveform is always as shown for the odd-field case.

Figure 5. PI, PS, T, and ABIN Timing



† 130 intervals equal 63.55 µs equals one horizontal-scan line
‡ 525 intervals equal 33.33 ms equals one TV frame

Figure 6. H Timing and WHTA, WHTB (V,H) Timing



NOTES: A. A 0.1-μF capacitor is connected between $\overline{SB}$ and GND.
B. The VD output is fed back to GP.
C. The 256 CCD refresh pulses are generated on PI, PS, and T even if VD is not fed back to GP.
D. When $\overline{SB}$ is low, PI, PS, T, S1, S2,3, GT, and $\overline{PD}$ are all low and ABIN is high.

Figure 7. Power-Up and Standby Timing

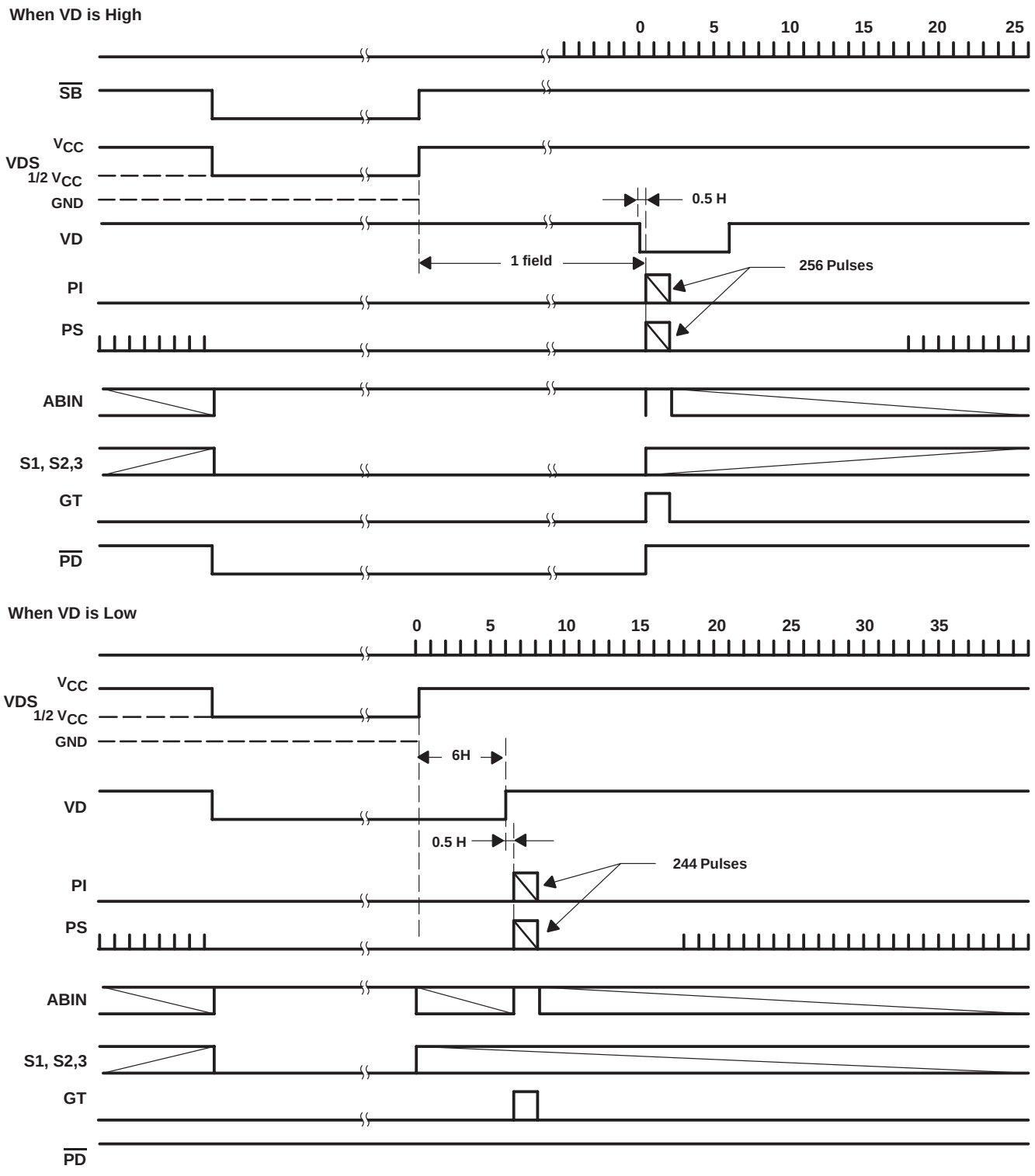
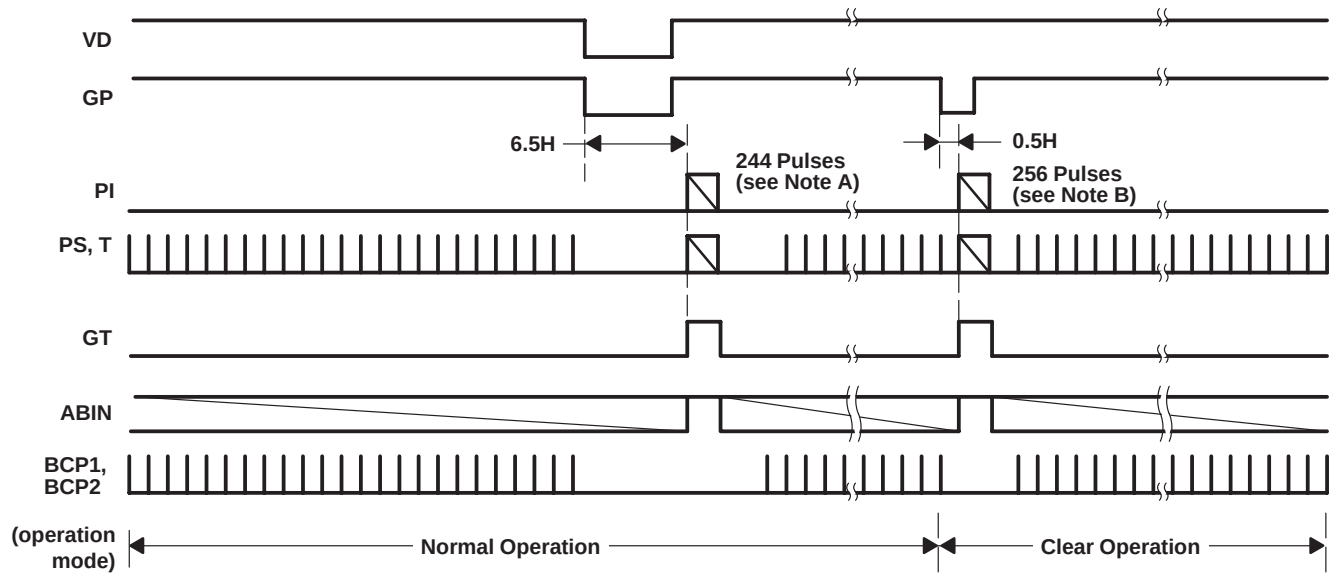
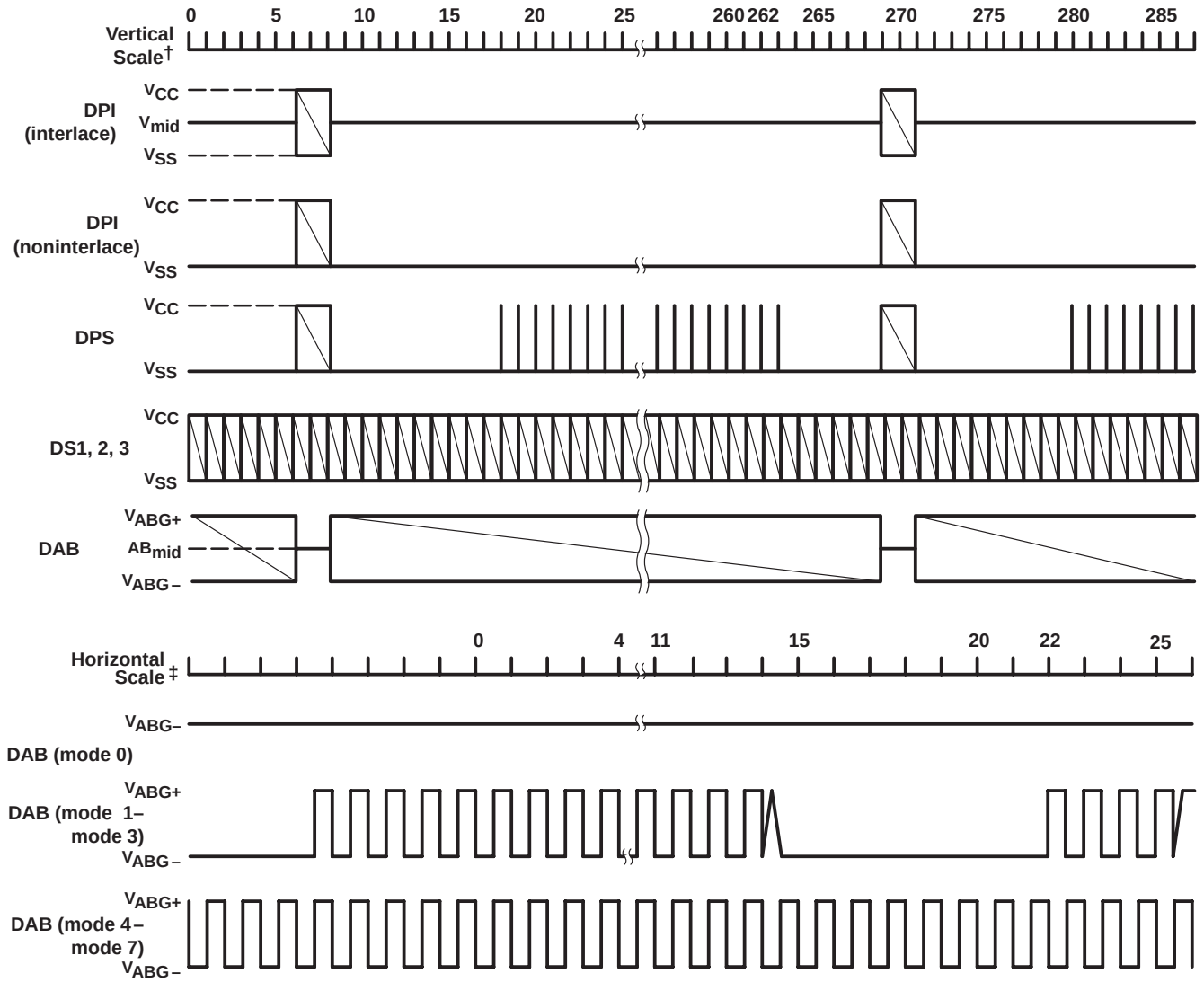


Figure 8. Timing for VDS in the Reset Mode



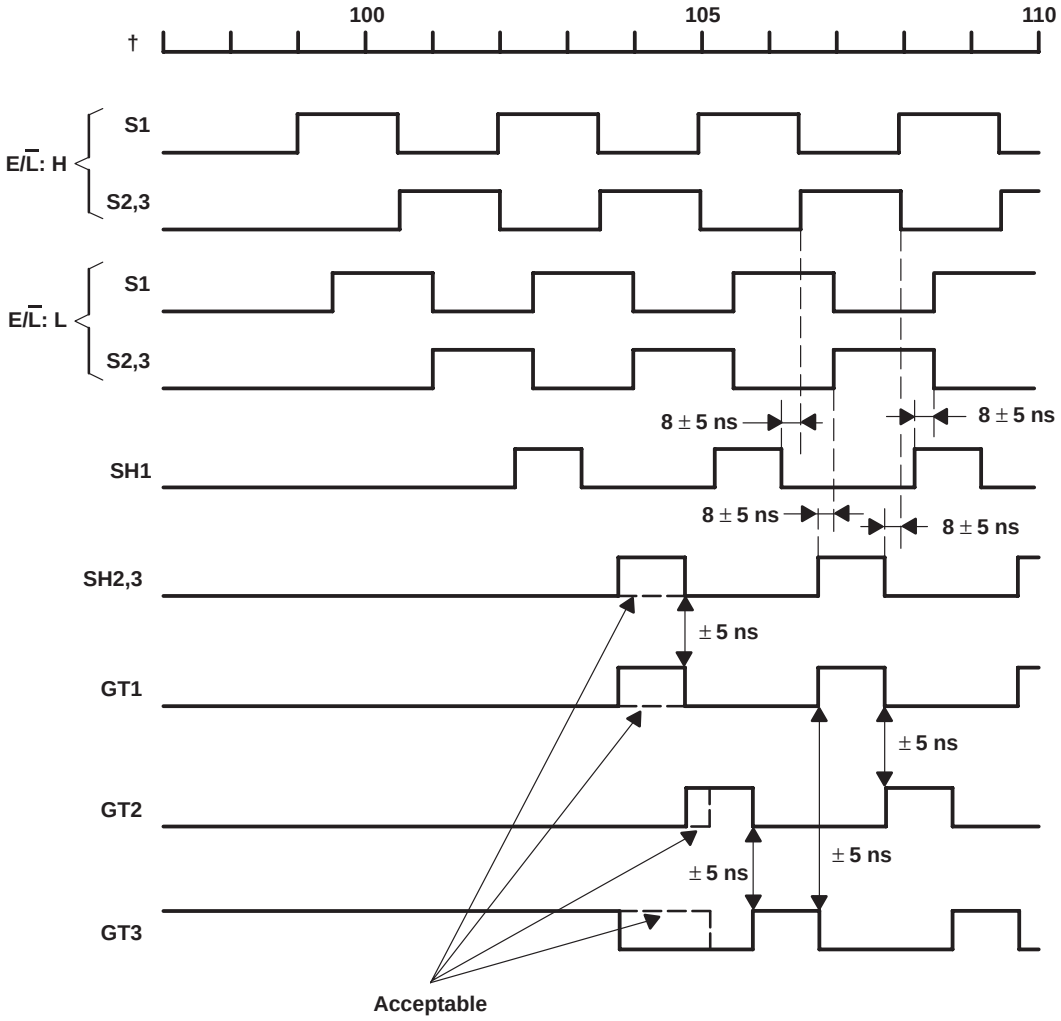
NOTES: A. When VD is low and GP goes low, 244 pulses are generated on PI, PS, and T.
B. If VD is high and not fed back to GP, then pulsing GP results in 256 pulses being generated on PI, PS, and T. This can be useful in clearing the imager. An external logic circuit is used to pulse GP.

Figure 9. GP Timing for Normal and Clear Modes



† 525 intervals equal 33.33 ms equals one TV frame
‡ 130 intervals equal 63.55 μs equals one horizontal-scan line

Figure 10. DPI, DPS, DS, and DAB Drive Timing

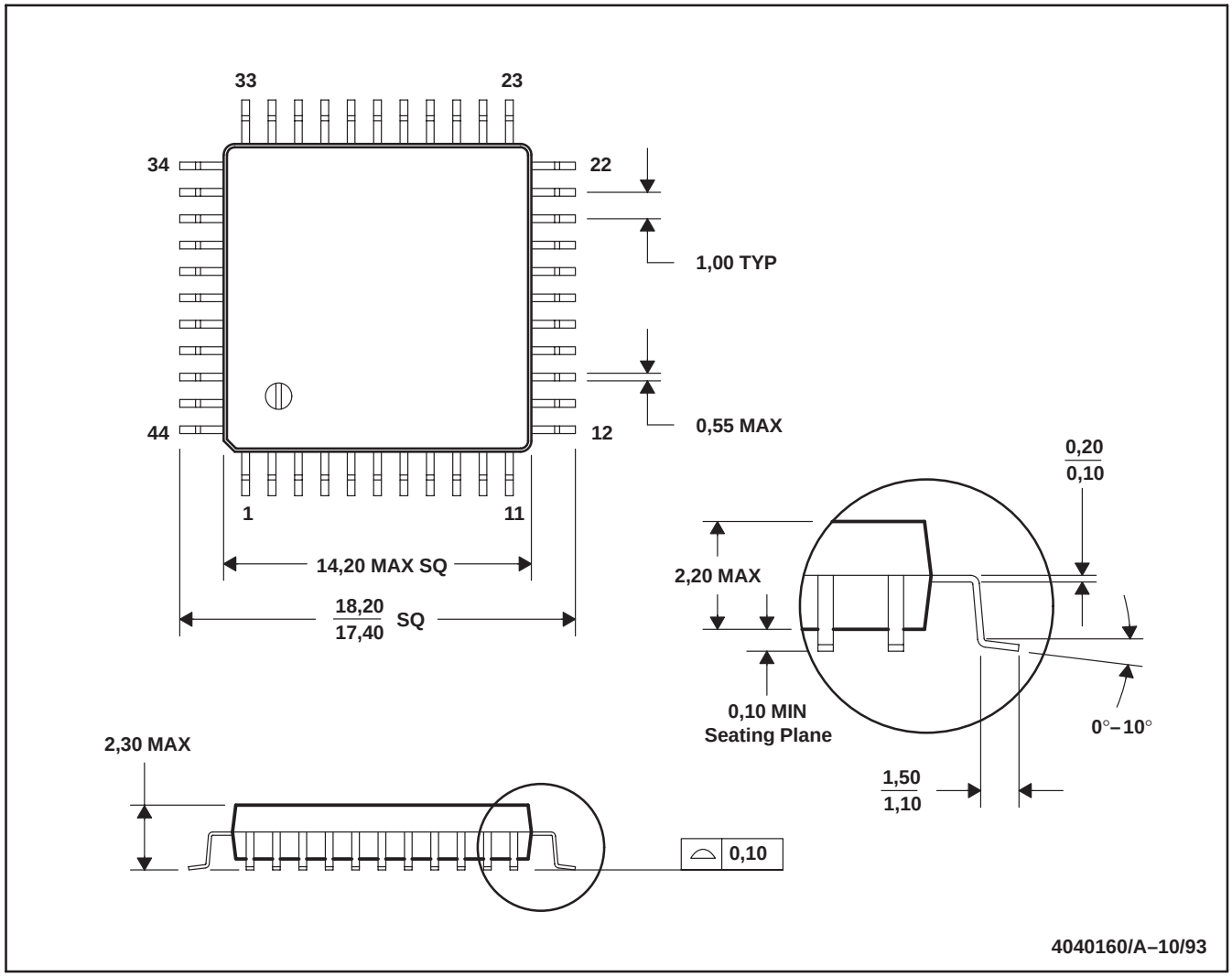


† Each interval equals one master clock interval equals 69.84 ns.

Figure 11. S1, S2,3, SH1, SH2,3, and GTn Waveforms

MECHANICAL DATA

FS/S-PQFP-G44 **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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