TLC32047C, TLC32047I
Data Manual

Wide-Band Analog Interface Circuit

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1 Introduction

The TLC32047 wide-band analog interface circuit (AIC) is a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32047 offers a powerful combination of options under DSP control: three operating modes [dual-word (telephone interface), word, and byte] combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order (sin x)/x correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board (sin x)/x correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to REF. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32047C is characterized for operation from 0°C to 70°C, and the TLC32047I is characterized for operation from –40°C to 85°C.

1.1 Features

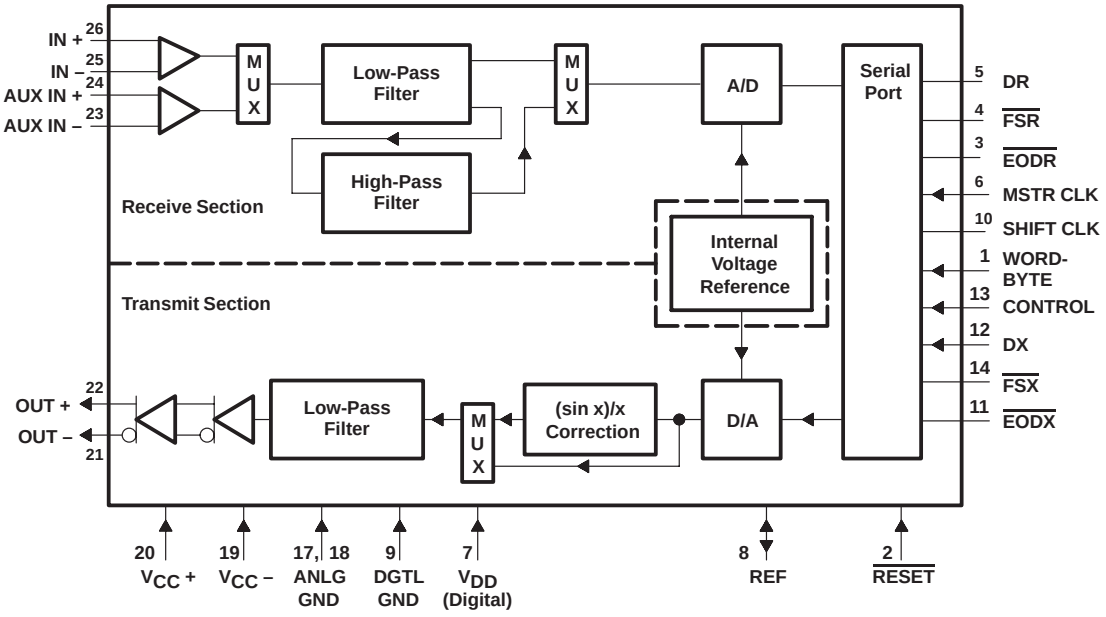
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input With Programmable Gain**
- **Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second**
- **Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Typical Applications**
  - **Speech Encryption for Digital Transmission**
  - **Speech Recognition and Storage Systems**
  - **Speech Synthesis**
  - **Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates**
  - **Industrial Process Control**
  - **Biomedical Instrumentation**
  - **Acoustical Signal Processing**
  - **Spectral Analysis**
  - **Instrumentation Recorders**
  - **Data Acquisition**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte**
- **600-mil Wide N Package**
- **Digital Output in Twos Complement Format**
- **CMOS Technology**

FUNCTION TABLE

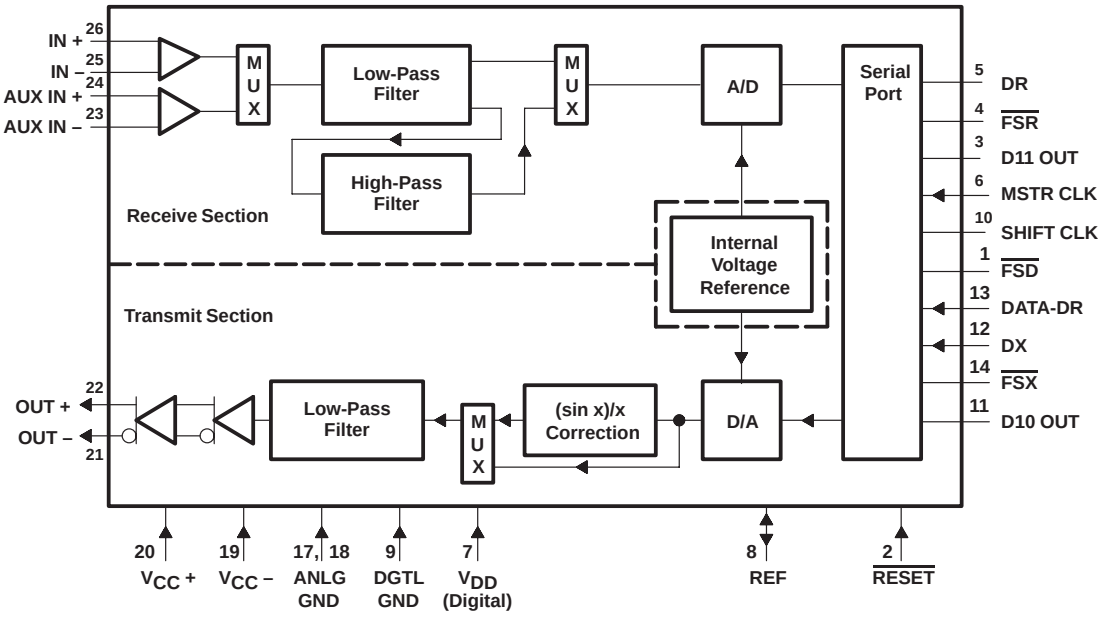
DATA FORMAT	SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1)	ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0)	FORCING CONDITION	DIRECT INTERFACE
16-bit format	Dual-word (telephone interface) mode	Dual-word (telephone interface) mode	$\overline{\text{DATA}}$-DR/CONTROL = 0 to 5 V $\overline{\text{FSD}}$/WORD-BYTE = 0 to 5 V	TMS32020, TMS320C25, TMS320C30
16-bit format	Word mode	Word mode	$\overline{\text{DATA}}$-DR/CONTROL = V_{CC-} (–5 V nom) $\overline{\text{FSD}}$/WORD-BYTE = V_{CC+} (5 V nom)	TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10 (see Figure 7)
8-bit format (2 bytes required)	Byte mode	Byte mode	$\overline{\text{DATA}}$-DR/CONTROL = V_{CC-} (–5 V nom) $\overline{\text{FSD}}$/WORD-BYTE = V_{CC-} (–5 V nom)	TMS320C17

1.2 Functional Block Diagrams

WORD OR BYTE MODE



DUAL-WORD (TELEPHONE INTERFACE) MODE



FRAME SYNCHRONIZATION FUNCTIONS

TLC32047 Function	Frame Sync Output
Receiving serial data on DX from processor to internal DAC	$\overline{\text{FSX}}$ low
Transmitting serial data on DR from internal ADC to processor, primary communications	$\overline{\text{FSR}}$ low
Transmitting serial data on DR from DATA-DR to processor, secondary communications in dual-word (telephone interface) mode only	$\overline{\text{FSD}}$ low

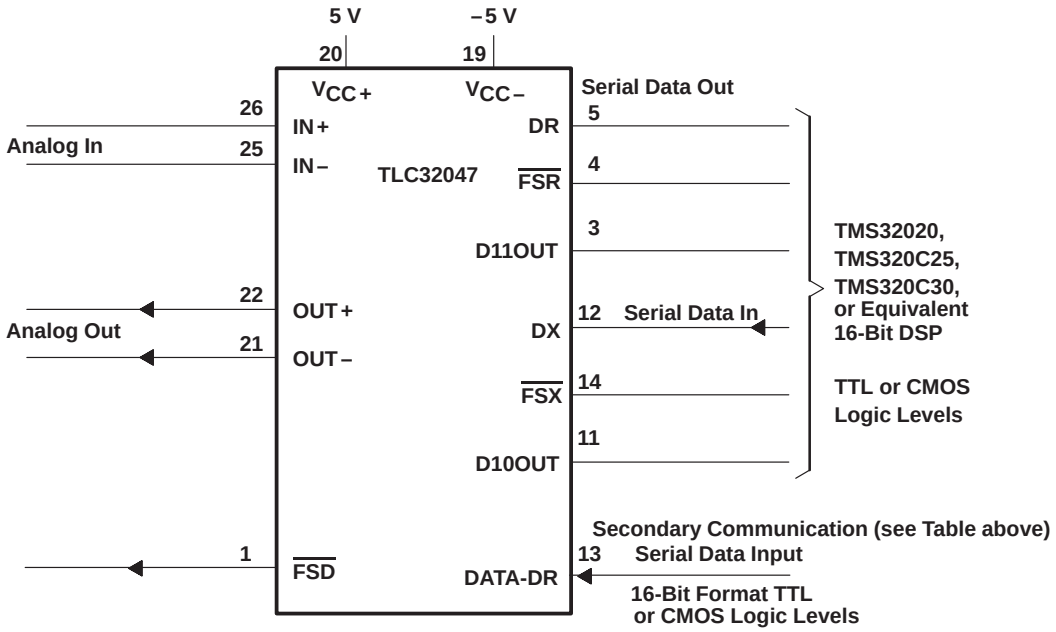


Figure 1–1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input is tied to a logic signal source varying between 0 and 5 V, the TLC32047 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when terminal 1, data frame synchronization ($\overline{\text{FSD}}$), outputs a low level. The $\overline{\text{FSD}}$ pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on D10OUT and D11OUT, respectively, as outputs.

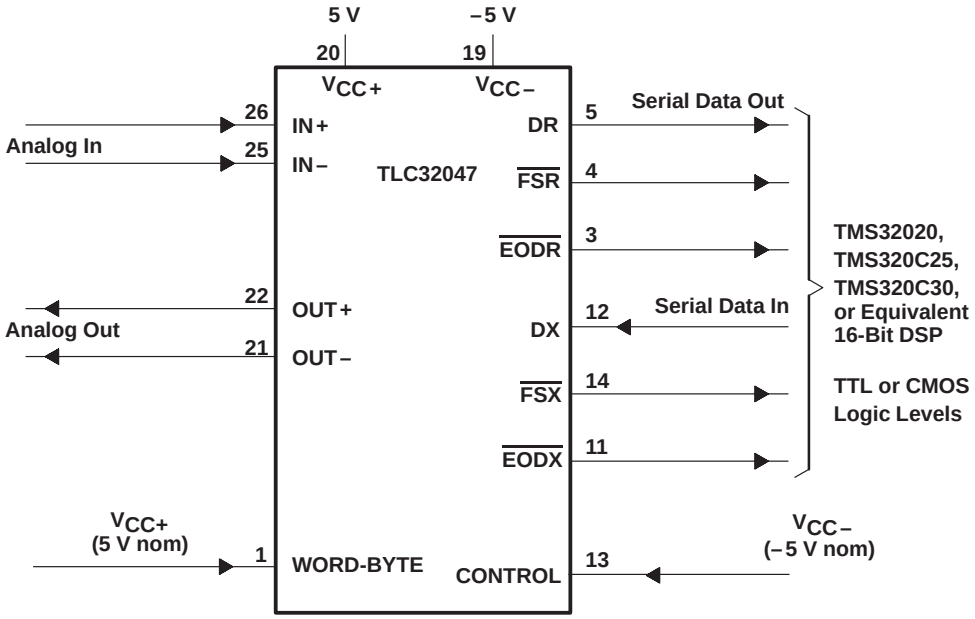


Figure 1–2. Word Mode

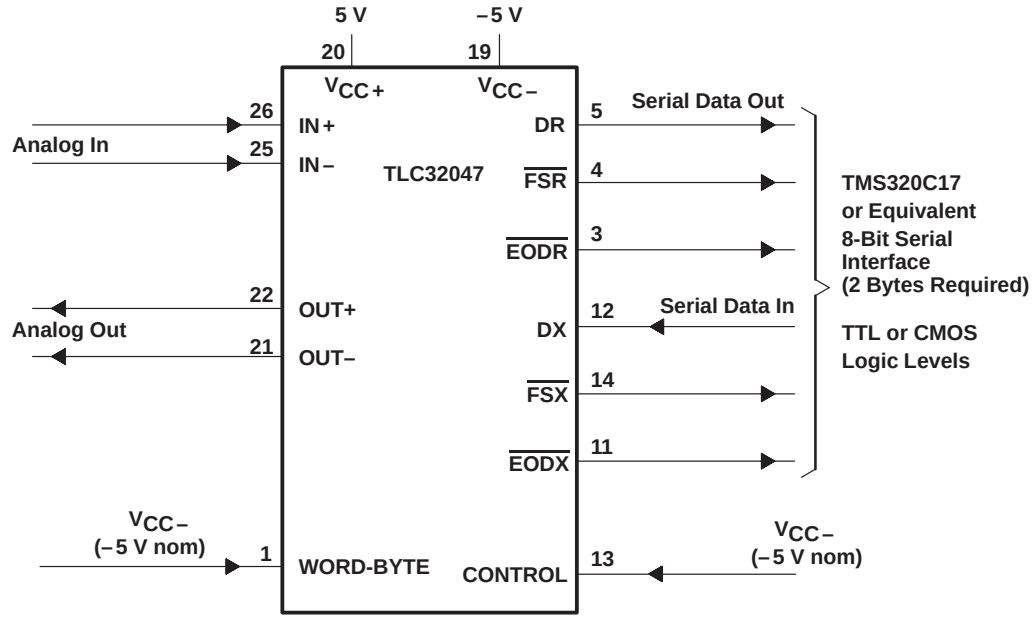
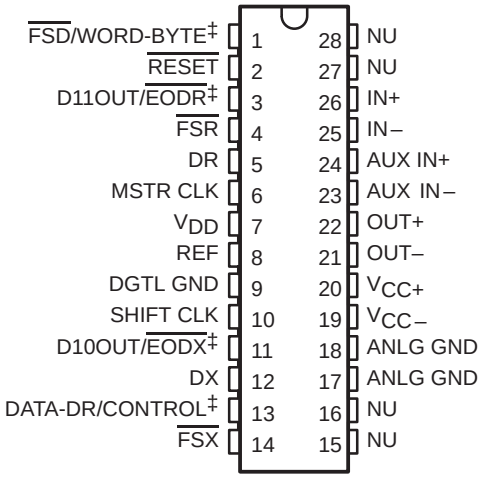


Figure 1–3. Byte Mode

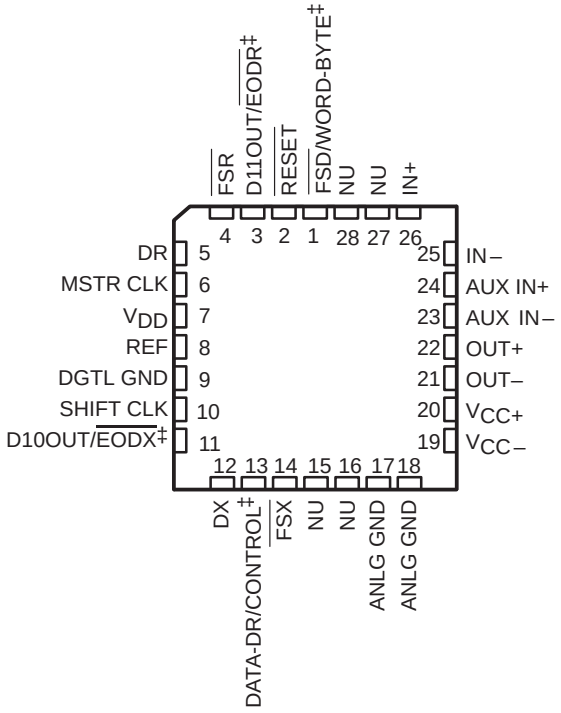
The word or byte mode is selected by first connecting the DATA-DR/CONTROL input to V_{CC-}. FSD/WORD-BYTE becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit ($\overline{EODX}$) and the end-of-data receive ($\overline{EODR}$) signals on terminals 11 and 3, respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

1.3 Terminal Assignments

N PACKAGE† (TOP VIEW)



FN PACKAGE (TOP VIEW)



NU - Nonusable; no external connection should be made to these pins.

† 600-mil wide

‡ The portion of the terminal name to the left of the slash is used for the dual-word (telephone interface) mode. The portion of the terminal name to the right of the slash is used for word-byte mode.

1.4 Ordering Information

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC32047CFN	TLC32047CN
–40°C to 85°C	TLC32047IFN	TLC32047IN

1.5 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ANLG GND	17,18		Analog ground return for all internal analog circuits. ANLG GND is internally connected to DGTL GND.
AUX IN+	24	I	Noninverting auxiliary analog input stage. AUX IN+ can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN– inputs. If the bit is a 0, the IN+ and IN– inputs are used (see the DX Serial Data Word Format).
AUX IN–	23	I	Inverting auxiliary analog input (see the above AUX IN+ description).
DATA-DR	13	I	The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to DATA-DR, allows DATA-DR to function as a data input. The data is then framed by the $\overline{\text{FSD}}$ signal and transmitted as an output to DR during secondary communication. The functions $\overline{\text{FSD}}$, D11OUT, and D10OUT are valid with this mode selection (see Table 2–1).
CONTROL			When CONTROL is tied to V_{CC}–, the device is in the word or byte mode. The functions WORD-BYTE, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are valid in this mode. $\overline{\text{FSD}}$/WORD-BYTE is then used to select either the word or byte mode (see Function Table).
DR	5	O	DR is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK signal.
DX	12	I	DX is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with the SHIFT CLK signal.
D10OUT	11	O	In the dual-word (telephone interface) mode, bit D10 of the control register is output to D10OUT. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10.
EODX			End of data transmit. During the word-mode timing, a low-going pulse occurs on EODX immediately after the 16 bits of DAC and control or register information have been transmitted from the TMS320 serial port to the AIC. EODX can be used to interrupt a microprocessor upon completion of serial communications. Also, EODX can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, EODX goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes.

1.5 Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
D11OUT	3	O	In the dual-word (telephone interface) mode, bit D11 of the control register is output to D11OUT. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11.
EODR			End of data receive. During the word-mode timing, a low-going pulse occurs on EODR immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. EODR can be used to interrupt a microprocessor upon completion of serial communications. Also, EODR can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, EODR goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes.
DGTL GND	9		Digital ground for all internal logic circuits. Not internally connected to ANLG GND.
$\overline{\text{FSD}}$	1	O	Frame sync data. The $\overline{\text{FSD}}$ output remains high during primary communication. In the dual-word (telephone interface) mode, the $\overline{\text{FSD}}$ output is identical to the $\overline{\text{FSX}}$ output during secondary communication.
WORD-BYTE		I	WORD-BYTE allows differentiation between the word and byte data format (see DATA-DR/CONTROL and Table 2-1 for details).
$\overline{\text{FSR}}$	4	O	Frame sync receive. $\overline{\text{FSR}}$ is held low during bit transmission. When $\overline{\text{FSR}}$ goes low, the TMS320 serial port begins receiving bits from the AIC via DR of the AIC. The most significant DR bit is present on DR before $\overline{\text{FSR}}$ goes low (see Serial Port Sections and Internal Timing Configuration Diagrams).
$\overline{\text{FSX}}$	14	O	Frame sync transmit. When $\overline{\text{FSX}}$ goes low, the TMS320 serial port begins transmitting bits to the AIC via DX of the AIC. $\overline{\text{FSX}}$ is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams).
IN+	26	I	Noninverting input to analog input amplifier stage
IN–	25	I	Inverting input to analog input amplifier stage
MSTR CLK	6	I	Master clock. MSTR CLK is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The internal timing configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration).
OUT+	22	O	Noninverting output of analog output power amplifier. OUT+ drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration.
OUT–	21	O	Inverting output of analog output power amplifier. OUT– is functionally identical with and complementary to OUT+.
REF	8	I/O	Internal voltage reference is brought out on REF. An external voltage reference can be applied to REF to override the internal voltage reference.

1.5 Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{RESET}}$	2	I	Reset. A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section): D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1 The shift clock (SCLK) is held high during $\overline{\text{RESET}}$. This initialization allows normal serial-port communication to occur between the AIC and the DSP.
SHIFT CLK	10	O	Shift clock. SHIFT CLK is obtained by dividing the master clock signal frequency by four. SHIFT CLK is used to clock the serial data transfers of the AIC.
V_{DD}	7		Digital supply voltage, 5 V ±5%
V_{CC+}	20		Positive analog supply voltage, 5 V ±5%
V_{CC-}	19		Negative analog supply voltage, –5 V ±5%

2 Detailed Description

Table 2–1. Mode-Selection Function Table

DATA-DR/ CONTROL	$\overline{\text{FSD}}$/ WORD-BYTE	CONTROL REGISTER BIT (D5)	OPERATING MODE	SERIAL CONFIGURATION	DESCRIPTION
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	1	Dual-Word (Telephone Interface)	Synchronous, One 16-Bit Word	Terminal functions DATA-DR†, $\overline{\text{FSD}}$†, D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication.
Data in (0 to 5 V)	$\overline{\text{FSD}}$ out (0 to 5 V)	0	Dual-Word (Telephone Interface)	Asynchronous, One 16-bit Word	Terminal functions DATA-DR†, $\overline{\text{FSD}}$†, D11OUT, and D10OUT are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from DR, $\overline{\text{FSD}}$ cannot go low, and data from DATA-DR cannot go onto DR.
V_{CC-}	V_{CC+}	1	WORD	Synchronous, One 16-Bit Word	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
		0		Asynchronous, One 16-bit Word	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
	V_{CC-}	1	BYTE	Synchronous, Two 8-Bit Bytes	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.
		0		Asynchronous, Two 8-Bit Bytes	Terminal functions CONTROL†, WORD-BYTE†, $\overline{\text{EODR}}$, and $\overline{\text{EODX}}$ are applicable in this configuration.

† DATA-DR/CONTROL has an internal pulldown resistor to –5 V, and $\overline{\text{FSD}}$/WORD-BYTE has an internal pullup resistor to 5 V.

2.1 Internal Timing Configuration (see Figure 2–1)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 432 kHz. If the clock frequency is not 432 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 432 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock}\text{ (kHz)}}{432} \quad (1)$$

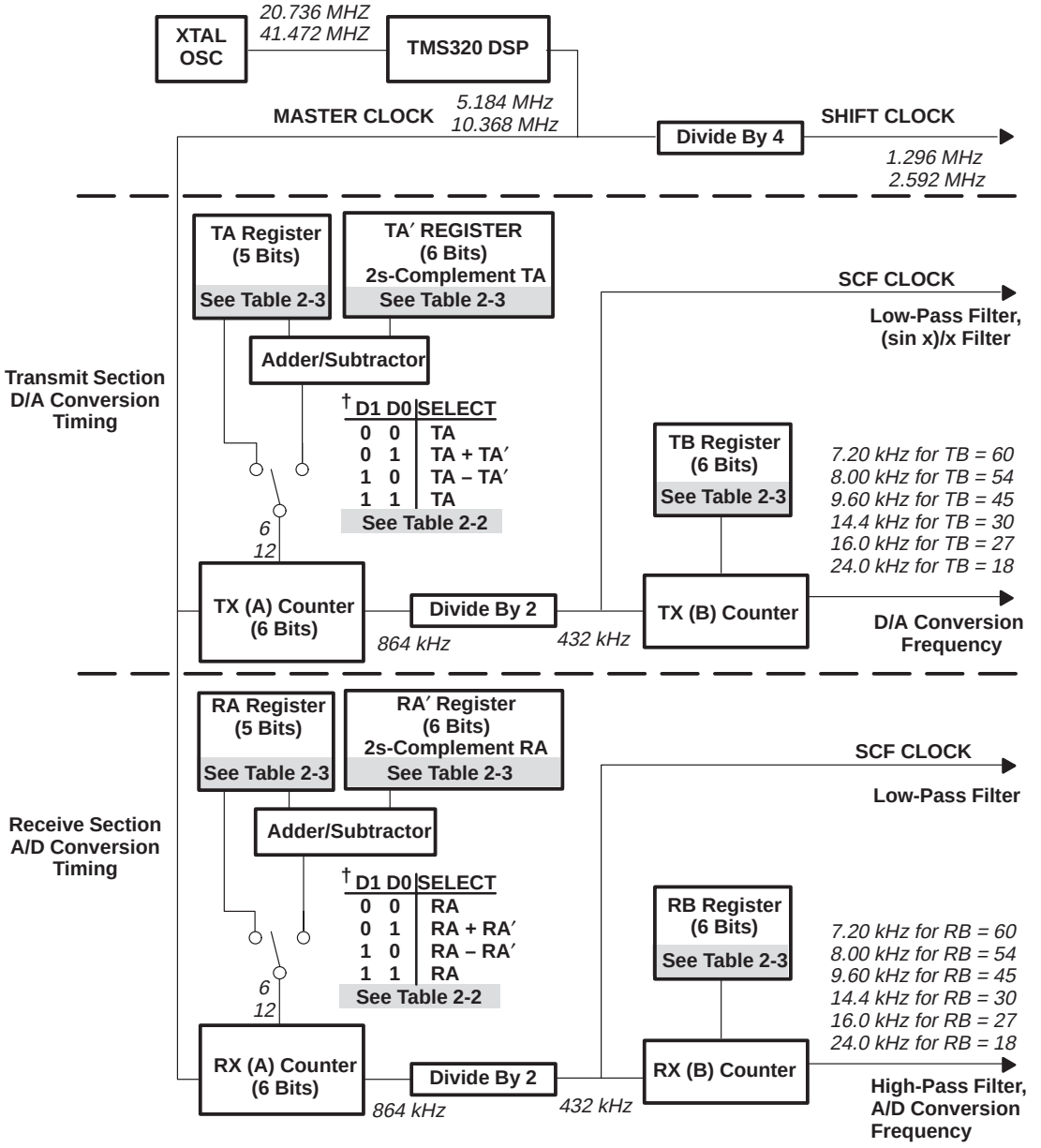
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 432-kHz switched-capacitor clock signal. This 432-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the shift clock frequency (SCF) is 432 kHz, the high-frequency roll-off of the low-pass section meets the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off is frequency-scaled by the ratio of the high-pass section's SCF clock to 432 kHz (see Figure 5–5). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 24 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 24 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA′ register, or the TA register plus the TA′ register. By selecting the TA register less the TA′ register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA′ times the signal period of the master clock. If the TA register plus the TA′ register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA′ times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA′ register, or the RA register plus the RA′ register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be synchronous, the RX(A) counter, RX(B) counter, RA register, RA′ register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

NOTES: A. Tables 2–2 and 2–3 (pages 2–9 and 2–10) are primary and secondary communication protocols, respectively.

B. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.

C. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP provides a master clock frequency of 5.184 MHz. The TLC32047 produces a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 6, the SCF clock frequency is then 432 kHz, and the D/A conversion frequency is 432 kHz ÷ T(B).

Figure 2–1. Asynchronous Internal Timing Configuration

2.2 Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 4–1). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 2–3). The multiplexing requires a 2-ms wait at SCF = 432 kHz (see Figure 5–3) for a valid output signal. A wide dynamic range is ensured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

2.3 A/D Band-Pass Filter, A/D Band-Pass Filter Clocking, and A/D Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is on page 3-5. This response results when the switched-capacitor filter clock frequency is 432 kHz and the A/D sample rate is 24 kHz. Several possible options can be used to attain a 432-kHz switched-capacitor filter clock. When the filter clock frequency is not 432 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 432 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 450 Hz and 300 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 24 kHz.

Figure 2–1 and the DX Serial Data Word Format sections of this data manual indicate the many options for attaining a 432-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 432-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

2.4 A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are on pages 3-2 and 3-3 of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

2.5 Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

2.6 D/A Low-Pass Filter, D/A Low-Pass Filter Clocking, and D/A Conversion Timing

The frequency response of these filters is on page 3-5. This response results when the low-pass switched-capacitor filter clock frequency is 432 kHz (see Equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 432 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 432-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 432-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

2.7 D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are on pages 3-3 and 3-4. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

2.8 Serial Port

The serial port has four possible configurations summarized in the function table on page 1-2. These configurations are briefly described below.

- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
- The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

2.9 Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The $\overline{\text{FSX}}$ and the $\overline{\text{FSR}}$ timing is identical during primary communication, but $\overline{\text{FSR}}$ is not asserted during secondary communication because there is no new A/D conversion result.

2.9.1 One 16-Bit Word [Dual-Word (Telephone Interface) or Word Mode]

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high.
4. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

2.9.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought low.
4. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ emit positive frame-sync pulses that are four shift clock cycles wide.
5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ are brought high.
7. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are brought high.

2.9.3 Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 2–1):

$$\text{Low-pass SCF clock frequency (D/A and A/D channels)} = \frac{\text{master clock frequency}}{\text{T(A)} \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\text{Conversion frequency (A/D and D/A channels)} = \frac{\text{Low pass SCF clock frequency}}{\text{T(B)}}$$

$$= \frac{\text{master clock frequency}}{\text{T(A)} \times 2 \times \text{T(B)}}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.10 Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

2.10.1 One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32047 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
4. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in either the word or byte mode only.

2.10.2 Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought low by the TLC32047 AIC.
2. One byte is transmitted or received.

3. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought low.
4. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ are brought high.
7. $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ are brought high.

2.10.3 Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 2–1):

$$\text{Low pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{\text{T(A)} \times 2}$$

$$\text{Low pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{\text{R(A)} \times 2}$$

$$\text{High pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \quad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{Low pass D/A SCF clock frequency}}{\text{T(B)}}$$

$$\text{A/D conversion frequency} = \frac{\text{Low pass A/D SCF clock frequency (for low pass receive filter)}}{\text{R(B)}} \quad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

2.11 Operation of TLC32047 With Internal Voltage Reference

The internal reference of the TLC32047 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to REF. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

2.12 Operation of TLC32047 With External Voltage Reference

REF can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be protected adequately from noise and crosstalk from the analog input.

2.13 Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on $\overline{\text{RESET}}$, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After a reset, TA=TB=RA=RB=18 (or 12 hexadecimal), TA′=RA′=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN– are disabled, the transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10 OUT is set to 0, and D11 OUT is set to 0.

2.14 Loopback

This feature allows the circuit to be tested remotely. In loopback, OUT+ and OUT– are internally connected to IN+ and IN–. The DAC bits (D15 to D2), which are transmitted to DX, can be compared with the ADC bits (D15 to D2) received from DR. The bits on DR equal the bits on DX. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic 1 for data bit D3 in the DX secondary communication to the control register (see Table 2–3).

2.15 Communications Word Sequence

In the dual-word (telephone interface) mode, there are two data words that are presented to the DSP or µP from DR. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to DATA-DR during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

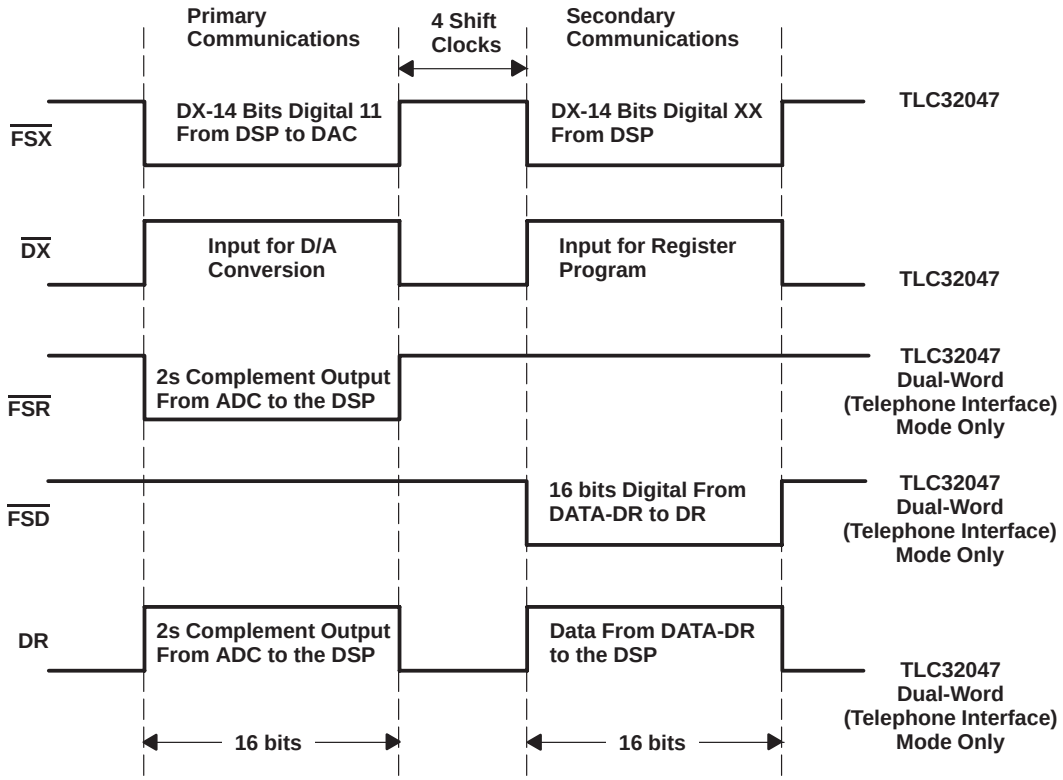
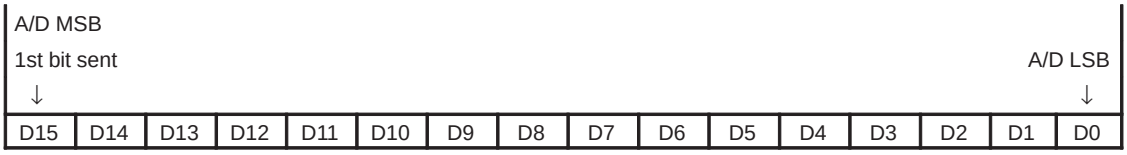


Figure 2–2. Primary and Secondary Communications Word Sequence

2.15.1 DR Word Bit Pattern



The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero. Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

2.15.2 Primary DX Word Bit Pattern

A/D OR D/A MSB

1st bit sent ↓ | 1st bit sent of 2nd byte ↓ | A/D or D/A LSB ↓

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2–2. Primary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1).	0	0
D15 (MSB)-D2 → DAC Register. TA+TA′ → TX(A), RA+RA′ → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the addition of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero (refer to Table 2–4, AIC Responses to Improper Conditions).	0	1
D15 (MSB)-D2 → DAC Register. TA–TA′ → TX(A), RA–RA′ → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). The next D/A and A/D conversion period is changed by the subtraction of TA′ and RA′ master clock cycles, in which TA′ and RA′ can be positive, negative, or zero (refer to Table 2–4, AIC Responses to Improper Conditions).	1	0
D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A) (see Figure 2–1). TB → TX(B), RB → RX(B) (see Figure 2–1). After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA-DR is routed to DR (Serial Data Output) during secondary transmission.	1	1

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, $\overline{\text{FSX}}$ remains high for four shift clock cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. $\overline{\text{FSR}}$ is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, $\overline{\text{FSD}}$ is asserted during secondary communications but not during primary communications.

2.15.3 Secondary DX Word Bit Pattern

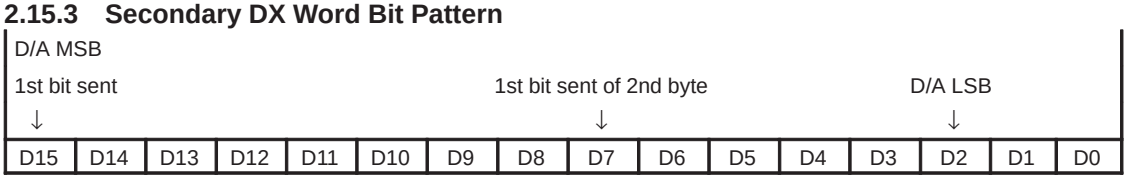


Table 2–3. Secondary DX Serial Communication Protocol

FUNCTIONS	D1	D0
D13 (MSB)-D9 → TA , 5 bits unsigned binary (see Figure 2–1). D6 (MSB)-D2 → RA, 5 bits unsigned binary (see Figure 2–1). D15, D14, D8, and D7 are unassigned.	0	0
D14 (sign bit)-D9 → TA′, 6 bits 2s complement (see Figure 2–1). D7 (sign bit)-D2 → RA′, 6 bits 2s complement (see Figure 2–1). D15 and D8 are unassigned.	0	1
D14 (MSB)-D9 → TB, 6 bits unsigned binary (see Figure 2–1). D7 (MSB)-D2 → RB, 6 bits unsigned binary (see Figure 2–1). D15 and D8 are unassigned.	1	0
D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables AUX IN+ and AUX IN–. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 4–1). D7 = 0/1 gain control bits (see Table 4–1). D9 = 0/1 delete/insert on-board second-order (sin x)/x correction filter D10 = 0/1 output to D10OUT [dual-word (telephone interface) mode] D11 = 0/1 output to D11OUT [dual-word (telephone interface) mode] D8, D12–D15 are unassigned.	1	1

2.16 Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on $\overline{\text{RESET}}$ initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively. Therefore, the filter bandwidths are 66% of those shown in the filter transfer function specification section. The AIC, excepting the control register, is initialized as follows (see AIC DX Data Word Format section):

REGISTER	TA	TA′	TB	RA	RA′	RB
INITIALIZED VALUE (HEX)	12	01	12	12	01	12

The control register bits are reset as follows (see Table 2–3):

D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA′, and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 2–3 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the Power-Up Sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

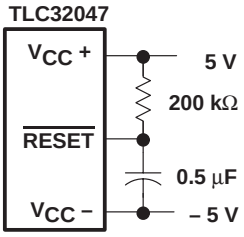


Figure 2–3. Reset on Power-Up Circuit

2.17 Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-}, then V_{CC+} and V_{DD}. Also, no input signal is applied until after power-up.

2.18 AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= High).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= Low).
3. TA′ register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = High).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = Low).
6. RA′ register can be either positive, negative, or zero.
7. (TA register ± TA′ register) must be > 1.
8. (RA register ± RA′ register) must be > 1.
9. TB register must be ≥ 15.
10. RB register must be ≥ 15.

2.19 AIC Responses to Improper Conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 2–4. The general procedure for correcting any improper operation is to apply a reset and reprogram the registers to the proper value.

Table 2–4. AIC Responses to Improper Conditions

IMPROPER CONDITION	AIC RESPONSE
TA register + TA′ register = 0 or 1 TA register – TA′ register = 0 or 1	Reprogram TX(A) counter with TA register value
TA register + TA′ register < 0	MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA′ register + 40 hex is loaded into TX(A) counter.
RA register + RA′ register = 0 or 1 RA register – RA′ register = 0 or 1	Reprogram RX(A) counter with RA register value
RA register + RA′ register = 0 or 1	MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA′ register + 40 hex is loaded into RX(A) counter.
TA register = 0 or 1 RA register = 0 or 1	AIC is shut down. Reprogram TA or RA registers after a reset.
TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode	The AIC serial port no longer operates. Reprogram TA or RA registers after a reset.
TB register < 15	ADC no longer operates
RB register < 15	DAC no longer operates
AIC and DSP cannot communicate	Hold last DAC output

2.20 Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A′ register result is too small. When incrementally adjusting the conversion period via the A + A′ register options, the designer should not violate this requirement. See Figure 2–4.

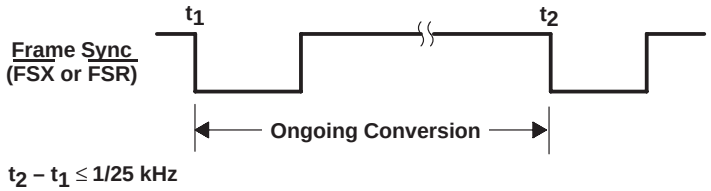


Figure 2–4. Conversion Times Too Close Together

2.21 More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an FSX frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2, the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B. The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent FSX frame (see Figure 2–5).

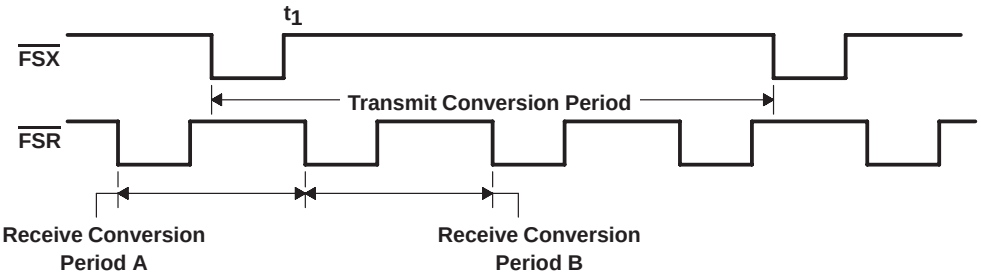


Figure 2–5. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

2.22 More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A′ or A – A′ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an $\overline{\text{FSX}}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 2–6. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2. If there is not sufficient time between t_1 and t_2, receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

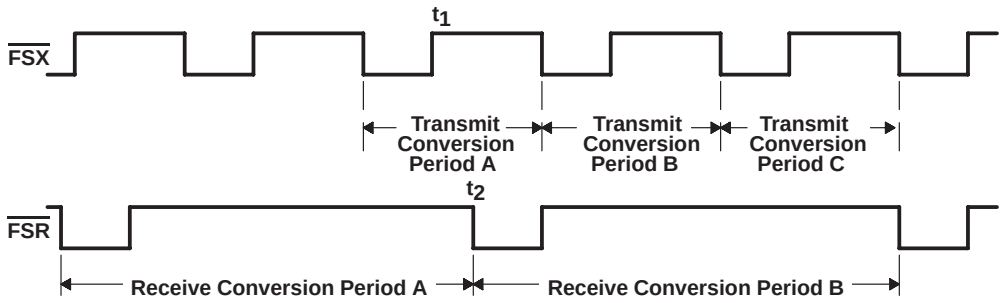


Figure 2–6. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

2.23 More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA′, TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1 and t_2, the TA, RA′, and RB register information, sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA′, and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA′, or RB information received during this receive conversion period is disregarded. See Figure 2–7.

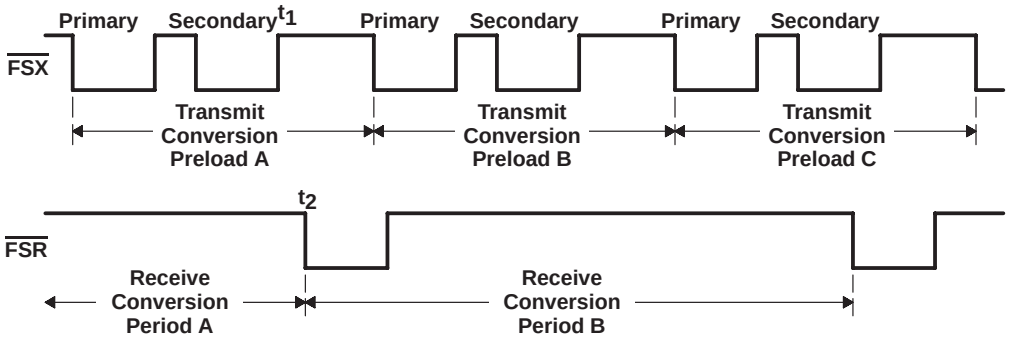


Figure 2–7. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

2.24 System Frequency Response Correction

The (sin x)/x correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order (sin x)/x correction filter (see Functional Block Diagram). This (sin x)/x correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the (sin x)/x correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 2–1) equals 15, the correction results of Figures 5–8, 5–9, and 5–10 can be obtained.

The (sin x)/x correction can also be accomplished by disabling the on-board second-order correction filter and performing the (sin x)/x correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the (sin x)/x Correction Section for more details).

2.25 (sin x)/x Correction

If the designer does not wish to use the on-board second-order (sin x)/x correction filter, correction can be accomplished in digital signal processor (DSP) software. (sin x)/x correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown below are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DSP. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

2.26 (sin x)/x Roll-Off for a Zero-Order Hold Function

The (sin x)/x roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 2–5 (see Figure 5–10).

Table 2–5. (sin x)/x Roll-Off Error

f_S (Hz)	Error = 20 log $\frac{\sin \pi f/f_S}{\pi f/f_S}$ f = 3000 Hz (dB)
7200	–2.64
8000	–2.11
9600	–1.44
14400	–0.63
16000	–0.50
19200	–0.35
25000	–0.21

The actual AIC (sin x)/x roll-off is slightly less than the figures above because the AIC has less than 100% duty cycle hold interval.

2.27 Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 2–8.

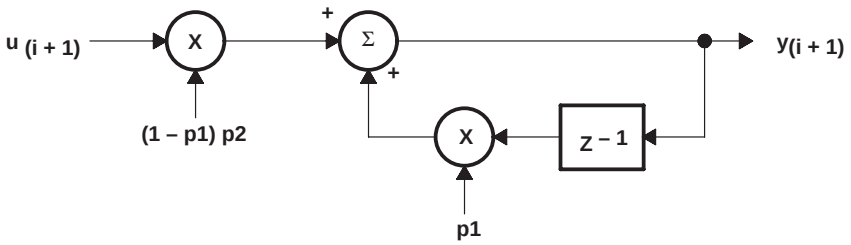


Figure 2–8. First-Order Correction Filter

The difference equation for this correction filter is:

$$y_{(i+1)} = p2 \cdot (1 - p1) \cdot u_{(i+1)} + p1 \cdot y_{(i)} \quad (4)$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{(p2)^2 \cdot (1-p1)^2}{1-2 \cdot p1 \cdot \cos(2\pi f/f_S) + (p1)^2} \quad (5)$$

2.28 Correction Results

Table 2-6 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 5–8, 5–9, and 5–10).

Table 2–6. (sin x)/x Correction Table for f_S = 8000 Hz and f_S = 9600 Hz

f (Hz)	ROLL-OFF ERROR (dB) f_S = 8000 Hz p1 = –0.14813 p2 = 0.9888	ROLL-OFF ERROR (dB) f_S = 9600 Hz p1 = –0.1307 p2 = 0.9951
300	–0.099	–0.043
600	–0.089	–0.043
900	–0.054	0
1200	–0.002	0
1500	0.041	0
1800	0.079	0.043
2100	0.100	0.043
2400	0.091	0.043
2700	–0.043	0
3000	–0.102	–0.043

2.29 TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$y_{(i+1)} = y_{(i)} \times k1 + u_{(i+1)} \times k2$$

where

k1 = p1
k2 = (1 – p1)p2
y(i) is the filter state
u(i+1)

The coefficients k1 and k2 must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

3 Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, V_{CC+} (see Note 1) . . . . . –0.3 V to 15 V
Supply voltage range, V_{CC-} (see Note 1) . . . . . –0.3 V to 15 V
Supply voltage range, V_{DD} . . . . . –0.3 V to 15 V
Output voltage range, V_O . . . . . –0.3 V to 15 V
Input voltage range, V_I . . . . . –0.3 V to 15 V
Digital ground voltage range . . . . . –0.3 V to 15 V
Operating free-air temperature range: TLC32047C . . . . . 0°C to 70°C
TLC32047I . . . . . –40°C to 85°C
Storage temperature range . . . . . –40°C to 125°C
Case temperature for 10 seconds: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-}.

3.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} (see Note 2)		4.75	5	5.25	V
Supply voltage, V_{CC-} (see Note 2)		−4.75	−5	−5.25	V
Digital supply voltage, V_{DD} (see Note 2)		4.75	5	5.25	V
Digital ground voltage with respect to ANLG GND, DGTL GND			0		V
Reference input voltage, $V_{ref(ext)}$ (see Note 2)		2		4	V
High-level input voltage, V_{IH}		2		V_{DD}	V
Low-level input voltage, V_{IL} (see Note 3)		0		0.8	V
Load resistance at OUT+ and/or OUT–, R_L		300			Ω
Load capacitance at OUT+ and/or OUT–, C_L				100	pF
MSTR CLK frequency (see Note 4)			5	10.368	MHz
Analog input amplifier common mode input voltage (see Note 5)				±1.5	V
A/D or D/A conversion rate				25	kHz
Operating free-air temperature range, T_A	TLC32047C	0		70	°C
	TLC32047I	−40		85	

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+}, and V_{CC-} are with respect to ANLG GND. Voltages at digital inputs and outputs and V_{DD} are with respect to DGTL GND.

3. The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.

4. The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 432 kHz and the high-pass section SCF clock is 24 kHz. If the low-pass SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 432 kHz. If the high-pass SCF clock is shifted from 24 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 24 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 432 kHz. If the SCF clock is shifted from 432 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 432 kHz.

5. This range applies when (IN+ – IN–) or (AUX IN+ – AUX IN–) equals ± 6 V.

3.3 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V (Unless Otherwise Noted)

3.3.1 Total Device, MSTR CLK Frequency = 5.184 MHz, Outputs Not Loaded

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V, I_{OH} = −300 µA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2 mA			0.4	V
I_{CC+}	Supply current from V_{CC+}	TLC32047C				35	mA
		TLC32047I				40	
I_{CC-}	Supply current from V_{CC-}	TLC32047C				−35	mA
		TLC32047I				−40	
I_{DD}	Supply current from V_{DD}					7	mA
V_{ref}	Internal reference output voltage			3		3.3	V
αV_{ref}	Temperature coefficient of internal reference voltage				250		ppm/°C
r_o	Output resistance at REF				100		kΩ

† All typical values are at T_A = 25°C.

3.3.2 Power Supply Rejection and Crosstalk Attenuation

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at DR (ADC output)		30		dB
	f = 30 kHz to 50 kHz			45		
V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended)	f = 0 to 30 kHz	Idle channel, supply signal at 200 mV p-p measured at OUT+		30		dB
	f = 30 kHz to 50 kHz			45		
Crosstalk attenuation, transmit-to-receive (single-ended)				80		dB

† All typical values are at T_A = 25°C.

3.3.3 Serial Port

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –300 µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current				±10	µA
I_I	Input current, DATA-DR/CONTROL				±100	µA
C_i	Input capacitance			15		pF
C_o	Output capacitance			15		pF

† All typical values are at T_A = 25°C.

3.3.4 Receive Amplifier Input

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	A/D converter offset error (filters in)			10	70	mV
CMRR	Common-mode rejection ratio at IN+, IN–, or AUX IN+, AUX IN–	See Note 6		55		dB
r_i	Input resistance at IN+, IN– or AUX IN+, AUX IN–, REF			100		kΩ

† All typical values are at T_A = 25°C.

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 24-kHz conversion rate.

3.3.5 Transmit Filter Output

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OO}	Output offset voltage at OUT+ or OUT– (single-ended relative to ANLG GND)			15	80	mV
V_{OM}	Maximum peak output voltage swing across R_L at OUT+ or OUT– (single-ended)	$R_L \geq 300\ \Omega$, Offset voltage = 0	±3			V
	Maximum peak output voltage swing between OUT+ and OUT– (differential output)	$R_L \geq 600\ \Omega$,	±6			V

† All typical values are at T_A = 25°C.

3.3.6 Receive and Transmit Channel System Distortion, SCF Clock Frequency = 432 kHz (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Attenuation of second harmonic of A/D input signal	single-ended	V_I = –0.1 dB to –24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of A/D input signal	single-ended			65		dB
	differential		57	65		
Attenuation of second harmonic of D/A input signal	single-ended	V_I = –0 dB to –24 dB		70		dB
	differential		62	70		
Attenuation of third and higher harmonics of D/A input signal	single-ended			65		dB
	differential		57	65		

† All typical values are at T_A = 25°C.

3.3.7 Receive Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	A_V = 1 V/V‡		A_V = 2 V/V‡		A_V = 4 V/V‡		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
A/D channel signal-to-distortion ratio	V_I = –6 dB to –0.1 dB	56		§		§		dB
	V_I = –12 dB to –6 dB	56		56		§		
	V_I = –18 dB to –12 dB	53		56		56		
	V_I = –24 dB to –18 dB	47		53		56		
	V_I = –30 dB to –24 dB	41		47		53		
	V_I = –36 dB to –30 dB	35		41		47		
	V_I = –42 dB to –36 dB	29		35		41		
	V_I = –48 dB to –42 dB	23		29		35		
	V_I = –54 dB to –48 dB	17		23		29		

‡ A_V is the programmable gain of the input amplifier.

§ Measurements under these conditions are unreliable due to overrange and signal clipping.

NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

3.3.8 Transmit Channel Signal-to-Distortion Ratio (see Note 7)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
D/A channel signal-to-distortion ratio	V_I = –6 dB to –0.1 dB	58		dB
	V_I = –12 dB to –6 dB	58		
	V_I = –18 dB to –12 dB	56		
	V_I = –24 dB to –18 dB	50		
	V_I = –30 dB to –24 dB	44		
	V_I = –36 dB to –30 dB	38		
	V_I = –42 dB to –36 dB	32		
	V_I = –48 dB to –42 dB	26		
	V_I = –54 dB to –48 dB	20		

NOTE 7: The test condition is a 1-kHz input signal with a 24-kHz conversion rate. The load impedance for the DAC is 600 Ω. Input and output voltages are referred to V_{ref}.

3.3.9 Receive and Transmit Gain and Dynamic Range (see Note 8)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit gain tracking error	V_O = –48 dB to 0 dB signal range		±0.05	±0.25	dB
Receive gain tracking error	V_I = –48 dB to 0 dB signal range		±0.05	±0.25	dB

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

3.3.10 Receive Channel Band-Pass Filter Transfer Function, SCF f_{clock} = 432 kHz, Input (IN+ – IN–) is a ±3-V Sine Wave‡ (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY	ADJUSTMENT	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f ≤ 150 Hz	K1 × 0 dB	–33	–29	–25	dB
		f = 300 Hz	K1 × –0.26 dB	–4	–2	–1	
		f = 450 Hz to 9300 Hz	K1 × 0 dB	–0.25	0	0.25	
		f = 9300 Hz to 9900 Hz	K1 × 0 dB	–0.3	0	0.3	
		f = 9900 Hz to 10950 Hz	K1 × 0 dB	–0.5	0	0.5	
		f = 11.4 kHz	K1 × 2.3 dB		–2	–0.5	
		f = 12 kHz	K1 × 2.7 dB		–16	–14	
		f ≥ 13.2 kHz	K1 × 3.2 dB			–40	
		f ≥ 15 kHz	K1 × 0 dB			–60	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF can result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 × [(SCF frequency – 432 kHz)/432 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

3.3.11 Receive and Transmit Channel Low-Pass Filter Transfer Function, SCF f_{clock} = 432 kHz (see Note 9)

PARAMETER	TEST CONDITION	FREQUENCY RANGE	ADJUSTMENT ADDEND‡	MIN	TYP†	MAX	UNIT
Filter gain	Input signal reference is 0 dB	f = 0 Hz to 9300 Hz	K1 × 0 dB	−0.25	0	0.25	dB
		f = 9300 Hz to 9900 Hz	K1 × 0 dB	−0.3	0	0.3	
		f = 9900 Hz to 10950 Hz	K1 × 0 dB	−0.5	0	0.5	
		f = 11.4 kHz	K1 × 2.3 dB	−5	−2	−0.5	
		f = 12 kHz	K1 × 2.7 dB		−16	−14	
		f ≥ 13.2 kHz	K1 × 3.2 dB			−40	
		f ≥ 15 kHz	K1 × 0 dB			−60	

† All typical values are at T_A = 25°C.

‡ The MIN, TYP, and MAX specifications are given for a 432-kHz SCF clock frequency. A slight error in the 432-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where K1 = 100 × [(SCF frequency – 432 kHz)/432 kHz]. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 450 Hz to 10.95 kHz and 0 to 10.95 kHz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 432 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 432 kHz.

3.4 Operating Characteristics Over Recommended Operating Free-Air Temperature Range, V_{CC+} = 5 V, V_{CC-} = −5 V, V_{DD} = 5 V

3.4.1 Receive and Transmit Noise (Measurement Includes Low-Pass and Band-Pass Switched-Capacitor Filters)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Transmit noise	broadband with (sin x)/x	DX = input = 00000000000000, constant input code		280	500	μV rms
	broadband without (sin x)/x			250	450	
	0 to 12 kHz with (sin x)/x			250	400	
	0 to 12 kHz without (sin x)/x			240	400	
Receive noise (see Note 10)		Inputs grounded, gain = 1		300	500	μV rms
				18		dBrnc0

† All typical values are at T_A = 25°C.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

3.5 Timing Requirements

3.5.1 Serial Port Recommended Input Signals

PARAMETER		MIN	MAX	UNIT
$t_{c(MCLK)}$	Master clock cycle time	95		ns
$t_{r(MCLK)}$	Master clock rise time		10	ns
$t_{f(MCLK)}$	Master clock fall time		10	ns
	Master clock duty cycle	25%	75%	
	$\overline{\text{RESET}}$ pulse duration (see Note 11)	800		ns
$t_{su(DX)}$	DX setup time before SCLK↓	20		ns
$t_{h(DX)}$	DX hold time after SCLK↓	$t_{c(SCLK)}/4$		ns

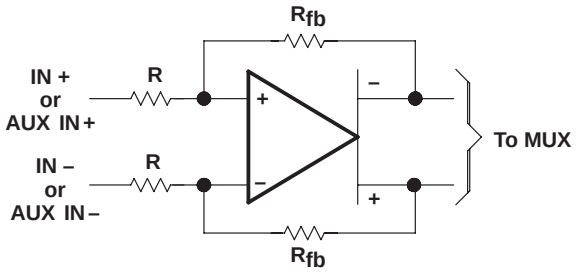
NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

3.5.2 Serial Port – AIC Output Signals, C_L = 30 pF for SHIFT CLK Output, C_L = 15 pF For All Other Outputs

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{c(SCLK)}$	Shift clock (SCLK) cycle time	380			ns
$t_{f(SCLK)}$	Shift clock (SCLK) fall time		3	8	ns
$t_{r(SCLK)}$	Shift clock (SCLK) rise time		3	8	ns
	Shift clock (SCLK) duty cycle	45		55	%
$t_{d(CH-FL)}$	Delay from SCLK↑ to $\overline{\text{FSR}}$/$\overline{\text{FSX}}$/$\overline{\text{FSD}}$↓		30		ns
$t_{d(CH-FH)}$	Delay from SCLK↑ to $\overline{\text{FSR}}$/$\overline{\text{FSX}}$/$\overline{\text{FSD}}$↑		35	90	ns
$t_{d(CH-DR)}$	DR valid after SCLK↑			90	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↓ in word mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↑ in word mode			90	ns
$t_{f(EODX)}$	$\overline{\text{EODX}}$ fall time		2	8	ns
$t_{f(EODR)}$	$\overline{\text{EODR}}$ fall time		2	8	ns
$t_{d(CH-EL)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↓ in byte mode			90	ns
$t_{d(CH-EH)}$	Delay from SCLK↑ to $\overline{\text{EODX}}$/$\overline{\text{EODR}}$↑ in byte mode			90	ns
$t_{d(MH-SL)}$	Delay from MSTR CLK↑ to SCLK↓		65	170	ns
$t_{d(MH-SH)}$	Delay from MSTR CLK↑ to SCLK↑		65	170	ns

† Typical values are at T_A = 25°C.

4 Parameter Measurement Information



R_{fb} = R for D6 = 1 and D7 = 1
D6 = 0 and D7 = 0
R_{fb} = 2R for D6 = 1 and D7 = 0
R_{fb} = 4R for D6 = 0, and D7 = 1

Figure 4–1. IN+ and IN– Gain Control Circuitry

Table 4–1. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)†

INPUT CONFIGURATIONS	CONTROL REGISTER BITS		ANALOG INPUT‡§	A/D CONVERSION RESULT
	D6	D7		
Differential configuration Analog input = IN+ – IN– = AUX IN+ – AUX IN–	1 0	1 0	V_{ID} = ±6 V	±full scale
	1	0	V_{ID} = ±3 V	±full scale
	0	1	V_{ID} = ±1.5 V	±full scale
Single-ended configuration Analog input = IN+ – ANLG GND = AUX IN+ – ANLG GND	1 0	1 0	V_I = ±3 V	±half scale
	1	0	V_I = ±3 V	±full scale
	0	1	V_I = ±1.5 V	±full scale

† V_{CC+} = 5 V, V_{CC-} = –5 V, V_{DD} = 5 V
‡ V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN– or AUX IN– connected to ground.
§ In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

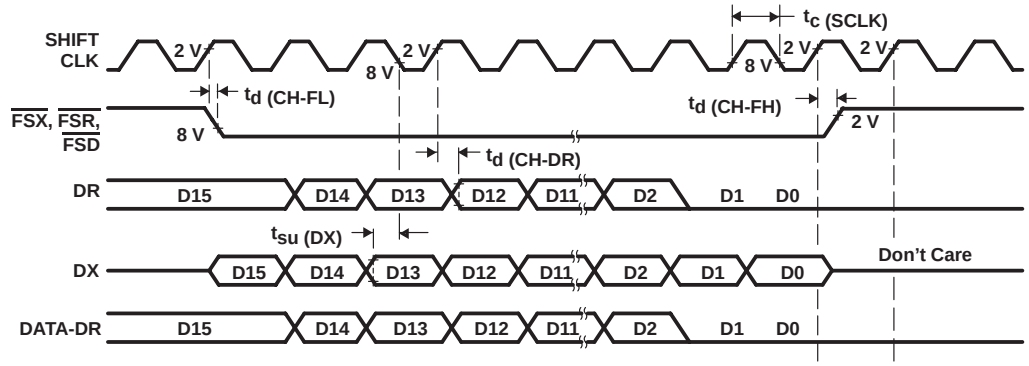


Figure 4–2. Dual-Word (Telephone Interface) Mode Timing

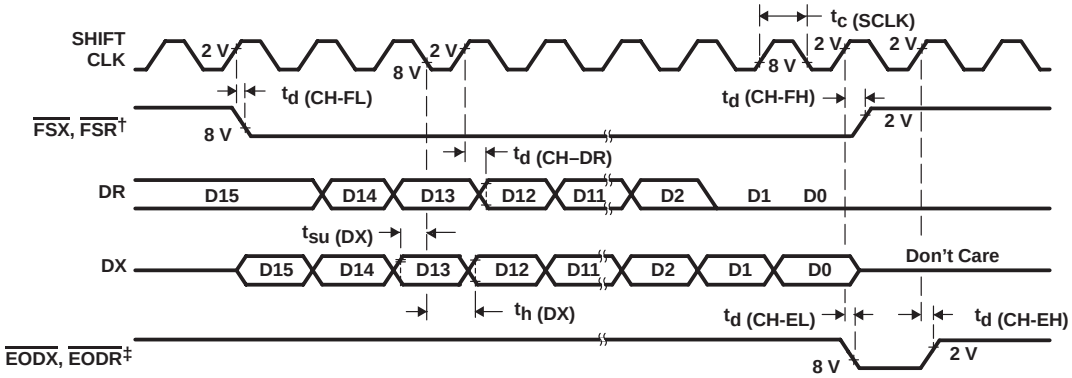


Figure 4–3. Word Timing

† The time between falling edges of $\overline{\text{FSR}}$ is the A/D conversion period and the time between falling edges of $\overline{\text{FSX}}$ is the D/A conversion period.

‡ In the word format, $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clocks wide, giving a four-clock period setup time between data words.

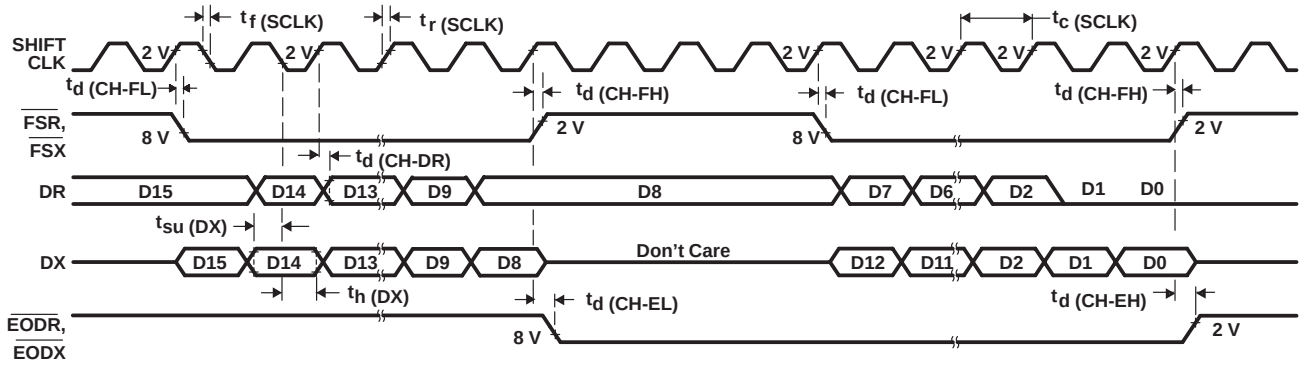


Figure 4–4. Byte-Mode Timing

†The time between falling edges of FSR is the A/D conversion period, and the time between fallling edges of $\overline{\text{FSX}}$ is the D/A conversion period.

‡In the byte mode, when $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clocks long, allowing for a four-shift-clock setup time between byte transmissions.

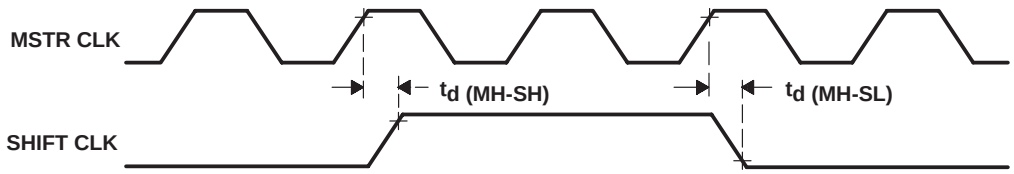


Figure 4–5. Shift-Clock Timing

4.1 TMS32047 – Processor Interface

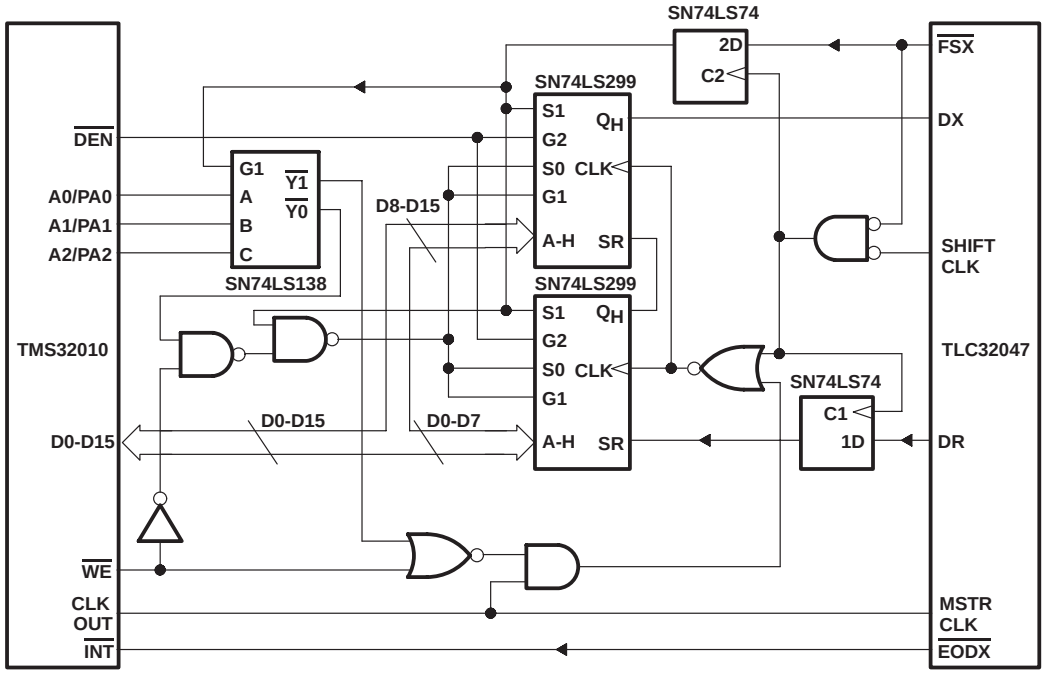
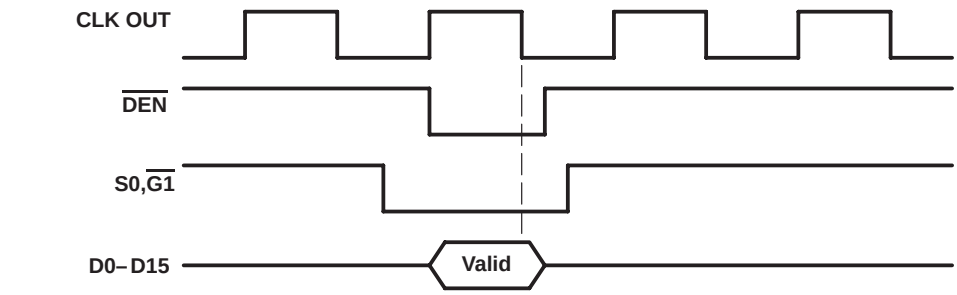
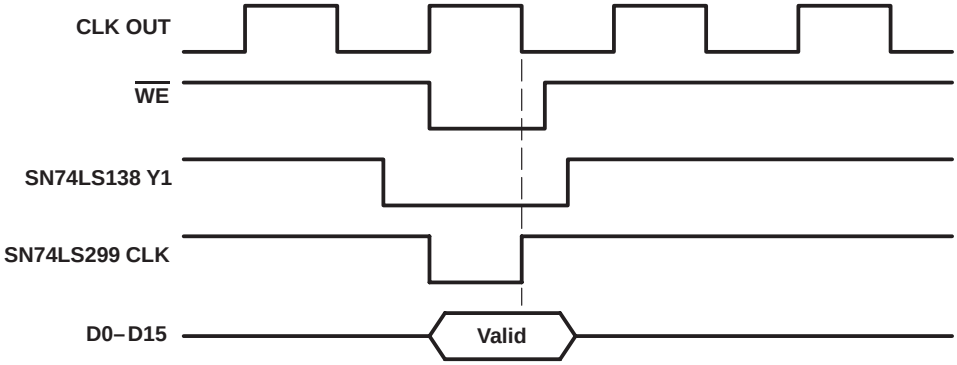


Figure 4–6. TMS32010/TMS320C15–TLC32047 Interface Circuit



(a) IN INSTRUCTION TIMING



(b) OUT INSTRUCTION TIMING

Figure 4–7. TMS32010/TMS320C15–TLC32047 Interface Timing

5 Typical Characteristics

D/A AND A/D LOW-PASS FILTER RESPONSE SIMULATION

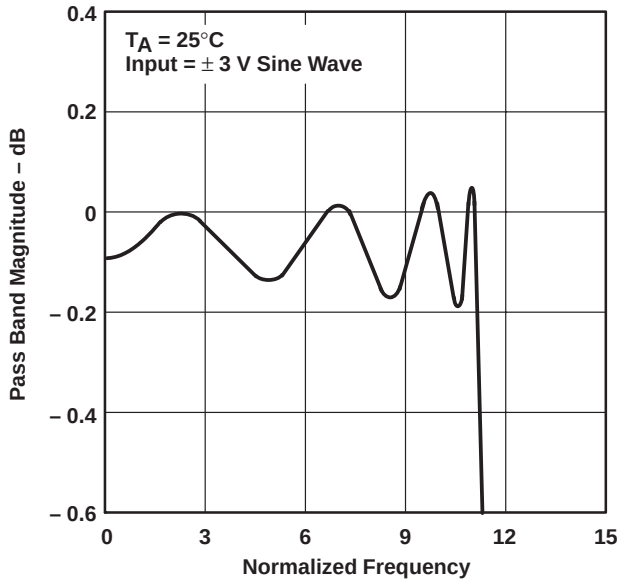


Figure 5–1

D/A AND A/D LOW-PASS FILTER RESPONSE SIMULATION

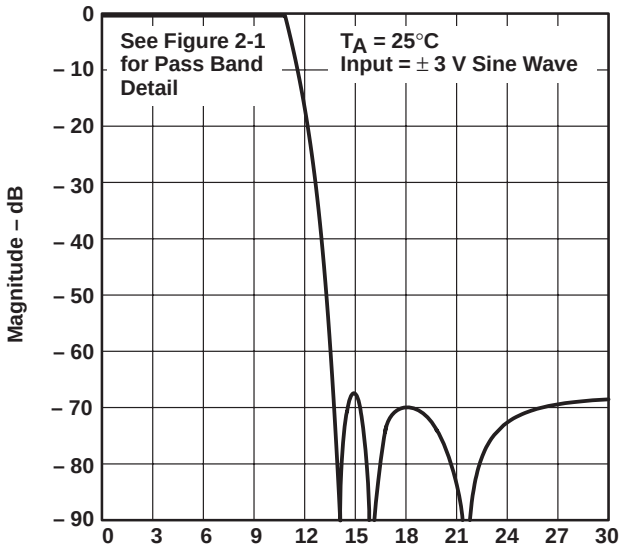


Figure 5–2

NOTE : Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

D/A AND A/D LOW-PASS GROUP DELAY

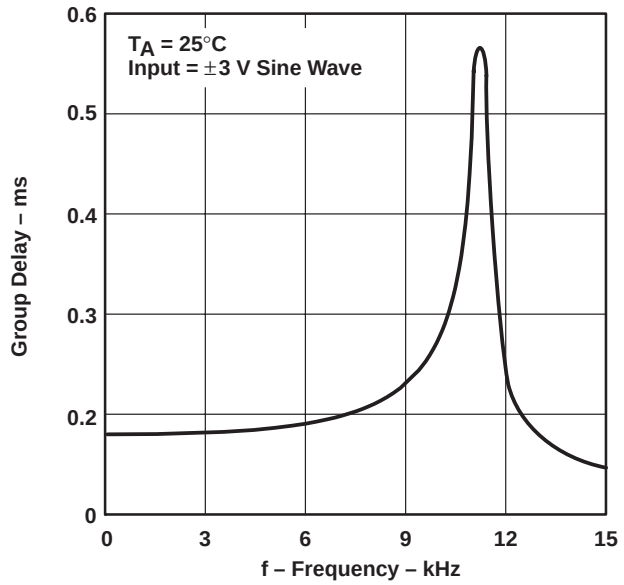


Figure 5–3

A/D BAND-PASS RESPONSE

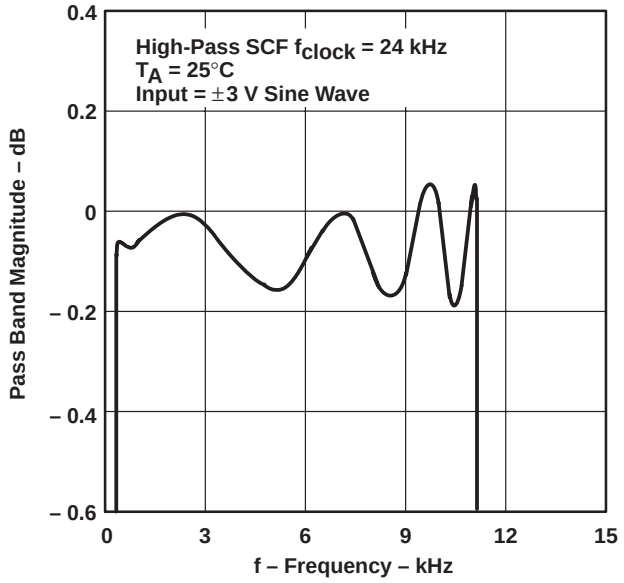


Figure 5–4

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$$

A/D BAND-PASS FILTER RESPONSE SIMULATION

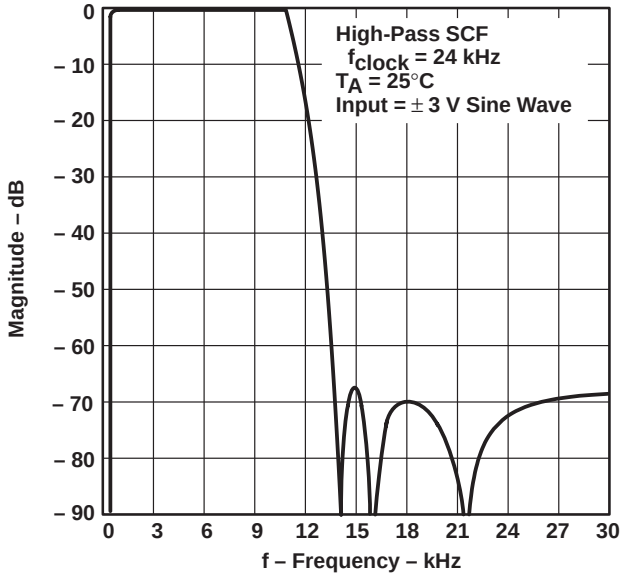


Figure 5–5

A/D BAND-PASS FILTER GROUP DELAY

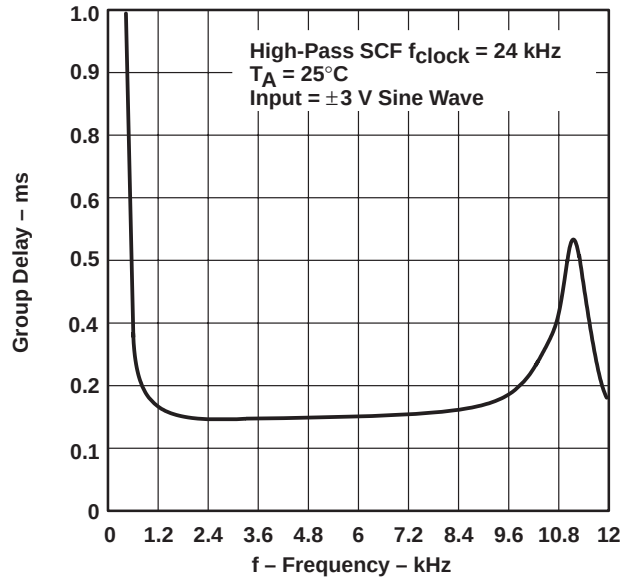


Figure 5–6

$$\text{NOTE : Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$$

A/D CHANNEL HIGH-PASS FILTER

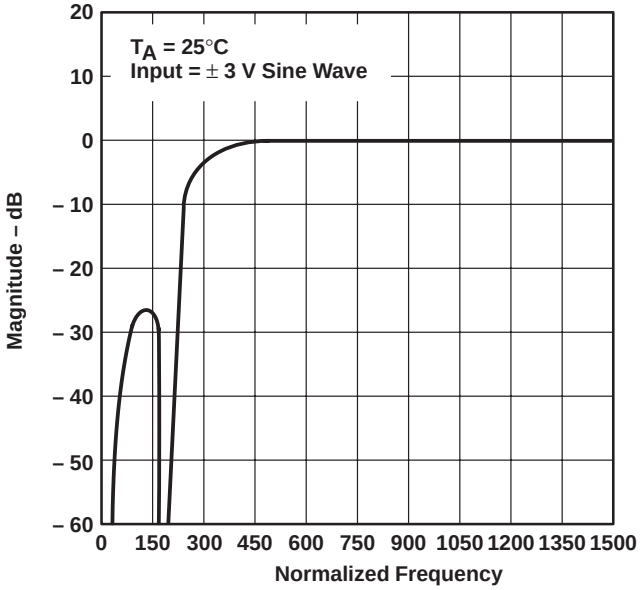


Figure 5–7

D/A (sin x)/x CORRECTION FILTER RESPONSE

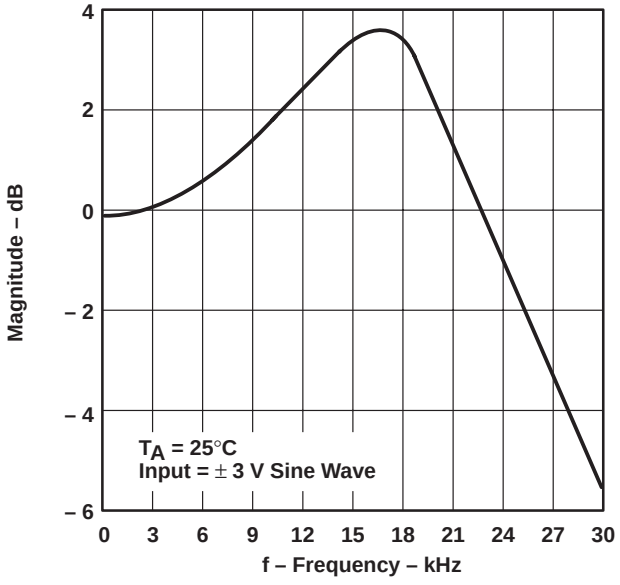


Figure 5–8

NOTE : Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

D/A (sin x)/x CORRECTION FILTER RESPONSE

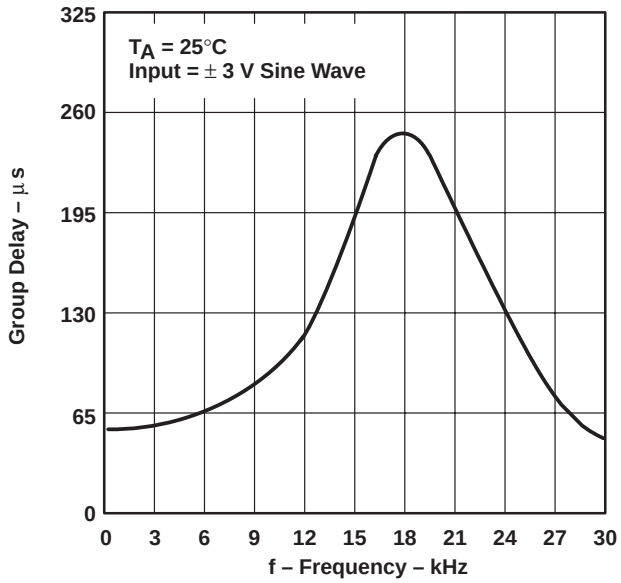


Figure 5–9

D/A (sin x)/x CORRECTION ERROR

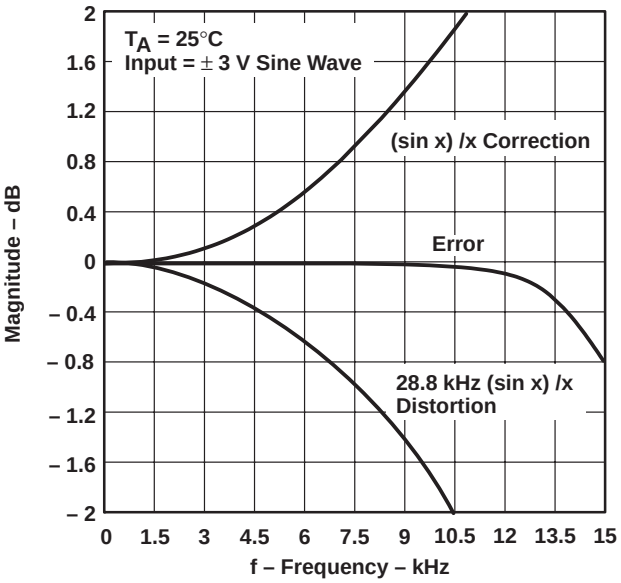


Figure 5–10

NOTE : Absolute Frequency (kHz) $= \dfrac{\text{Normalized Frequency} \times \text{SCF } f_{clock} \text{ (kHz)}}{432}$

A/D BAND-PASS GROUP DELAY

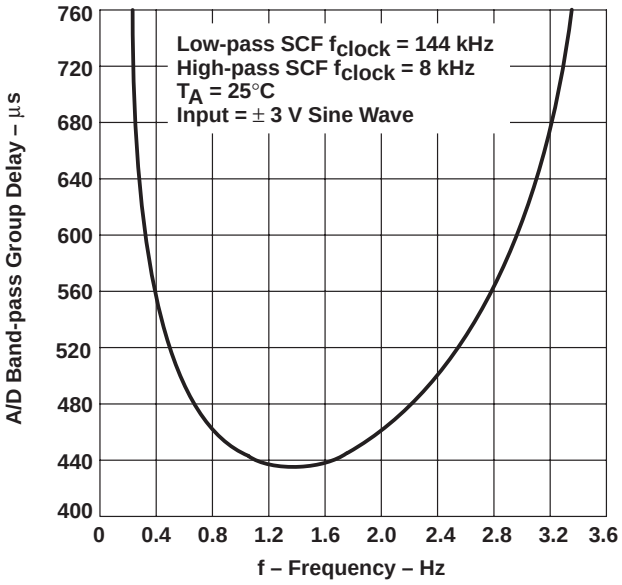


Figure 5–11

D/A LOW-PASS GROUP DELAY

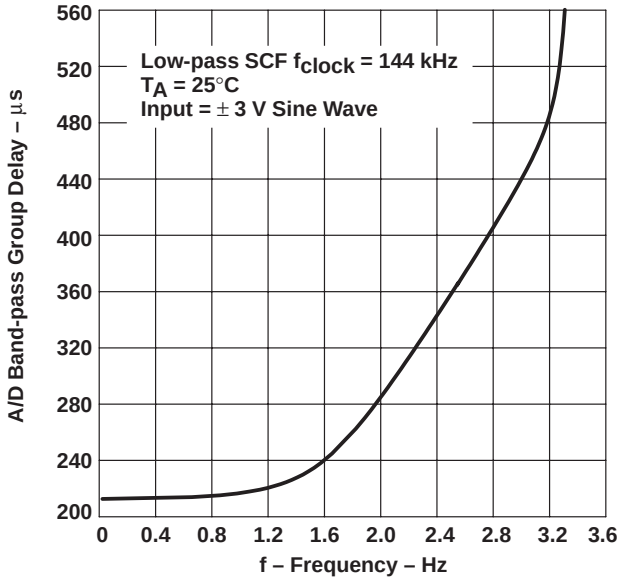


Figure 5–12

A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL

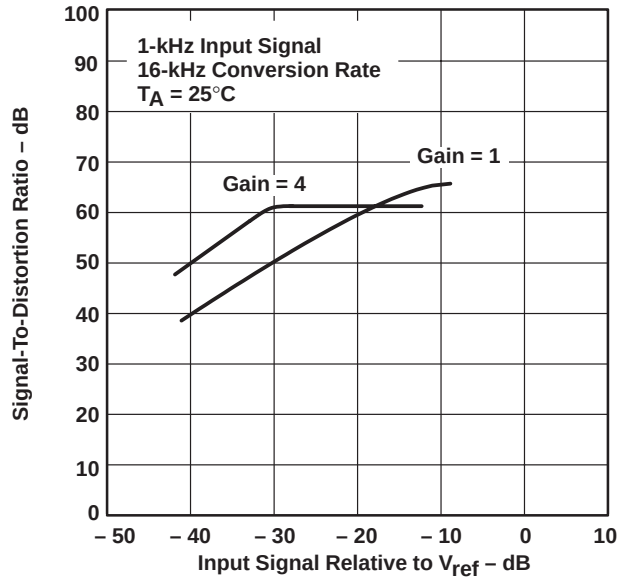


Figure 5–13

A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

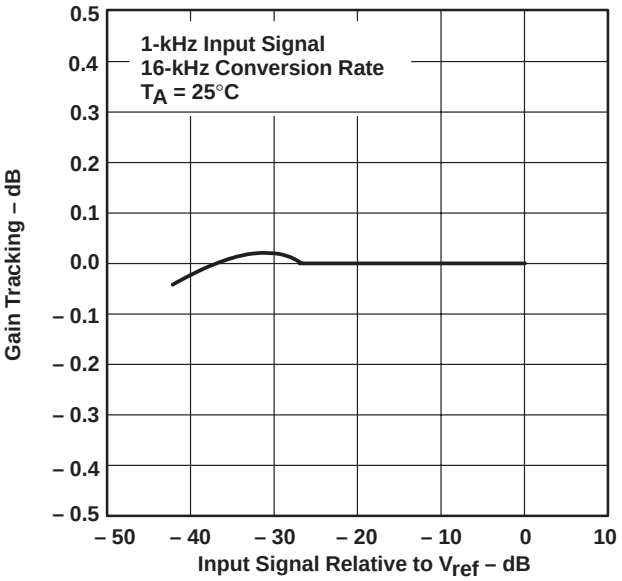


Figure 5–14

D/A CONVERTER SIGNAL-TO-DISTORTION RATIO vs INPUT SIGNAL

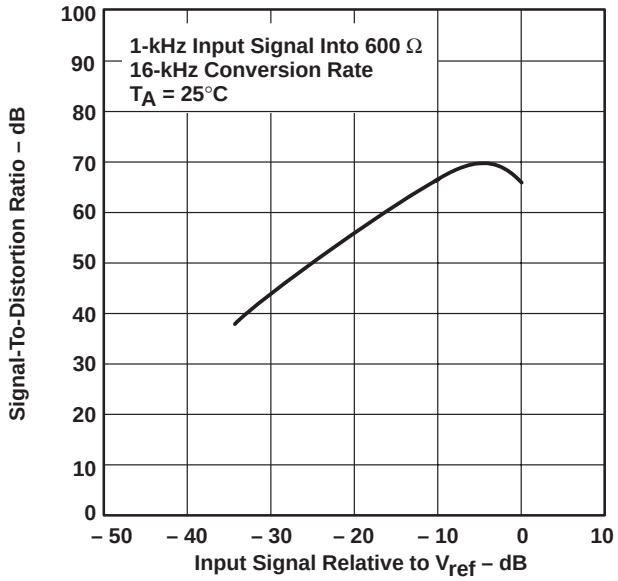


Figure 5–15

D/A GAIN TRACKING (GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)

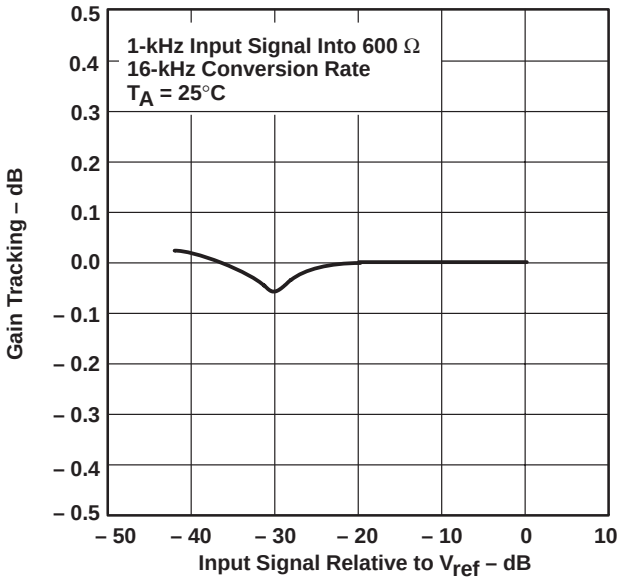


Figure 5–16

A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

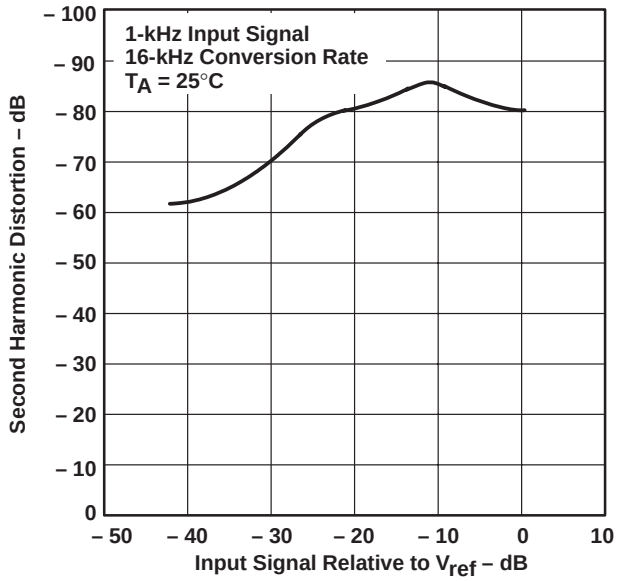


Figure 5–17

D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL

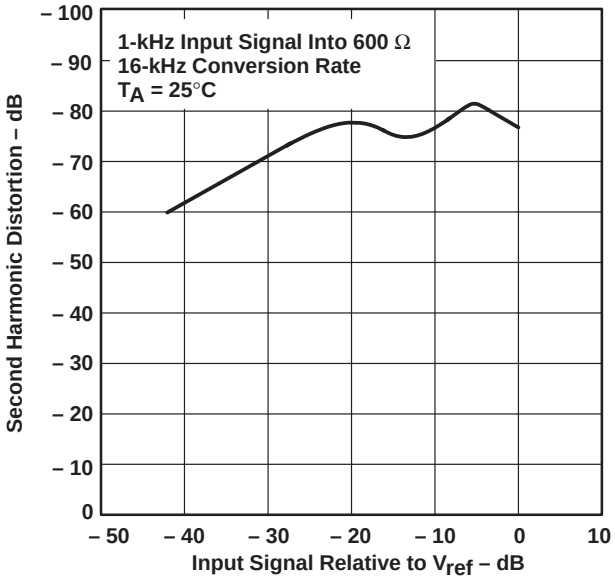


Figure 5–18

A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

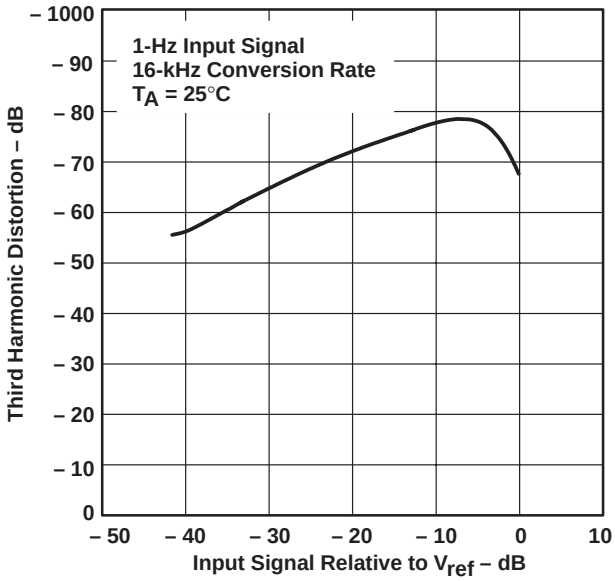


Figure 5–19

D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL

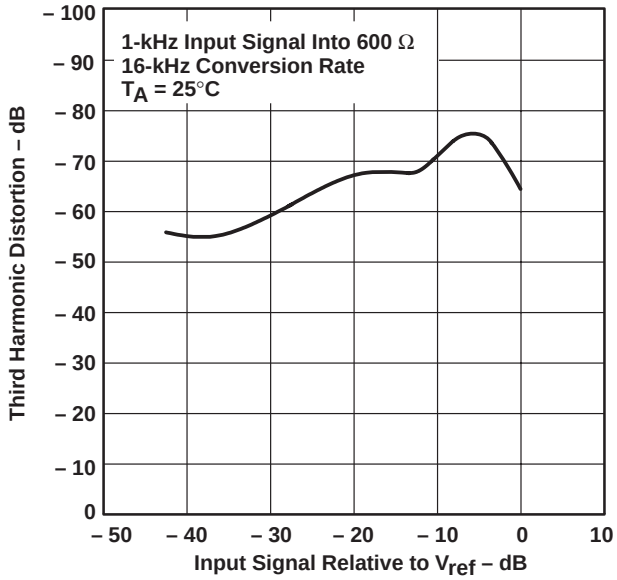


Figure 5–20

6 Application Information

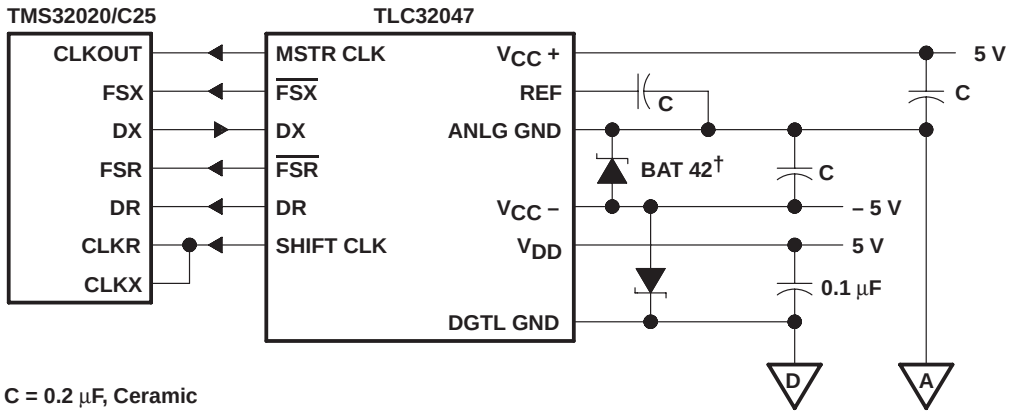


Figure 6–1. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors

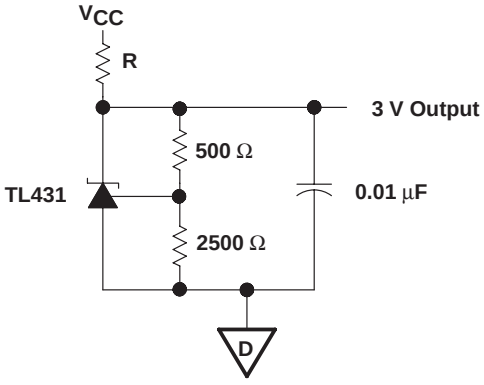


Figure 6–2. External Reference Circuit for TLC32047

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