TMP42x-Q1 ±1°C Remote and Local Temperature Sensor

1 Features

- AEC-Q100 Qualified with the Following Results
  - Temperature Grade 1: –40°C to +125°C
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- SOT23-8 Package
- ±1°C Remote Diode Sensor (Maximum)
- ±1.5°C Local Temperature Sensor (Maximum)
- Series Resistance Cancellation
- n-Factor Correction
- Two-Wire I^2C or SMBus™ Compatible Serial Interface
- Multiple Interface Addresses
- Diode Fault Detection
- RoHS Compliant and No Sb/Br

2 Applications

- Processor and FPGA Temperature Monitoring
- LCD, DLP, and LCOS Projectors
- Servers
- Central Office Telecom Equipment
- Storage Area Networks (SAN)

3 Description

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 devices are single, dual, and triple remote, automotive-qualified temperature sensor monitors with a built-in local temperature sensor. The remote temperature sensor diode-connected transistors are typically low-cost, NPN- or PNP-type transistors or diodes that are an integral part of microcontrollers, microprocessors, or field-programmable gate arrays (FPGAs).

Remote accuracy is ±1°C for multiple device manufacturers, with no calibration needed. The two-wire serial interface accepts SMBus write byte, read byte, send byte, and receive byte commands to configure the device.

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 include series resistance cancellation, programmable non-ideality factor, wide remote temperature measurement range (up to +150°C), and diode fault detection.

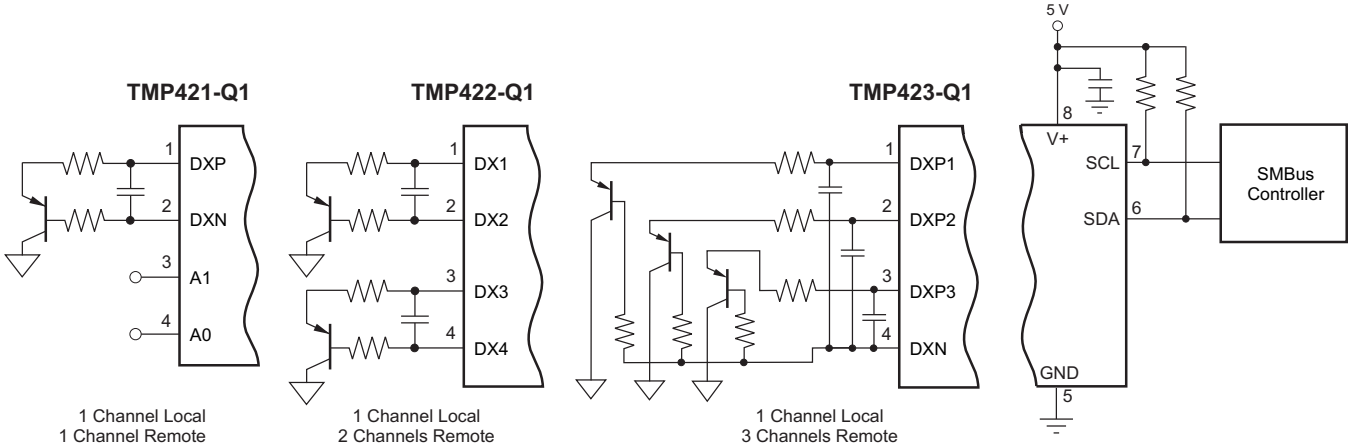
The TMP421-Q1, TMP422-Q1, and TMP423-Q1 are all available in an 8-pin SOT-23 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP421-Q1 TMP422-Q1 TMP423-Q1	SOT-23 (8)	2.90 mm × 1.63 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Diode Input Configurations for the TMP421-Q1, TMP422-Q1, and TMP423-Q1



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4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

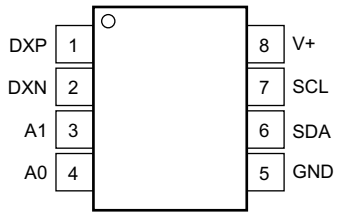
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5 Device Comparison Table

PART NUMBER	DESCRIPTION	TWO-WIRE ADDRESS
TMP421-Q1	Single-channel remote junction temperature sensor	100 11xx
TMP422-Q1	Dual-channel remote junction temperature sensor	100 11xx
TMP423-Q1	Triple-channel remote junction temperature sensor	100 1100

6 Pin Configuration and Functions

TMP421-Q1 DCN Package
8-Pin SOT-23
Top View

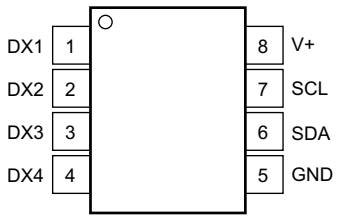


TMP421-Q1 Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DXP	Analog input	Positive connection to remote temperature sensor
2	DXN	Analog input	Negative connection to remote temperature sensor
3	A1	Digital input	Address pin
4	A0	Digital input	Address pin
5	GND	Ground	Ground
6	SDA	Bidirectional digital input-output	Serial data line for SMBus, open-drain; requires pullup resistor to V+
7	SCL	Digital input	Serial clock line for SMBus, open-drain; requires pullup resistor to V+
8	V+	Power supply	Positive supply voltage (2.7 V to 5.5 V for the TMP421-Q1)

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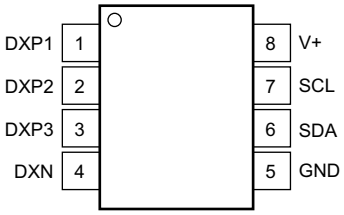
TMP422-Q1 DCN Package
8-Pin SOT-23
Top View



TMP422-Q1 Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DX1	Analog input	Channel 1 remote temperature sensor connection pin. Also sets the TMP422-Q1 address; see Table 4.
2	DX2	Analog input	Channel 1 remote temperature sensor connection pin. Also sets the TMP422-Q1 address; see Table 4.
3	DX3	Analog input	Channel 2 remote temperature sensor connection pin. Also sets the TMP422-Q1 address; see Table 4.
4	DX4	Analog input	Channel 2 remote temperature sensor connection pin. Also sets the TMP422-Q1 address; see Table 4.
5	GND	Ground	Ground
6	SDA	Bidirectional digital input-output	Serial data line for SMBus, open-drain; requires pullup resistor to V+.
7	SCL	Digital input	Serial clock line for SMBus, open-drain; requires pullup resistor to V+.
8	V+	Power supply	Positive supply voltage (2.7 V to 5.5 V).

TMP423-Q1 DCN Package
8-Pin SOT-23
Top View



TMP423-Q1 Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DXP1	Analog input	Channel 1 positive connection to remote temperature sensor
2	DXP2	Analog input	Channel 2 positive connection to remote temperature sensor
3	DXP3	Analog input	Channel 3 positive connection to remote temperature sensor
4	DXN	Analog input	Common negative connection to remote temperature sensors, channel 1, channel 2, and channel 3
5	GND	Ground	Ground
6	SDA	Bidirectional digital input-output	Serial data line for SMBus, open-drain; requires pullup resistor to V+
7	SCL	Digital input	Serial clock line for SMBus, open-drain; requires pullup resistor to V+
8	V+	Power supply	Positive supply voltage (2.7 V to 5.5 V)

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply, V_S			7	V
Input voltage	Pins 1, 2, 3, and 4 only	–0.5	V_S + 0.5	V
	Pins 6 and 7 only	–0.5	7	
Input current			10	mA
Operational temperature		–55	127	°C
Junction temperature, T_J max			150	°C
Storage temperature, T_{stg}		–60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±3000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Temperature	–40	125	°C
Power-supply voltage	2.7	5.5	V

7.4 Thermal Information

THERMAL METRIC(1)		TMP42x-Q1 DCN (SOT-23) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

at T_A = –40°C to +125°C and V+ = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE ERROR						
TE_{LOCAL}	Local temperature sensor	T_A = –40°C to +125°C	–2.5	±1.25	2.5	°C
		T_A = 15°C to 85°C, V+ = 3.3 V	–1.5	±0.25	1.5	
TE_{REMOTE}	Remote temperature sensor(1)	T_A = 15°C to 85°C, T_D = –40°C to +150°C, V+ = 3.3 V	–1	±0.25	1	°C
		T_A = –40°C to +100°C, T_D = –40°C to +150°C, V+ = 3.3 V	–3	±1	3	
		T_A = –40°C to +125°C, T_D = –40°C to +150°C	–5	±3	5	
PSS	Local and remote power-supply sensitivity	V+ = 2.7 V to 5.5 V	–0.5	±0.2	0.5	°C/V
TEMPERATURE MEASUREMENT						
	Conversion time (per channel)		100	115	130	ms
	Resolution	Local temperature sensor (programmable)		12		Bits
		Remote temperature sensor		12		
	Remote sensor source currents	High, series resistance = 3 kΩ maximum		120		µA
		Medium high		60		
		Medium low		12		
		Low		6		
η	Remote transistor ideality factor	TMP42x-Q1 optimized ideality factor		1.008		
SMBus INTERFACE						
V_{IH}	Logic input high voltage (SCL, SDA)		2.1			V
V_{IL}	Logic input low voltage (SCL, SDA)				0.8	V
	Hysteresis			500		mV
	SMBus output low sink current		6			mA
V_{OL}	SDA output low voltage	I_{OUT} = 6 mA		0.15	0.4	V
	Logic input current	0 ≤ V_{IN} ≤ 6 V	–1		1	µA
DIGITAL INPUTS						
	Input capacitance			3		pF
V_{IH}	Input logic high voltage		0.7(V+)		(V+)+0.5	V
V_{IL}	Input logic low voltage		–0.5		0.3(V+)	V
I_{IN}	Leakage input current	0 V ≤ V_{IN} ≤ V+			1	µA
POWER SUPPLY						
V+	Specified voltage range		2.7		5.5	V
I_Q	Quiescent current	0.0625 conversions per second		32	38	µA
		Eight conversions per second		400	525	µA
		Serial bus inactive, shutdown mode		3	10	µA
		Serial bus active, f_S = 400 kHz, shutdown mode		90		µA
		Serial bus active, f_S = 3.4 MHz, shutdown mode		350		µA
UVLO	Undervoltage lockout		2.3	2.4	2.6	V
POR	Power-on-reset threshold			1.6	2.3	V

(1) Tested with less than 5-Ω effective series resistance and 100-pF differential input capacitance.

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7.6 Timing Requirements

at –40°C to +125°C and V+ = 2.7 V to 5.5 V (unless otherwise noted); values are based on statistical analysis of samples tested during initial release

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.56	MHz
$t_{(BUF)}$	Bus free time between STOP and START condition	1300		160		ns
$t_{(HD;STA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SU;STA)}$	Repeated START condition setup time	600		160		ns
$t_{(SU;STO)}$	STOP condition setup time	600		160		ns
$t_{(HD;DAT)}$	Data hold time	25	See (1)	5	90	ns
$t_{(VD.DAT)}$	Data valid time (data response time) (2)		900	Not applicable		ns
$t_{(SU;DAT)}$	Data setup time	100		10		ns
$t_{(LOW)}$	SCL clock LOW period	1300		250		ns
$t_{(HIGH)}$	SCL clock HIGH period	600		60		ns
t_F – SDA	Data fall time		300		150	ns
t_F – SCL	Clock fall time		300		40	ns
t_R	Clock, data rise time		1000			ns
	Serial bus timeout	25	35	25	35	ms

(1) The maximum $t_{HD;DAT}$ can be 0.9 µs for Fast-Mode, and is less than the maximum $t_{VD;DAT}$ by a transition time.
(2) t_{VDDATA} = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

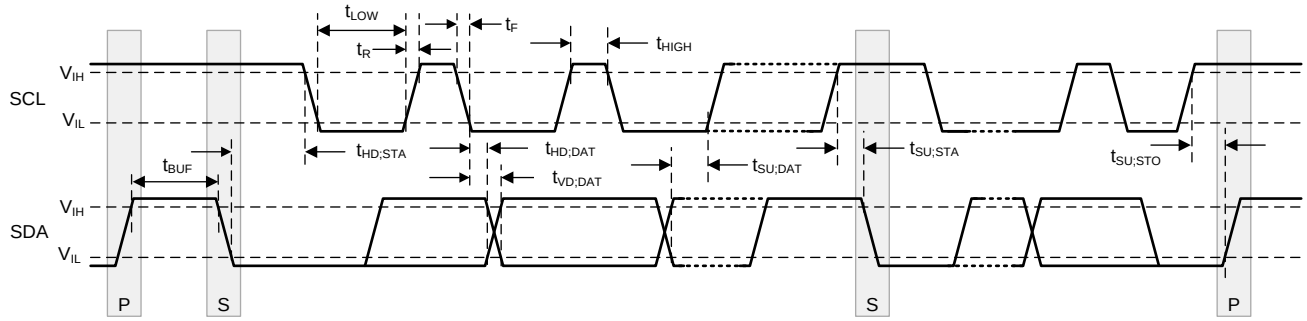


Figure 1. Two-Wire Timing Diagram

7.7 Typical Characteristics

at T_A = 25°C and V+ = 5 V (unless otherwise noted)

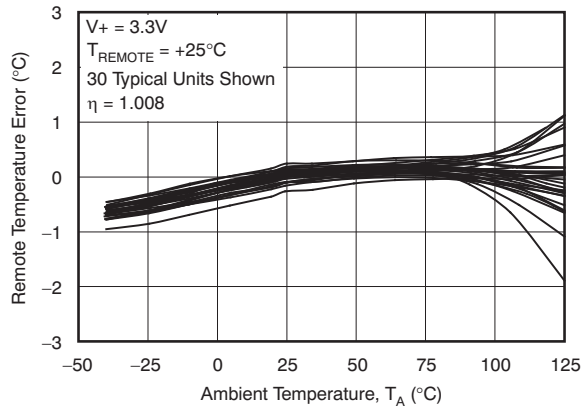


Figure 2. Remote Temperature Error vs Temperature

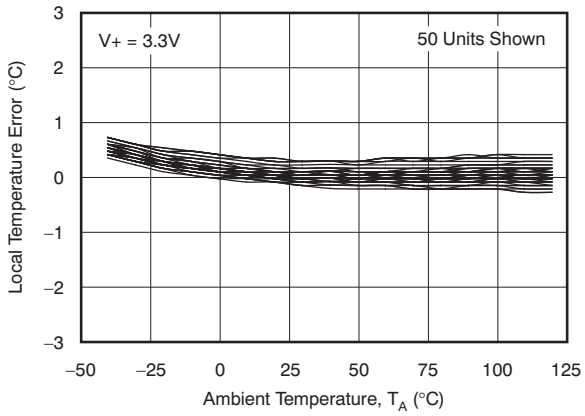


Figure 3. Local Temperature Error vs Temperature

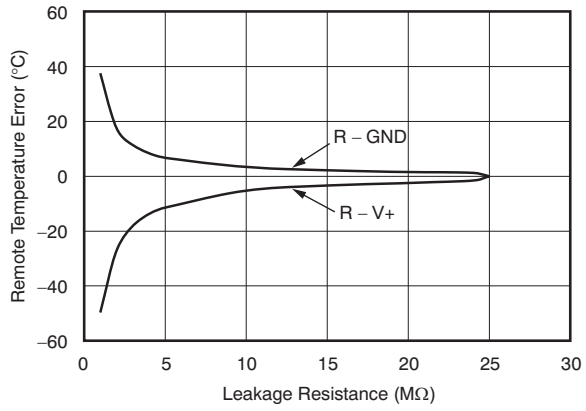


Figure 4. Remote Temperature Error vs Leakage Resistance

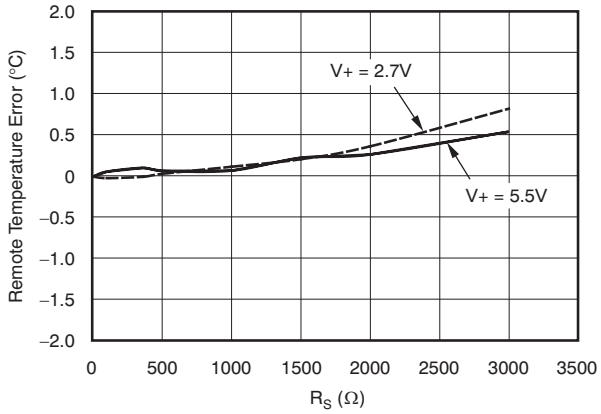


Figure 5. Remote Temperature Error vs Series Resistance (Diode-Connected Transistor, 2N3906 PNP)

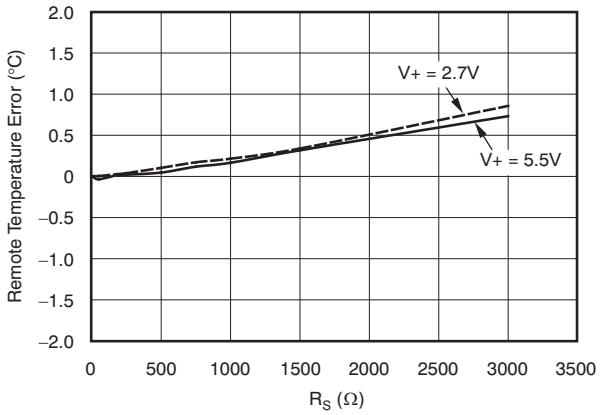


Figure 6. Remote Temperature Error vs Series Resistance (GND Collector-Connected Transistor, 2N3906 PNP)

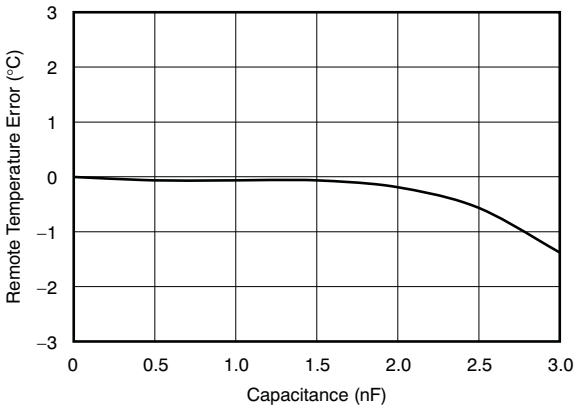


Figure 7. Remote Temperature Error vs Differential Capacitance

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Typical Characteristics (continued)

at T_A = 25°C and V+ = 5 V (unless otherwise noted)

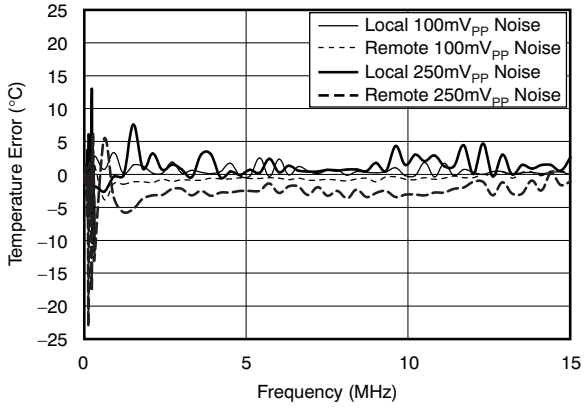


Figure 8. Temperature Error vs Power-Supply Noise Frequency

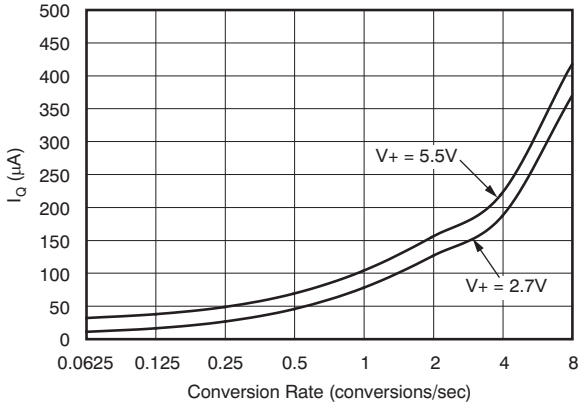


Figure 9. Quiescent Current vs Conversion Rate

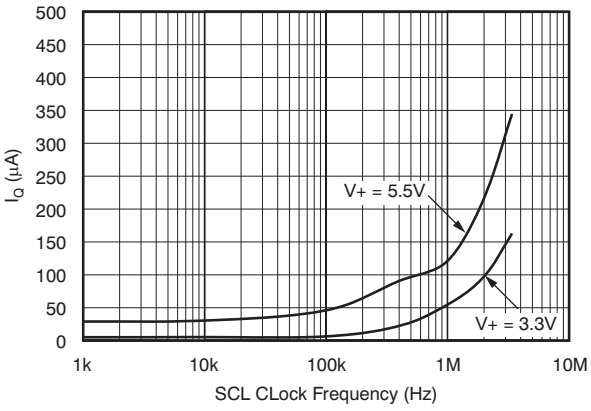


Figure 10. Shutdown Quiescent Current vs SCL Clock Frequency

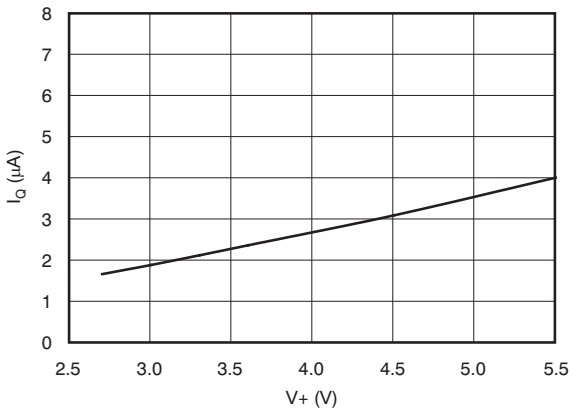


Figure 11. Shutdown Quiescent Current vs Supply Voltage

8 Detailed Description

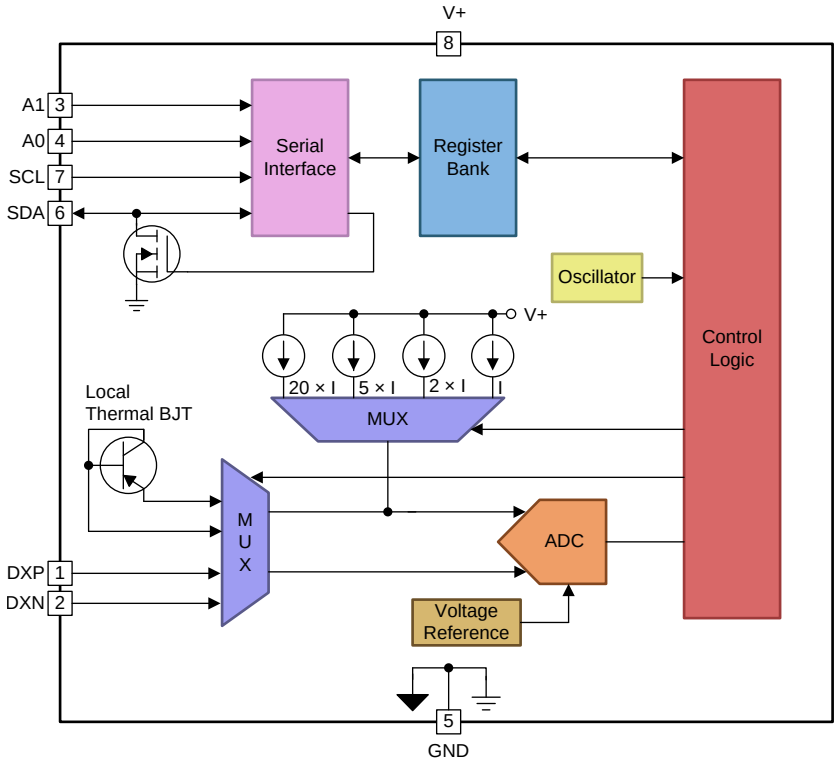
8.1 Overview

The TMP421-Q1 is a two-channel digital temperature sensor that combines a local die temperature-measurement channel and a remote-junction temperature-measurement channel, and is available in an 8-pin SOT-23 package. The TMP422-Q1 (three-channel), and TMP423-Q1 (four-channel) are digital temperature sensors that combine a local die temperature measurement channel and two or three remote junction temperature measurement channels, respectively, in a single 8-pin SOT-23 package. These devices are two-wire- and SMBus interface-compatible and are specified over a temperature range of –40°C to +125°C. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 each contain multiple registers for holding configuration information and temperature measurement results.

For proper remote temperature sensing operation, the TMP421-Q1 requires only a transistor connected between DXP and DXN pins. If the remote channel is not utilized, DXP can be left open or tied to GND.

The TMP422-Q1 requires transistors connected between DX1 and DX2 and between DX3 and DX4. Unused channels on the TMP422-Q1 must be connected to GND. The TMP423-Q1 requires a transistor connected to each positive channel (DXP1, DXP2, and DXP3), with the base of each channel tied to the common negative, DXN. For an unused channel, the TMP423-Q1 DXP pin can be left open or tied to GND.

8.2 Functional Block Diagram

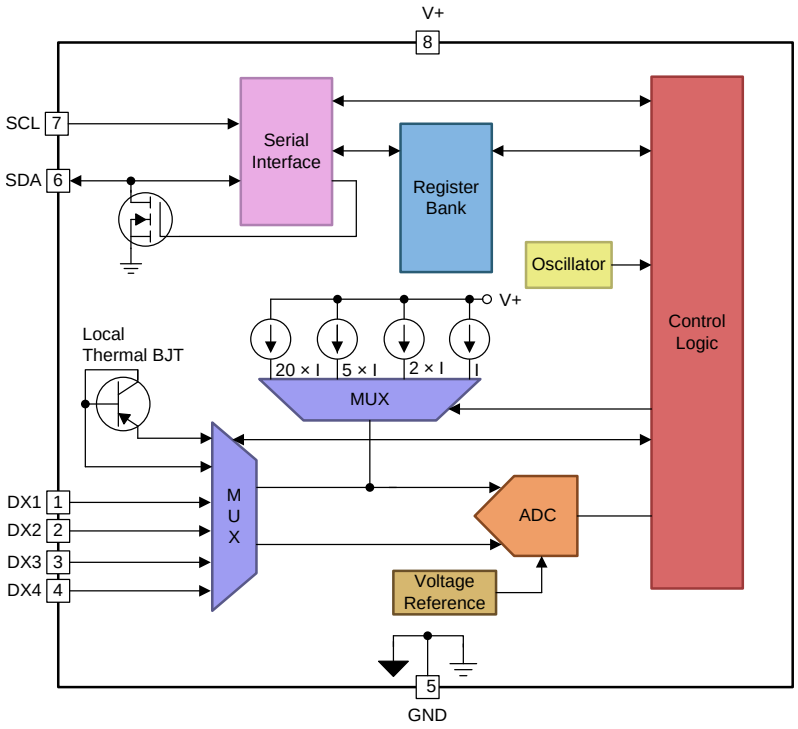


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Figure 12. The TMP421-Q1 Supports Multiple Slave Addresses and a Single Remote Diode Input

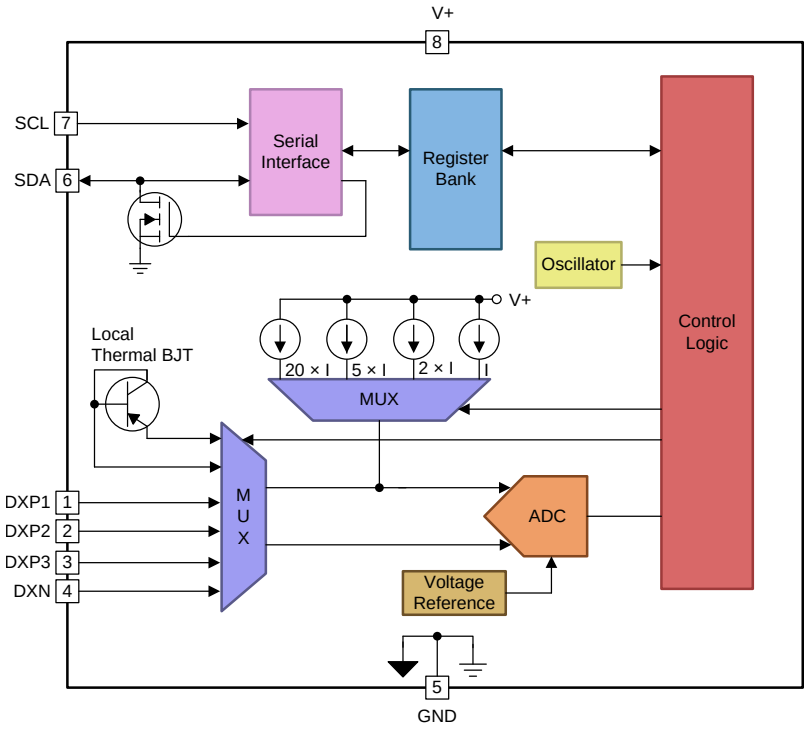
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Functional Block Diagram (continued)



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Figure 13. The TMP422-Q1 With Four Possible Remote Diode Inputs



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Figure 14. The TMP423-Q1 With Three Remote Diode Inputs

8.3 Feature Description

8.3.1 Temperature Measurement Data

Temperature measurement data can be taken over an operating range of –40°C to +127°C for both local and remote locations.

However, measurements from –55°C to +150°C can be made both locally and remotely by reconfiguring the TMP421-Q1, TMP422-Q1, and TMP423-Q1 for the extended temperature range, as described as follows.

Temperature data that result from conversions within the default measurement range are represented in binary form, as shown in Table 1, *2s Complement Standard Binary* column. Note that although the device is rated to only measure temperatures down to –55°C, the device can read temperatures below this level. However, any temperature below –64°C results in a data value of –64 (C0h). Likewise, temperatures above 127°C result in a value of 127 (7Fh). The device can be set to measure over an extended temperature range by changing bit 2 (RANGE) of Configuration Register 1 from low to high. The change in measurement range and data format from standard binary to extended binary occurs at the next temperature conversion. For data captured in the extended temperature range configuration, an offset of 64 (40h) is added to the standard binary value, as shown in the *Extended Binary* column of Table 1. This configuration allows measurement of temperatures as low as –64°C, and as high as 191°C; however, most temperature-sensing diodes only measure with the range of –55°C to +150°C. Additionally, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 are rated only for ambient temperatures ranging from –40°C to +125°C. Parameters in the *Absolute Maximum Ratings* table must be observed.

Table 1. Temperature Data Format (Local and Remote Temperature High Bytes)

TEMPERATURE (°C)	LOCAL/REMOTE TEMPERATURE REGISTER HIGH BYTE VALUE (1°C RESOLUTION)			
	2s COMPLEMENT STANDARD BINARY(1)		EXTENDED BINARY(2)	
	BINARY	HEX	BINARY	HEX
–64	1100 0000	C0	0000 0000	00
–50	1100 1110	CE	0000 1110	0E
–25	1110 0111	E7	0010 0111	27
0	0000 0000	00	0100 0000	40
1	0000 0001	01	0100 0001	41
5	0000 0101	05	0100 0101	45
10	0000 1010	0A	0100 1010	4A
25	0001 1001	19	0101 1001	59
50	0011 0010	32	0111 0010	72
75	0100 1011	4B	1000 1011	8B
100	0110 0100	64	1010 0100	A4
125	0111 1101	7D	1011 1101	BD
127	0111 1111	7F	1011 1111	BF
150	0111 1111	7F	1101 0110	D6
175	0111 1111	7F	1110 1111	EF
191	0111 1111	7F	1111 1111	FF

(1) Resolution is 1°C/count. Negative numbers are represented in 2s-complement format.
(2) Resolution is 1°C/count. All values are unsigned with a –64°C offset.

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Both local and remote temperature data use two bytes for data storage. The high byte stores the temperature with 1°C resolution. The second or low byte stores the decimal fraction value of the temperature and allows a higher measurement resolution, as shown in Table 2. The measurement resolution for the both the local and remote channels is 0.0625°C, and is not adjustable.

Table 2. Decimal Fraction Temperature Data Format (Local and Remote Temperature Low Bytes)

TEMPERATURE (°C)	TEMPERATURE REGISTER LOW BYTE VALUE (0.0625°C RESOLUTION)(1)	
	STANDARD AND EXTENDED BINARY	HEX
0	0000 0000	00
0.0625	0001 0000	10
0.1250	0010 0000	20
0.1875	0011 0000	30
0.2500	0100 0000	40
0.3125	0101 0000	50
0.3750	0110 0000	60
0.4375	0111 0000	70
0.5000	1000 0000	80
0.5625	1001 0000	90
0.6250	1010 0000	A0
0.6875	1011 0000	B0
0.7500	1100 0000	C0
0.8125	1101 0000	D0
0.8750	1110 0000	E0
0.9385	1111 0000	F0

(1) Resolution is 0.0625°C/count. All possible values are shown.

8.3.2 Remote Sensing

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 are designed to be used with either discrete transistors or substrate transistors built into processor chips and ASICs. Either NPN or PNP transistors can be used, as long as the base-emitter junction is used as the remote temperature sense. NPN transistors must be diode-connected. PNP transistors can either be transistor- or diode-connected (see Figure 20, Figure 21, and Figure 22).

8.3.3 Series Resistance Cancellation

Series resistance in an application circuit that typically results from printed circuit board (PCB) trace resistance and remote line length is automatically cancelled by the TMP421-Q1, TMP422-Q1, and TMP423-Q1, preventing what would otherwise result in a temperature offset. A total of up to 3 kΩ of series line resistance is cancelled by the TMP421-Q1, TMP422-Q1, and TMP423-Q1, eliminating the need for additional characterization and temperature offset correction. See the two *Remote Temperature Error vs Series Resistance* typical characteristic curves (Figure 5 and Figure 6) for details on the effects of series resistance and power-supply voltage on sensed remote temperature error.

8.3.4 Differential Input Capacitance

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 tolerate differential input capacitance of up to 1000 pF with minimal change in temperature error. The effect of capacitance on sensed remote temperature error is illustrated in Figure 7, *Remote Temperature Error vs Differential Capacitance*.

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8.3.5 Filtering

Remote junction temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals, and can corrupt measurements. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 have a built-in 65-kHz filter on the inputs of DXP and DXN (TMP421-Q1 and TMP423-Q1), or on the inputs of DX1 through DX4 (TMP422-Q1), to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor is recommended to make the application more robust against unwanted coupled signals. The value of this capacitor must be between 100 pF and 1 nF. Some applications attain better overall accuracy with additional series resistance; however, this increased accuracy is *application-specific*. When series resistance is added, the total value must not be greater than 3 kΩ. If filtering is needed, suggested component values are 100 pF and 50 Ω on each input; exact values are application-specific.

8.3.6 Sensor Fault

The TMP421-Q1 can sense a fault at the DXP input resulting from incorrect diode connection. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 can all sense an open circuit. Short-circuit conditions return a value of –64°C. The detection circuitry consists of a voltage comparator that trips when the voltage at DXP exceeds (V+) – 0.6V (typical). The comparator output is continuously checked during a conversion. If a fault is detected, the OPEN bit (bit 0) in the temperature result register is set to 1 and the rest of the register bits must be ignored.

When not using the remote sensor with the TMP421-Q1, the DXP and DXN inputs must be connected together to prevent meaningless fault warnings. When not using a remote sensor with the TMP422-Q1, connect the DX pins (see Table 4) such that DXP connections are grounded and DXN connections are left open (unconnected). Unused TMP423-Q1 DXP pins can be left open or connected to GND.

8.3.7 Undervoltage Lockout

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 sense when the power-supply voltage has reached a minimum voltage level for the ADC to function. The detection circuitry consists of a voltage comparator that enables the ADC after the power supply (V+) exceeds 2.45 V (typical). The comparator output is continuously checked during a conversion. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 do not perform a temperature conversion if the power supply is not valid. The PVLD bit (bit 1, see Table 6) of the individual Local/Remote Temperature Register is set to 1 and the temperature result may be incorrect.

8.3.8 Timeout Function

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 reset the serial interface if the SCL or SDA lines are held low for 30 ms (typical) between a START and STOP condition. If the TMP421-Q1, TMP422-Q1, and TMP423-Q1 are holding the bus low, the device releases the bus and waits for a START condition. To avoid activating the timeout function, a communication speed of at least 1 kHz must be maintained for the SCL operating frequency.

8.4 Device Functional Modes

8.4.1 Shutdown Mode (SD)

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 Shutdown Mode allows the user to save maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 3 μA; see Figure 11, *Shutdown Quiescent Current vs Supply Voltage*. Shutdown Mode is enabled when the SD bit (bit 6) of Configuration Register 1 is high; the device shuts down when the current conversion is completed. When SD is low, the device maintains a continuous conversion state.

8.5 Programming

8.5.1 Serial Interface

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 operate only as a slave device on the two-wire bus (I^2C or SMBus). Connections to either bus are made via the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 support the transmission protocol for fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted MSB first.

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Programming (continued)

8.5.2 Bus Overview

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 are SMBus or I^2C interface compatible. In SMBus protocol, the device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. START is indicated by pulling the data line (SDA) from a high-to-low logic level when SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer SDA must remain stable when SCL is high, because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the master generates a STOP condition. STOP is indicated by pulling SDA from low to high, when SCL is high.

8.5.3 Bus Definitions

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 are two-wire and SMBus-compatible. Figure 1 and Figure 15 to Figure 17 describe the timing for various operations on the TMP421-Q1, TMP422-Q1, and TMP423-Q1. Parameters for Figure 1 are defined in *Timing Requirements*. Bus definitions are:

Bus Idle Both SDA and SCL lines remain high.

Start Data Transfer A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer initiates with a START condition. Denoted as *S* in Figure 1.

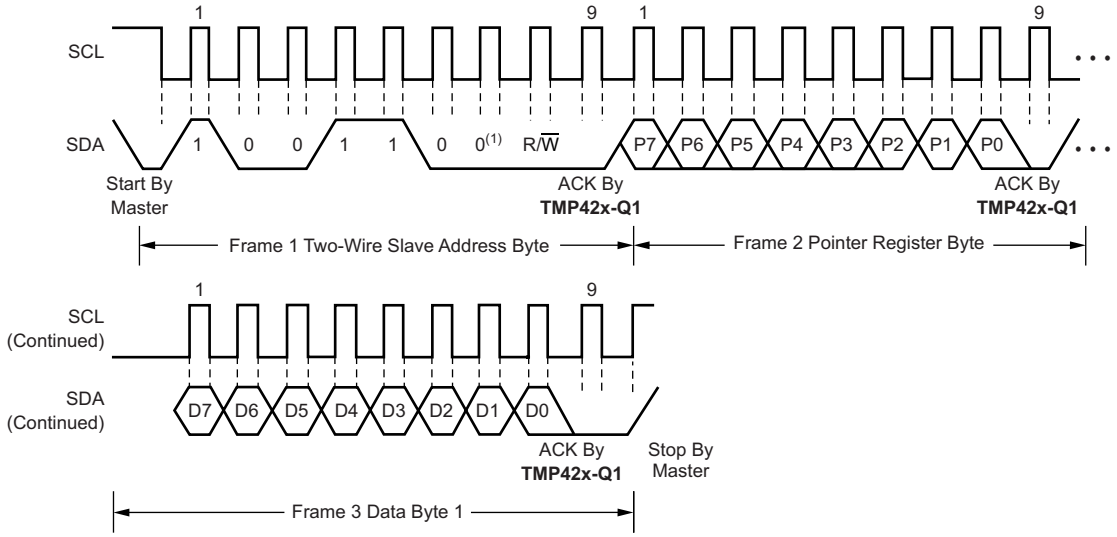
Stop Data Transfer A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer terminates with a repeated START or STOP condition. Denoted as *P* in Figure 1.

Data Transfer The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges data transfer.

Acknowledge Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, data transfer termination can be signaled by the master generating a Not-Acknowledge on the last byte transmitted by the slave.

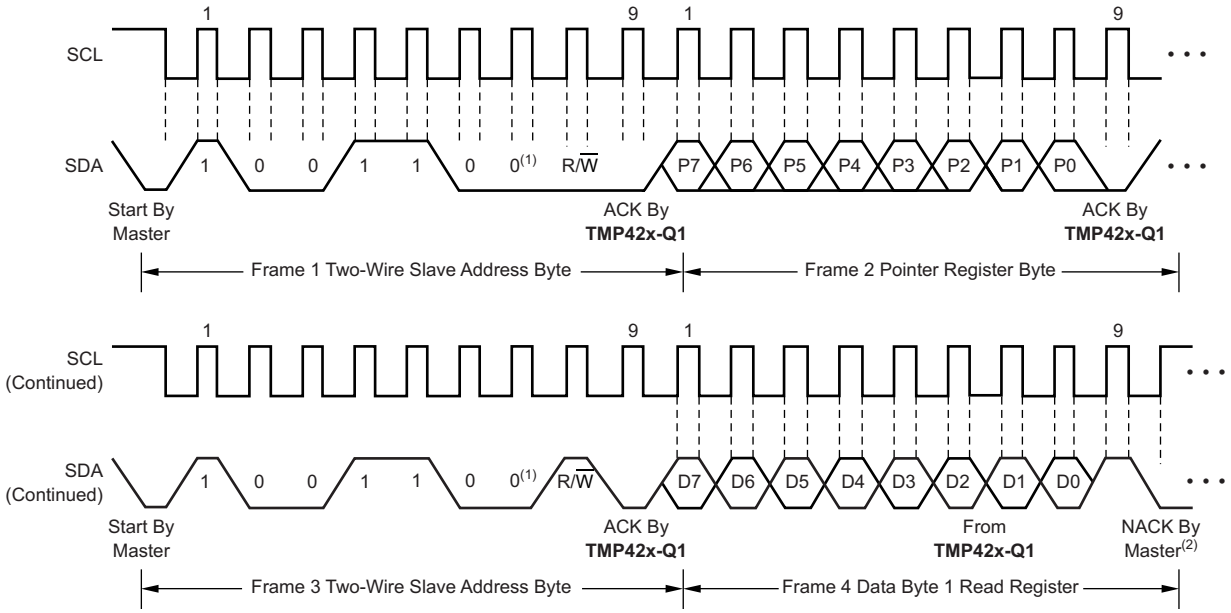
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Programming (continued)



(1) Slave address 1001100 shown.

Figure 15. Two-Wire Timing Diagram for Write Word Format



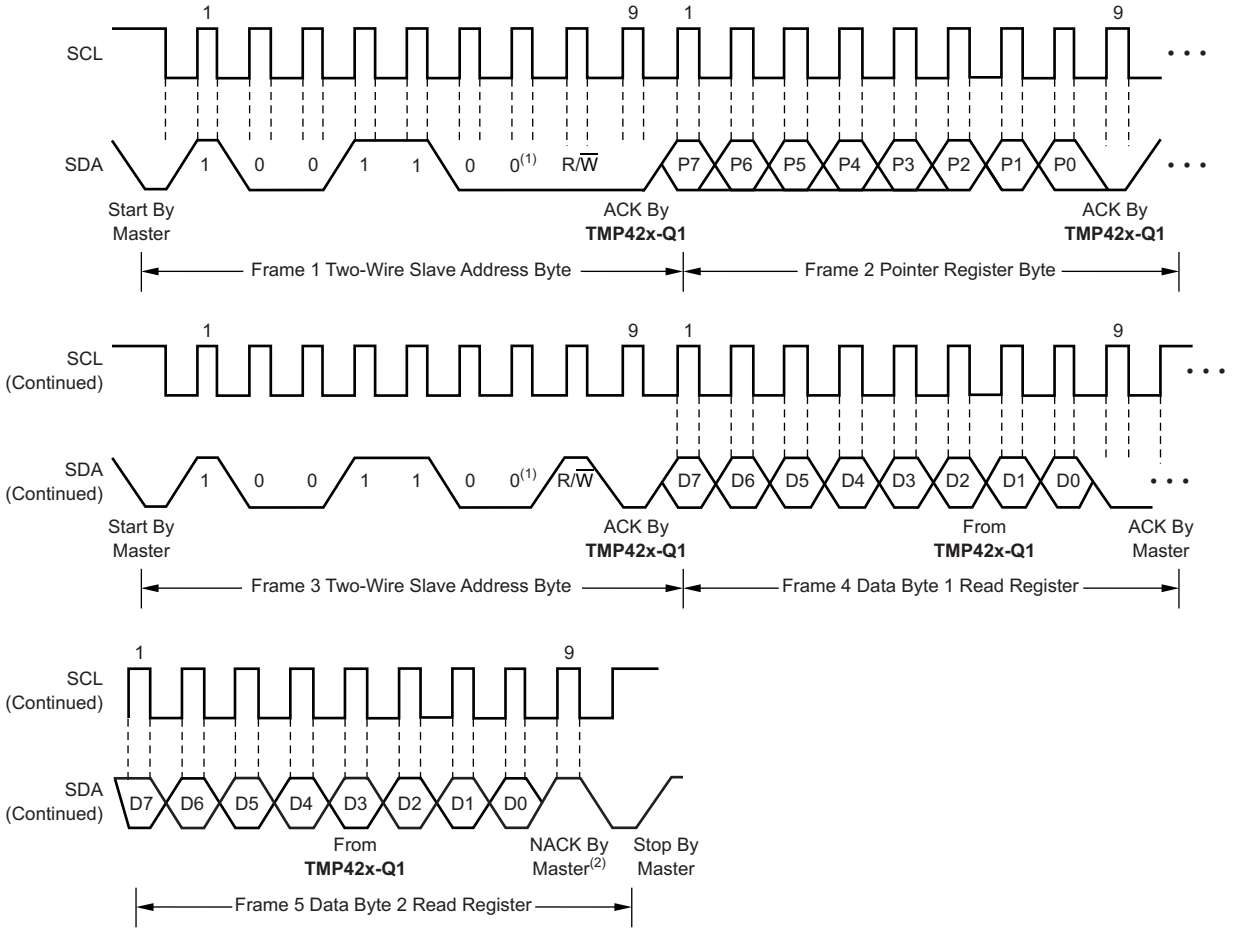
(1) Slave address 1001100 shown.

(2) The master must leave the SDA high to terminate a single-byte read operation.

Figure 16. Two-Wire Timing Diagram for Single-Byte Read Format

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Programming (continued)



(1) Slave address 1001100 shown.

(2) The master must leave the SDA high to terminate a two-byte read operation.

Figure 17. Two-Wire Timing Diagram for Two-Byte Read Format

8.5.4 Serial Bus Address

To communicate with the TMP421-Q1, TMP422-Q1, and TMP423-Q1, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

8.5.5 Two-Wire Interface Slave Device Addresses

The TMP421-Q1 supports nine slave device addresses and the TMP422-Q1 supports four slave device addresses. The TMP423-Q1 has one of two factory-preset slave addresses.

The slave device address for the TMP421-Q1 is set by the A1 and A0 pins according to Table 3.

The slave device address for the TMP422-Q1 is set by the connections between the external transistors and the TMP422-Q1 according to Figure 18 and Table 4. If one of the channels is unused, the respective DXP connection must be connected to GND, and the DXN connection must be left unconnected. The polarity of the transistor for external channel 2 (pins 3 and 4) sets the least significant bit of the slave address. The polarity of the transistor for external channel 1 (pins 1 and 2) sets the next least significant bit of the slave address.

Programming (continued)

Table 3. TMP421-Q1 Slave Address Options

TWO-WIRE SLAVE ADDRESS	A1	A0
0011 100	Float	0
0011 101	Float	1
0011 110	0	Float
0011 111	1	Float
0101 010	Float	Float
1001 100	0	0
1001 101	0	1
1001 110	1	0
1001 111	1	1

Table 4. TMP422-Q1 Slave Address Options

TWO-WIRE SLAVE ADDRESS	DX1	DX2	DX3	DX4
1001 100	DXP1	DXN1	DXP2	DXN2
1001 101	DXP1	DXN1	DXN2	DXP2
1001 110	DXN1	DXP1	DXP2	DXN2
1001 111	DXN1	DXP1	DXN2	DXP2

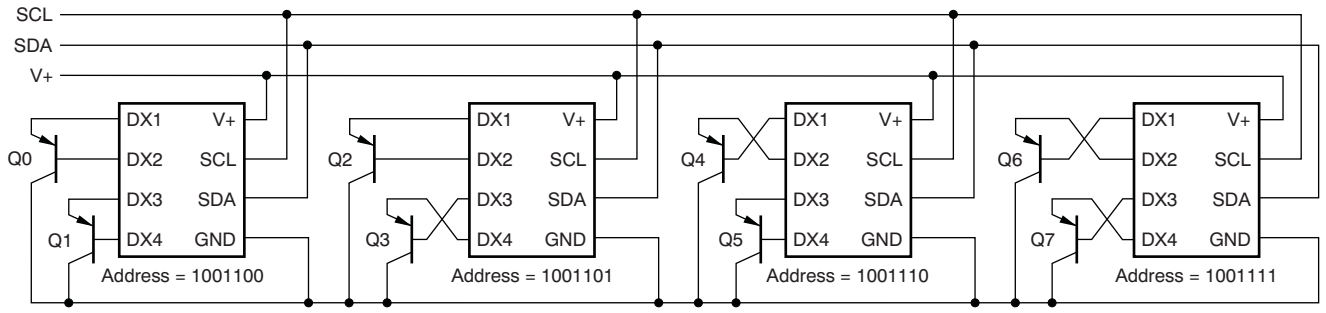


Figure 18. TMP422-Q1 Connections for Device Address Setup

The TMP422-Q1 checks the polarity of the external transistor at power-on, or after software reset, by forcing current to pin 1 when connecting pin 2 to approximately 0.6 V. If the voltage on pin 1 does not pull up to near the V+ of the TMP422-Q1, pin 1 functions as DXP for channel 1, and the second LSB of the slave address is 0. If the voltage on pin 1 does pull up to near V+, the TMP422-Q1 forces current to pin 2 when connecting pin 1 to 0.6 V. If the voltage on pin 2 does not pull up to near V+, the TMP422-Q1 uses pin 2 for the DXP of channel 1, and sets the second LSB of the slave address to 1. If both pins are shorted to GND or if both pins are open, the TMP422-Q1 uses pin 1 as the DXP and sets the address bit to 0. This process is then repeated for channel 2 (pins 3 and 4).

If the TMP422-Q1 is to be used with transistors that are located on another device (such as a CPU, DSP, or graphics processor), Pin 1 or pin 3 are recommended to be used as the DXP to ensure correct address detection. If the other device has a lower supply voltage or is not powered when the TMP422-Q1 tries to detect the slave address, a protection diode can turn on during the detection process and the TMP422-Q1 can incorrectly choose the DXP pin and corresponding slave address. Using pin 1 or pin 3 for transistors that are on other devices ensures the correct operation independent of supply sequencing or levels.

The TMP423-Q1 has a factory-preset slave address. The TMP423A-Q1 slave address is 1001100b, and the TMP423B-Q1 slave address is 1001101b. The configuration of the DXP and DXN channels are independent of the address. Unused DXP channels can be left open or tied to GND.

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8.5.6 Read and Write Operations

Accessing a particular register on the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP421-Q1, TMP422-Q1, and TMP423-Q1 requires a value for the Pointer Register (see Figure 15).

When reading from the TMP421-Q1, TMP422-Q1, and TMP423-Q1, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change which register is read for a read operation, a new value must be written to the Pointer Register. This transaction is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer Register byte; no additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 17 for details of this sequence. If repeated reads from the same register are desired, the Pointer Register bytes do not have to be continually sent because the TMP421-Q1, TMP422-Q1, and TMP423-Q1 retain the Pointer Register value until that value is changed by the next write operation. Note that register bytes are sent MSB first, followed by the LSB.

Read operations must be terminated by issuing a Not-Acknowledge command at the end of the last byte to be read. For a single-byte operation, the master must leave the SDA line high during the Acknowledge time of the first byte that is read from the slave. For a two-byte read operation, the master must pull SDA low during the Acknowledge time of the first byte read, and must leave SDA high during the Acknowledge time of the second byte read from the slave.

8.5.7 High-Speed Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue a High-Speed mode (Hs-mode) master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 do not acknowledge this byte, but switch the input filters on SDA and SCL and the output filter on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 switch the input and output filters back to fast mode operation.

8.5.8 One-Shot Conversion

When the TMP421-Q1, TMP422-Q1, and TMP423-Q1 are in shutdown mode (SD = 1 in the Configuration Register 1), a single conversion is started on all enabled channels by writing any value to the One-Shot Start Register, pointer address 0Fh. This write operation starts one conversion; the TMP421-Q1, TMP422-Q1, and TMP423-Q1 return to shutdown mode when that conversion completes. The value of the data sent in the write command is irrelevant and is not stored by the TMP421-Q1, TMP422-Q1, and TMP423-Q1. When the TMP421-Q1, TMP422-Q1, and TMP423-Q1 are in shutdown mode, the conversion sequence currently in process must be completed before a one-shot command can be issued. One-shot commands issued during a conversion are ignored.

8.5.9 η-Factor Correction Register

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 allow for a different η-factor value to be used for converting remote channel measurements to temperature. The remote channel uses sequential current excitation to extract a differential V_{BE} voltage measurement to determine the temperature of the remote transistor. Equation 1 describes this voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{\eta k T}{q} \ln\left(\frac{I_2}{I_1}\right) \quad (1)$$

The value η in Equation 1 is a characteristic of the particular transistor used for the remote channel. The power-on reset value for the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is η = 1.008. The value in the η-Factor Correction Register can be used to adjust the effective η-factor according to Equation 2 and Equation 3.

$$\eta_{eff} = \left(\frac{1.008 \times 300}{300 - N_{ADJUST}}\right) \quad (2)$$

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$$N_{ADJUST} = 300 - \left(\frac{300 \times 1.008}{\eta_{eff}} \right) \quad (3)$$

The η-correction value must be stored in two's-complement format, yielding an effective data range from –128 to +127. The *n*-correction value can be written to and read from pointer address 21h. The η-correction value for the second remote channel (TMP422-Q1 and TMP423-Q1) can be written and read from pointer address 22h. The η-correction value for the third remote channel (TMP423-Q1 only) can be written to and read from pointer address 23h. The register power-on reset value is 00h, thus having no effect unless the register is written to.

8.5.10 Software Reset

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 can be reset by writing any value to the Software Reset Register (pointer address FCh). This action restores the power-on reset state to all of the TMP421-Q1, TMP422-Q1, and TMP423-Q1 registers as well as aborts any conversion in process. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 also support reset via the two-wire general call address (0000 0000). The *General Call Reset* section contains more information.

Table 5. η-Factor Range

N_{ADJUST}			η
BINARY	HEX	DECIMAL	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008
1111 1111	FF	–1	1.004651
1111 1110	FE	–2	1.001325
1111 1100	FC	–4	0.994737
1111 1010	FA	–6	0.988235
1111 1000	F8	–8	0.981818
1111 0110	F6	–10	0.975484
1000 0000	80	–128	0.706542

8.5.11 General Call Reset

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 support reset via the two-wire General Call address 00h (0000 0000b). The TMP421-Q1, TMP422-Q1, and TMP423-Q1 acknowledge the General Call address and respond to the second byte. If the second byte is 06h (0000 0110b), the TMP421-Q1, TMP422-Q1, and TMP423-Q1 execute a software reset. This software reset restores the power-on reset state to all TMP421-Q1, TMP422-Q1, and TMP423-Q1 registers, and aborts any conversion in progress. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 take no action in response to other values in the second byte.

8.5.12 Identification Registers

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 allow for the two-wire bus controller to query the device for manufacturer and device IDs to enable software identification of the device at the particular two-wire bus address. The manufacturer ID is obtained by reading from pointer address FEh. The device ID is obtained by reading from pointer address FFh. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 each return 55h for the manufacturer code. The TMP421-Q1 returns 21h for the device ID; the TMP422-Q1 returns 22h for the device ID; and the TMP423-Q1 returns 23h for the device ID. These registers are read-only.

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8.6 Register Maps

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 contain multiple registers for holding configuration information, temperature measurement results, and status information. These registers are described in Figure 19 and Table 6.

8.6.1 Pointer Register

Figure 19 shows the internal register structure of the TMP421-Q1, TMP422-Q1, and TMP423-Q1. The 8-bit Pointer Register is used to address a given data register. The Pointer Register identifies which of the data registers must respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the Pointer Register before executing a read command. Table 6 describes the pointer address of the TMP421-Q1, TMP422-Q1, and TMP423-Q1 registers. The power-on reset (POR) value of the Pointer Register is 00h (0000 0000b).

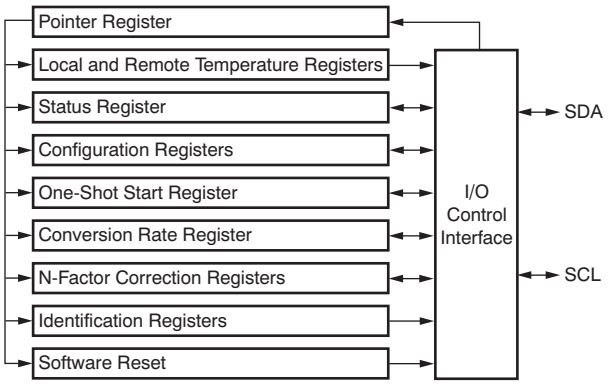


Figure 19. Internal Register Structure

Table 6. Register Map

POINTER (HEX)	POR (HEX)	BIT DESCRIPTION								REGISTER DESCRIPTION
		7	6	5	4	3	2	1	0	
00	00	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	Local Temperature (High Byte)(1)
01	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature 1 (High Byte)(1)
02	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature 2 (High Byte)(1) (2) (3)
03	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature 3 (High Byte)(1) (3)
08		BUSY	0	0	0	0	0	0	0	Status Register
09	00	0	SD	0	0	0	RANGE	0	0	Configuration Register 1
0A	1C/3C(2)/ 7C(3)	0	REN3(3)	REN2(2) (3)	REN	LEN	RC	0	0	Configuration Register 2
0B	07	0	0	0	0	0	R2	R1	R0	Conversion Rate Register
0F		X	X	X	X	X	X	X	X	One-Shot Start(4)
10	00	LT3	LT2	LT1	LT0	0	0	$\overline{\text{PVLD}}$	0	Local Temperature (Low Byte)
11	00	RT3	RT2	RT1	RT0	0	0	$\overline{\text{PVLD}}$	OPEN	Remote Temperature 1 (Low Byte)
12	00	RT3	RT2	RT1	RT0	0	0	$\overline{\text{PVLD}}$	OPEN	Remote Temperature 2 (Low Byte)(2) (3)
13	00	RT3	RT2	RT1	RT0	0	0	$\overline{\text{PLVD}}$	OPEN	Remote Temperature 3 (Low Byte)(3)
21	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N Correction 1
22	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N Correction 2(2) (3)
23	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N Correction 3(3)

(1) Compatible with Two-Byte Read; see Figure 17.
(2) TMP422-Q1.
(3) TMP423-Q1.
(4) X = undefined. Writing any value to this register initiates a one-shot start; see the *One-Shot Conversion* section.

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Register Maps (continued)

Table 6. Register Map (continued)

POINTER (HEX)	POR (HEX)	BIT DESCRIPTION								REGISTER DESCRIPTION
		7	6	5	4	3	2	1	0	
FC		X	X	X	X	X	X	X	X	Software Reset[5]
FE	55	0	1	0	1	0	1	0	1	Manufacturer ID
FF	21	0	0	1	0	0	0	0	1	TMP421-Q1 Device ID
		0	0	1	0	0	0	1	0	TMP422-Q1 Device ID
		0	0	1	0	0	0	1	1	TMP423-Q1 Device ID

(5) X = undefined. Writing any value to this register initiates a software reset; see the *Software Reset* section.

8.6.2 Temperature Registers

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 have multiple 8-bit registers that hold temperature measurement results. The local channel and each of the remote channels have a high byte register that contains the most significant bits (MSBs) of the temperature analog-to-digital converter (ADC) result and a low byte register that contains the least significant bits (LSBs) of the temperature ADC result. The local channel high byte address is 00h; the local channel low byte address is 10h. The remote channel high byte is at address 01h; the remote channel low byte address is 11h. For the TMP422-Q1, the second remote channel high byte address is 02h; the second remote channel low byte is 12h. The TMP 423 uses the same local and remote address as the TMP421-Q1 and TMP422-Q1, with the third remote channel high byte of 03h; the third remote channel low byte is 13h. These registers are read-only and are updated by the ADC each time a temperature measurement is completed.

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 contain circuitry to assure that a low byte register read command returns data from the same ADC conversion as the immediately preceding high byte read command. This assurance remains valid only until another register is read. For proper operation, the high byte of a temperature register must be read first. The low byte register must be read in the next read command. The low byte register can be left unread if the LSBs are not needed. Alternatively, the temperature registers can be read as a 16-bit register by using a single two-byte read command from address 00h for the local channel result, or from address 01h for the remote channel result (02h for the second remote channel result, and 03h for the third remote channel). The high byte is output first, followed by the low byte. Both bytes of this read operation are from the same ADC conversion. The power-on reset value of all temperature registers is 00h.

8.6.3 Status Register

The Status Register reports the state of the temperature ADCs. Table 7 summarizes the Status Register bits. The Status Register is read-only, and is read by accessing pointer address 08h.

The BUSY bit = 1 if the ADC is making a conversion; BUSY is set to 0 if the ADC is not converting.

Table 7. Status Register Format

STATUS REGISTER (READ = 08h, WRITE = NA)								
BIT #	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BUSY	0	0	0	0	0	0	0
POR VALUE	0[1]	0	0	0	0	0	0	0

(1) **FOR TMP421-Q1 AND TMP423-Q1:** BUSY changes to 1 almost immediately (< 100 μs) following power-up, when the TMP421-Q1 and TMP423-Q1 begin the first temperature conversion. BUSY is high whenever the TMP421-Q1 and TMP423-Q1 convert a temperature reading.
FOR TMP422-Q1: The BUSY bit changes to 1 approximately 1 ms following power-up. BUSY is high whenever the TMP422-Q1 converts a temperature reading.

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8.6.4 Configuration Register 1

Configuration Register 1 (pointer address 09h) sets the temperature range and controls the shutdown mode. The Configuration Register is set by writing to pointer address 09h and read by reading from pointer address 09h. Table 8 summarizes the bits of Configuration Register 1.

The shutdown (SD) bit (bit 6) enables or disables the temperature measurement circuitry. If SD = 0, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 convert continuously at the rate set in the conversion rate register. When SD is set to 1, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 stop converting when the current conversion sequence is complete and enter a shutdown mode. When SD is set to 0 again, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 resume continuous conversions. When SD = 1, a single conversion can be started by writing to the One-Shot Register. See the *One-Shot Conversion* section for more information.

The temperature range is set by configuring the RANGE bit (bit 2) of the Configuration Register. Setting this bit low configures the TMP421-Q1, TMP422-Q1, and TMP423-Q1 for the standard measurement range (–40°C to +127°C); temperature conversions are stored in the standard binary format. Setting bit 2 high configures the TMP421-Q1, TMP422-Q1, and TMP423-Q1 for the extended measurement range (–55°C to +150°C); temperature conversions are stored in the extended binary format (see Table 1).

The remaining bits of the Configuration Register are reserved and must always be set to 0. The power-on reset value for this register is 00h.

Table 8. Configuration Register 1 Bit Descriptions

CONFIGURATION REGISTER 1 (Read/Write = 09h, POR = 00h)			
BIT	**NAME**	**FUNCTION**	**POWER-ON RESET VALUE**
7	Reserved	—	0
6	SD	0 = Run 1 = Shut Down	0
5, 4, 3	Reserved	—	0
2	Temperature Range	0 = –40°C to +127°C 1 = –55°C to +150°C	0
1, 0	Reserved	—	0

8.6.5 Configuration Register 2

Configuration Register 2 (pointer address 0Ah) controls which temperature measurement channels are enabled and whether the external channels have the resistance correction feature enabled or disabled. Table 9 summarizes the bits of Configuration Register 2.

The RC bit (bit 2) enables the resistance correction feature for the external temperature channels. If RC = 1, series resistance correction is enabled; if RC = 0, resistance correction is disabled. Resistance correction must be enabled for most applications. However, disabling the resistance correction can yield slightly improved temperature measurement noise performance, and reduce conversion time by about 50%, which can lower power consumption when conversion rates of two per second or less are selected.

The LEN bit (bit 3) enables the local temperature measurement channel. If LEN = 1, the local channel is enabled; if LEN = 0, the local channel is disabled.

The REN bit (bit 4) enables external temperature measurement for channel 1. If REN = 1, the first external channel is enabled; if REN = 0, the external channel is disabled.

For the TMP422-Q1 and TMP423-Q1 only, the REN2 bit (bit 5) enables the second external measurement channel. If REN2 = 1, the second external channel is enabled; if REN2 = 0, the second external channel is disabled.

For the TMP423-Q1 only, the REN3 bit (bit 6) enables the third external measurement channel. If REN3 = 1, the third external channel is enabled; if REN3 = 0, the third external channel is disabled.

The temperature measurement sequence is: local channel, external channel 1, external channel 2, external channel 3, shutdown, and delay (to set conversion rate, if necessary). The sequence starts over with the local channel. If any of the channels are disabled, they are bypassed in the sequence.

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Table 9. Configuration Register 2 Bit Descriptions

CONFIGURATION REGISTER 2 (Read/Write = 0Ah, POR = 1Ch for TMP421-Q1; 3Ch for TMP422-Q1; 7Ch for TMP423-Q1)			
BIT	**NAME**	**FUNCTION**	**POWER-ON RESET VALUE**
7	Reserved	—	0
6	REN3	0 = External channel 3 disabled 1 = External channel 3 enabled	1 (TMP423-Q1) 0 (TMP421-Q1, TMP422-Q1)
5	REN2	0 = External channel 2 disabled 1 = External channel 2 enabled	1 (TMP422-Q1, TMP423-Q1) 0 (TMP421-Q1)
4	REN	0 = External channel 1 disabled 1 = External channel 1 enabled	1
3	LEN	0 = Local channel disabled 1 = Local channel enabled	1
2	RC	0 = Resistance correction disabled 1 = Resistance correction enabled	1
1, 0	Reserved	—	0

8.6.6 Conversion Rate Register

The Conversion Rate Register (pointer address 0Bh) controls the rate at which temperature conversions are performed. This register adjusts the idle time between conversions but not the conversion timing itself, thereby allowing the TMP421-Q1, TMP422-Q1, and TMP423-Q1 power dissipation to be balanced with the temperature register update rate. Table 10 describes the conversion rate options and corresponding current consumption. A one-shot command can be used during the idle time between conversions to immediately start temperature conversions on all enabled channels.

Table 10. Conversion Rate Register

CONVERSION RATE REGISTER (Read/Write = 0Bh, POR = 07h)										
R7	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**	**CONVERSIONS/SEC**	**AVERAGE I_Q (TYP) (μA)**	
									V+ = 2.7 V	**V+ = 5.5 V**
0	0	0	0	0	0	0	0	0.0625	11	32
0	0	0	0	0	0	0	1	0.125	17	38
0	0	0	0	0	0	1	0	0.25	28	49
0	0	0	0	0	0	1	1	0.5	47	69
0	0	0	0	0	1	0	0	1	80	103
0	0	0	0	0	1	0	1	2	128	155
0	0	0	0	0	1	1	0	4 (1)	190	220
0	0	0	0	0	1	1	1	8 (2)	373	413

(1) Conversion rate shown is for only one or two enabled measurement channels. When three channels are enabled, the conversion rate is 2 and 2/3 conversions-per-second. When four channels are enabled, the conversion rate is 2 per second.
(2) Conversion rate shown is for only one enabled measurement channel. When two channels are enabled, the conversion rate is 4 conversions-per-second. When three channels are enabled, the conversion rate is 2.667 conversions-per-second. When four channels are enabled, the conversion rate is 2 conversions-per-second.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

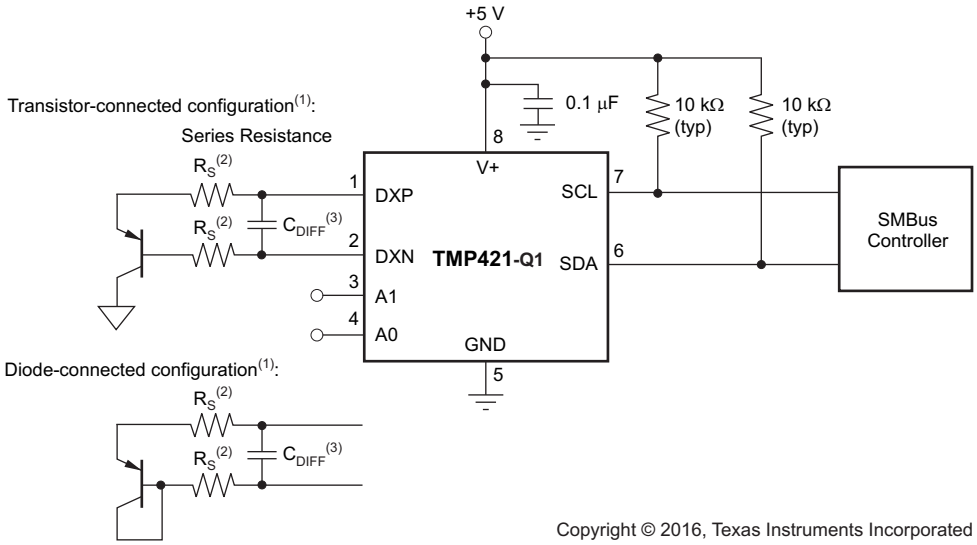
9.1 Application Information

The TMP42x-Q1 require a transistor connected between the DXP and DXN pins for remote temperature measurement. The SDA (and SCL if driven by an open-drain output) require pulllup resistors as part of the communication bus. The TMP421-Q1 includes slave address select pins (A1 and A0) allowing more than one device to reside on the same bus.

9.2 Typical Applications

9.2.1 TMP421-Q1 Basic Connections

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 SCL and SDA interface pins each require pull-up resistors as part of the communication bus. A 0.1-µF power-supply bypass capacitor is recommended for local bypassing. Figure 20, Figure 21, and Figure 22 illustrate typical configurations for the TMP421-Q1, TMP422-Q1, and TMP423-Q1, respectively.



(1) Diode-connected configuration provides better settling time. Transistor-connected configuration provides better series resistance cancellation.

(2) R_S (optional) must be < 1.5 kΩ in most applications. Selection of R_S depends on application; see the *Filtering* section.

(3) C_{DIFF} (optional) must be < 1000 pF in most applications. Selection of C_{DIFF} depends on application; see the *Filtering* section and Figure 7, *Remote Temperature Error vs Differential Capacitance*.

Figure 20. TMP421-Q1 Basic Connections

9.2.1.1 Design Requirements

The TMP421-Q1, TMP422-Q1, and TMP423-Q1 are designed to be used with either discrete transistors or substrate transistors built into processor chips, field programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs). Either NPN or PNP transistors can be used, as long as the base-emitter junction is used as the remote temperature sense. NPN transistors must be diode-connected. PNP transistors can either be transistor or diode-connected.

Errors in remote temperature sensor readings are typically the consequence of the ideality factor and current excitation used by the TMP421-Q1, TMP422-Q1, and TMP423-Q1 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a high-level and low-level current for the temperature-sensing substrate transistors. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 use 6 μA for I_{LOW} and 120 μA for I_{HIGH}.

The ideality factor (η-factor) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The TMP421-Q1, TMP422-Q1, and TMP423-Q1 allow for different η-factor values; see the *η-Factor Correction Register* section.

The ideality factor for the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is trimmed to be 1.008. For transistors that have an ideality factor that does not match the TMP421-Q1, TMP422-Q1, and TMP423-Q1, Equation 4 can be used to calculate the temperature error. Note that for the equation to be used correctly, actual temperature (°C) must be converted to kelvins (K).

$$T_{ERR} = \left(\frac{\eta - 1.008}{1.008}\right) \times (273.15 + T(°C)) \quad (4)$$

where

- η = ideality factor of remote temperature sensor
- T(°C) = actual temperature
- T_{ERR} = error in TMP421-Q1, TMP422-Q1, and TMP423-Q1 because η ≠ 1.008
- Degree delta is the same for °C and K

For η = 1.004 and T (°C) = 100°C:

$$T_{ERR} = \left(\frac{1.004 - 1.008}{1.008}\right) \times 273.15 + 100°C$$

$$T_{ERR} = 1.48°C \quad (5)$$

If a discrete transistor is used as the remote temperature sensor with the TMP421-Q1, TMP422-Q1, and TMP423-Q1, the best accuracy can be achieved by selecting the transistor according to the following criteria:

1. Base-emitter voltage > 0.25 V at 6 μA, at the highest sensed temperature.
2. Base-emitter voltage < 0.95 V at 120 μA, at the lowest sensed temperature.
3. Base resistance < 100 Ω.
4. Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (that is, 50 to 150).

Based on these criteria, two recommended small-signal transistors are the 2N3904 (NPN) or 2N3906 (PNP).

9.2.1.2 Detailed Design Procedure

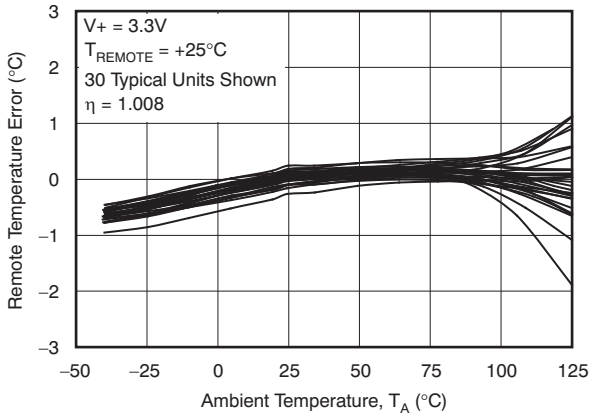
The local temperature sensor inside the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is influenced by the ambient air around the device but mainly monitors the PCB temperature that it is mounted to. In most applications, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 package is in electrical, and therefore thermal, contact with the printed-circuit board (PCB), as well as subjected to forced airflow. The accuracy of the measured temperature directly depends on how accurately the PCB and forced airflow temperatures represent the temperature that the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is measuring. Additionally, the internal power dissipation of the TMP421-Q1, TMP422-Q1, and TMP423-Q1 can cause the temperature to rise above the ambient or PCB temperature. The internal power is negligible because of the small current drawn by TMP421-Q1, TMP422-Q1, and TMP423-Q1 (see the *Measurement Accuracy and Thermal Considerations* section for more details).

For this design example a diode connected 2N3906 transistor was used thus the default setting of the n-factor and offset can be used.

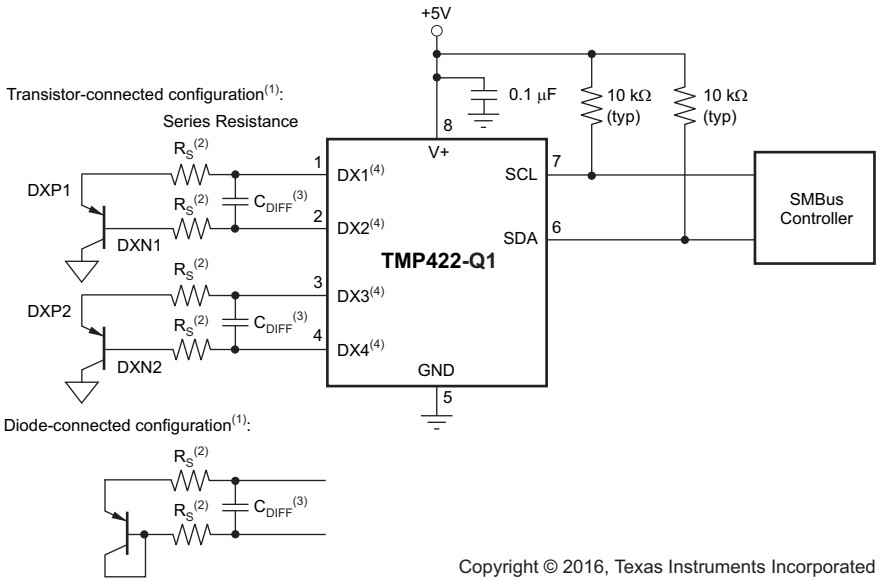
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9.2.1.3 Application Curve

The following curve shows the typical accuracy of the TMP421-Q1, TMP422-Q1, and TMP423-Q1 when connected to a 2N3906 remote transistor. All three TMP421-Q1, TMP422-Q1, and TMP423-Q1 will have the same performance and have identical design requirements when it comes to the accuracy of the remote sensor.



9.2.2 TMP422-Q1 Basic Connections



(1) Diode-connected configuration provides better settling time. Transistor-connected configuration provides better series resistance cancellation.

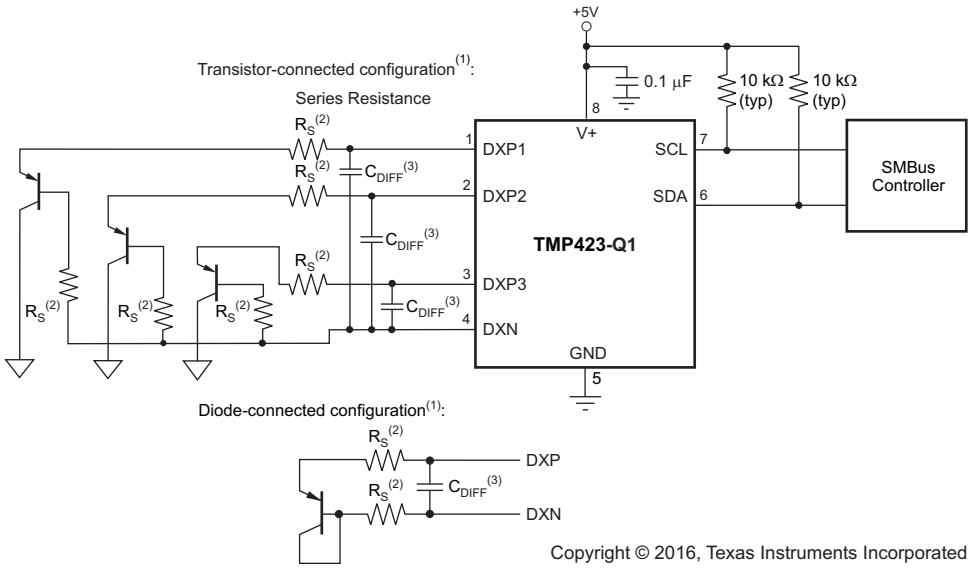
(2) R_S (optional) must be < 1.5 kΩ in most applications. Selection of R_S depends on application; see the *Filtering* section.

(3) C_{DIFF} (optional) must be < 1000 pF in most applications. Selection of C_{DIFF} depends on application; see the *Filtering* section and Figure 7, *Remote Temperature Error vs Differential Capacitance*.

(4) TMP422-Q1 SMBus slave address is *1001 100* when connected as shown.

Figure 21. TMP422-Q1 Basic Connections

9.2.3 TMP423-Q1 Basic Connections



(1) Diode-connected configuration provides better settling time. Transistor-connected configuration provides better series resistance
cancellation.

(2) R_S (optional) must be < 1.5 kΩ in most applications. Selection of R_S depends on application; see the *Filtering* section.

(3) C_{DIFF} (optional) must be < 1000 pF in most applications. Selection of C_{DIFF} depends on application; see the *Filtering* section and
Figure 7, *Remote Temperature Error vs Differential Capacitance*.

Figure 22. TMP423-Q1 Basic Connections

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10 Power Supply Recommendations

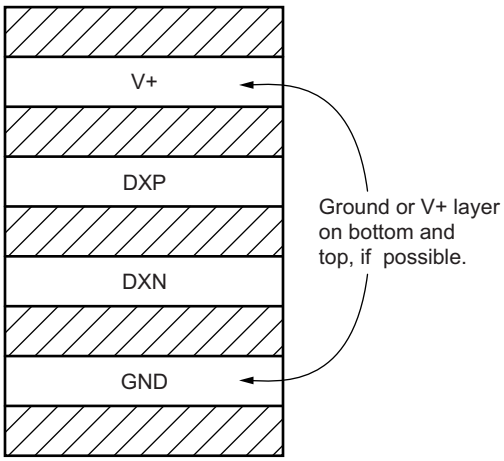
The TMP421-Q1, TMP422-Q1, and TMP423-Q1 operates with a power-supply range of 2.7 V to 5.5 V. The device is optimized for operation at a 3.3 V supply but can measure temperature accurately in the full supply range. TI recommends a power-supply bypass capacitor. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 μF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

Remote temperature sensing on the TMP421-Q1, TMP422-Q1, and TMP423-Q1 measures very small voltages using very low currents; therefore, noise at the device inputs must be minimized. Most applications using the TMP421-Q1, TMP422-Q1, and TMP423-Q1 have high digital content, with several clocks and logic level transitions creating a noisy environment. Layout must adhere to the following guidelines:

1. Place the TMP421-Q1, TMP422-Q1, and TMP423-Q1 as close to the remote junction sensor as possible.
2. Route the DXP and DXN traces next to each other and shield them from adjacent signals through the use of ground guard traces, as shown in Figure 23. If a multilayer PCB is used, bury these traces between ground or V+ planes to shield them from extrinsic noise sources. 5 mil (0.127 mm) PCB traces are recommended.
3. Minimize additional thermocouple junctions caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the DXP and DXN connections to cancel any thermocouple effects.
4. Use a 0.1-μF local bypass capacitor directly between the V+ and GND of the TMP421-Q1, TMP422-Q1, and TMP423-Q1; see Figure 24. Minimize filter capacitance between DXP and DXN to 1000 pF or less for optimum measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and the TMP421-Q1, TMP422-Q1, and TMP423-Q1.
5. If the connection between the remote temperature sensor and the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is less than 8 in (20.32 cm) long, use a twisted-wire pair connection. Beyond 8 in, use a twisted, shielded pair with the shield grounded as close to the TMP421-Q1, TMP422-Q1, and TMP423-Q1 as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60-Hz pickup.
6. Thoroughly clean and remove all flux residue in and around the pins of the TMP421-Q1, TMP422-Q1, and TMP423-Q1 to avoid temperature offset readings as a result of leakage paths between DXP or DXN and GND, or between DXP or DXN and V+.



NOTE: Use minimum 5 mil (0.127mm) traces with 5 mil spacing.

Figure 23. Suggested PCB Layer Cross-Section

11.2 Layout Example

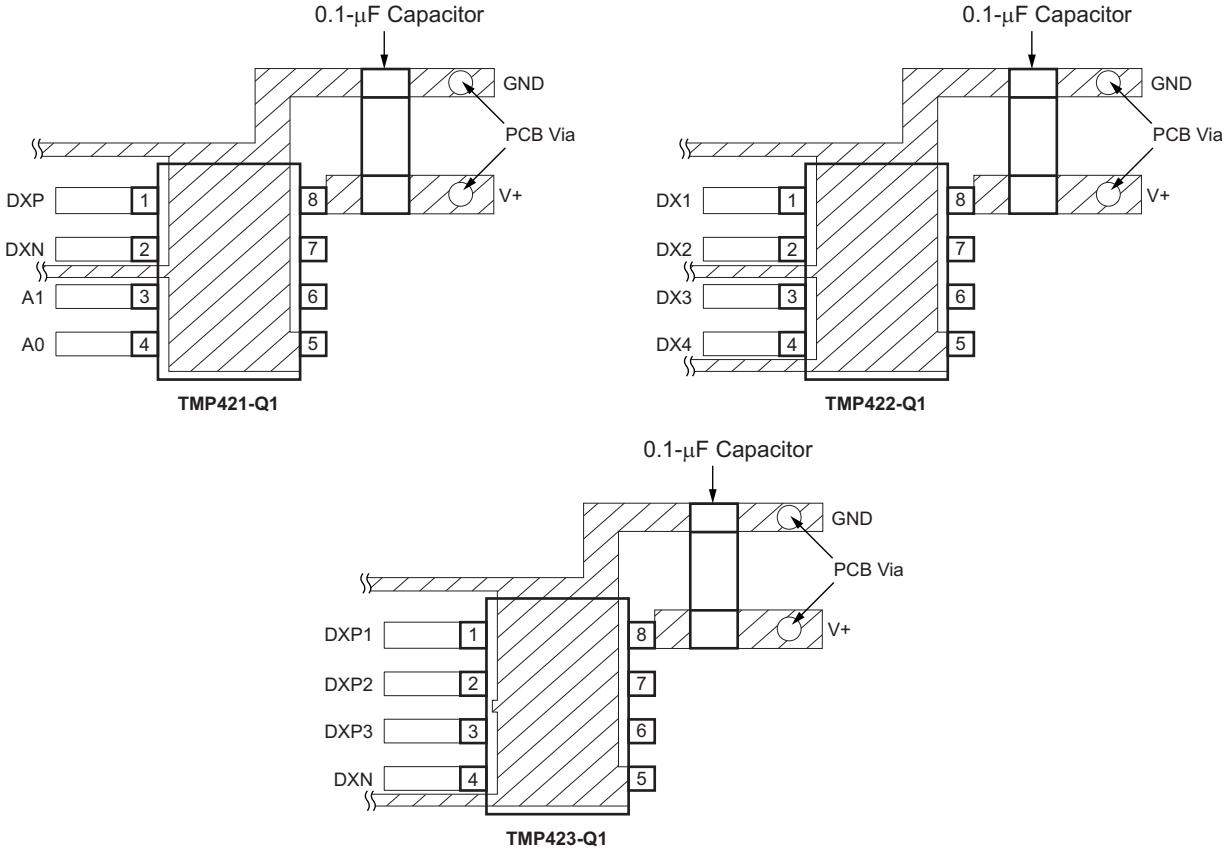


Figure 24. Suggested Bypass Capacitor Placement and Trace Shielding

11.3 Measurement Accuracy and Thermal Considerations

The temperature measurement accuracy of the TMP421-Q1, TMP422-Q1, and TMP423-Q1 depends on the remote and local temperature sensor being at the same temperature as the system point being monitored. Clearly, if the temperature sensor is not in good thermal contact with the part of the system being monitored, then there is a delay in the response of the sensor to a temperature change in the system. For remote temperature-sensing applications using a substrate transistor (or a small, SOT-23 transistor) placed close to the device being monitored, this delay is usually not a concern.

The local temperature sensor inside the TMP421-Q1, TMP422-Q1, and TMP423-Q1 monitors the ambient air around the device. The thermal time constant for the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is approximately two seconds. This constant implies that if the ambient air changes quickly by 100°C, then the TMP421-Q1, TMP422-Q1, and TMP423-Q1 requires approximately 10 seconds (that is, five thermal time constants) to settle to within 1°C of the final value. In most applications, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 package is in electrical, and therefore thermal, contact with the printed circuit board (PCB), as well as subjected to forced airflow. The accuracy of the measured temperature directly depends on how accurately the PCB and forced airflow temperatures represent the temperature that the TMP421-Q1, TMP422-Q1, and TMP423-Q1 is measuring. Additionally, the internal power dissipation of the TMP421-Q1, TMP422-Q1, and TMP423-Q1 can cause the temperature to rise above the ambient or PCB temperature. The internal power dissipated as a result of exciting the remote temperature sensor is negligible because of the small currents used. For a 5.5-V supply and maximum conversion rate of eight conversions per second, the TMP421-Q1, TMP422-Q1, and TMP423-Q1 dissipate 2.3 mW (PD_{IQ} = 5.5 V × 415 µA). A θ_{JA} of 100°C/W (for SOT-23 package) causes the junction temperature to rise approximately 0.23°C above the ambient.

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12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMP421-Q1	Click here	Click here	Click here	Click here	Click here
TMP422-Q1	Click here	Click here	Click here	Click here	Click here
TMP423-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
SMBus is a trademark of Intel Corporation.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP421AQDCNRQ1	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	421Q	Samples
TMP421AQDCNTQ1	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	421Q	Samples
TMP422AQDCNRQ1	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	422Q	Samples
TMP422AQDCNTQ1	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	422Q	Samples
TMP423AQDCNRQ1	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	423Q	Samples
TMP423AQDCNTQ1	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	423Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP421-Q1, TMP422-Q1, TMP423-Q1 :

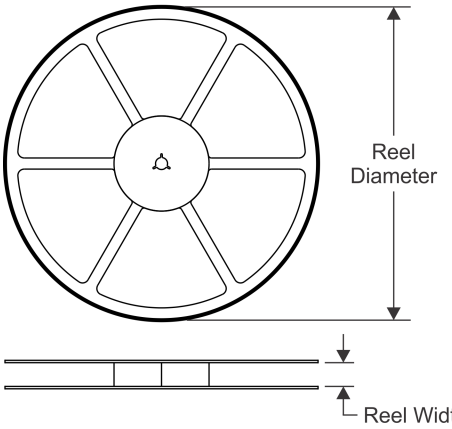
- Catalog: TMP421, TMP422, TMP423
- Enhanced Product: TMP422-EP

NOTE: Qualified Version Definitions:

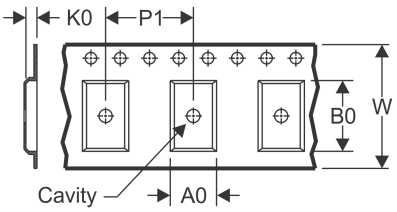
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

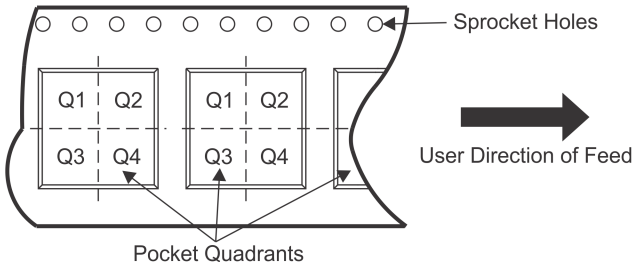


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

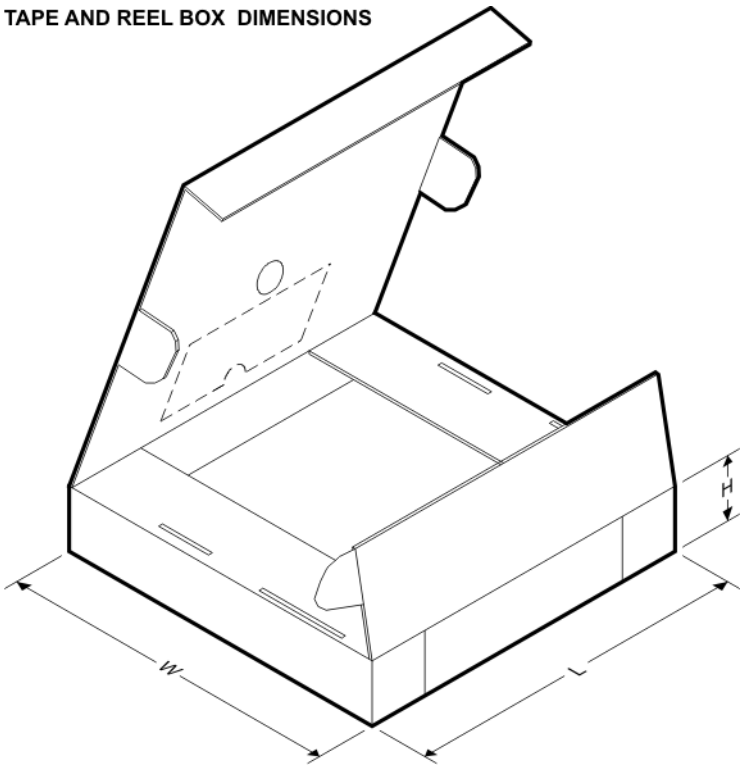
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP421AQDCNRQ1	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP421AQDCNTQ1	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP422AQDCNRQ1	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP422AQDCNTQ1	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP423AQDCNRQ1	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TMP423AQDCNTQ1	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

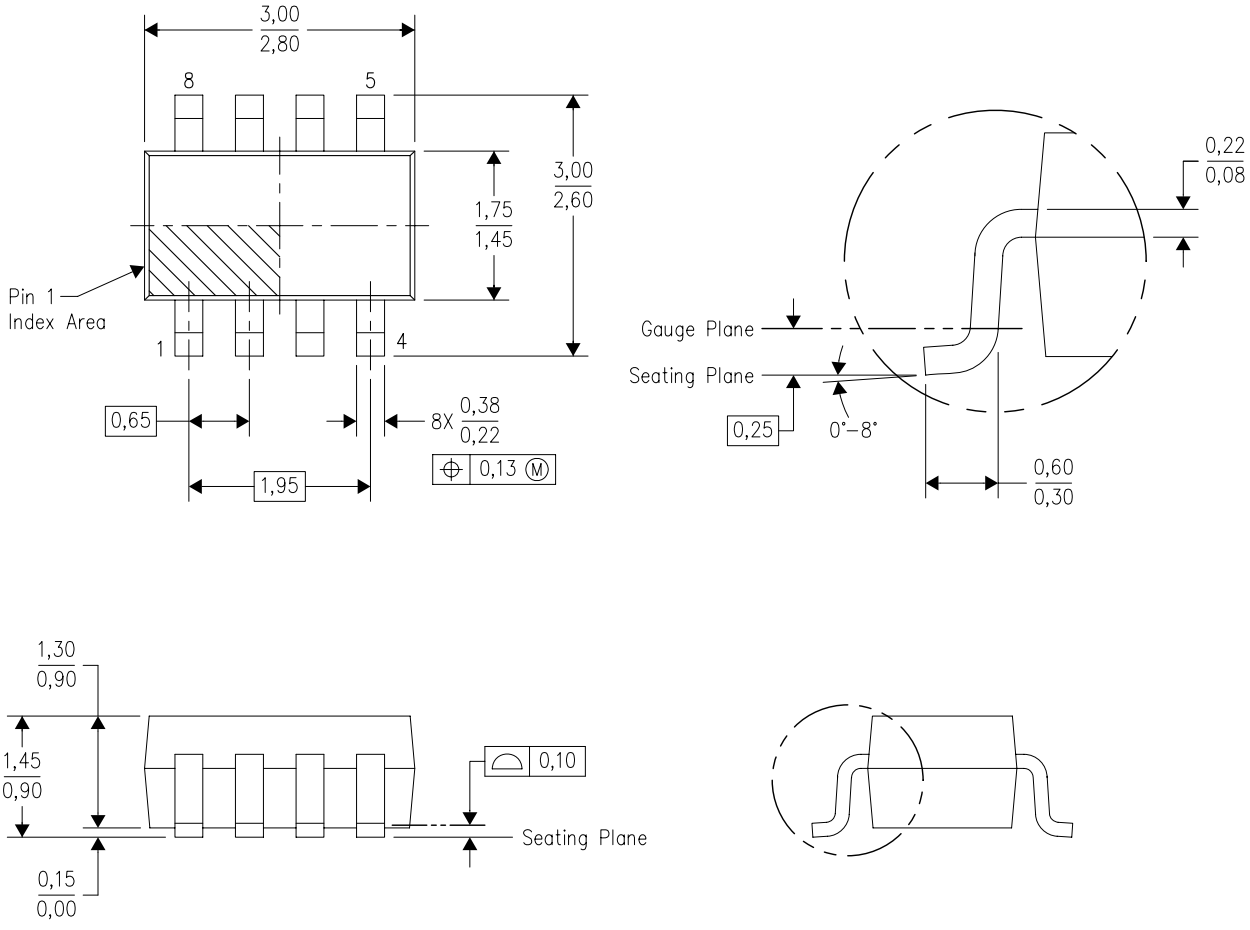
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

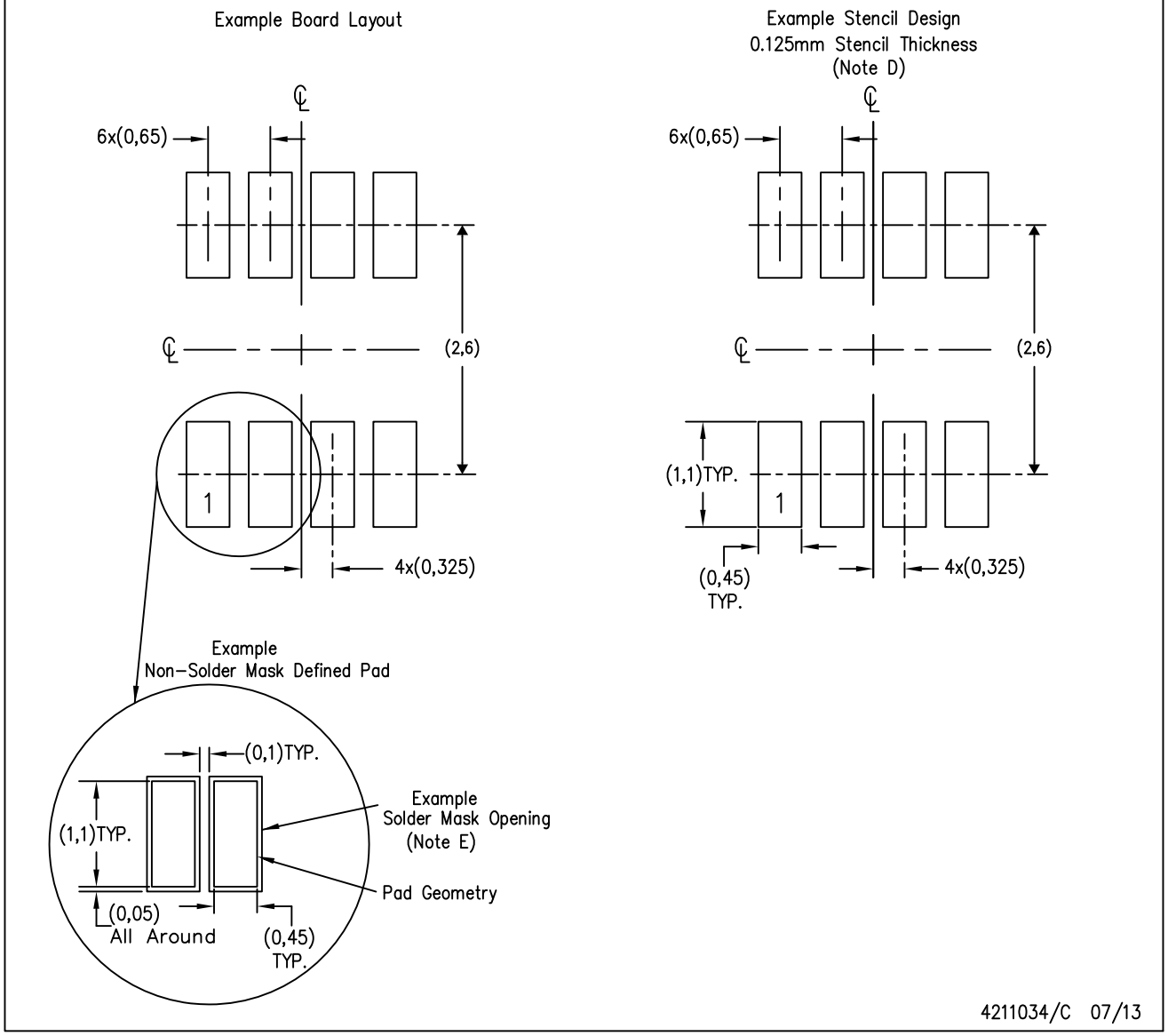
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP421AQDCNRQ1	SOT-23	DCN	8	3000	195.0	200.0	45.0
TMP421AQDCNTQ1	SOT-23	DCN	8	250	195.0	200.0	45.0
TMP422AQDCNRQ1	SOT-23	DCN	8	3000	195.0	200.0	45.0
TMP422AQDCNTQ1	SOT-23	DCN	8	250	195.0	200.0	45.0
TMP423AQDCNRQ1	SOT-23	DCN	8	3000	195.0	200.0	45.0
TMP423AQDCNTQ1	SOT-23	DCN	8	250	195.0	200.0	45.0

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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