- **Organization**
  TM124MBK36B . . . 1 048 576 × 36
  TM248NBK36B . . . 2 097 152 × 36
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-pin Leadless Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124MBK36B–Utilizes Eight 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages and One 4-Megabit Quad-$\overline{CAS}$ DRAM in a Plastic Small-Outline J-Lead (SOJ) Package**
- **TM248NBK36B–Utilizes Sixteen 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 4-Megabit Quad-$\overline{CAS}$ DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Nine Common Data-In and Data-Out Lines, in Four Blocks**
- **Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
’124MBK36B-60	60 ns	30 ns	15 ns	110 ns
’124MBK36B-70	70 ns	35 ns	18 ns	130 ns
’124MBK36B-80	80 ns	40 ns	20 ns	150 ns
’248NBK36B-60	60 ns	30 ns	15 ns	110 ns
’248NBK36B-70	70 ns	35 ns	18 ns	130 ns
’248NBK36B-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:†**
  - **TM124MBK36B**
  - **TM248NBK36B**
- **Tin-Lead (Solder) Tabbed Versions Available:**
  - **TM124MBK36R**
  - **TM248NBK36R**

description

TM124MBK36B

The TM124MBK36B is a dynamic random-access memory (DRAM) organized as four times 1 048 576 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit DRAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and one TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ DRAM in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 or TMS44460 data sheet, respectively.

The TM124MBK36B is available in the single-sided BK leadless module for use with sockets.

The TM124MBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C.

TM248NBK36B

The TM248NBK36B is a DRAM organized as four times 2 097 152 × 9 (bit 9 is generally used for parity) in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS44400DJ, 1 048 576 × 4-bit DRAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and two TMS44460DJ, 1 048 576 × 4-bit Quad-$\overline{CAS}$ DRAMs, each in a 24/26-lead plastic small-outline J-lead package (SOJ), mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 and TMS44460 data sheet, respectively.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TM248NBK36B (continued)

The TM124NBK36B is available in the double-sided BK leadless module for use with sockets.

The TM124NBK36B features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C

operation

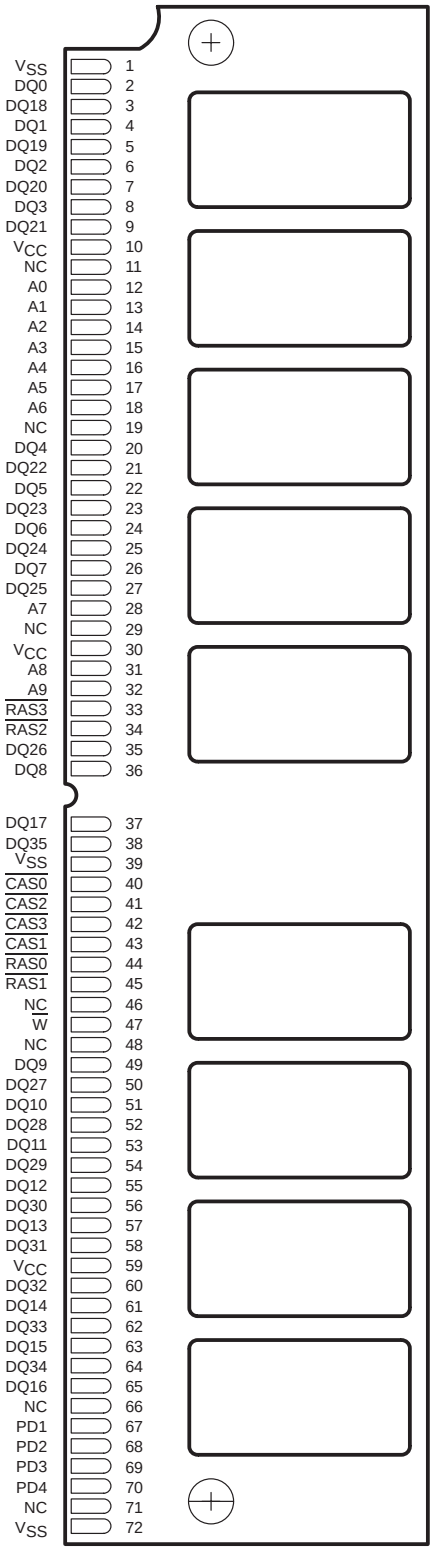
TM124MBK36B

The TM124MBK36B operates as eight TMS44400DJs and one TMS44460DJ connected as shown in the functional block diagram and Table 1. The parity bits are provided by the TMS44460DJ and are controlled by $\overline{RAS2}$. To ensure proper parity bit operation all memory accesses should include a $\overline{RAS2}$ pulse. Refer to the TMS44400 and TMS44460 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

TM248NBK36B

The TM248NBK36B operates as sixteen TMS44400DJs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The parity bits are provided by the TMS44460DJ and are controlled by $\overline{RAS2}$ on side 1 and $\overline{RAS3}$ on side 2. To ensure proper parity bit operation, all memory accesses should include a $\overline{RAS2}$ or $\overline{RAS3}$ pulse. Refer to the TMS44400 and TMS44460 data sheets for details of operation. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

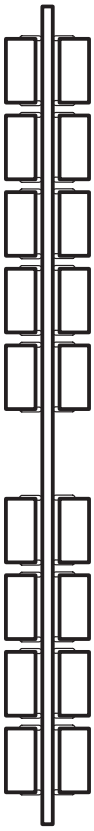
BK SINGLE IN-LINE MEMORY MODULE
(TOP VIEW)



TM124MBK36B
(SIDE VIEW)



TM248NBK36B
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36B	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248NBK36B	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

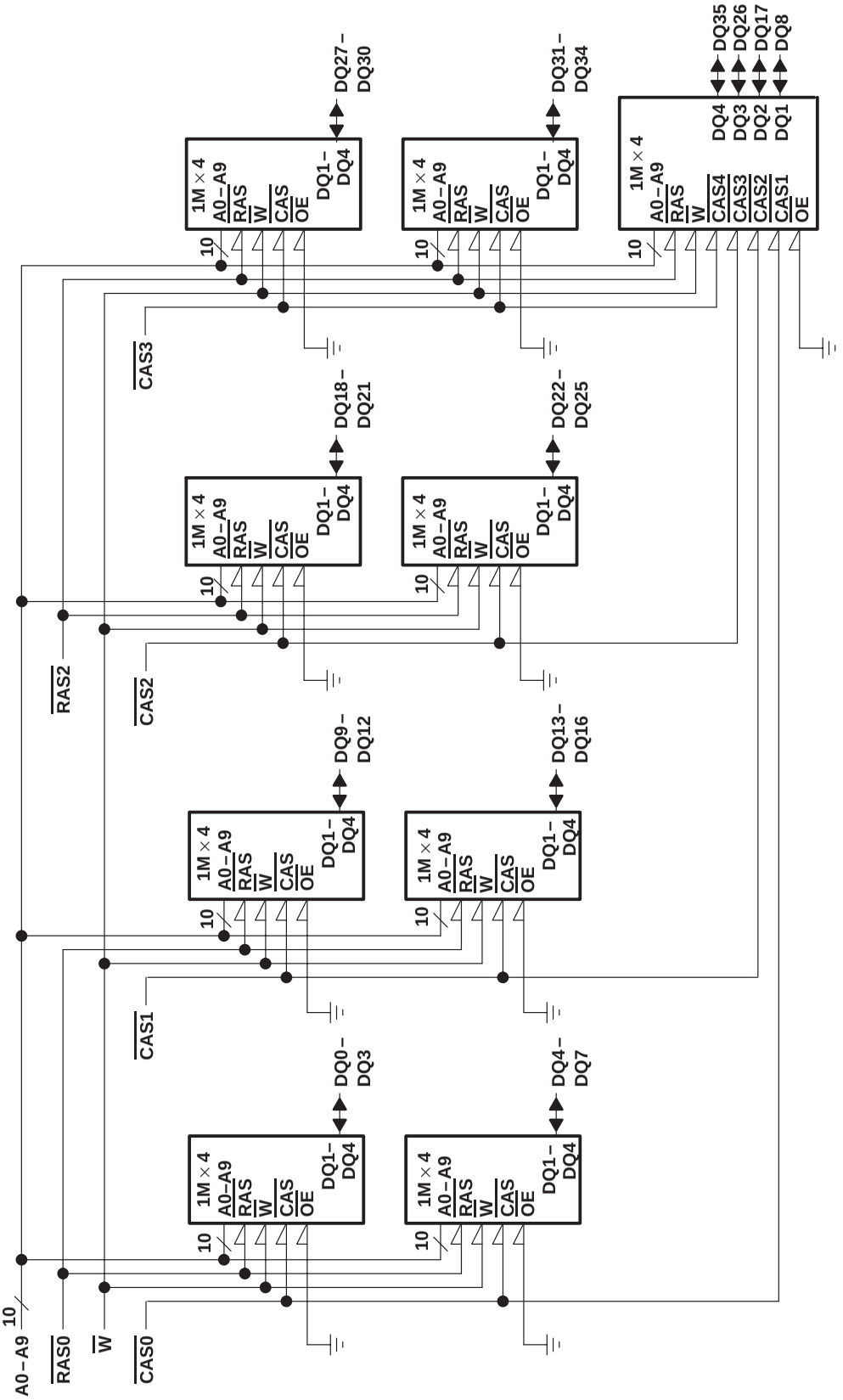
DATA BLOCK	$\overline{RAS}$x		$\overline{CAS}$x
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS0}$
DQ9–DQ16	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ17	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS1}$
DQ18–DQ25	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ26	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ27–DQ34	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$
DQ35	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248NBK36B only.

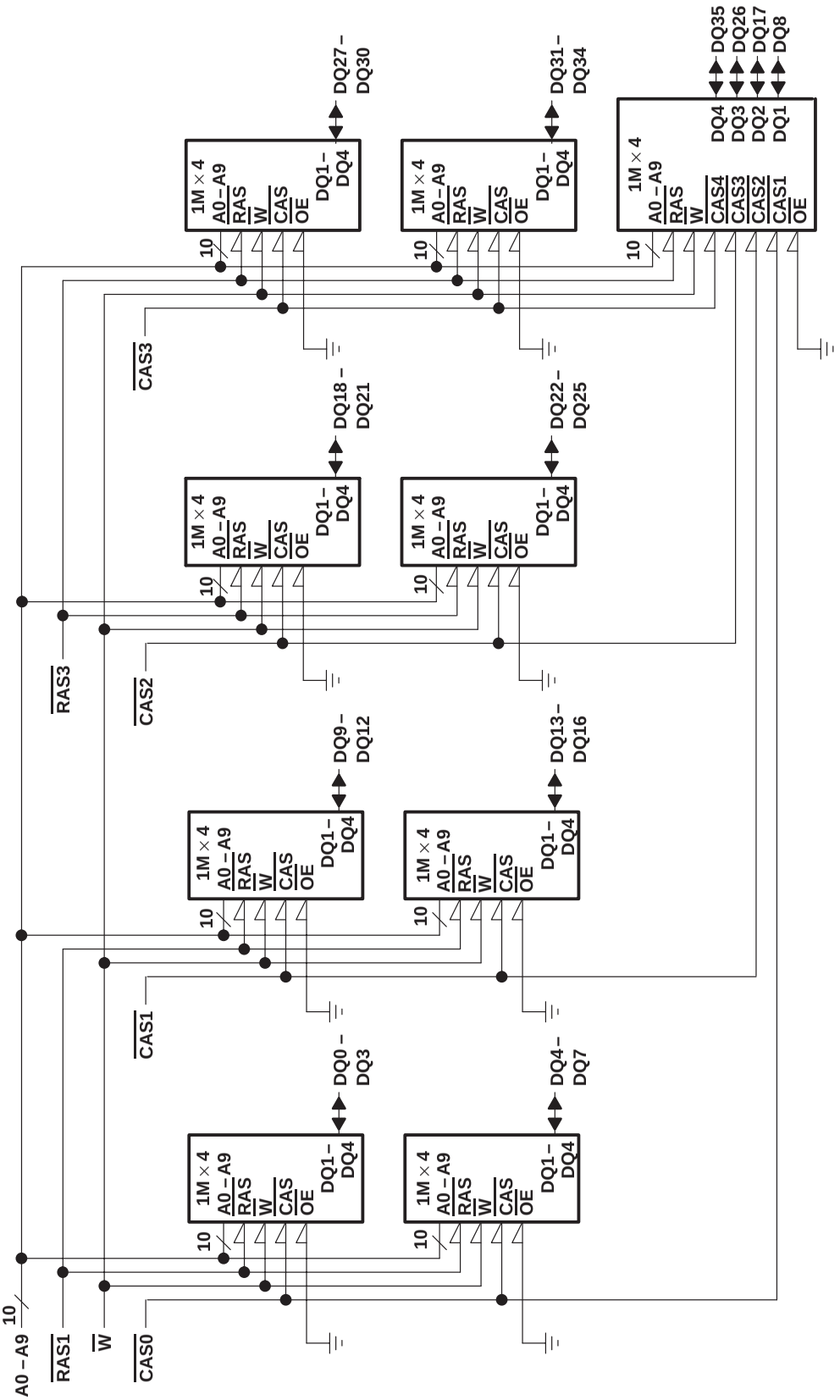
single-in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124MBK36B and TM248NBK36B: Nickel plate and gold plate over copper
Contact area for TM124MBK36R and TM248NBK36R: Nickel plate and tin-lead over copper

functional block diagram (TM124MBK36B and TM248NBK36B, side 1)



functional block diagram (TM248NBK36B, side 2)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 9 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124MBK36B-60		'124MBK36B-70		'124MBK36B-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		945		810		720	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		18		18		18	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		9		9		9	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		945		810		720	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		810		720		630	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248NBK36B-60		'248NBK36B-70		'248NBK36B-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		963		828		738	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		36		36		36	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		18		18		18	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1890		1620		1440	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling		828		738		648	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36B		'248NBK36B		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0 – A9		45		90	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$		35		35	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$		21		42	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		63		126	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		’124MBK36B-60 ’248NBK36B-60		’124MBK36B-70 ’248NBK36B-70		’124MBK36B-80 ’248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{AA}	Access time from column address		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low impedance	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’124MBK36B-60 ’248NBK36B-60		’124MBK36B-70 ’248NBK36B-70		’124MBK36B-80 ’248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read write	130		153		175		ns
t_{PC}	Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, write	15		15		15		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	Setup time, $\overline{W}$ high (see Note 9)	10		10		10		ns

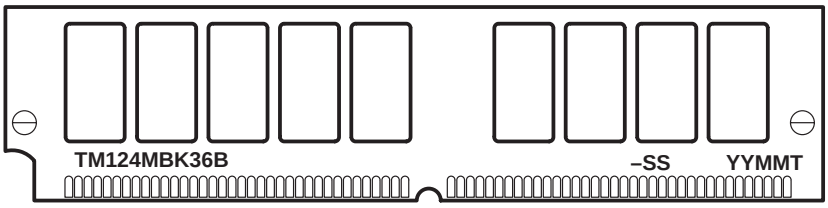
NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ 5 ns.
9. CBR refresh only

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		’124MBK36B-60 ’248NBK36B-60		’124MBK36B-70 ’248NBK36B-70		’124MBK36B-80 ’248NBK36B-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{DH}	Hold time, data	10		15		15		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{CLCH}	Hold time, $\overline{CAS}$ low to $\overline{CAS}$ high	5		5		5		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 10)	50		55		60		ns
t_{WHR}	Hold time, $\overline{W}$ high (see Note 9)	10		10		10		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 12)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 12)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 9. CBR refresh only
10. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. The maximum value is specified only to assure access time.

device symbolization (TM124MBK36B illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code

NOTE: Location of symbolization may vary.

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