TLV8544 500 nA RRIO Nanopower Operational Amplifier for Cost-Optimized Systems

1 Features

- For Cost-Optimized Systems
- Nanopower Supply Current: 500 nA/channel
- Offset Voltage: 4 mV (Max)
- TcVos: 1.5 µV/°C
- Gain-Bandwidth: 8 kHz
- Unity-Gain Stable
- Low Input Bias Current: 100 fA
- Wide Supply Range: 1.7 V to 3.6 V
- Rail to Rail Input And Output (RRIO)
- Temperature Range –40°C to 125°C
- Industry Standard Package
  - Quad in 14-pin TSSOP

2 Applications

- Gas Detectors
- Motion Detectors using PIR sensors
- Motion Detectors using microwave sensors
- Ionizaton Smoke Alarms
- Thermostats
- Remote Sensors, IoT (Internet of Things)
- Active RFID Readers and Tags
- Portable Medical Equipment

3 Description

The TLV8544 ultra-low-power operational amplifier is ideal for cost-optimized sensing applications in wireless and low-power wired equipment. The TLV8544 amplifier minimizes power consumption in equipment such as motion detecting security systems (like microwave and PIR motion sensing) where operational battery life is critical. It also has a carefully designed CMOS input stage enabling very low, femto-amp bias currents, thereby reducing I_{BIAS} and I_{OS} errors that would otherwise impact sensitive applications like transimpedance amplifier (TIA) configurations with megaohm feedback resistors, and high source impedance sensing applicaitons. Additionally, built-in EMI protection reduces sensitivity to unwanted RF signals from sources like mobile phones, WiFi, radio transmitters and tab readers.

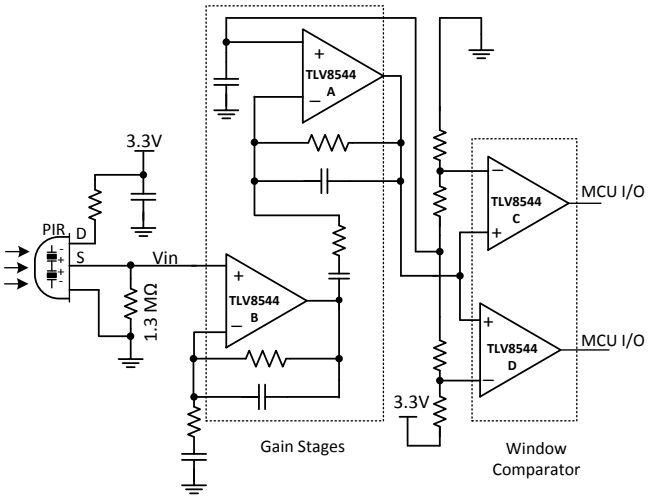
The TLV8544 amplifier operates with a single supply voltage down to 1.7V, providing continuous performance in low battery situations over the extended temperature range of -40ºC to 125ºC. The quad TLV8544 is available in the industry standard 14-pin TSSOP package.

Device Information(1)

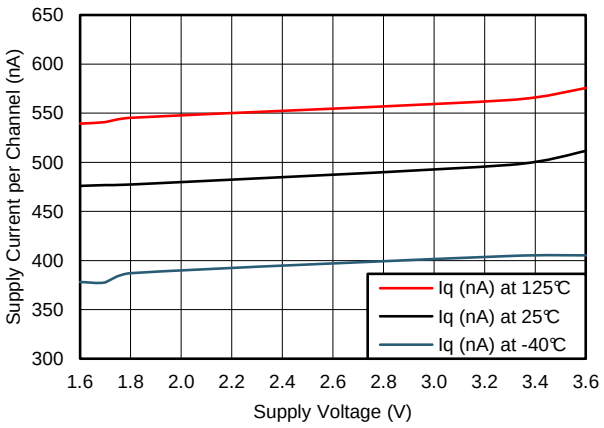
PART NUMBER	PACKAGE	BODY SIZE
TLV8544	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Low Power PIR Motion Detector



Quiescent Supply Current vs. Supply Voltage



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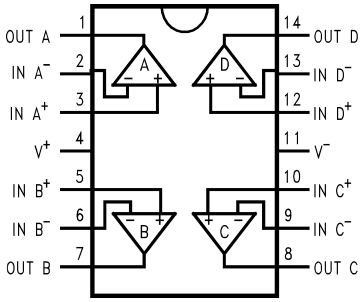
4 Revision History

DATE	REVISION	NOTES
December 2016	*	Initial release.

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5 Pin Configuration and Functions

TLV8544 PW Package
14-Pin TSSOP
Top View



Pin Functions: TLV8544 PW

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT A	O	Channel A Output
2	IN A-	I	Channel A Inverting Input
3	IN A+	I	Channel A Non-Inverting Input
4	V+	P	Positive (highest) power supply
5	IN B+	I	Channel B Non-Inverting Input
6	IN B-	I	Channel B Inverting Input
7	OUT B	O	Channel B Output
8	OUT C	O	Channel C Output
9	IN C-	I	Channel C Inverting Input
10	IN C+	I	Channel C Non-Inverting Input
11	V-	P	Negative (lowest) power supply
12	IN D+	I	Channel D Non-Inverting Input
13	IN D-	I	Channel D Inverting Input
14	OUT D	O	Channel D Output

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) - (V-)			–0.3	4	V
Input pins	Voltage	Common mode	(V–) - 0.3	(V+) + 0.3	V
		Differential	(V–) - 0.3	(V+) + 0.3	V
Input pins	Current		–10	10	mA
Output short current (4)			Continuous	Continuous	
Operating temperature			–40	125	°C
Storage temperature, T_{stg}			–65	150	°C
Junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	1.7		3.6	V
Specified temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TLV8544 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

T_A = 25°C, V_S = 1.8 V to 3.3 V, V_{CM} = V_{OUT} = V_S / 2, and R_L≥ 10 MΩ to V_S / 2, unless otherwise noted.

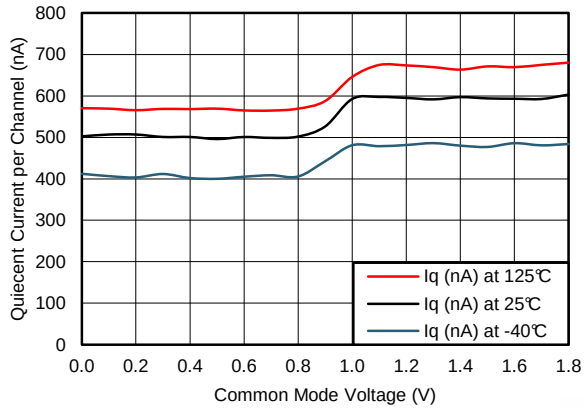
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = V– , Vs = 1.8V and 3.3V	–4	±0.5	4	mV
		V_{CM} = V+, Vs = 1.8V and 3.3V	–4	±0.5	4	
dV_{OS}/dT	Input offset drift	V_{CM} = V–, T_A = –40°C to 125°C		1.5		µV/°C
PSRR	Power-supply rejection ratio	V_{CM} = V– , Vs =1.8V and 3.3V	60	90		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 3.3 V	0		3.3	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+), V_S = 3.3 V	60	75		dB
		(V–) ≤ V_{CM} ≤ (V+) – 1.2 V		95		
INPUT BIAS CURRENT						
I_B	Input bias current			100		fA
I_{OS}	Input offset current			100		fA
INPUT IMPEDANCE						
	Differential			2		pF
	Common mode			4		pF
NOISE						
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz		8.6		µVp–p
e_n	Input voltage noise density	f = 1 kHz		264		nV/√Hz
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V ≤ V_O ≤ (V+) – 0.3 V, R_L = 100 kΩ to V^+/2		100		dB
OUTPUT						
V_{OH}	Voltage output swing from positive rail	R_L = 100 kΩ to V^+/2, V_S = 3.3 V	20			mV
V_{OL}	Voltage output swing from negative rail	R_L = 100 kΩ to V^+/2, V_S = 3.3 V			20	
I_{SC}	Short-circuit current	Sourcing, V_O to V–, VIN(diff) = 100 mV, V_S = 3.3 V		15		mA
		Sinking, V_O to V+, VIN(diff) = –100 mV, V_S = 3.3 V		30		
Z_O	Open loop output impedance	f = 1 kHz, I_O = 0 A		8		kΩ
FREQUENCY RESPONSE						
GBP	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ		8		kHz
SR	Slew rate (10% to 90%)	G = 1, Rising Edge, C_L = 20 pF		3.5		V/ms
		G = 1, Falling Edge, C_L = 20 pF		4.5		
POWER SUPPLY						
$I_{Q–TLV8544}$	Quiescent Current, Per Channel	V_{CM} = V–, I_O = 0, V_S = 3.3 V		500	850	nA

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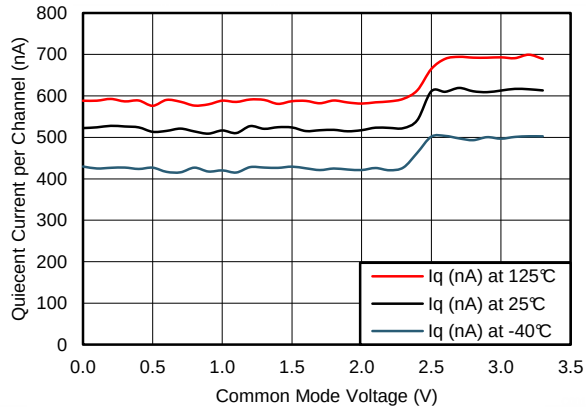
6.6 Typical Characteristics

TA = 25°C, R_L = 10MΩ to V_S/2 ,C_L = 50pF, V_{CM} = V_S / 2V unless otherwise specified.



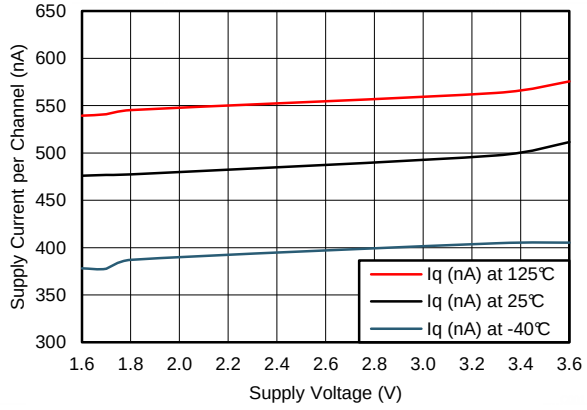
T_A = -40, 25, 125°C
V_S= 1.8V
Per Channel
R_L= No Load
C_L= No Load

Figure 1. Supply Current vs. Common Mode Voltage



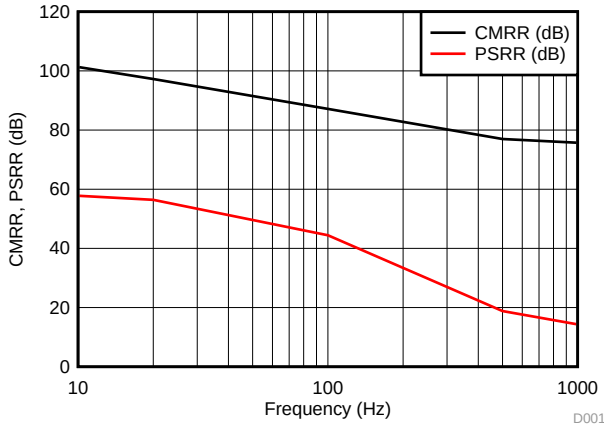
T_A = -40, 25, 125°C
V_S= 3.3V
Per Channel
R_L= No Load
C_L= No Load

Figure 2. Supply Current vs. Common Mode Voltage



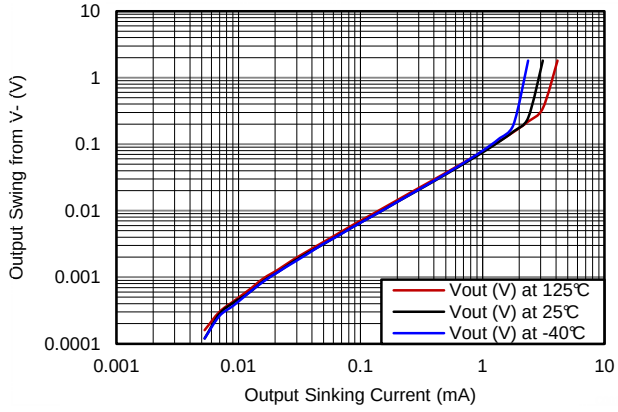
T_A = -40, 25, 125°C
V_S= 1.6 to 3.6V
V_{CM} = V-
R_L= No Load
C_L= No Load

Figure 3. Supply Current vs. Supply Voltage, Low VCM



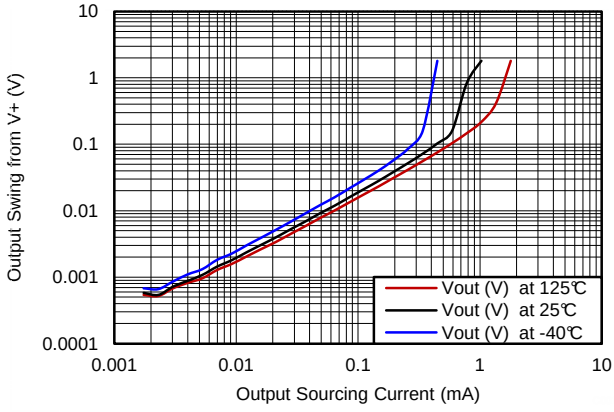
T_A = 25°C
V_S= 3.3V
V_{CM} = Vs/2
R_L= 1MΩ
C_L= 50pF

Figure 4. CMRR and PSRR vs. Supply Voltage, High VCM



T_A = -40, 25, 125°C
V_S= 1.8V
R_L= No Load
C_L= No Load

Figure 5. Output Swing vs. Sinking Current



T_A = -40, 25, 125°C
V_S= 1.8V
R_L= No Load
C_L= No Load

Figure 6. Output Swing vs. Sourcing Current

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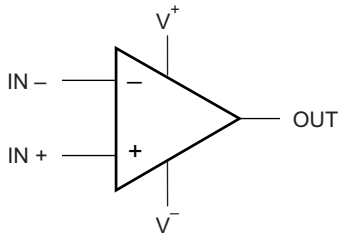
7 Detailed Description

7.1 Overview

The TLV8544 amplifier is unity-gain stable and can operate on a single supply, making it highly versatile and easy to use.

Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* curves.

7.2 Functional Block Diagram



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7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (IN+) and an inverting input (IN–). The device amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ – IN^–) \quad (1)$$

where

- A_{OL} is the open-loop gain of the amplifier, typically around 100 dB.

7.4 Device Functional Modes

7.4.1 Rail-To-Rail Input

The input common-mode voltage range of the TLV8544 extends to the supply rails. This is achieved with a complementary input stage — an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 800 mV to 200 mV above the positive supply, while the P-channel pair is on for inputs from 300 mV below the negative supply to approximately (V+) – 800 mV. There is a small transition region, typically (V+) – 1.2 V to (V+) – 0.8 V, in which both pairs are on. This 400 mV transition region can vary 200 mV with process variation. Within the 400 mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

7.4.2 Supply Current Changes over Common Mode

Because of the ultra-low supply current, changes in common mode voltages will cause a noticeable change in the supply current as the input stages transition through the transition region, as shown in Figure 7 below.

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Device Functional Modes (continued)

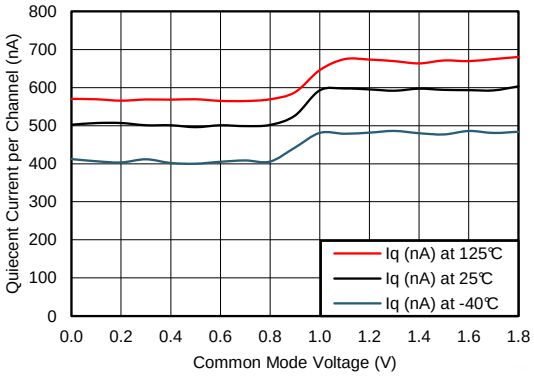


Figure 7. Supply Current Change Over Common Mode at 1.8V

For the lowest supply current operation, keep the input common mode range between V- and 1 V below V+.

7.4.3 Design Optimization With Rail-To-Rail Input

In most applications, operation is within the range of only one differential pair. However, some applications can subject the amplifier to a common-mode signal in the transition region. Under this condition, the inherent mismatch between the two differential pairs may lead to degradation of the CMRR and THD. The unity-gain buffer configuration is the most problematic as it will traverse through the transition region if a sufficiently wide input swing is required.

7.4.4 Design Optimization for Nanopower Operation

When designing for ultralow power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors will react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. A feedback capacitor may be required to assure stability and limit overshoot or gain peaking.

When possible, use AC coupling and AC feedback to reduce static current draw through the feedback elements. Use film or ceramic capacitors since large electolytics may have static leakage currents in the tens to hundreds of nanoamps.

7.4.5 Common-Mode Rejection

The CMRR for the TLV8544 is specified in two ways so the best match for a given application may be used. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 1.2 V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR at V_S = 3.3 V over the entire common-mode range is specified.

7.4.6 Output Stage

The TLV8544 output voltage swings 20 mV from rails at 3.3 V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The TLV8544 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load.

7.4.7 Driving Capacitive Load

The TLV8544 is internally compensated for stable unity gain operation, with a 8 kHz typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

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Device Functional Modes (continued)

In order to drive heavy (>50pF) capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 8. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

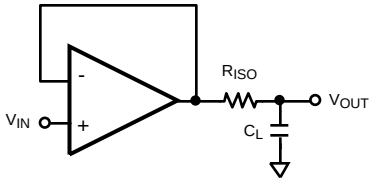


Figure 8. Resistive Isolation Of Capacitive Load

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV8544 is a ultra-low power operational amplifier that provides 8kHz bandwidth with only 500nA typical quiescent current, and near precision drift specifications at a low cost. These rail-to-rail input and output amplifiers are specifically designed for battery-powered applications. The input common-mode voltage range extends to the power-supply rails and the output swings to within millivolts of the rails, maintaining a wide dynamic range.

8.2 Typical Application: 60 Hz Twin "T" Notch Filter

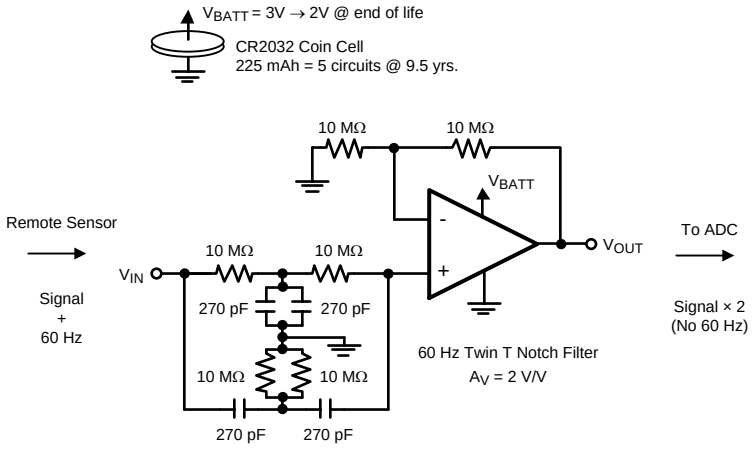


Figure 9. 60 Hz Notch Filter

8.2.1 Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60 Hz interference from AC power lines. The circuit of Figure 9 notches out the 60 Hz and provides a system gain of A_V = 2 for the sensor signal represented by a 1 kHz sine wave. Similar stages may be cascaded to remove 2nd and 3rd harmonics of 60 Hz. Thanks to the nA power consumption of the TLV8544, even 5 such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3 V and an end of life voltage of 2 V. With an operating voltage from 1.7V to 3.6V the TLV8544 can function over this voltage range.

8.2.2 Detailed Design Procedure

The notch frequency is set by:

$$F_0 = 1 / 2\pi RC. \quad (2)$$

To achieve a 60 Hz notch use R = 10 MΩ and C = 270 pF. If eliminating 50 Hz noise, use R = 11.8 MΩ and C = 270 pF.

The Twin T Notch Filter works by having two separate paths from V_{IN} to the amplifier's input. A low frequency path through the series input resistors and another separate high frequency path through the series input capacitors. However, at frequencies around the notch frequency, the two paths have opposing phase angles and the two signals will tend to cancel at the amplifier's input.

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Typical Application: 60 Hz Twin "T" Notch Filter (continued)

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter needs to be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected clean board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in Figure 9 can be done over a bandwidth of 2 kHz, which takes the conservative approach of overestimating the bandwidth (TLV8544 typical GBW/A_V is lower, where A_V is the system's gain). The total noise at the output is approximately 800 µVpp, which is excellent considering the total consumption of the circuit is only 900 nA. The dominant noise terms are op amp voltage noise , current noise through the feedback network (430 µVpp), and current noise through the notch filter network (280 µVpp). Thus the total circuit's noise is below 1/2 LSB of a 10-bit system with a 2 V reference, which is 1 mV.

8.2.3 Application Curve

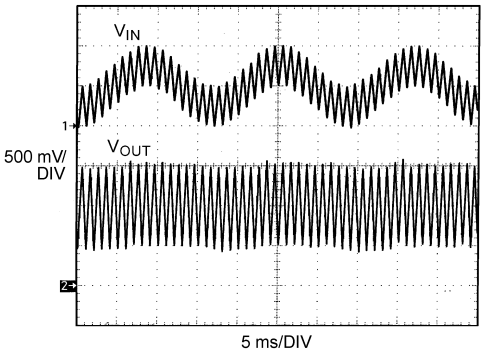


Figure 10. 60 Hz Notch Filter Waveform

8.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, particularly cables, Muxes and ADC inputs.

Do add series current limiting resistors and external schottky clamp diodes if input voltage is expected to exceed the supplies. Limit the current to 1mA or less (1KΩ per volt).

9 Power Supply Recommendations

The TLV8544 is specified for operation from 1.7 V to 3.6 V (±0.85 V to ±1.8 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 3.6 V can permanently damage the device.

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 100 nF capacitors be placed as close as possible to the operational amplifier power supply pins. For single supply, place a capacitor between V^+ and V^- supply leads. For dual supplies, place one capacitor between V^+ and ground, and one capacitor between V^- and ground.

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Low bandwidth nanopower devices do not have good high frequency (> 1 kHz) AC PSRR rejection against high-frequency switching supplies and other 1 kHz and above noise sources, so extra supply filtering is recommended if kilohertz or above noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

The V+ pin should be bypassed to ground with a low ESR capacitor.

The optimum placement is closest to the V+ and ground pins.

Care should be taken to minimize the loop area formed by the bypass capacitor connection between V+ and ground.

The ground pin should be connected to the PCB ground plane at the pin of the device.

The feedback components should be placed as close to the device as possible to minimize stray impedance.

10.2 Layout Example

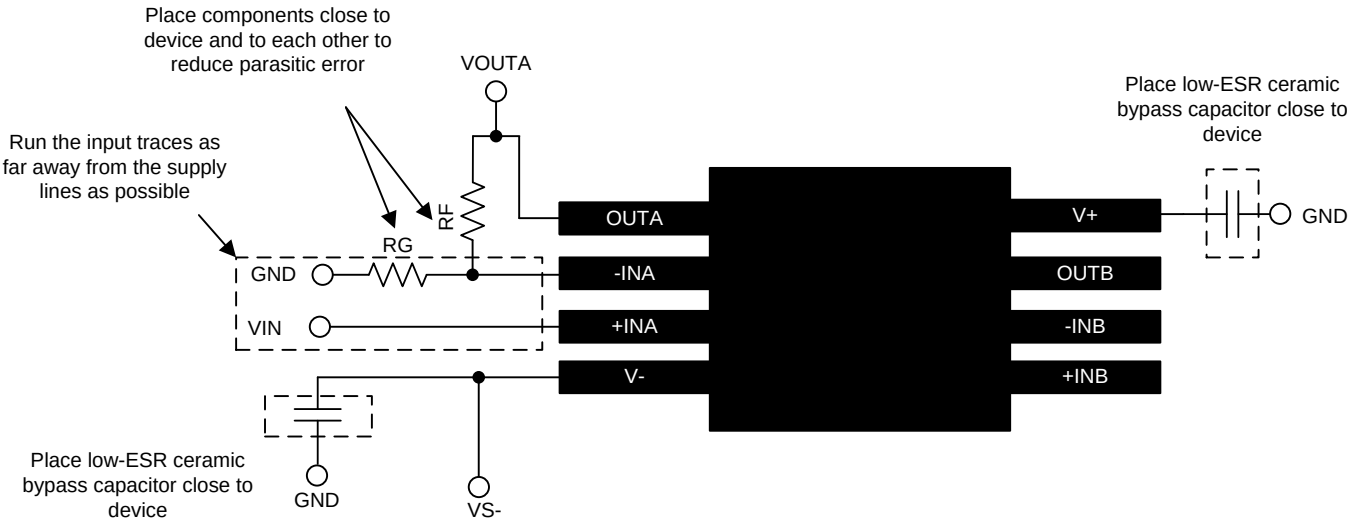


Figure 11. Layout Example of a Typical Dual Channel Package (Top View)

ADVANCE INFORMATION

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

TINA-TI SPICE-Based Analog Simulation Program

DIP Adapter Evaluation Module

TI Universal Operational Amplifier Evaluation Module

TI FilterPro Filter Design Software

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *AN-1798 Designing with Electro-Chemical Sensors*
- *AN-1803 Design Considerations for a Transimpedance Amplifier*
- *AN-1852 Designing With pH Electrodes*
- *Compensate Transimpedance Amplifiers Intuitively*
- *Transimpedance Considerations for High-Speed Operational Amplifiers*
- *Noise Analysis of FET Transimpedance Amplifiers*
- *Circuit Board Layout Techniques*
- *Handbook of Operational Amplifier Applications*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV8544PWT	ACTIVE	TSSOP	PW	14	250	TBD	Call TI	Call TI	-40 to 125		Samples
TLV8544PWR	PREVIEW	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		
TLV8544PWT	PREVIEW	TSSOP	PW	14	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

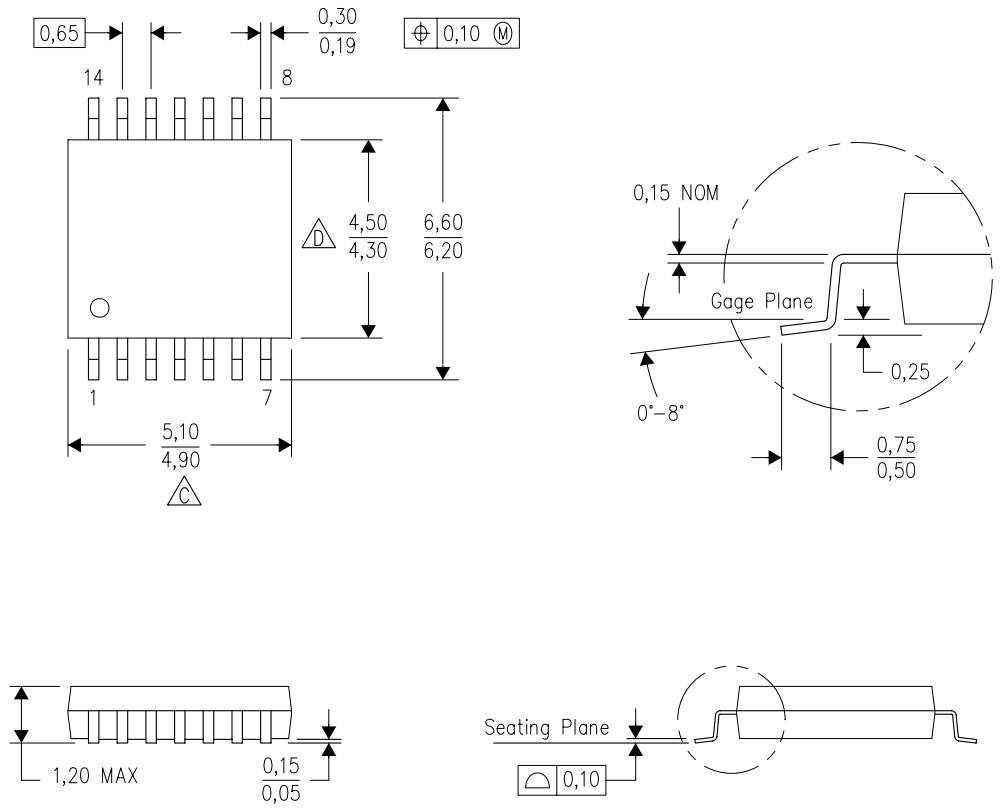
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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