TLV840EVM Voltage Supervisor User Guide

This user guide describes the TLV840EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

Contents

1 Introduction 3
1.1 Related Documentation 4
1.2 TLV840 Applications 4
2 Schematic, Bill of Materials, and Layout 4
2.1 TLV840EVM Schematic 5
2.2 TLV840EVM Bill of Materials 6
2.3 Layout and Component Placement 7
3 EVM Connectors 9
3.1 EVM Test Points 9
3.2 EVM Jumpers 9
4 EVM Setup and Operation 10
4.1 Input Power (V_{DD}) 10
4.2 Monitoring Voltage on VDD 10
4.3 Reset Output ($\overline{\text{RESET}}$) 11
4.4 Reset Time Delay Programming (Program t_D via CT) 11

List of Figures

1 TLV840EVM Board Top 3
2 TLV840EVM Board Bottom 4
3 TLV840EVM Schematic 5
4 Component Placement—Top Assembly 7
5 Component Placement—Bottom Assembly 7
6 Layout—Top 7
7 Layout—Bottom 7
8 Top Layer 7
9 Bottom Layer 7
10 Top Solder Mask 8
11 TLV840EVM $\overline{\text{RESET}}$ Asserted Due to $\overline{\text{MR}}$ Pulled Low 10
12 TLV840EVM $\overline{\text{RESET}}$ Deasserted Due to $\overline{\text{MR}}$ Pulled High, C_T Floating 10
13 TLV840EVM Glitch Immunity 10
14 TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Tied to GND Through 0.1-µF Capacitor 12
15 TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Tied to GND Through 0.01-µF Capacitor 12
16 TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Floating 12

List of Tables

1 BOM 6
2 Test Points 9
3 List of Onboard Jumpers 9
4 Nominal Supply and Typical Threshold Voltages 10

Copyright © 2020, Texas Instruments Incorporated

Trademarks

All trademarks are the property of their respective owners.

Copyright © 2020, Texas Instruments Incorporated

1 Introduction

The TLV840EVM is an evaluation module (EVM) for the TLV840 voltage supervisor. The TLV840EVM can be used with any TLV840 device variant but note that if using the push-pull variants (TLV840PLXX or TLV840PHXX), the shunt on J2 must be removed as push-pull devices do not use a pull-up resistor so R1 must be disconnected. If using TLV840EVM with the active-high variant (TLV840PHXX), the active-low $\overline{\text{RESET}}$ label on the EVM board and throughout this user guide becomes active-high RESET. The TLV840 has a supply voltage range of 0.7 V to 6 V, and offers input connections for all device input and output pins. Test points are provided to give the user access to an extra ground connection if needed for oscilloscope or multimeter measurements.

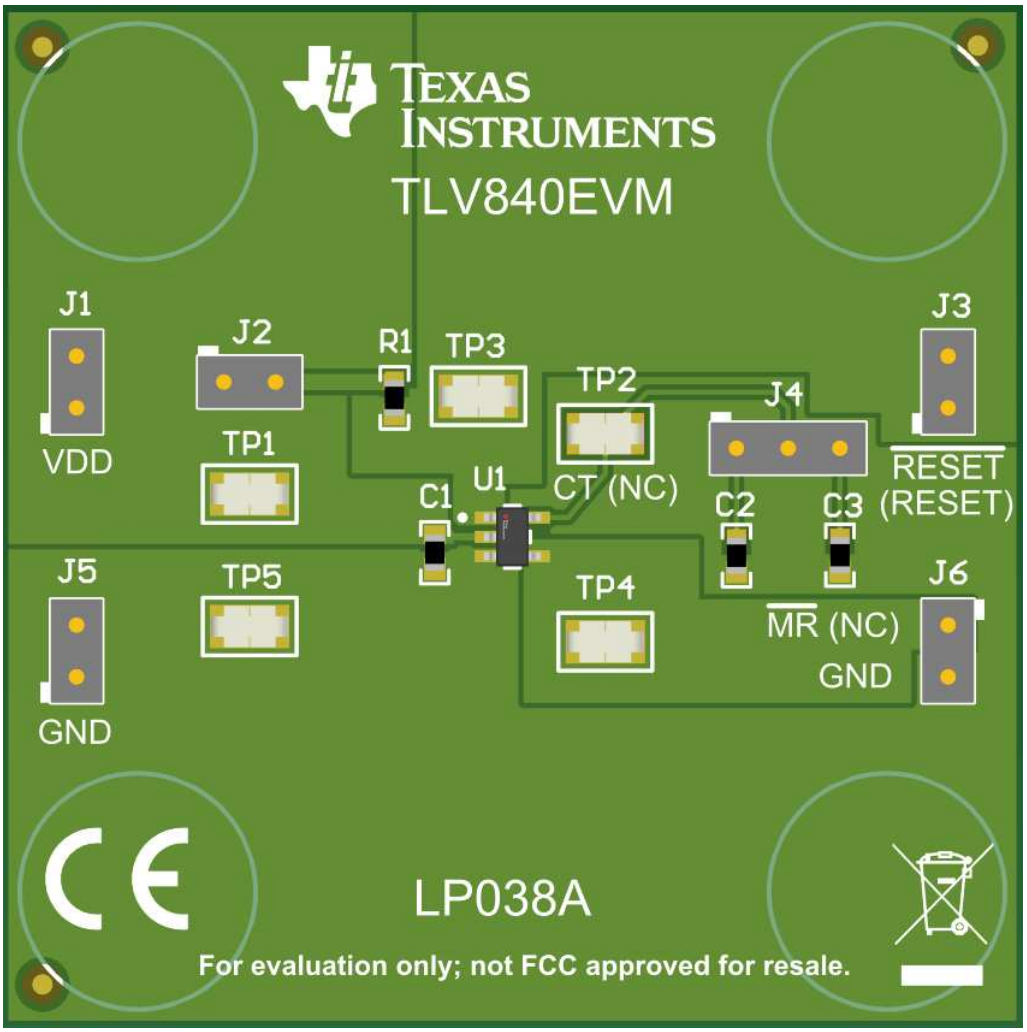

Figure 1. TLV840EVM Board Top

Copyright © 2020, Texas Instruments Incorporated

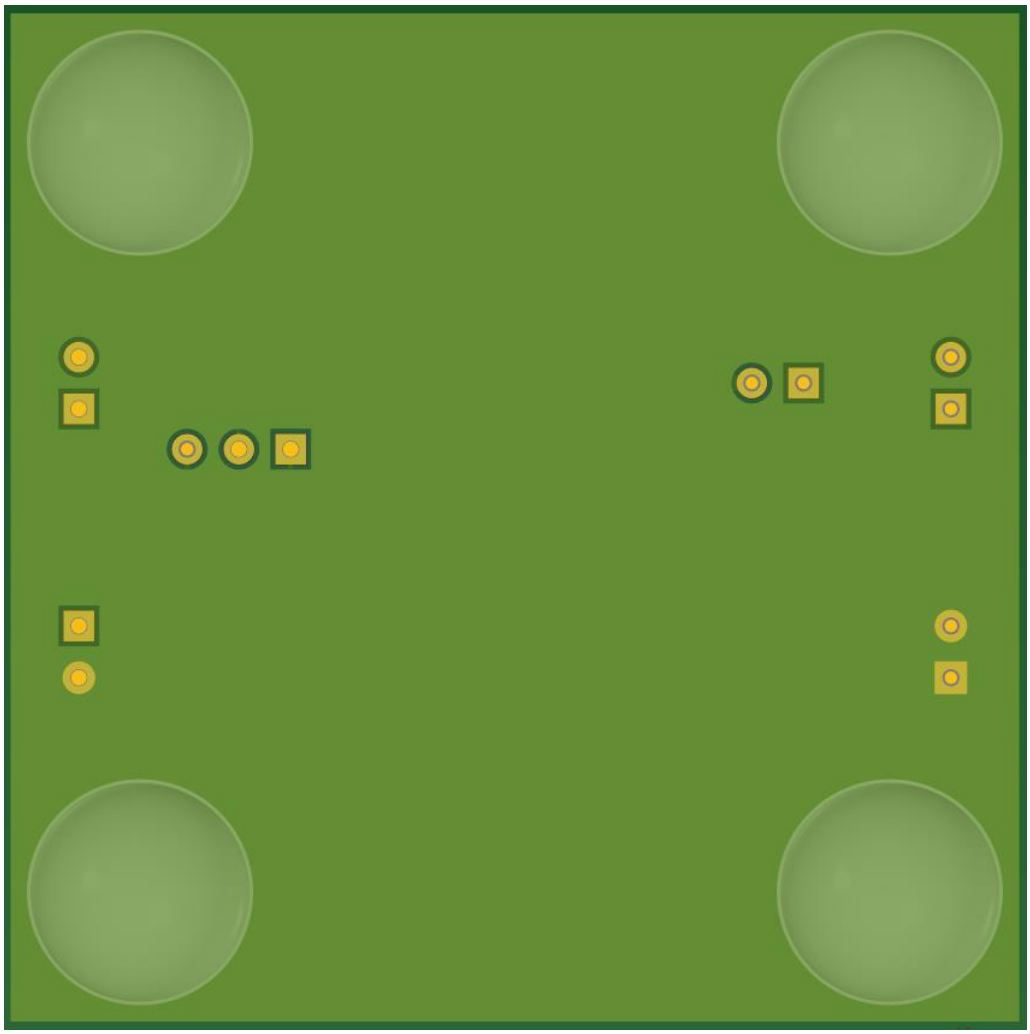

Figure 2. TLV840EVM Board Bottom

1.1 Related Documentation

TLV840 Nano-Power, Ultra-Low Voltage Supervisor with Ajustable Reset Time Delay data sheet, SBVSBC3

1.2 TLV840 Applications

- Motor Drives
- Factory Automation and Control
- Home Theater and Entertainment
- Electronic Point of Sale
- Grid Infrastructure
- Data Center and Enterprise Computing
- Multifunction Printer

2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TLV840EVM schematic, bill of materials (BOM), and layout.

Copyright © 2020, Texas Instruments Incorporated

2.1 TLV840EVM Schematic

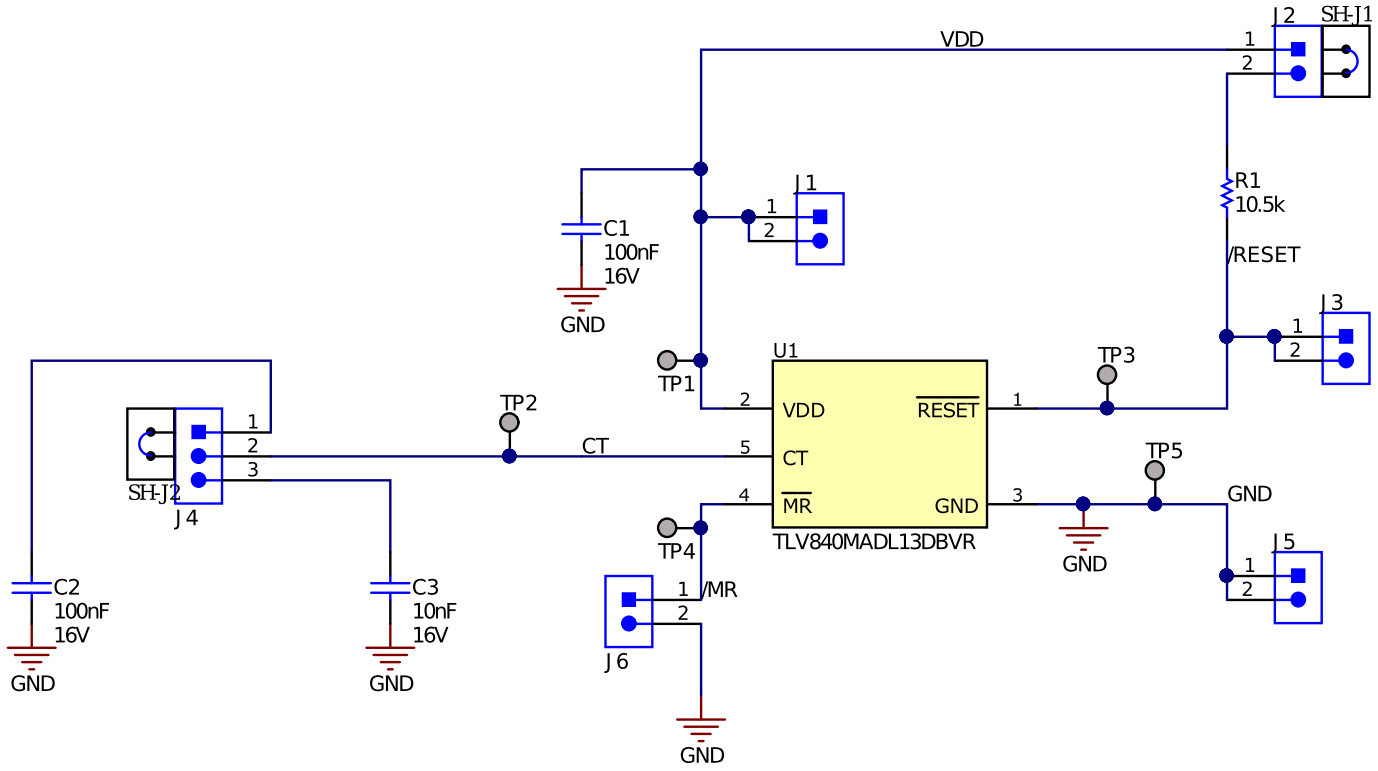

Figure 3. TLV840EVM Schematic

Copyright © 2020, Texas Instruments Incorporated

2.2 TLV840EVM Bill of Materials

Table 1. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB	1		Printed Circuit Board		TLV840EVM	Any
C1, C2	2	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 10%, X7R, 0603	0603	C0603C104K4RACTU	Kemet
C3	1	0.01 µF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	0603	C0603C103K4RACTU	Kemet
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J5, J6	5		Header, 100mil, 2x1, TH	Header, 2x1, 100mil, TH	800-10-002-10-001000	Mill-Max
J4	1		Header, 100mil, 3x1, TH	Header, 3x1, 100mil, TH	800-10-003-10-001000	Mill-Max
R1	1	10.5k	RES, 10.5 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710K5L	Yageo America
SH-J1, SH-J2	2		Shunt, 100mil, Tin plated, Black	Shunt Connector Black Open Top, 2x1	SNT-100-BK-T-H	Samtec
TP1, TP2, TP3, TP4, TP5	5		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		Ultra-Low Voltage Supervisor with Adjustable Reset Time Delay and Manual Reset Option	SOT23-5	TLV840MADL13DBVR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

Copyright © 2020, Texas Instruments Incorporated

2.3 Layout and Component Placement

Figure 4 and Figure 5 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 6 and Figure 7 show the top and bottom layouts, Figure 8 and Figure 9 show the top and bottom layers, and Figure 10 shows the top solder mask of the EVM.

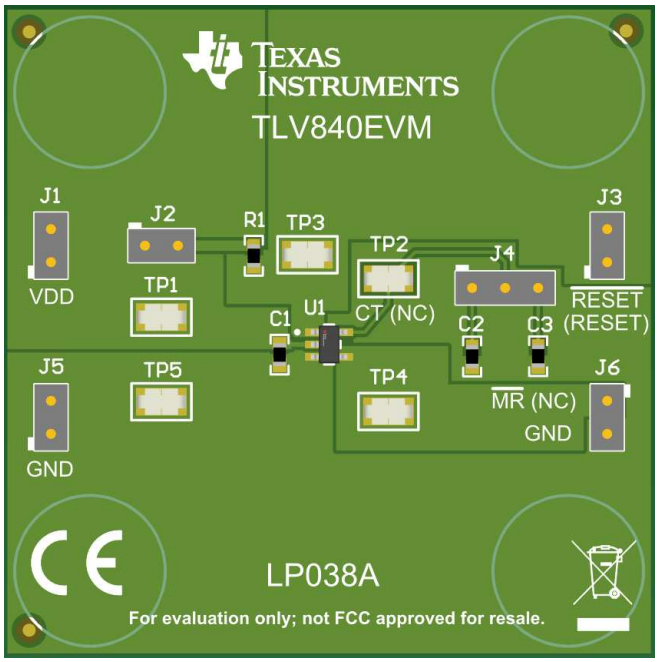

Figure 4. Component Placement—Top Assembly

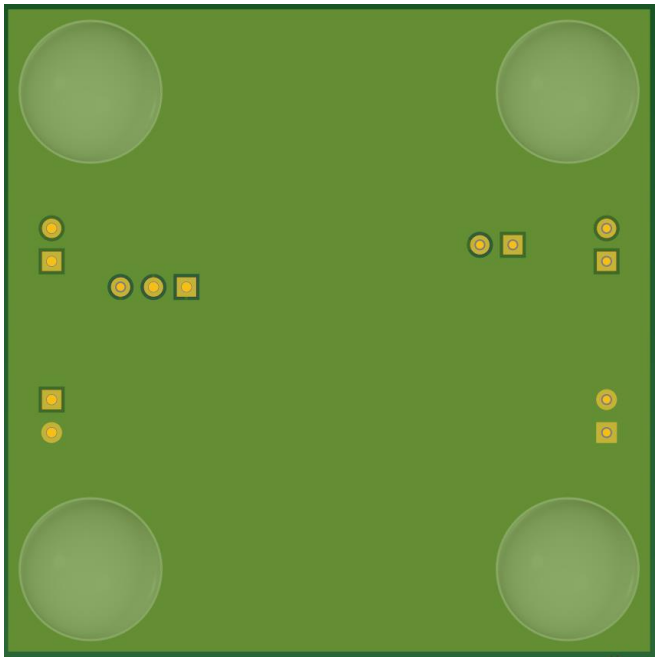

Figure 5. Component Placement—Bottom Assembly

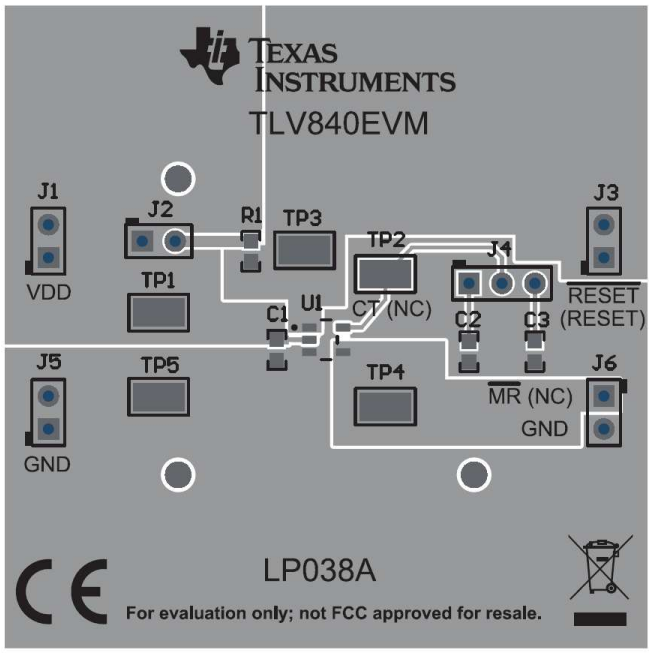

Figure 6. Layout—Top

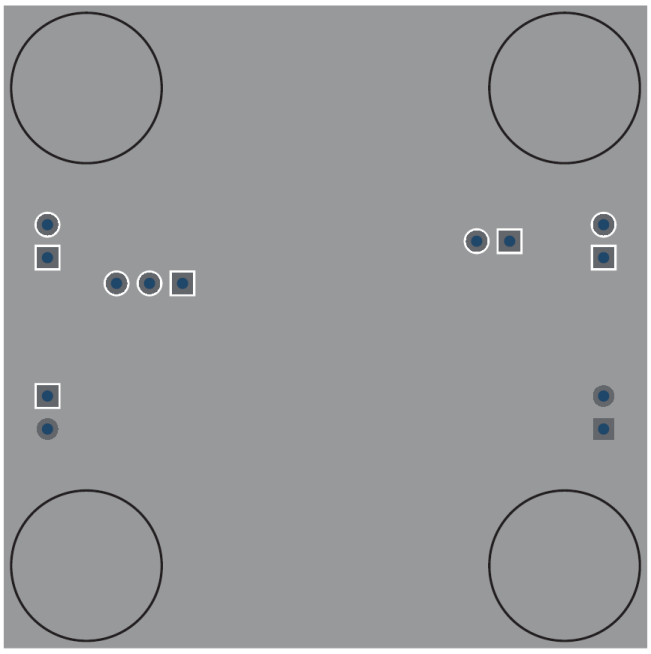

Figure 7. Layout—Bottom

Copyright © 2020, Texas Instruments Incorporated

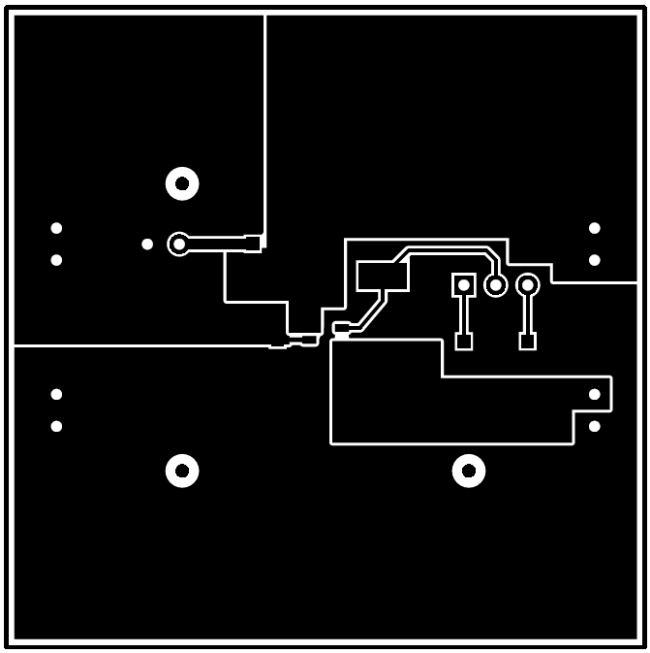

Figure 8. Top Layer

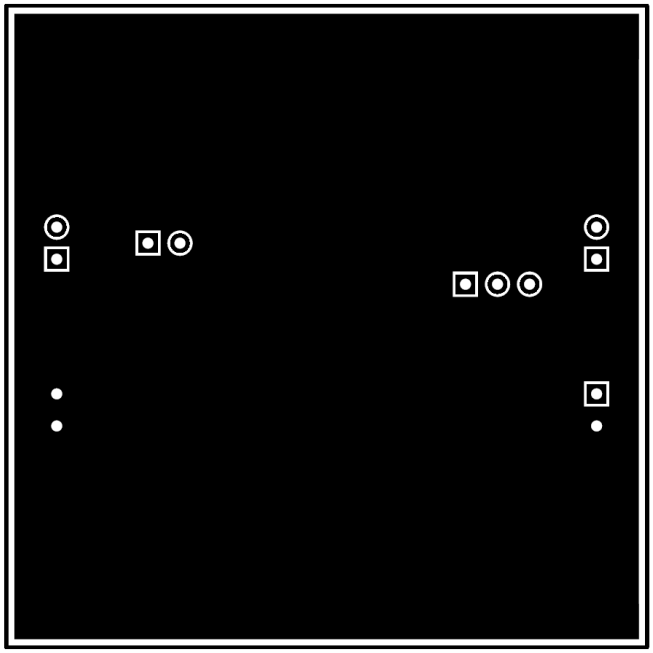

Figure 9. Bottom Layer

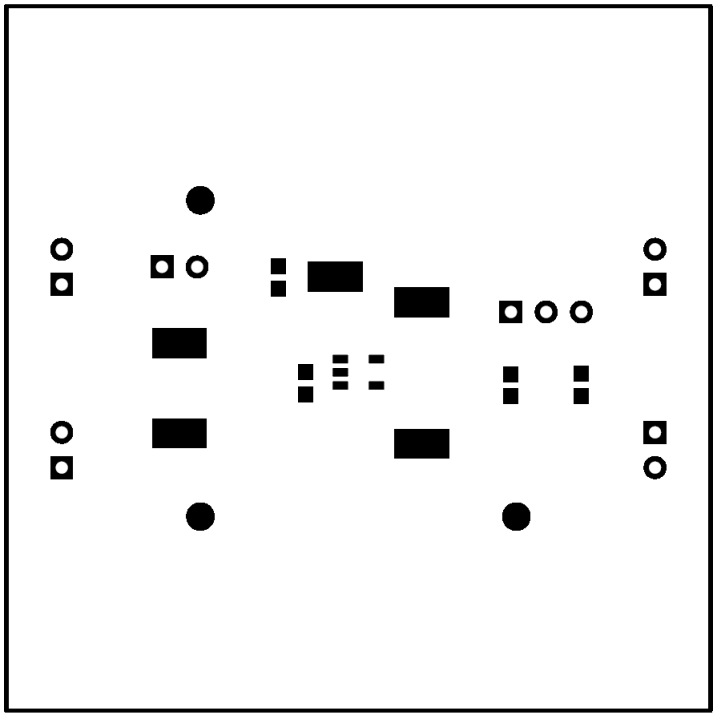

Figure 10. Top Solder Mask

Copyright © 2020, Texas Instruments Incorporated

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 2 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 2. Test Points

TEST POINT NUMBER	TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
TP1	VDD	Connection to VDD pin	Allows user to monitor the VDD pin. The VDD pin connects to the input power supply.
TP2	CT	Connection to CT pin	Allows user to monitor the CT pin. This pin charges up according to the CT pin configuration. The CT capacitor sets the reset delay.
TP3	$\overline{\text{RESET}}$	Connection to $\overline{\text{RESET}}$ pin	Allows user to monitor the $\overline{\text{RESET}}$ output pin.
TP4	$\overline{\text{MR}}$	Connection to $\overline{\text{MR}}$ pin	Allows user to monitor the logic level of the manual reset pin. Logic low on $\overline{\text{MR}}$ forces a reset.
TP5	GND	Connection to GND pin.	Allows user to connect to the ground plane.

3.2 EVM Jumpers

Table 3 lists the jumpers on the TLV840EVM. As ordered, the EVM will have five jumpers installed.

Table 3. List of Onboard Jumpers

JUMPER	DEFAULT CONNECTION	DESCRIPTION
J1	Shorted	Both pins on J1 are connected together. Connect either pin on jumper J1 to the input power supply.
J2	Closed	Connect a shunt jumper to jumper J2 to use R1 as the pull-up resistor on the $\overline{\text{RESET}}$ output pin.
J3	Shorted	Both pins on J3 are connected together. Use either pin on jumper J3 to monitor the $\overline{\text{RESET}}$ output pin.
J4	Closed (pin 1, pin 2)	Jumper J4 configures the CT pin to set the reset delay. Connect a shunt jumper to pin 1 and pin 2 of jumper J4 to use C2 as the delay capacitor for the CT pin. Connect shunt jumper to pin 2 and pin 3 of jumper J4 to use C3 as the delay capacitor. Remove shunt jumper from jumper J4 to set the default fixed delay of 80 µs (maximum).
J5	Shorted	Both pins on J5 are connected together. Use either pin on jumper J5 as the ground connection.
J6	Open	Jumper J6 configures the manual reset pin. Remove shunt jumper from J6 and leave floating for normal operation. Connect shunt jumper to J6 to force a reset. Pin 1 of jumper J6 can also be connected to a control signal to set the logic level on $\overline{\text{MR}}$ pin. If pin 1 on jumper J6 is logic low, the device remains in reset.

Copyright © 2020, Texas Instruments Incorporated

4 EVM Setup and Operation

This section describes the functionality and operation of the TLV840EVM. The user must read the TLV840 datasheet for electrical characteristics of the device.

4.1 Input Power (V_{DD})

The VDD supply is connected through the J1 header on board. Both pins of jumper J1 are connected together so power can be applied to either pin. Supply voltage is dependent on what the user wants to monitor, but the range is 0.7 V to 6 V. Table 4 details the nominal supply and typical threshold voltage.

Table 4. Nominal Supply and Typical Threshold Voltages

Device	Nominal Supply Voltage (V)	Typical Threshold Voltage (V)
TLV840MADL13	1.3	1.3 ± 1%

4.1.1 Manual Reset ($\overline{MR}$)

The TLV840 devices offers a manual reset pin that is utilized via jumper J6. If a shunt jumper is placed on jumper J6, the $\overline{RESET}$ pin is asserted and forced into a low state. After the shunt jumper is removed and VDD is above its reset threshold, $\overline{MR}$ returns to a logic high due to the internal pull-up resistor, and $\overline{RESET}$ is deasserted to logic high after the user-defined delay expires. If jumper J6 is left floating, the device operates normally as the $\overline{MR}$ pin defaults to logic high. Pin 1 of jumper J6 can also be connected to a control signal to set the logic level on $\overline{MR}$ pin. If pin 1 on jumper J6 is logic low, the device asserts a reset. There is also a test point TP4 connected directly to the $\overline{MR}$ pin in case the user wants to monitor the $\overline{MR}$ pin. See Figure 11 through Figure 14.

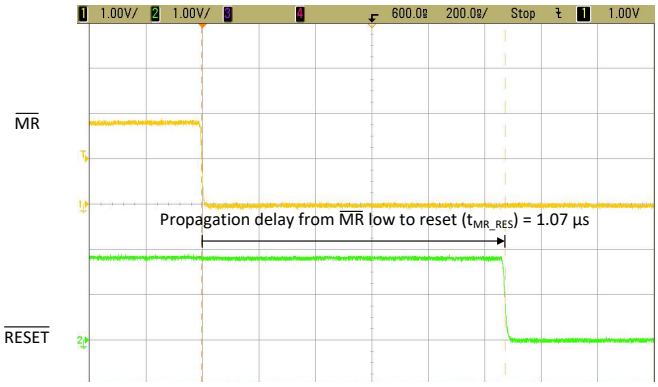

Figure 11. TLV840EVM $\overline{RESET}$ Asserted Due to $\overline{MR}$ Pulled Low

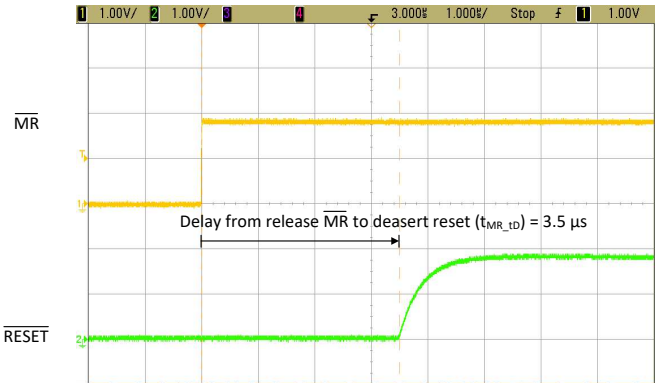

Figure 12. TLV840EVM $\overline{RESET}$ Deasserted Due to $\overline{MR}$ Pulled High, C_T Floating

4.2 Monitoring Voltage on VDD

The TLV840 device monitors voltage via the VDD pin. The EVM provides jumper J1 and test point TP1 for connecting the power supply input to the VDD pin. If the voltage on this pin drops below V_{IT-}, $\overline{RESET}$ is asserted low. The VDD pin is connected internally to a comparator through an internal resistor divider at the positive input and the negative input is connected to an internal reference. The internal resistor divider is set to provide the input voltage threshold to cause a reset, V_{IT-}, that corresponds to the chosen device variant. Please see the Device Comparison Table in the TLV840 Datasheet for more information on the different device variants.

Upon startup, the TLV840 requires VDD to be above $V_{DD\ (MIN)}$ = 0.7 V before the $\overline{RESET}$ output is in the correct logic state. The TLV840 has built-in glitch immunity so voltage transients on VDD are ignored if the pulse duration is 10 µs or less as shown in Figure 13. The glitch immunity specification depends on the amplitude of the voltage transient and the operating conditions. Please see the Glitch Immunity specification in the Timing Requirements section of the TLV840 Datasheet for more detailed information.

Copyright © 2020, Texas Instruments Incorporated

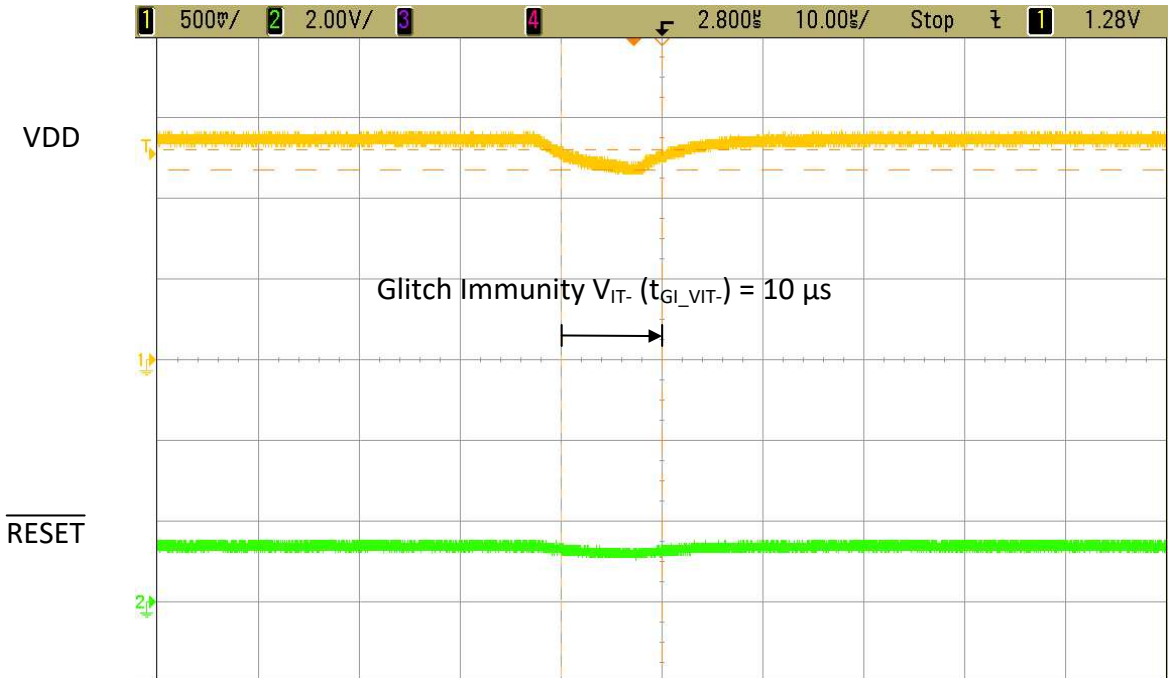

Figure 13. TLV840EVM Glitch Immunity

4.3 Reset Output ($\overline{RESET}$)

The TLV840EVM comes populated with TLV840MADL29 device variant which has open-drain, active-low output topology for the $\overline{RESET}$ pin. The other device variants provide different output topolgies and can be used on this EVM. Note: if using a TLV840 device variant with push-pull output topology, the pull-up resistor must be disconnected by leaving jumper J2 open. The EVM provides a jumper J3 and a test point TP3 connected directly to the $\overline{RESET}$ pin for monitoring and/or interfacing to other devices. The reset signal will be asserted low when $\overline{MR}$ is pulled low or when the voltage on the VDD pin falls below VIT-. When the voltage on VDD rises higher than the hysteresis voltage above the threshold voltage, and the $\overline{MR}$ pin is pulled high or floating, the reset pins will deassert and remain deasserted until a reset condition occurs again.

4.4 Reset Time Delay Programming (Program t_D via CT)

The TLV840 device has two options for setting the $\overline{RESET}$ time delay: connect CT pin to a capacitor to GND, or leave CT pin floating. The reset time delay can be set to a minimum value of 80 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed to any value within the range by connecting a capacitor no larger than 10 µF between CT pin and GND. The relationship between external capacitor (C_{CT_EXT}) at CT pin and the $\overline{RESET}$ time delay is given by Equation 1.

$$t_D = -\ln(0.29) \times R_{CT} \times C_{CT_EXT} + t_D \text{ (no cap)} \quad (1)$$

Equation 1 is simplified to Equation 2 by plugging R_{CT} and $T_{D(no\ cap)}$ given in the Electrical Characteristics Table in TLV840 Datasheet

$$t_D = 618937 \times C_{CT_EXT} + 80\mu s \quad (2)$$

Equation 3 solves for external capacitor value (C_{CT_EXT})

$$C_{CT_EXT} = (t_D - 80\mu s) \div 618937 \quad (3)$$

The recommended maximum delay capacitor for the TLV840 is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

Copyright © 2020, Texas Instruments Incorporated

The EVM provides the jumper J4 to configure the CT pin and test point TP2 to monitor the CT pin. Place a shunt jumper on pin 1 (left pin) and pin 2 (middle pin) of jumper J4 to connect CT to delay capacitor C2. This connects the CT pin to a 0.1-µF capacitor to set the $\overline{\text{RESET}}$ delay (t_D) to ~61.9 ms as shown in Figure 14. Or place a shunt jumper on pin 2 (middle pin) and pin 3 (right pin) of jumper J4 to connect CT to delay capacitor C3. This connects the CT pin to a 0.01-µF capacitor to set the $\overline{\text{RESET}}$ delay (t_D) to ~6.2 ms as shown in Figure 15. By removing the shunt jumper from jumper J4, the $\overline{\text{RESET}}$ time delay defaults to the minimum value of 40 µs. Figure 16 shows the actual delay with no capacitor may be shorter than the typical value of 40 µs. If using a different delay capacitor, the capacitor must be ≥ 100pF to be recognized.

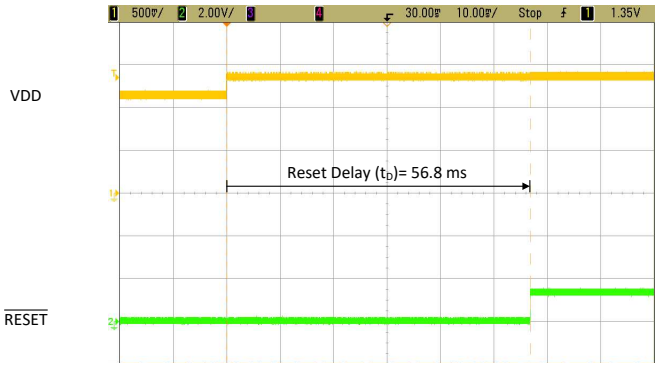

Figure 14. TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Tied to GND Through 0.1-µF Capacitor

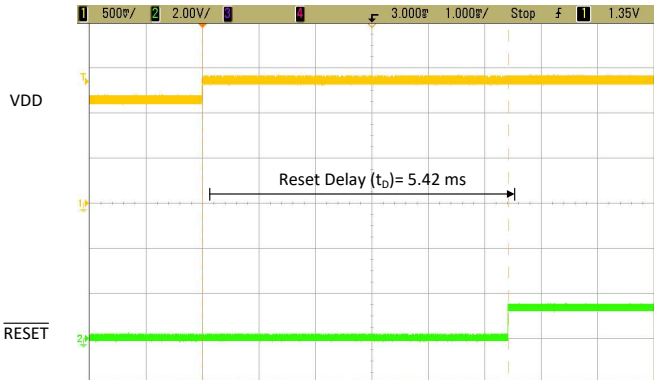

Figure 15. TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Tied to GND Through 0.01-µF Capacitor



Figure 16. TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Floating

Revision History

DATE	REVISION	NOTES
February 2020	*	Initial Release

Copyright © 2020, Texas Instruments Incorporated

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated