200-mA, Low-I_Q, Low-Noise, Low-Dropout Regulator for Portable Devices

FEATURES

- **Very Low Dropout: 250 mV at 150 mA**
- **0.5% Typical Accuracy**
- **1.5% Accuracy over Temperature**
- **Low I_Q: 25 µA**
- **Fixed-Output Voltage Combinations Possible from 1.2 V to 5.0 V(1)**
- **High PSRR:**
  - **70 dB at 100 Hz**
  - **50 dB at 1 MHz**
- **Stable with Effective Capacitance of 0.1 µF(2)**
- **Thermal Shutdown and Overcurrent Protection**
- **Package: 1-mm × 1-mm DFN (SON)**

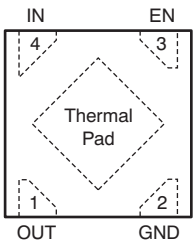
(1) See Package Option Addendum at end of this document for complete list of available voltage options.

(2) See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

APPLICATIONS

- **Wireless Handsets, Smart Phones, and PDAs**
- **MP3 Players and Other Handheld Devices**
- **WLAN and Other PC Add-On Cards**

TLV707 Series
DQN PACKAGE
1-mm × 1-mm DFN-4
(TOP VIEW)



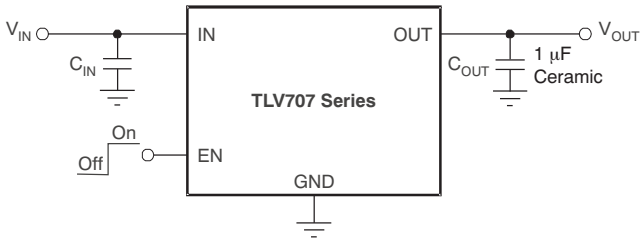
DESCRIPTION

The TLV707 series (TLV707xx and TLV707xxP) of low-dropout linear regulators (LDOs) are low quiescent current devices with excellent line and load transient performance, and are designed for power-sensitive applications. These devices provide a typical accuracy of 0.5%. All versions have thermal shutdown and overcurrent protection for safety. Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. These devices also regulate to the specified accuracy with no output load.

The TLV707xxP also provides an active pull-down circuit to quickly discarge the outputs.

The TLV707 series are available in a 1-mm x 1-mm DFN (SON) package that makes them ideal for handheld applications.

Typical Application Circuit
(Fixed Voltage Versions)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TLV707**xx(x)***Pyyyz*	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8V, 285 = 2.85V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is package quantity. Use ***R*** for reel (3000 pieces), and ***T*** for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 1.2 V to 5.0 V in 50-mV increments are available. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	+6.0	V
	EN	–0.3	+6.0	V
	OUT	–0.3	+6.0	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Ratings(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV707xx, TLV707xxP	UNITS
		DQN (DFN)	
		4 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	249.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	N/A	
θ_{JB}	Junction-to-board thermal resistance	N/A	
ψ_{JT}	Junction-to-top characterization parameter	6.0	
ψ_{JB}	Junction-to-board characterization parameter	N/A	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	T_A < +25°C	T_A = +70°C	T_A = +85°C
DQN	249.9°C/W	400 mW	220 mW	160 mW
DCK	354.4°C/W	282 mW	155.2 mW	112.9 mW

ELECTRICAL CHARACTERISTICS

At V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.0 V (whichever is greater); I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 0.47 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER		TEST CONDITIONS			TLV707 Series MIN	TLV707 Series TYP	TLV707 Series MAX	UNIT
V_{IN}	Input voltage range				2.0		5.5	V
V_O	Output voltage range				1.2		5.0	V
V_{OUT}	DC output accuracy	T_A = +25°C				0.5		%
		V_{OUT} ≥ 1.2 V, T_A = –40°C to +85°C			–1.5		+1.5	%
$\Delta V_O/\Delta V_{IN}$	Line regulation					1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA				10	20	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98 x $V_{OUT(NOM)}$	2.0 V < V_{OUT} ≤ 2.4 V	I_{OUT} = 30 mA		65		mV
				I_{OUT} = 150 mA		325	360	mV
			2.4 V < V_{OUT} ≤ 2.8 V	I_{OUT} = 30 mA		50		mV
				I_{OUT} = 150 mA		250	300	mV
			2.8 V < V_{OUT} ≤ 3.3 V	I_{OUT} = 30 mA		45		mV
				I_{OUT} = 150 mA		220	270	mV
			3.3 V < V_{OUT} ≤ 5.0 V	I_{OUT} = 30 mA		40		mV
				I_{OUT} = 150 mA		200	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$			240	300	450	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA				25	50	µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V				1		µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA		f = 100 Hz		70		dB
				f = 10 kHz		55		dB
				f = 1 MHz		50		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA				45		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA				100		µs
$V_{EN(HI)}$	EN pin high (enabled)				0.9		V_{IN}	V
$V_{EN(LO)}$	EN pin low (disabled)				0		0.4	V
I_{EN}	EN pin current	V_{EN} = 5.5 V				0.01		µA
UVLO	Undervoltage lockout	V_{IN} rising				1.9		V
$R_{PULLDOWN}$	Pull-down resistance (TLV707xxP only)					120		Ω
T_J	Operating junction temperature				–40		+125	°C

(1) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAMS

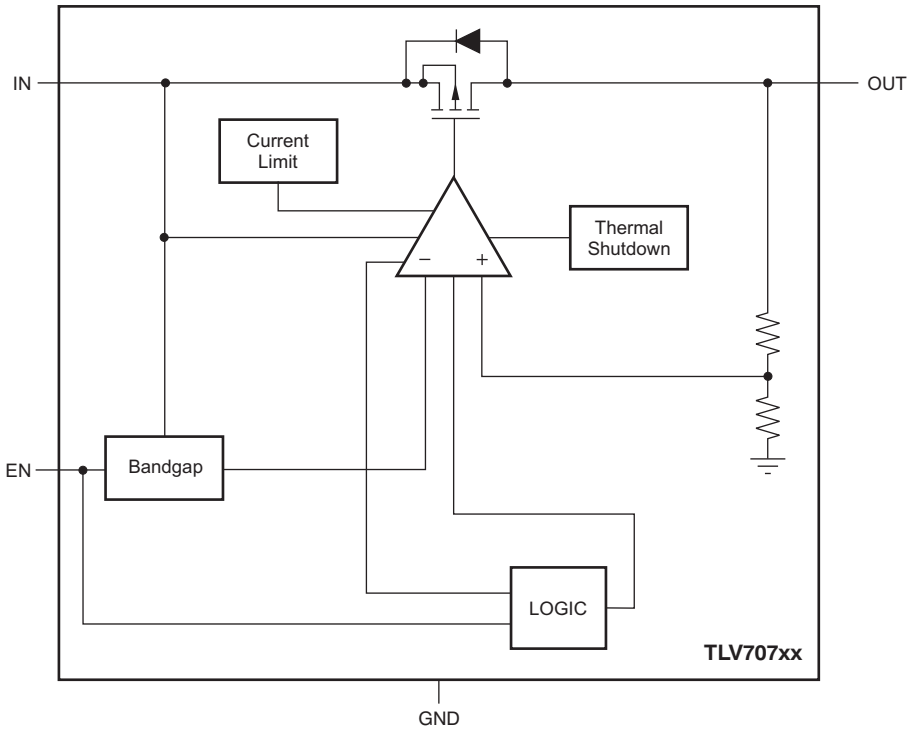


Figure 1. TLV707xx Block Diagram

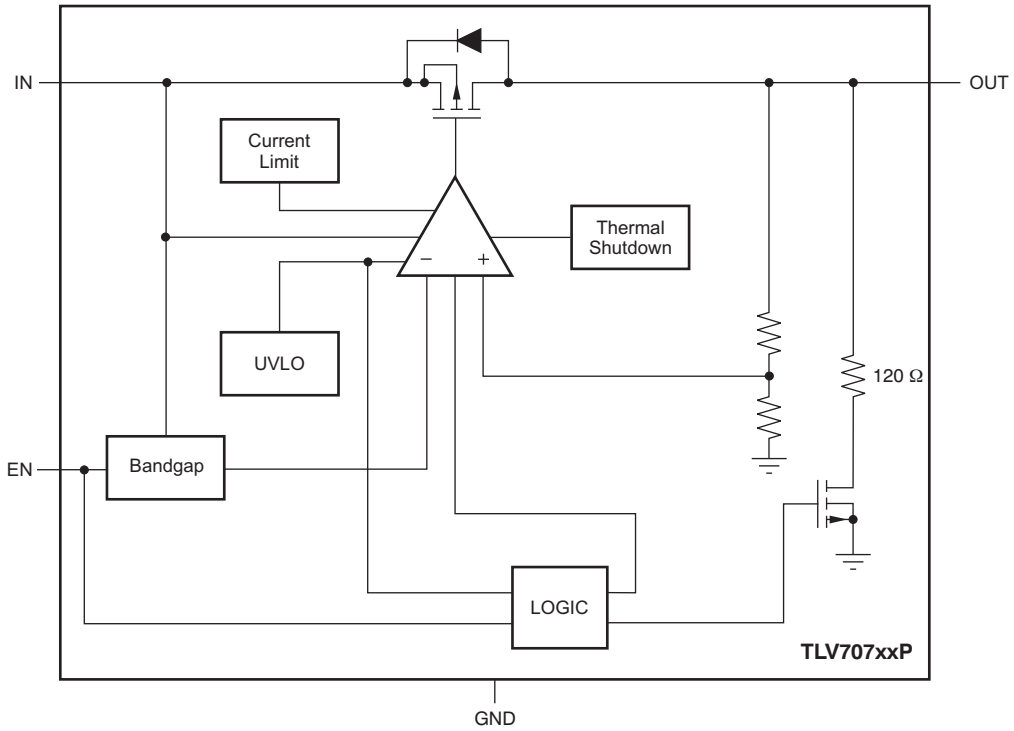
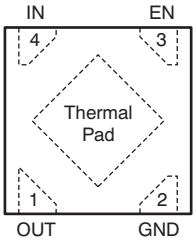


Figure 2. TLV707xxP Block Diagram

PIN CONFIGURATIONS

DQN PACKAGE
DFN-4
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
OUT	1	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	2	Ground pin
EN	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode For TLV707xxP, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
IN	4	Input pin. A small 1µF ceramic capacitor is recommended from this pin to ground for good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
NC	—	No connection. This pin can be tied to ground to improve thermal dissipation.

TYPICAL CHARACTERISTICS

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

LOAD REGULATION

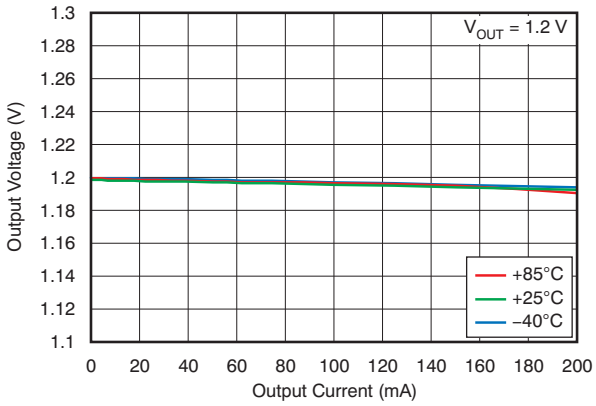


Figure 3.

LOAD REGULATION

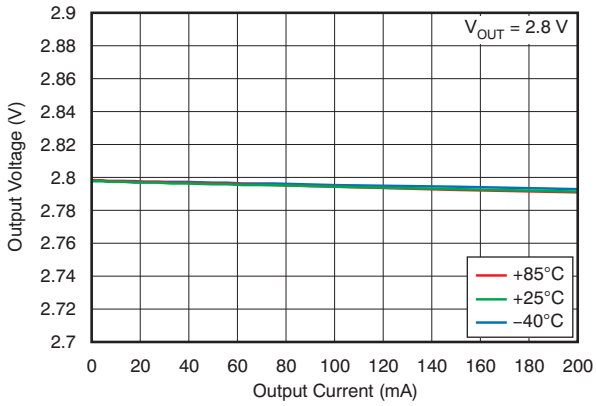


Figure 4.

LOAD REGULATION

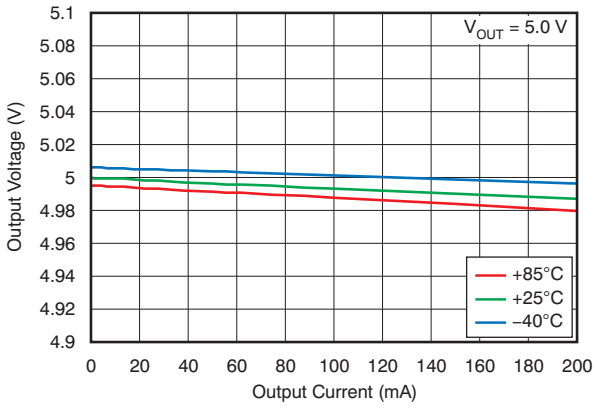


Figure 5.

LINE REGULATION

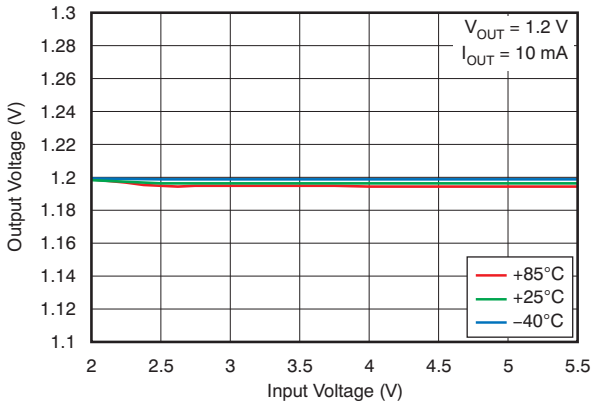


Figure 6.

LINE REGULATION

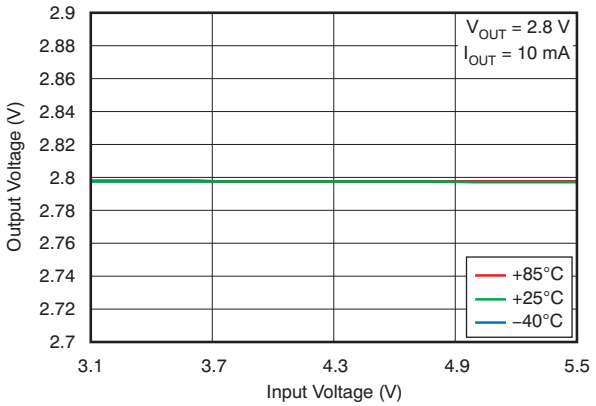


Figure 7.

LINE REGULATION

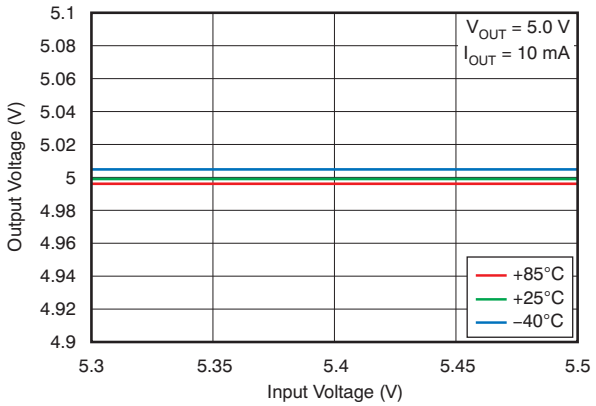


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

LINE REGULATION

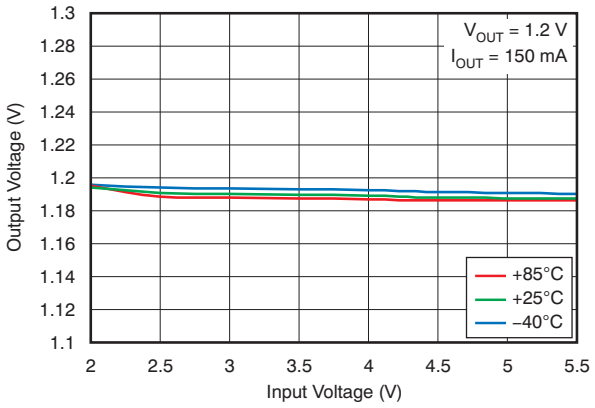


Figure 9.

LINE REGULATION

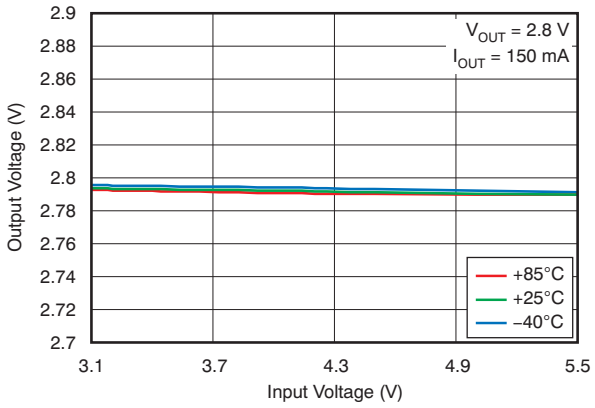


Figure 10.

LINE REGULATION

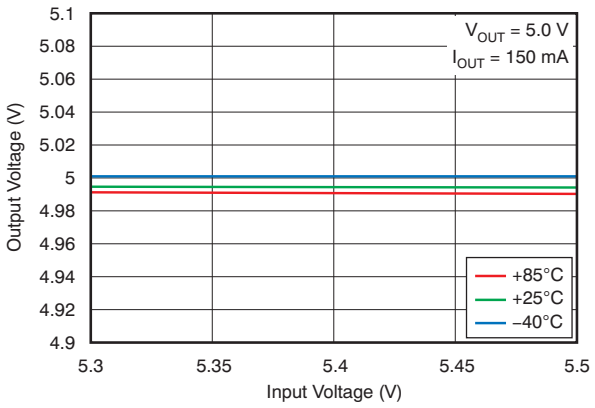


Figure 11.

OUTPUT VOLTAGE vs TEMPERATURE

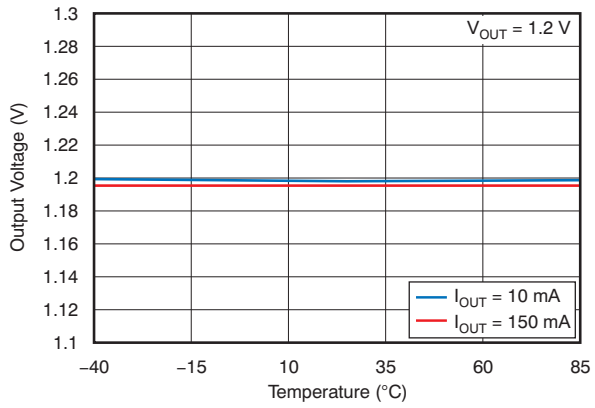


Figure 12.

OUTPUT VOLTAGE vs TEMPERATURE

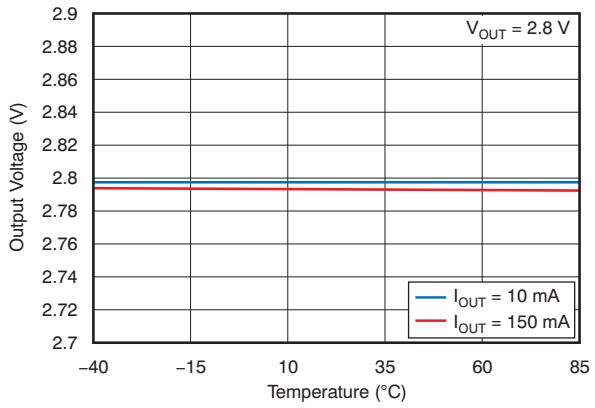


Figure 13.

OUTPUT VOLTAGE vs TEMPERATURE

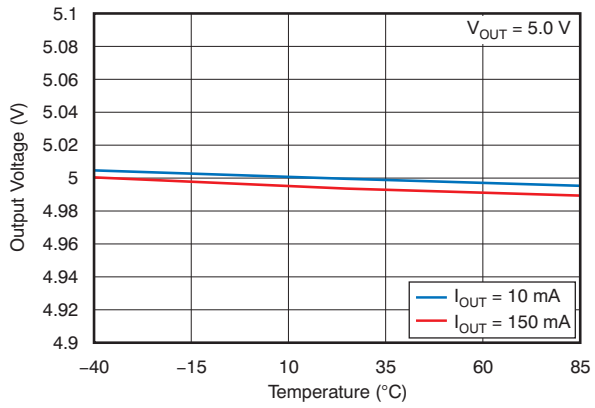


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

DROPOUT VOLTAGE vs INPUT VOLTAGE

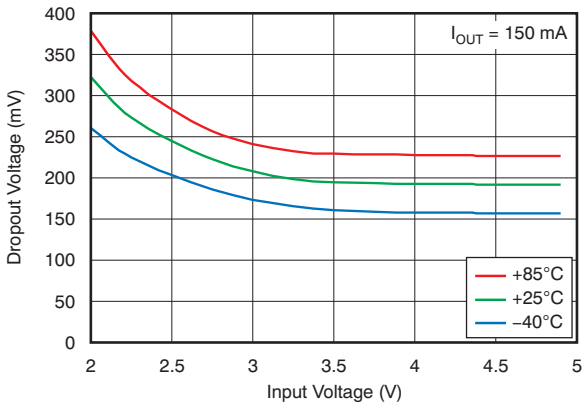


Figure 15.

DROPOUT VOLTAGE vs INPUT VOLTAGE

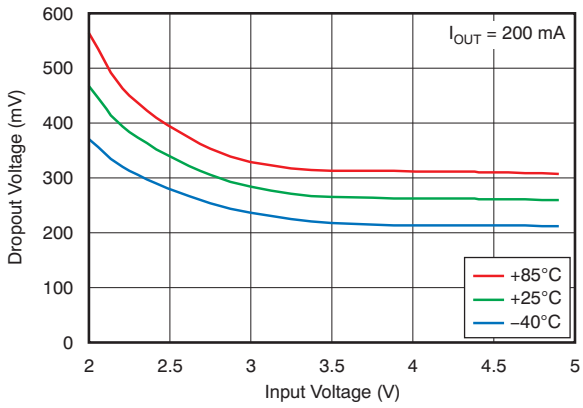


Figure 16.

DROPOUT VOLTAGE vs OUTPUT CURRENT

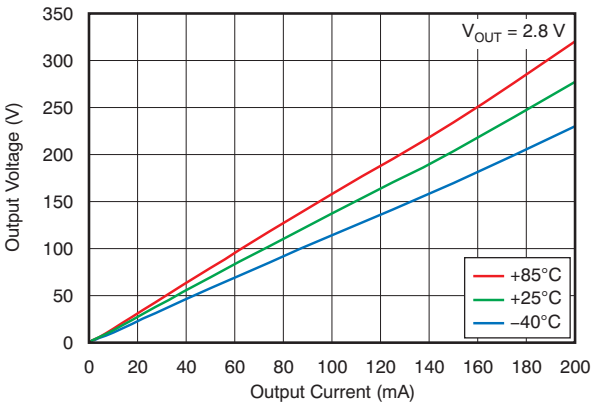


Figure 17.

DROPOUT VOLTAGE vs OUTPUT CURRENT

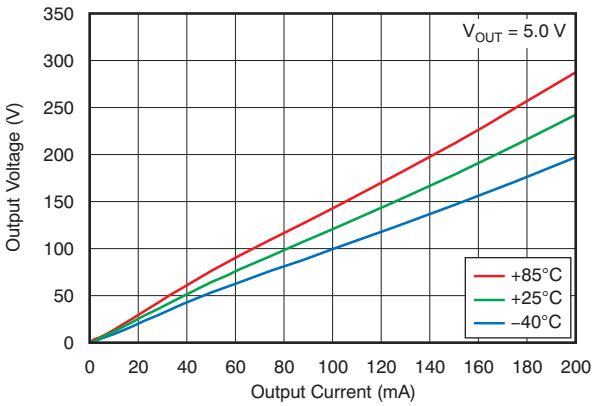


Figure 18.

GROUND PIN CURRENT vs INPUT VOLTAGE

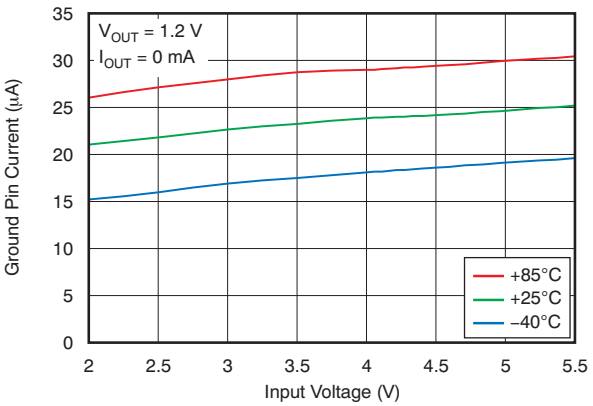


Figure 19.

GROUND PIN CURRENT vs INPUT VOLTAGE

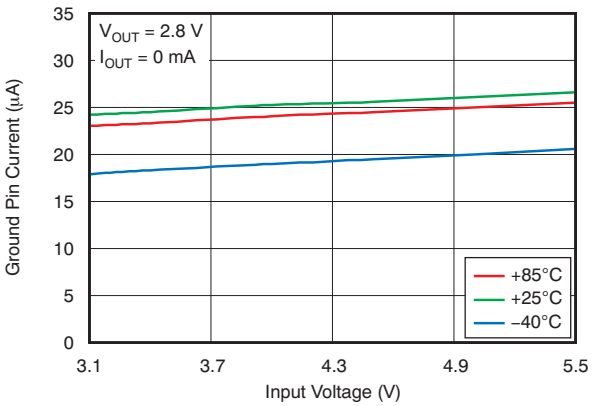


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At $V_{IN} = V_{OUT(TYP)} + 0.5$ V or 2.0 V (whichever is greater); $I_{OUT} = 10$ mA, $V_{EN} = V_{IN}$, $C_{OUT} = 1$ µF, and $T_A = –40°C$ to +85°C, unless otherwise noted. Typical values are at $T_A = +25°C$.

GROUND PIN CURRENT vs INPUT VOLTAGE

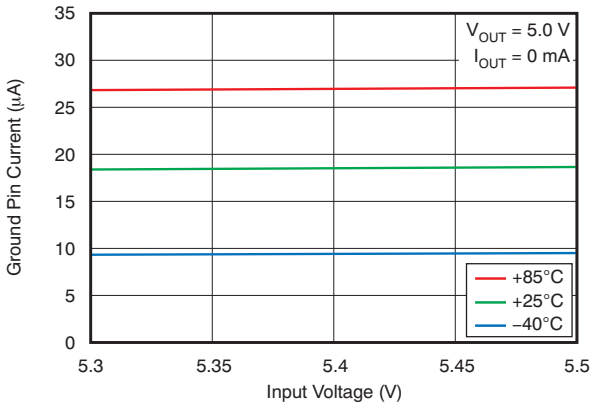


Figure 21.

GROUND PIN CURRENT vs TEMPERATURE

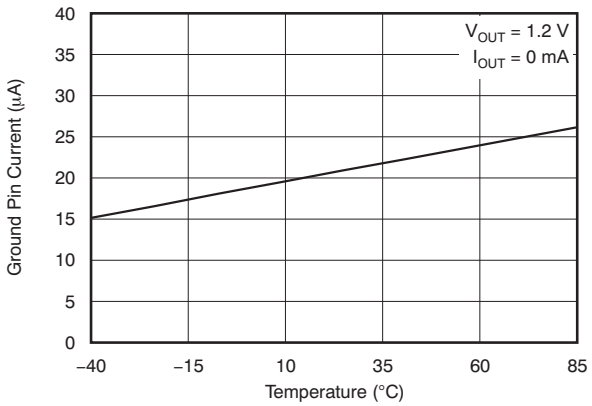


Figure 22.

GROUND PIN CURRENT vs TEMPERATURE

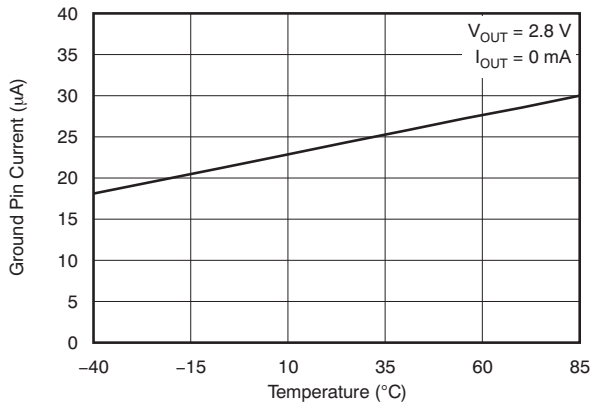


Figure 23.

GROUND PIN CURRENT vs TEMPERATURE

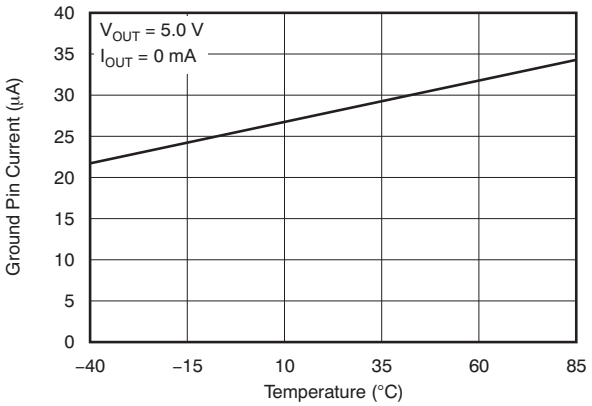


Figure 24.

GROUND PIN CURRENT vs OUTPUT CURRENT

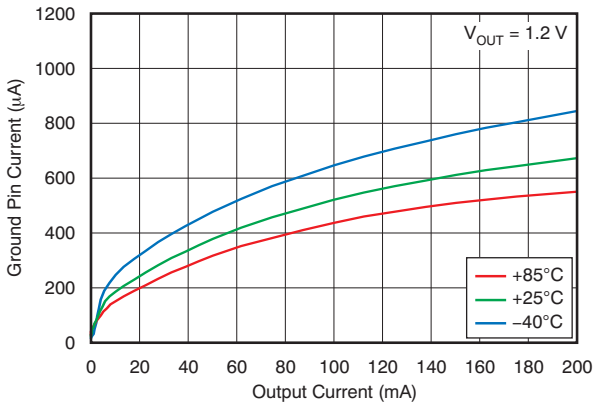


Figure 25.

GROUND PIN CURRENT vs OUTPUT CURRENT

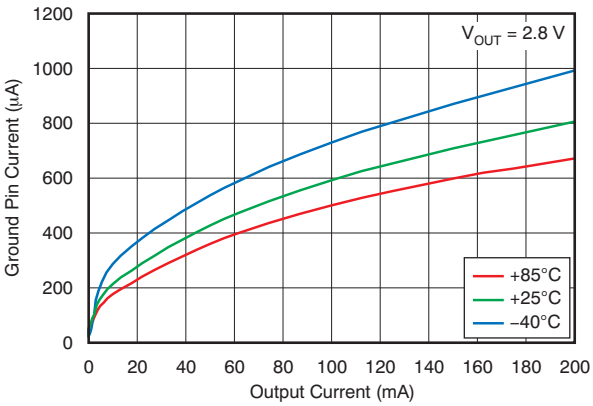


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

GROUND PIN CURRENT vs OUTPUT CURRENT

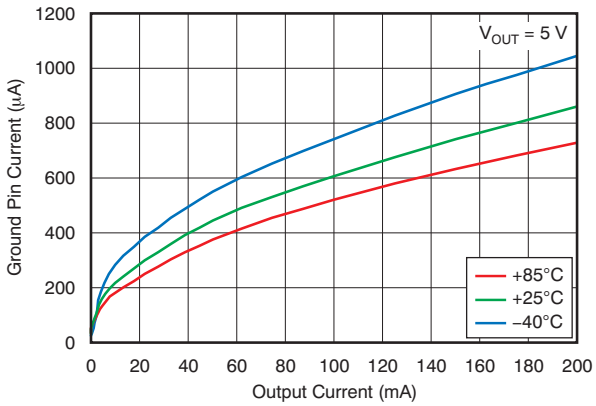


Figure 27.

SHUTDOWN CURRENT vs INPUT VOLTAGE

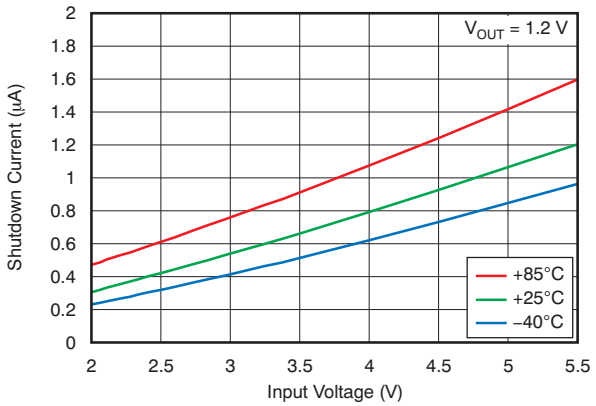


Figure 28.

SHUTDOWN CURRENT vs INPUT VOLTAGE

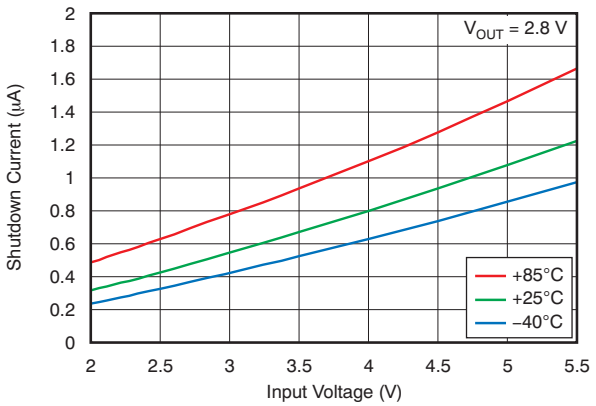


Figure 29.

SHUTDOWN CURRENT vs INPUT VOLTAGE

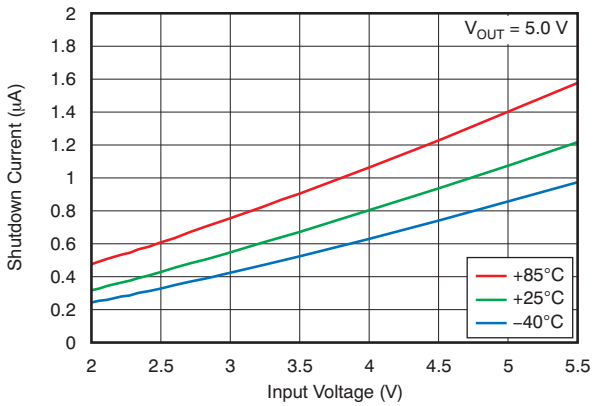


Figure 30.

CURRENT LIMIT vs INPUT VOLTAGE

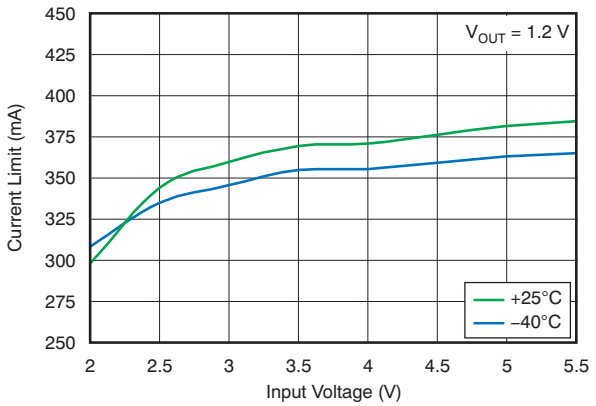


Figure 31.

CURRENT LIMIT vs INPUT VOLTAGE

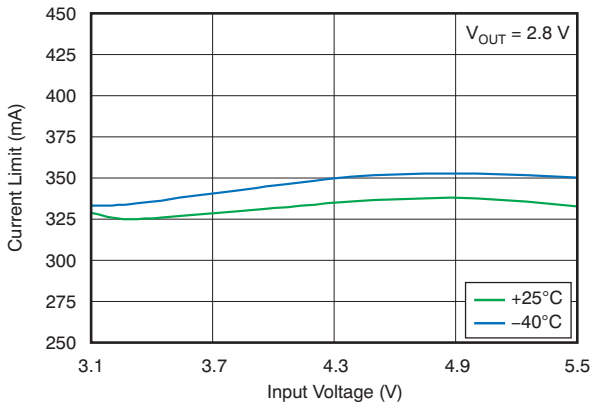


Figure 32.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

CURRENT LIMIT vs INPUT VOLTAGE

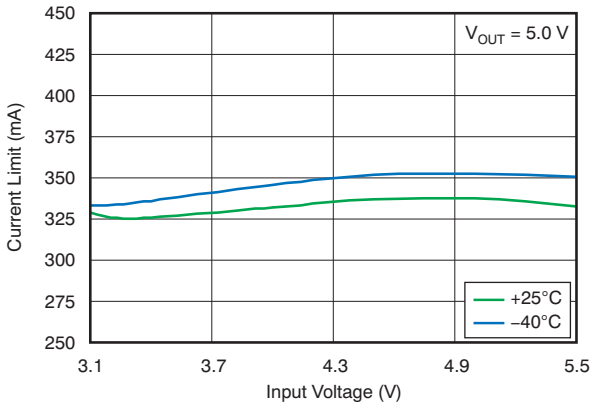


Figure 33.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

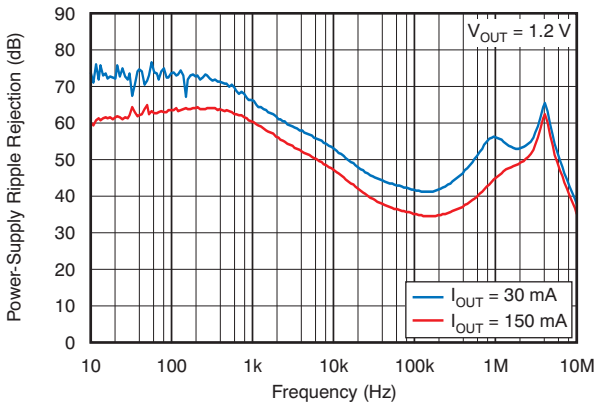


Figure 34.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

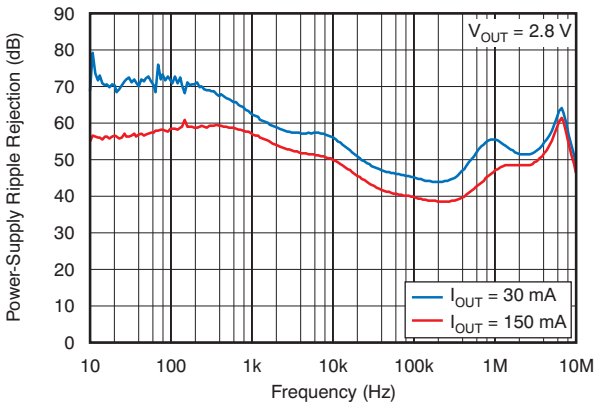


Figure 35.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

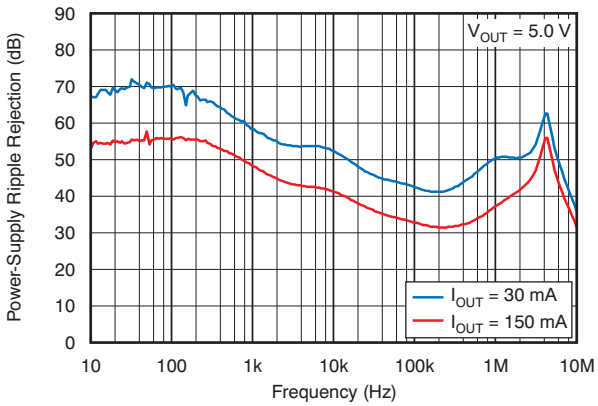


Figure 36.

POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE

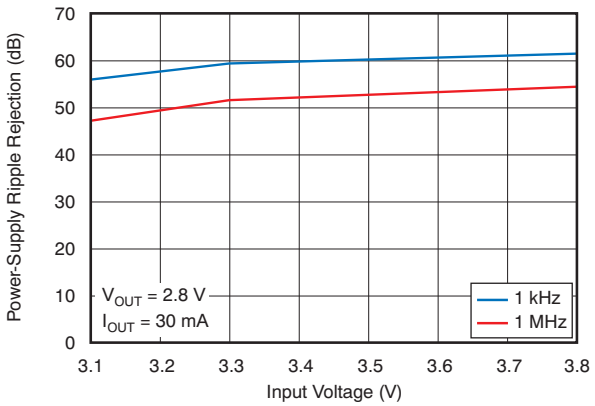


Figure 37.

POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE

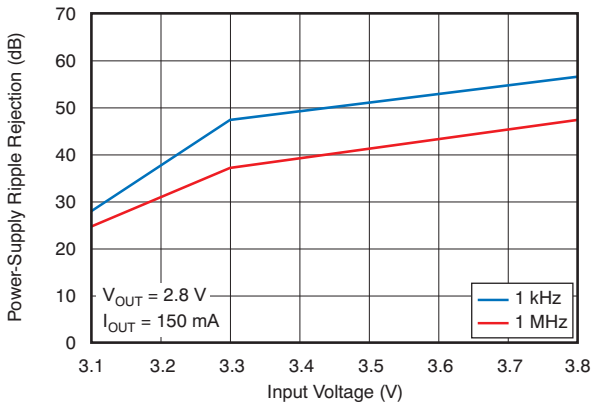


Figure 38.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE

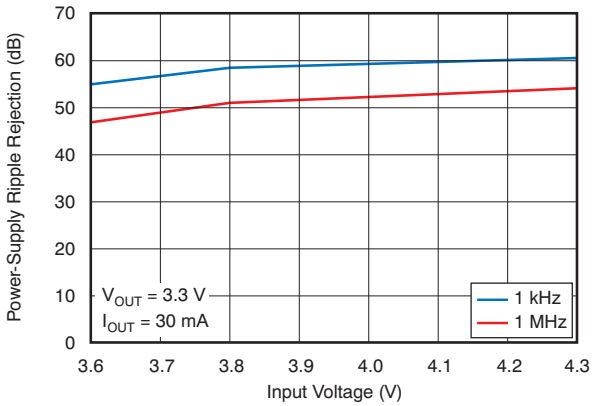


Figure 39.

POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE

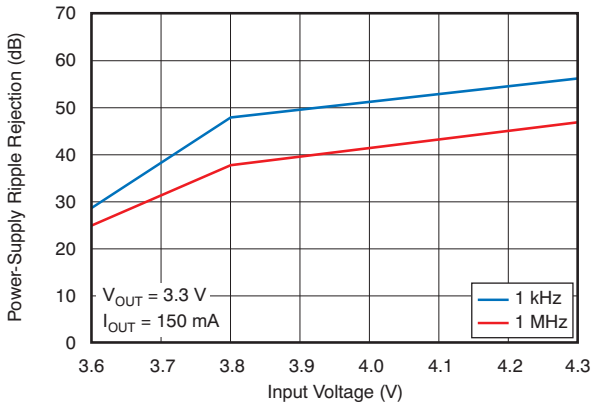


Figure 40.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

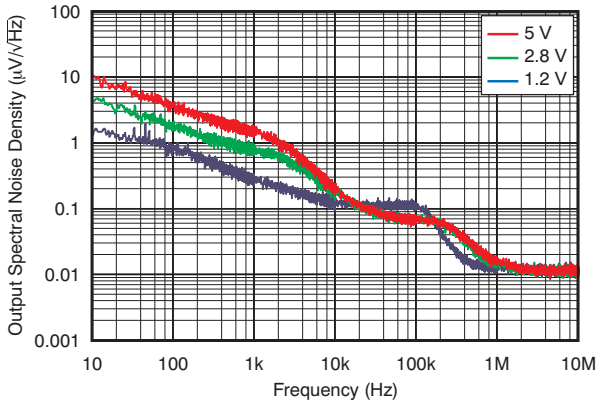


Figure 41.

LOAD TRANSIENT RESPONSE

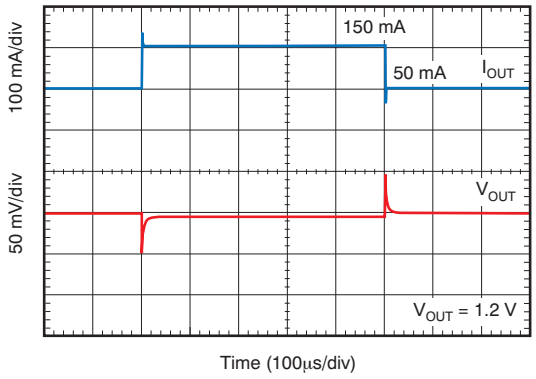


Figure 42.

LOAD TRANSIENT RESPONSE

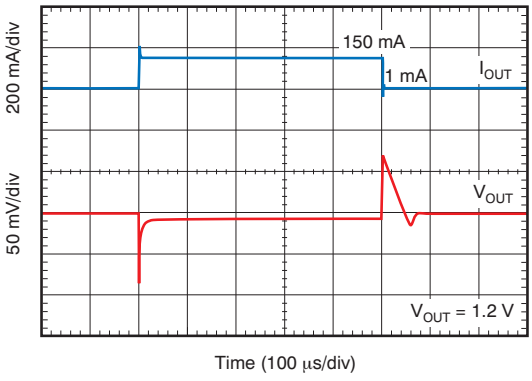


Figure 43.

LOAD TRANSIENT RESPONSE

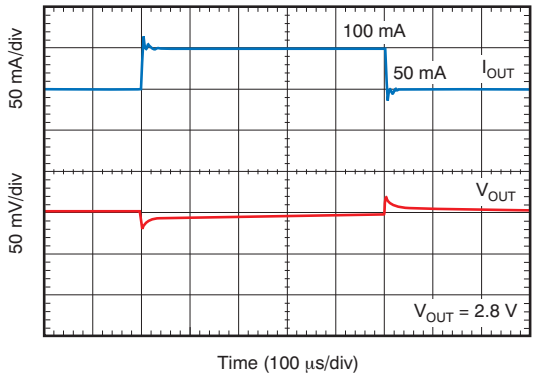


Figure 44.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

LOAD TRANSIENT RESPONSE

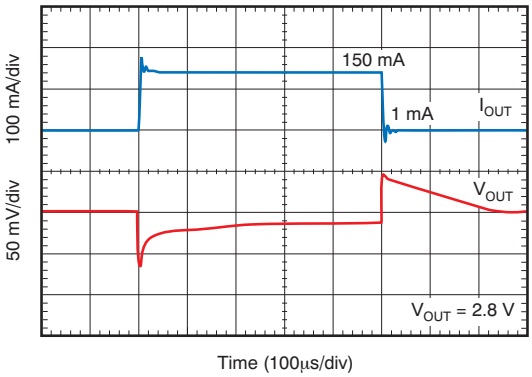


Figure 45.

LOAD TRANSIENT RESPONSE

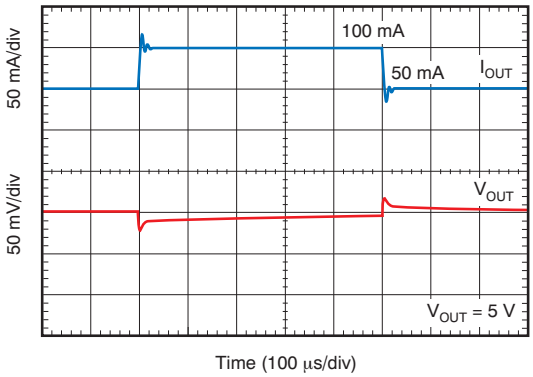


Figure 46.

LOAD TRANSIENT RESPONSE

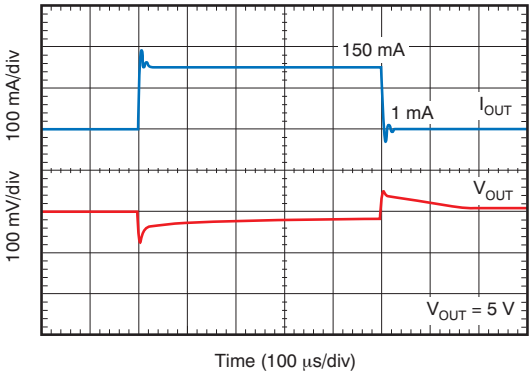


Figure 47.

LINE TRANSIENT RESPONSE

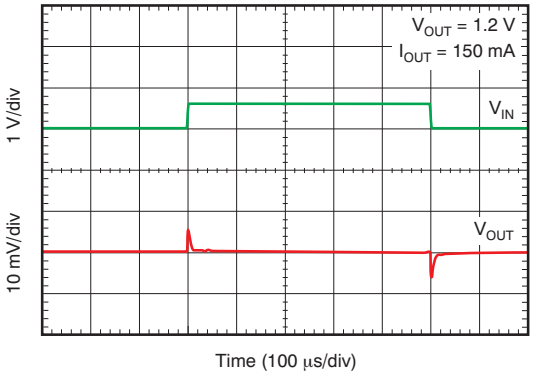


Figure 48.

LINE TRANSIENT RESPONSE

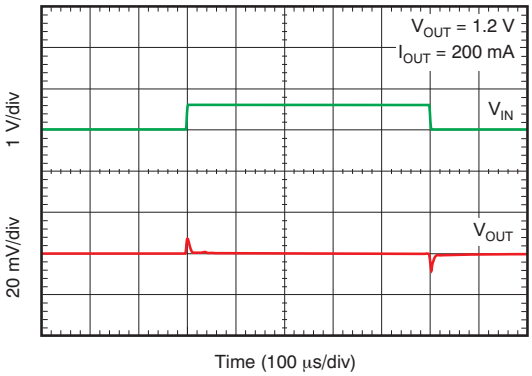


Figure 49.

LINE TRANSIENT RESPONSE

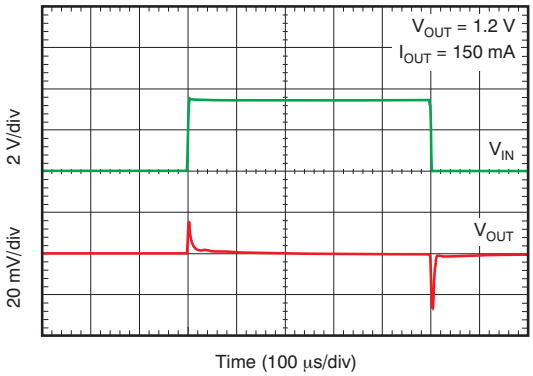


Figure 50.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

LINE TRANSIENT RESPONSE

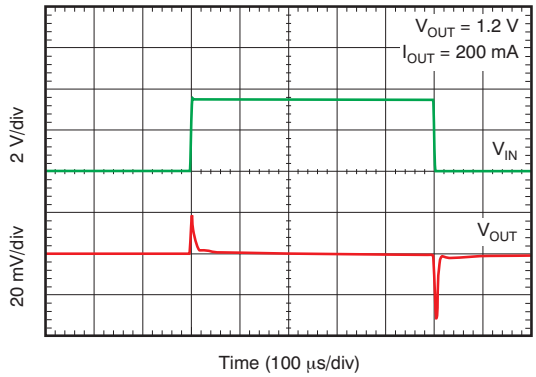


Figure 51.

LINE TRANSIENT RESPONSE

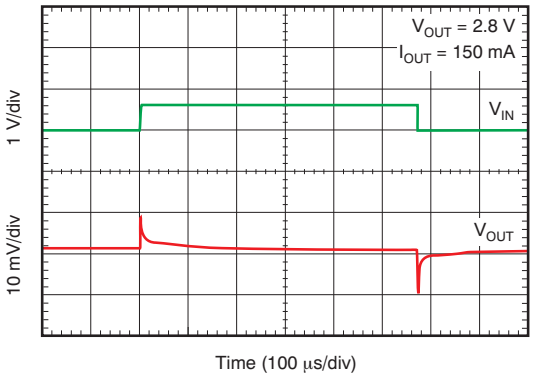


Figure 52.

LINE TRANSIENT RESPONSE

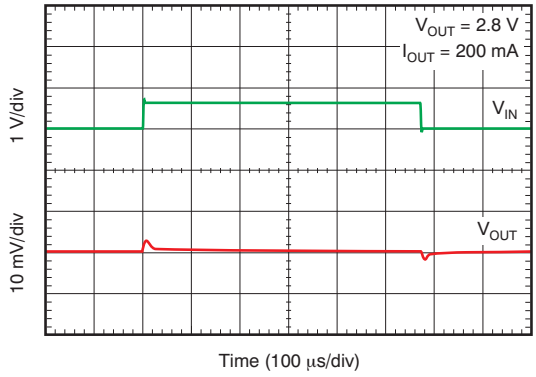


Figure 53.

LINE TRANSIENT RESPONSE

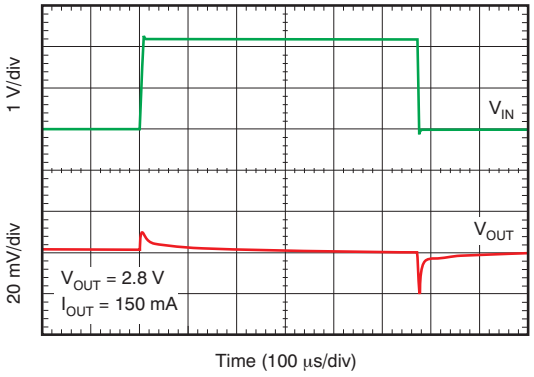


Figure 54.

LINE TRANSIENT RESPONSE

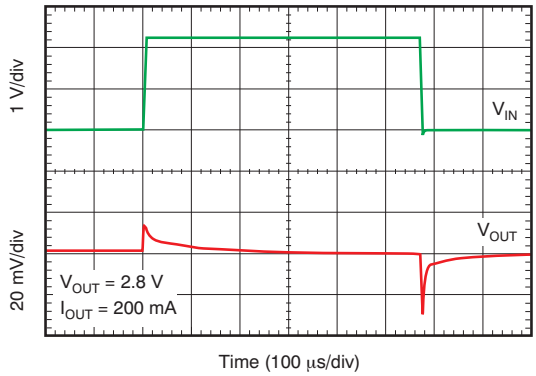


Figure 55.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

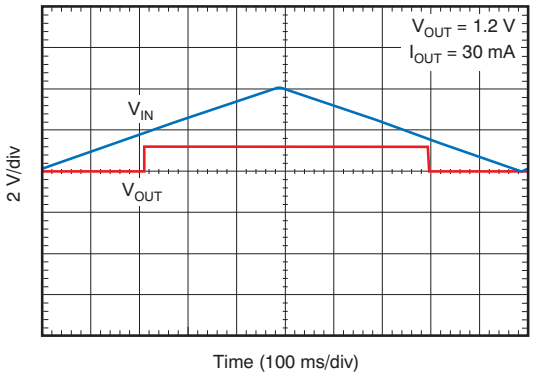


Figure 56.

TYPICAL CHARACTERISTICS (continued)

At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

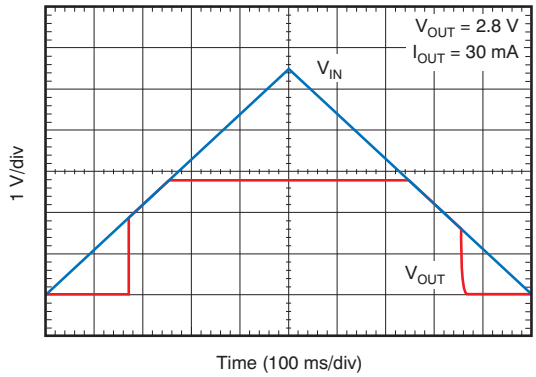


Figure 57.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

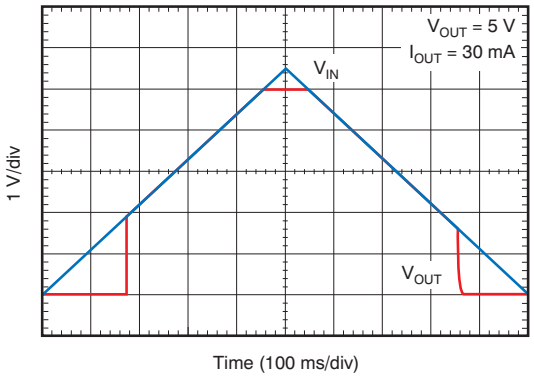


Figure 58.

APPLICATION INFORMATION

GENERAL DESCRIPTION

The TLV707 series (TLV707xx and TLV707xxP) belongs to a new family of next-generation value low-dropout regulators (LDOs). These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications.

This family of regulators offers current limit and themal protection. The operating junction temperature of these devices is –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Generally, 1.0-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV707 is designed to be stable with an effective capacitance of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

NOTE: Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2-Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV707 internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} - V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. As the device cools, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The PMOS pass element in the TLV707 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn on the LDO can also be used to power the device when it is connected to a GPIO of a newer processor, where the GPIO Logic 1 voltage level is lower than that of traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV707xxP version has internal active pull-down circuitry that discharges the output with a time constant of:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

DROPOUT VOLTAGE

The TLV707 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 14 in the Typical Characteristics section.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV707 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV707 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV707 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for JEDEC low- and high-K boards are given in the Dissipation Ratings. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV707 are available from the Texas Instruments web site at www.ti.com. The recommended land pattern for the DQN (DFN-4) package is shown towards the end of this data sheet.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2011) to Revision B **Page**

- Deleted reference to DCK package from Features 1
- Deleted DCK package pinout drawing 1
- Deleted DCK package from Thermal Information table 2
- Deleted DCK package pinout drawing 5
- Deleted column for DCK package from Pin Descriptions table 5
- Deleted reference to DCK package from *Package Mounting* section. 17

Changes from Original (February 2011) to Revision A **Page**

- Added footnote to Features to show available voltage options 1
- Added preview banner over DCK pinout drawing 1
- Added preview banner over DCK pinout drawing 5
- Deleted two manually-inserted land pattern drawings 17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV70712PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70712PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70715PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70715PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV707185DQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV707185DQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70718DQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70718DQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70718PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70718PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70719PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70719PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV707285DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV707285DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV707285PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV707285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70728PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV70728PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70730DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70730DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70730PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70730PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70733DQNR	PREVIEW	X2SON	DQN	4	3000	TBD	Call TI	Call TI	
TLV70733DQNT	PREVIEW	X2SON	DQN	4	250	TBD	Call TI	Call TI	
TLV70733PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLV70733PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

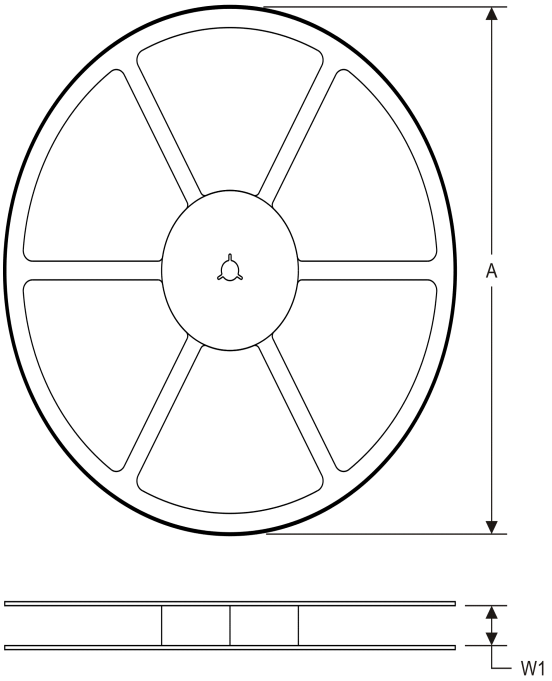
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

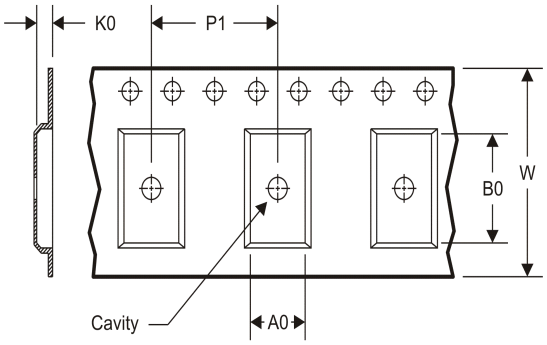
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



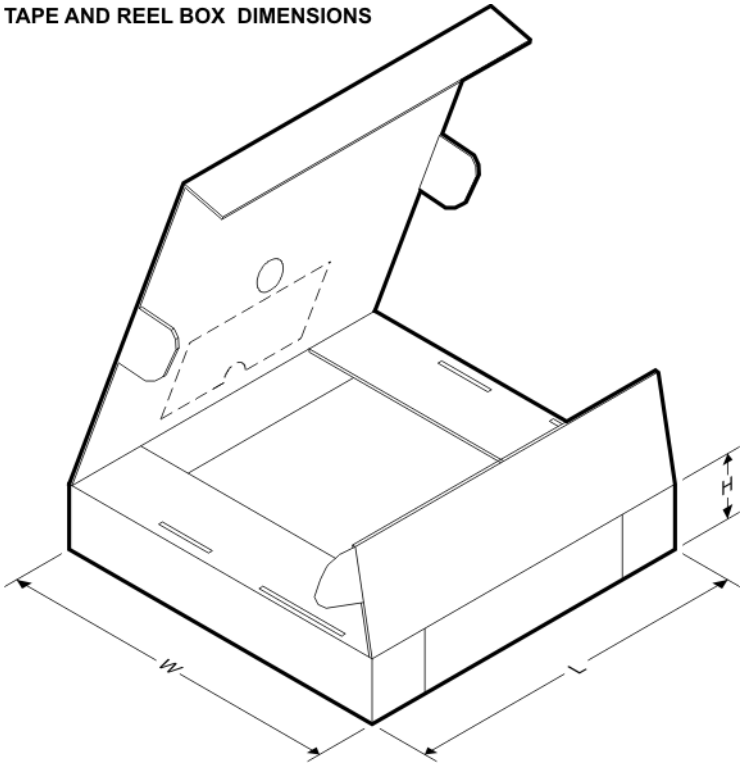
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70718PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70718PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285DQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV707285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70728PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70730PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV70733PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

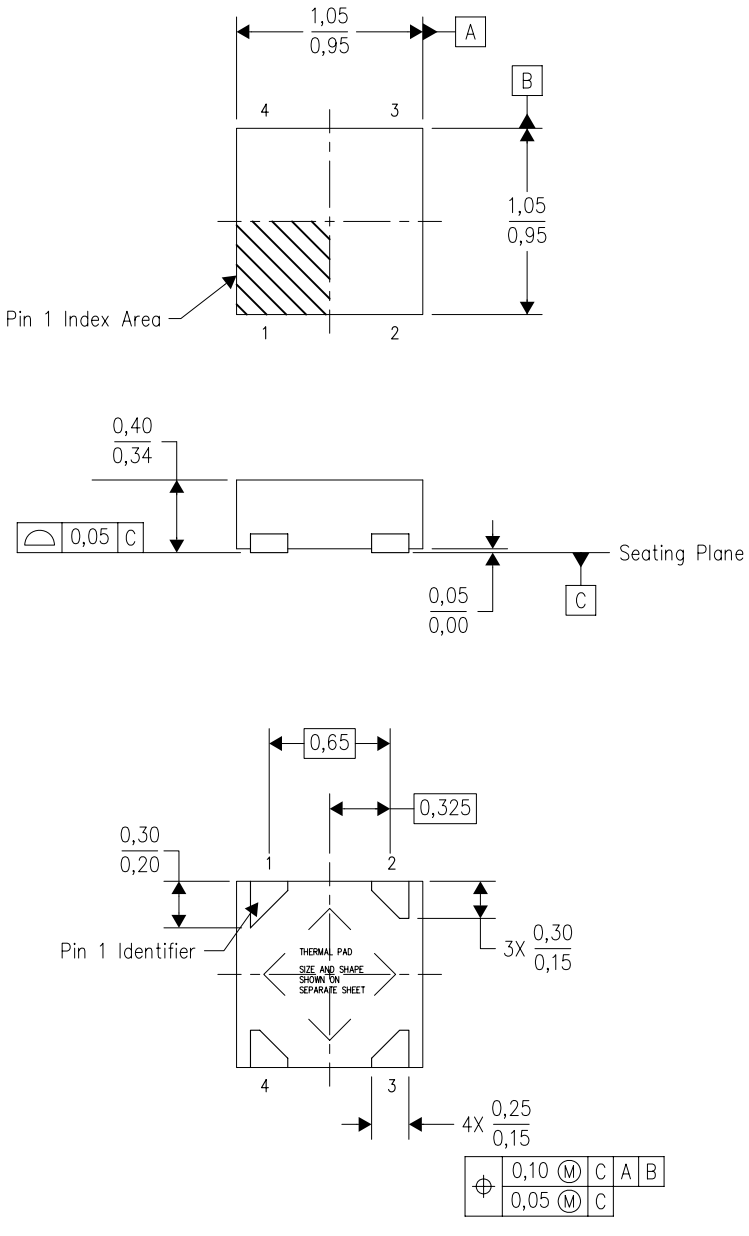
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70718PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV70718PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV707285DQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV707285DQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV707285DQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV707285DQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV707285PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV707285PDQNR	X2SON	DQN	4	3000	202.0	201.0	28.0
TLV707285PDQNT	X2SON	DQN	4	250	202.0	201.0	28.0
TLV707285PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV70728PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV70728PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV70730DQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV70730DQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV70730PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV70730PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV70733PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV70733PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4210367/C 05/2011

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

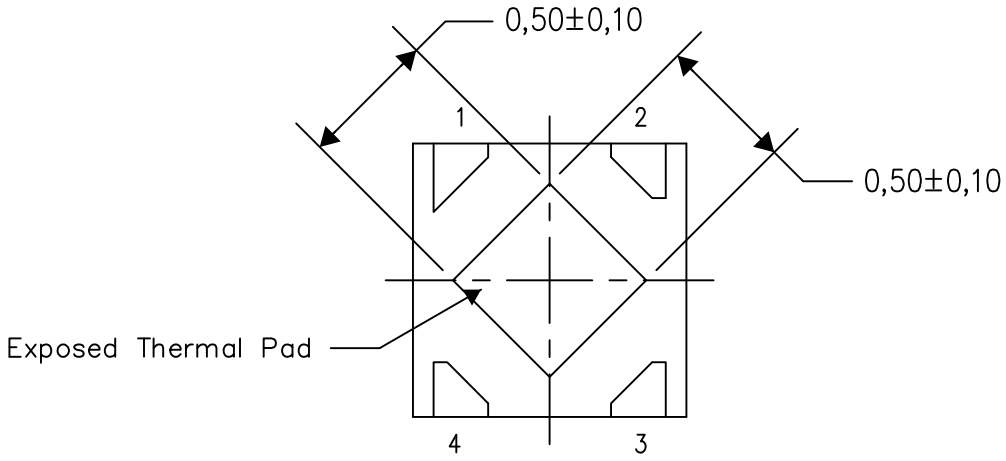
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



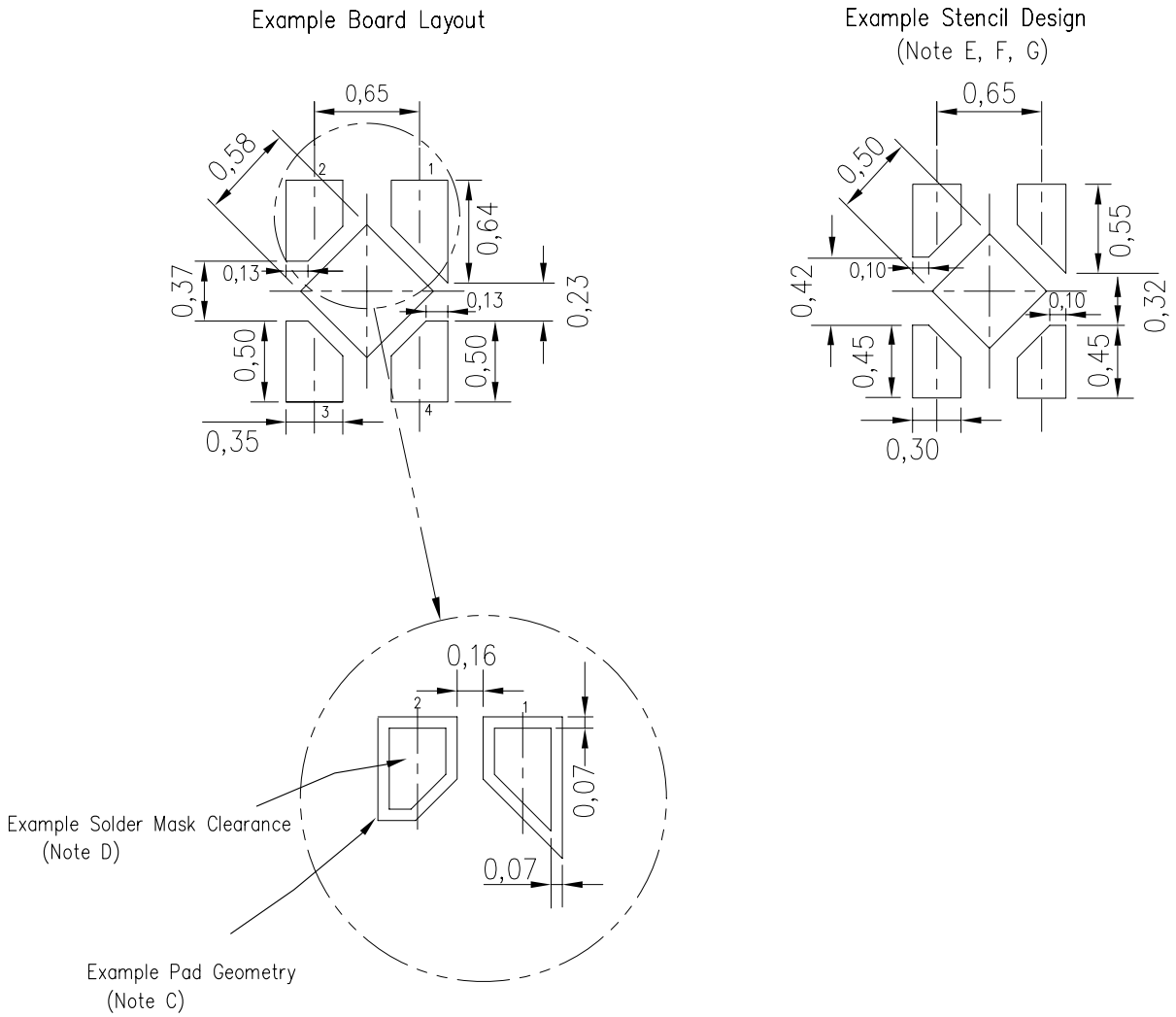
Bottom View

Exposed Thermal Pad Dimensions

4210393–2/E 04/12

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

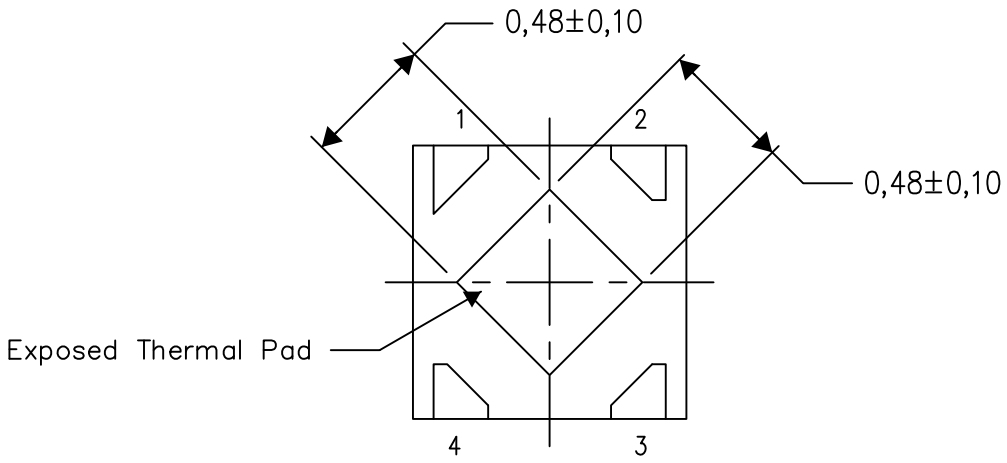
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4210393–3/E 04/12

NOTE: All linear dimensions are in millimeters

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