# TLV62568EVM-789 and TLV62569EVM-789 Evaluation Modules

This user's guide describes the characteristics, operation, and use of TI's TLV62568 and TLV62569 evaluation modules (EVM). These EVMs are designed to help the user easily evaluate and test the operation and functionality of the TLV62568 (1-A) and TLV62569 (2-A) buck converters. The EVMs convert a 2.5-V to 5.5-V input voltage to a regulated 1.8-V output voltage that delivers up to 2 A. This user's guide includes setup instructions for the hardware, a printed-circuit board (PCB) layout, a schematic diagram, a bill of materials (BOM), and test results of the EVM. Throughout this document, TLV6256xEVM-789 is used as an abbreviation representing the TLV62568EVM-789 (001) and TLV62569EVM-789 (002) EVMs.

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## Trademarks

# 1 Introduction

The TLV62568DBV and TLV62569DBV are synchronous step-down converters in 2.9-mm × 2.8-mm, 5-pin SOT-23 package. The TLV62568EVM-789 (PWR789-001) uses the TLV62568DBV integrated circuit (IC). The TLV62569EVM-789 (PWR789-002) uses the TLV62569DBV IC.

## 1.1 Performance Specification

Table 1 provides a summary of the TLV6256xEVM-789 performance specifications.

**Table 1. Performance Specification Summary**

| Specification | | Test Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Input voltage | | | 2.5 | | 5.5 | V |
| Output voltage setpoint | | | | 1.8 | | V |
| Output current | TLV62568EVM-789 | | 0 | | 1 | A |
| | TLV62569EVM-789 | | 0 | | 2 | A |

## 1.2 Thermal Data

Table 2 and Table 3 show the TLV62568EVM-789 and TLV62569EVM-789 thermal data after considering the printed-circuit board (PCB) design of real applications compared to the JEDEC values listed in the data sheet.

**Table 2. TLV62568EVM-789 Thermal Data**

| Thermal Metric(1) | | TLV62568EVM-789 | TLV62568 Data Sheet (JEDEC) | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 154.2 | 191.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | N/A | 141.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | N/A | 44.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 23.2 | 34.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 83.3 | 43.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

**Table 3. TLV62569EVM-789 Thermal Data**

| Thermal Metric(1) | | TLV62569EVM-789 | TLV62569 Data Sheet (JEDEC) | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 151 | 188.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | N/A | 137.5 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | N/A | 41.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 20.3 | 31.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 80.1 | 40.6 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 1.3 Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate the adjustable voltage version of this IC. On the EVM, additional input and output capacitors can be added. Finally, a feedforward capacitor can be added.

### 1.3.1 Input and Output Capacitors

C4 is provided for an additional input capacitor. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple.

C6, C7, and C8 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple and to improve the load transient response. The output capacitance must remain within the recommended range in the TPS62568 (SLVSD89) and TPS62569 (SLVSDG1) data sheet for proper operation.

### 1.3.2 Feedforward Capacitor

C5 is provided for the installation of an optional feedforward capacitor. This capacitor is not required for proper operation but can be used to improve the load transient performance.

# 2 Setup

This section describes how to properly use the TLV6256xEVM-789.

## 2.1 Connector Descriptions

| | |
|---|---|
| **J1, Pin 1 and 2 – VIN** | Positive input voltage connection from the input supply for the EVM. |
| **J1, Pin 3 and 4 – S+/S–** | Input voltage sense connections. Measure the input voltage at this point. |
| **J1, Pin 5 and 6 – GND** | Input return connection from the input supply for the EVM. |
| **J2, Pin 1 and 2 – VOUT** | Positive output voltage connection. |
| **J2, Pin 3 and 4 – S+/S–** | Output voltage sense connections. Measure the output voltage at this point. |
| **J2, Pin 5 and 6 – GND** | Output return connection. |
| **JP1 – EN** | EN pin jumper. Place the supplied jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC. |

## 2.2 Hardware Setup

To operate the EVM, set jumpers JP1 to the desired positions per Section 2.1. Connect the input supply to J1, and connect the load to J2.

# 3 TLV6256xEVM-789 Test Results

The TLV6256xEVM-789 was used to take the data in the TLV62568 and TLV62569 data sheet. See the device data sheet for the performance of this EVM.

## 4 Board Layout

This section provides the TLV6256xEVM-789 board layout and illustrations. The Gerbers are available on the EVM product pages: TLV62568EVM-789 and TLV62569EVM-789.

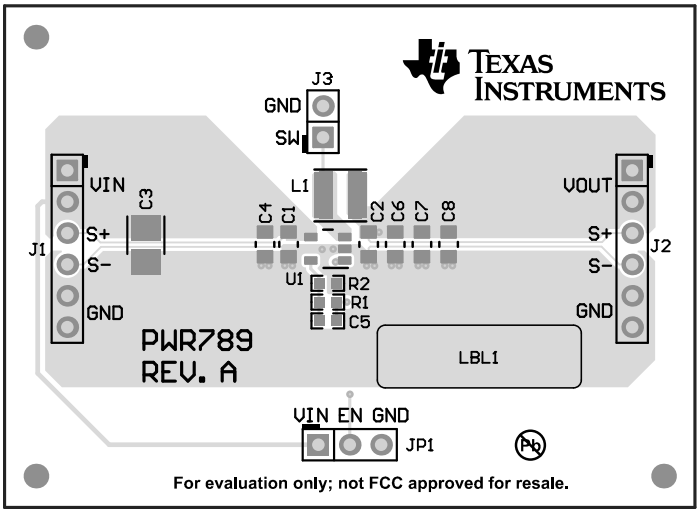


**Figure 1. Top Assembly**

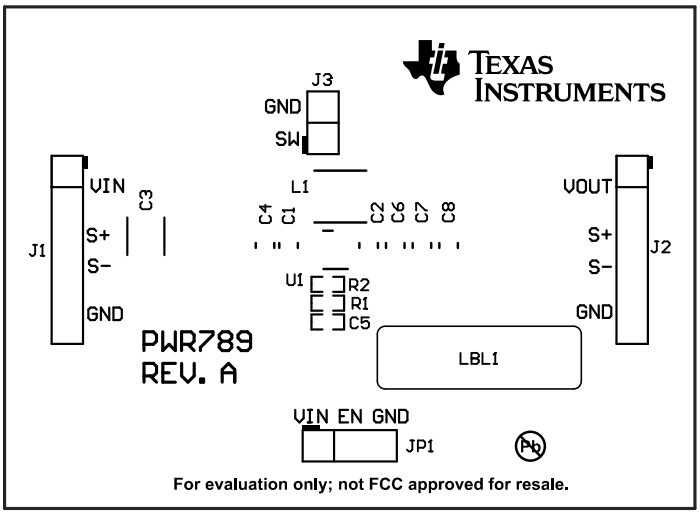


**Figure 2. Top Overlay**

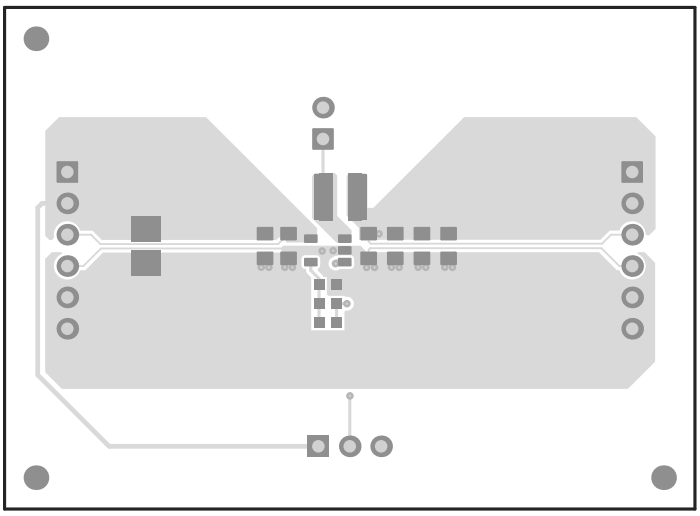

**Figure 3. Top Layer**

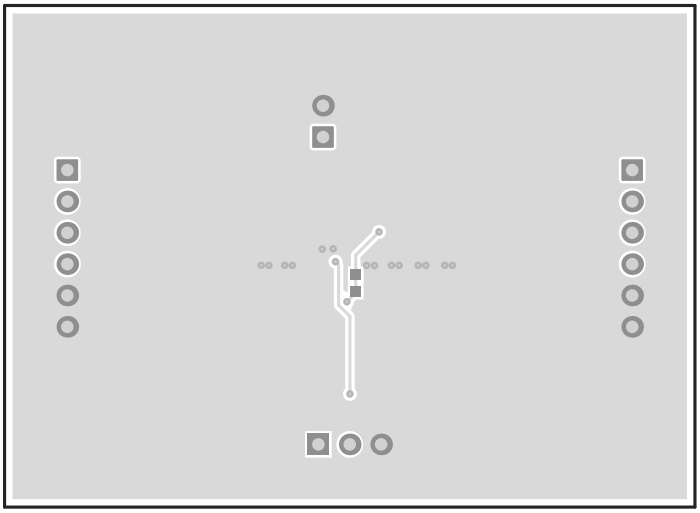

**Figure 4. Bottom Layer**

# 5 Schematic and Bill of Materials

This section provides the TLV6256xEVM-789 schematic and bill of materials.

## 5.1 Schematic

Figure 5 illustrates the EVM schematic.

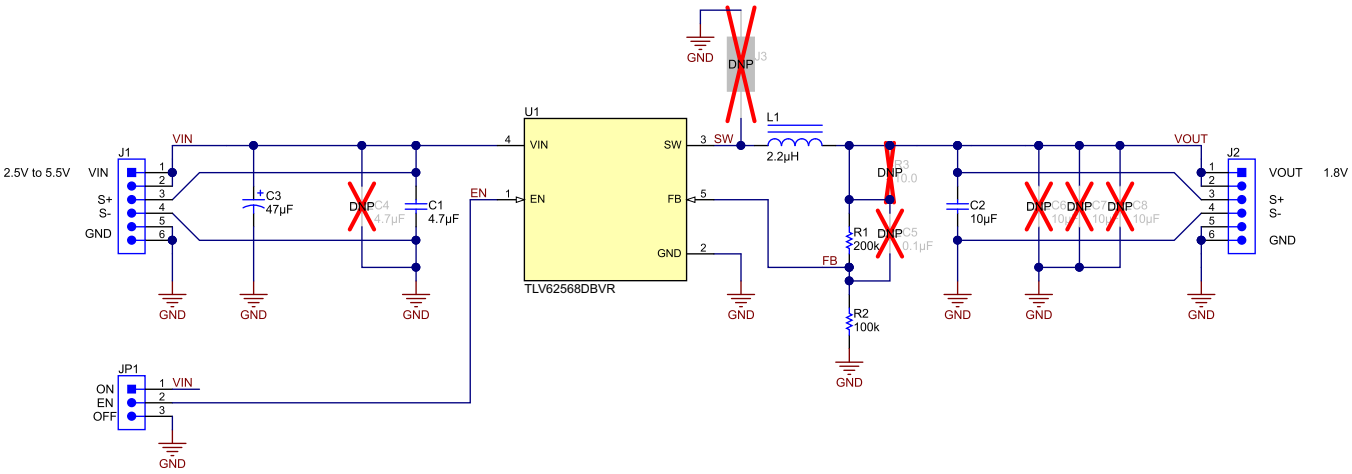


**Figure 5. TLV6256xEVM-789 Schematic**

## 5.2 Bill of Materials

Table 4 lists the BOM for this EVM.

**Table 4. TLV6256xEVM-789 Bill of Materials**

| Qty | | Ref Des | Value | Description | Size | Part Number | Manufacturer |
|---|---|---|---|---|---|---|---|
| TLV62568EVM-789 | TLV62569EVM-789 | | | | | | |
| 1 | 1 | C1 | 4.7uF | Capacitor, Ceramic, 10V, X7R, +/- 10% | 0805 | GRM21BR71A475KA73L | Murata |
| 1 | 1 | C2 | 10uF | Capacitor, Ceramic, 10V, X7R, +/- 10% | 0805 | GRM21BR71A106KE51L | Murata |
| 1 | 1 | C3 | 47uF | Capacitor, Tantalum, 6.3V, +/- 20% | 3528-21 | T520B476M006ATE025 | Kemet |
| 1 | 0 | L1 | 2.2uH | Inductor, Shielded, 2.8 A, 0.045 ohm | 4x4mm | SDER041H-2R2MS | Cyntec |
| 0 | 1 | L1 | 2.2uH | Inductor, Shielded, 5.5 A, 0.04 ohm | 4x4mm | XAL4020-222MEB | Coilcraft |
| 1 | 1 | R1 | 200k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | 1 | R2 | 100k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| 1 | 0 | U1 | TLV62568 | IC, 5.5V 1A Step-Down Converter | 2.9x2.8mm | TLV62568DBV | TI |
| 0 | 1 | U1 | TLV62569 | IC, 5.5V 2A Step-Down Converter | 2.9x2.8mm | TLV62569DBV | TI |

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- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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**Concernant les EVMs avec antennes détachables**

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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