

SLCS137B – NOVEMBER 2000 – REVISED AUGUST 2001

# FAMILY OF NANOPOWER PUSH-PULL OUTPUT COMPARATORS

## FEATURES

- **Low Supply Current . . . 560 nA/Per Channel**
- **Input Common-Mode Range Exceeds the Rails . . . –0.1 V to $V_{CC}$ + 5 V**
- **Supply Voltage Range . . . 2.5 V to 16 V**
- **Reverse Battery Protection Up to 18 V**
- **Push-Pull CMOS Output Stage**
- **Specified Temperature Range**
  - **0°C to 70°C – Commercial Grade**
  - **–40°C to 125°C – Industrial Grade**
- **Ultrasmall Packaging**
  - **5-Pin SOT-23 (TLV3701)**
  - **8-Pin MSOP (TLV3702)**
- **Universal Op-Amp EVM (Reference SLOU060 for more information)**

## APPLICATIONS

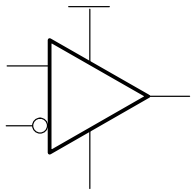
- **Portable Battery Monitoring**
- **Consumer Medical Electronics**
- **Security Detection Systems**

## DESCRIPTION

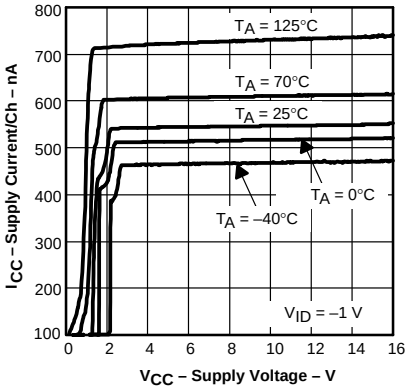
The TLV370x is Texas Instruments' first family of nanopower comparators with only 560 nA per channel supply current, which make this device ideal for battery power and wireless handset applications.

The TLV370x has a minimum operating supply voltage of 2.7 V over the extended industrial temperature range ($T_A$ = –40°C to 125°C), while having an input common-mode range of –0.1 to $V_{CC}$ + 5 V. The low supply current makes it an ideal choice for battery powered portable applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an over-current condition due to improper battery installation. For harsh environments, the inputs can be taken 5 V above the positive supply rail without damage to the device.

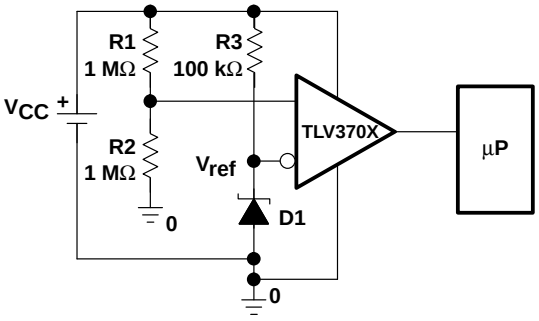
All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.



**SUPPLY CURRENT vs SUPPLY VOLTAGE**




**high side voltage sense circuit**




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**A SELECTION OF OUTPUT COMPARATORS†**

| DEVICE | $V_{CC}$ (V) | $V_{IO}$ (μV) | $I_{CC}$/Ch (μA) | $I_{IB}$ (pA) | $t_{PLH}$ (μs) | $t_{PHL}$ (μs) | $t_f$ (μs) | $t_r$ (μs) | RAIL-TO-RAIL | OUTPUT STAGE |
|---|---|---|---|---|---|---|---|---|---|---|
| TLV370x | 2.5 – 16 | 250 | 0.56 | 80 | 56 | 83 | 22 | 8 | I | PP |
| TLV340x | 2.5 – 16 | 250 | 0.47 | 80 | 55 | 30 | 5 | – | I | OD |
| TLC3702/4 | 3 – 16 | 1200 | 9 | 5 | 1.1 | 0.65 | 0.5 | 0.125 | – | PP |
| TLC393/339 | 3 – 16 | 1400 | 11 | 5 | 1.1 | 0.55 | 0.22 | – | – | OD |
| TLC372/4 | 3 – 16 | 1000 | 75 | 5 | 0.65 | 0.65 | – | – | – | OD |

† All specifications are typical values measured at 5 V.

**TLV3701 AVAILABLE OPTIONS**

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | | |
|---|---|---|---|---|---|
| | | SMALL OUTLINE (D)† | SOT-23 (DBV)‡ | SYMBOL | PLASTIC DIP (P) |
| 0°C to 70°C | 5000 μV | TLV3701CD | TLV3701CDBV | VBCC | — |
| -40°C to 125°C | | TLV3701ID | TLV3701IDBV | VBCI | TLV3701IP |

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV3701CDR).
‡ This package is only available taped and reeled. For standard quantities (3000 pieces per reel), add an R suffix (i.e., TLV3701CDBVR). For small quantities (250 pieces per mini-reel), add a T suffix to the part number (e.g., TLV3701CDBVT).

**TLV3702 AVAILABLE OPTIONS**

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | | |
|---|---|---|---|---|---|
| | | SMALL OUTLINE (D)† | MSOP (DGK)† | SYMBOL | PLASTIC DIP (P) |
| 0°C to 70°C | 5000 μV | TLV3702CD | TLV3702CDGK | xxTIAKC | — |
| –40°C to 125°C | | TLV3702ID | TLV3702IDGK | xxTIAKD | TLV3702IP |

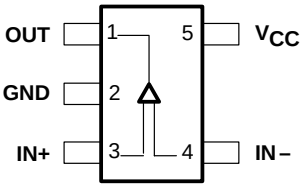
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV3702CDR).

**TLV3704 AVAILABLE OPTIONS**

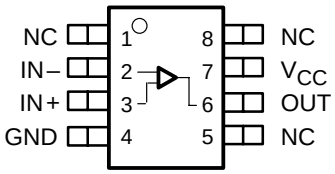
| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | |
|---|---|---|---|---|
| | | SMALL OUTLINE (D)† | PLASTIC DIP (N) | TSSOP (PW) |
| 0°C to 70°C | 5000 μV | TLV3704CD | — | TLV3704CPW |
| –40°C to 125°C | | TLV3704ID | TLV3704IN | TLV3704IPW |

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV3704CDR).

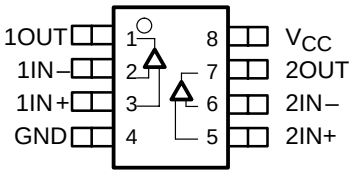
**TLV3701**
**DBV PACKAGE**
**(TOP VIEW)**



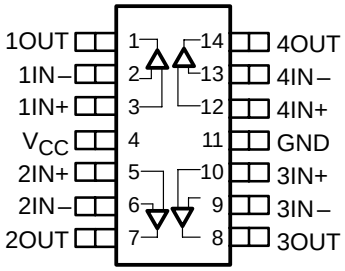

**TLV3701**
**D OR P PACKAGE**
**(TOP VIEW)**




**TLV3702**
**D, DGK, OR P PACKAGE**
**(TOP VIEW)**




**TLV3704**
**D, N, OR PW PACKAGE**
**(TOP VIEW)**




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 17 V
Differential input voltage, $V_{ID}$ . . . . . ±20 V
Input voltage range, $V_I$ (see Notes 1 and 2) . . . . . 0 to $V_{CC}$ + 5 V
Input current range, $I_I$ . . . . . ±10 mA
Output current range, $I_O$ . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 125°C
Maximum junction temperature, $T_J$ . . . . . 150°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. Input voltage range is limited to 20 V max or $V_{CC}$ + 5 V, whichever is smaller.

**DISSIPATION RATING TABLE**

| PACKAGE | $\theta_{JC}$ (°C/W) | $\theta_{JA}$ (°C/W) | $T_A \le 25°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| D (8) | 38.3 | 176 | 710 mW | 142 mW |
| D (14) | 26.9 | 122.6 | 1022 mW | 204.4 mW |
| DBV (5) | 55 | 324.1 | 385 mW | 77.1 mW |
| DGK (8) | 54.2 | 259.9 | 481 mW | 96.2 mW |
| N (14) | 32 | 78 | 1600 mW | 320.5 mW |
| P (8) | 41 | 104 | 1200 mW | 240.4 mW |
| PW (14) | 29.3 | 173.6 | 720 mW | 144 mW |

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | Single supply | C-suffix | 2.5 | 16 | V |
| | | I-suffix | 2.7 | 16 | |
| | Split supply | C-suffix | ±1.25 | ±8 | |
| | | I-suffix | ±1.35 | ±8 | |
| Common-mode input voltage range, $V_{ICR}$ | | | –0.1 | $V_{CC}$+5 | V |
| Operating free-air temperature, $T_A$ | C-suffix | | 0 | 70 | °C |
| | I-suffix | | –40 | 125 | |

## electrical characteristics at specified operating free-air temperature, $V_{CC}$ = 2.7 V, 5 V, 15 V (unless otherwise noted)

### dc performance

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{IC}$= $V_{CC}$/2, | $R_S$ = 50 Ω | 25°C | | 250 | 5000 | μV |
| | | | | Full range | | | 7000 | |
| $\alpha_{VIO}$ | Offset voltage drift | | | 25°C | | 3 | | μV/°C |
| CMRR | Common-mode rejection ratio | $V_{IC}$= 0 to 2.7 V, | $R_S$ = 50 Ω | 25°C | 55 | 72 | | dB |
| | | | | Full range | 50 | | | |
| | | $V_{IC}$= 0 to 5 V, | $R_S$ = 50 Ω | 25°C | 60 | 76 | | |
| | | | | Full range | 55 | | | |
| | | $V_{IC}$= 0 to 15 V, | $R_S$ = 50 Ω | 25°C | 65 | 88 | | |
| | | | | Full range | 60 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | | | 25°C | | 1000 | | V/mV |

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

### input/output characteristics

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{IO}$ | Input offset current | $V_{IC}$ = $V_{CC}$/2, | $R_S$ = 50 Ω | 25°C | | 20 | 100 | pA |
| | | | | Full range | | | 1000 | |
| $I_{IB}$ | Input bias current | | | 25°C | | 80 | 250 | pA |
| | | | | Full range | | | 1500 | |
| $r_{i(d)}$ | Differential input resistance | | | 25°C | | 300 | | MΩ |
| $V_{OH}$ | High-level output voltage | $V_{IC}$ = $V_{CC}$/2, | $I_{OH}$ = 2 μA, $V_{ID}$ = 1 V | 25°C | | $V_{CC}$– 0.08 | | mV |
| | | $V_{IC}$ = $V_{CC}$/2, | $I_{OH}$ = –50 μA, $V_{ID}$ = 1 V | 25°C | $V_{CC}$– 320 | | | |
| | | | | Full range | $V_{CC}$– 450 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = $V_{CC}$/2, | $I_{OH}$ = 2 μA, $V_{ID}$ = –1 V | 25°C | | 8 | | mV |
| | | $V_{IC}$ = $V_{CC}$/2, | $I_{OH}$ = 50 μA, $V_{ID}$ = –1 V | 25°C | | 80 | 200 | |
| | | | | Full range | | | 300 | |

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

### power supply

| PARAMETER | | TEST CONDITIONS | | $T_A$† | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply current (per channel) | Output state high | | 25°C | | 560 | 800 | nA |
| | | | | Full range | | | 1000 | |
| PSRR | Power supply rejection ratio | $V_{IC}$ = $V_{CC}$/2 V, No load | $V_{CC}$= 2.7 V to 5 V | 25°C | 75 | 100 | | dB |
| | | | | Full range | 70 | | | |
| | | | $V_{CC}$= 5 V to 15 V | 25°C | 85 | 105 | | |
| | | | | Full range | 80 | | | |

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

### switching characteristics at recommended operating conditions, $V_{CC}$ = 2.7 V, 5 V, 15 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{(PLH)}$ | Propagation response time, low-to-high-level output (see Note 3) | f = 10 kHz, $V_{STEP}$ = 100 mV, $C_L$ = 10 pF, $V_{CC}$ = 2.7 V | Overdrive = 2 mV | | 240 | | µs |
| | | | Overdrive = 10 mV | | 64 | | |
| | | | Overdrive = 50 mV | | 36 | | |
| $t_{(PHL)}$ | Propagation response time, high-to-low-level output (see Note 3) | | Overdrive = 2 mV | | 167 | | |
| | | | Overdrive = 10 mV | | 67 | | |
| | | | Overdrive = 50 mV | | 37 | | |
| $t_r$ | Rise time | $C_L$ = 10 pF, $V_{CC}$ = 2.7 V | | | 7 | | µs |
| $t_f$ | Fall time | $C_L$ = 10 pF, $V_{CC}$ = 2.7 V | | | 9 | | µs |

NOTE 3: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V. Propagation responses are longer at higher supply voltages, refer to Figures 12–17 for further details.

## TYPICAL CHARACTERISTICS

### Table of Graphs



| | | | FIGURE |
|---|---|---|---|
| | Input bias/offset current | vs Free-air temperature | 1 |
| | Open collector leakage current | vs Free-air temperature | 2 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | 3, 5, 7 |
| $V_{OH}$ | High-level output voltage | vs High-level output current | 4, 6, 8 |
| $I_{CC}$ | Supply current | vs Supply voltage | 9 |
| | | vs Free-air temperature | 10 |
| | Output fall time/rise time | vs Supply voltage | 11 |
| | Low-to-high level output response for various input overdrives | | 12, 14, 16 |
| | High-to-low level output response for various input overdrives | | 13, 15, 17 |



**INPUT BIAS/OFFSET CURRENT vs FREE-AIR TEMPERATURE**

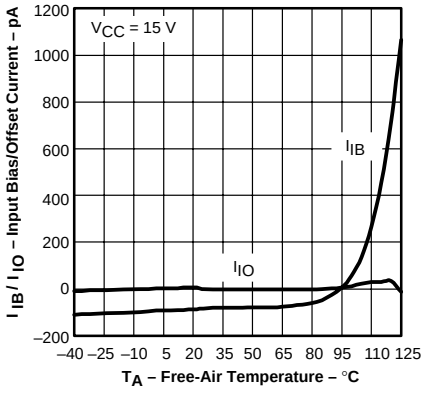



Figure 1

**OPEN COLLECTOR LEAKAGE CURRENT vs FREE-AIR TEMPERATURE**

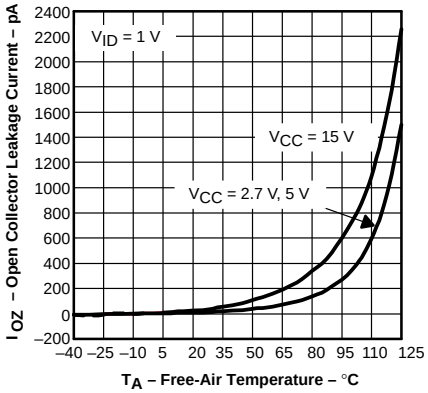



Figure 2

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

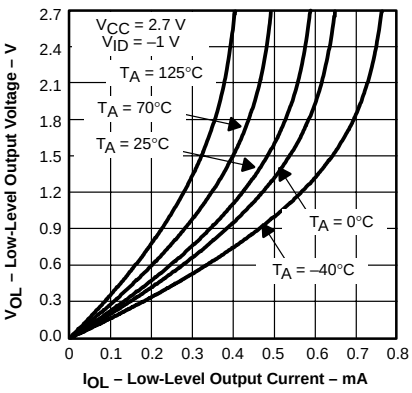



Figure 3

## TYPICAL CHARACTERISTICS

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

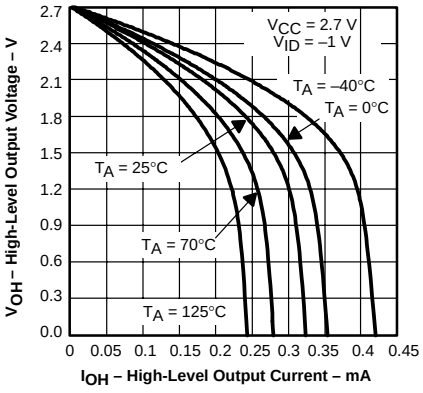



Figure 4

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

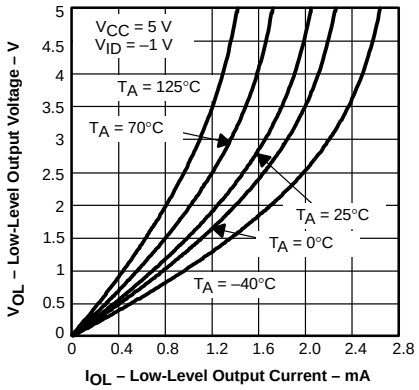



Figure 5

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

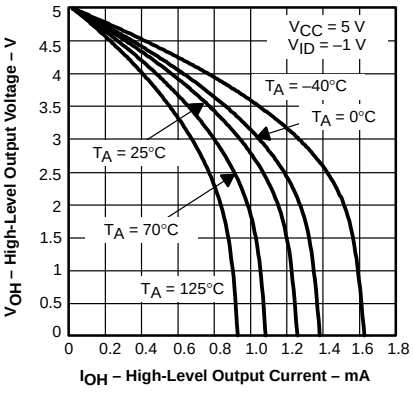



Figure 6

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

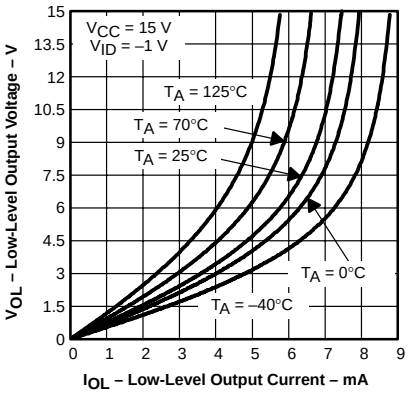



Figure 7

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

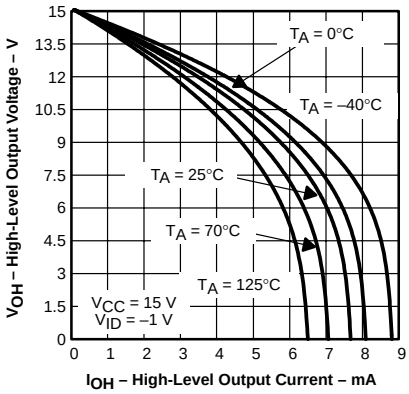



Figure 8

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

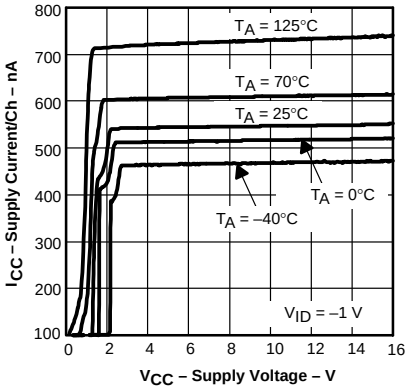



Figure 9

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

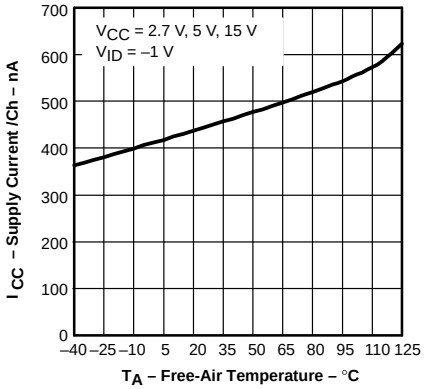



Figure 10

**OUTPUT RISE/FALL TIME vs SUPPLY VOLTAGE**

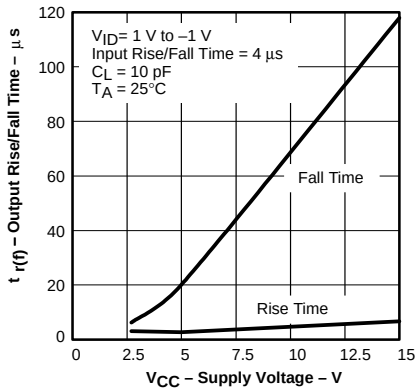



Figure 11

## TYPICAL CHARACTERISTICS

**LOW-TO-HIGH OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES**

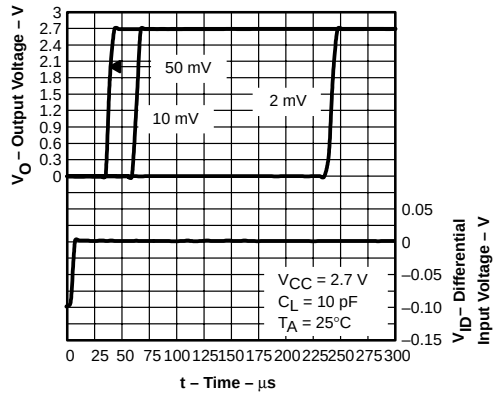



**Figure 12**

**HIGH-TO-LOW LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES**

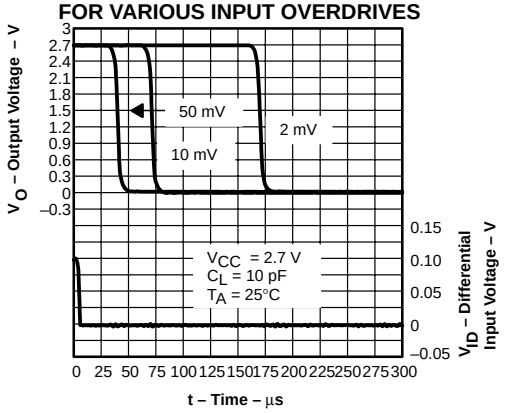



**Figure 13**

**LOW-TO-HIGH LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES**

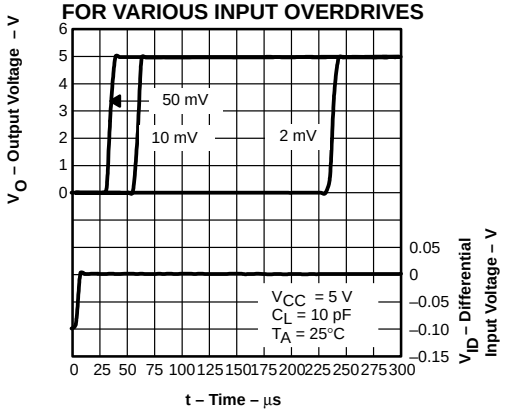



**Figure 14**

**HIGH-TO-LOW LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES**

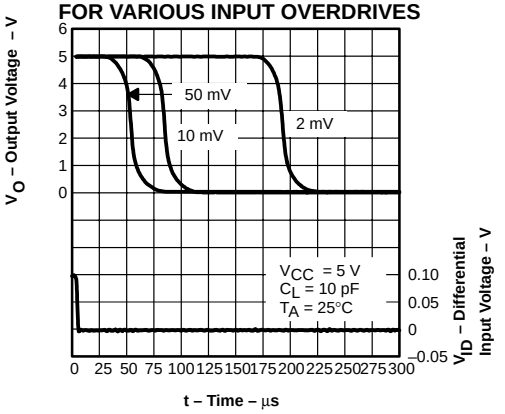



**Figure 15**

**LOW-TO-HIGH LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES**

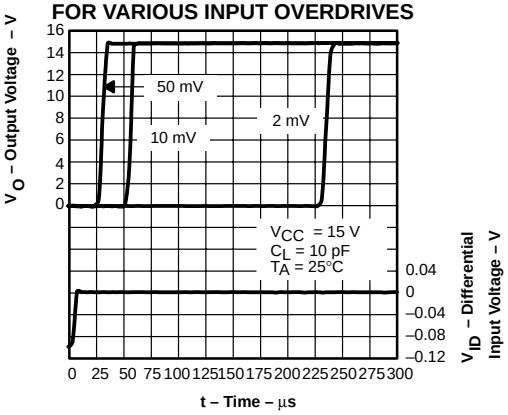



**Figure 16**

**HIGH-TO-LOW LEVEL OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVES**

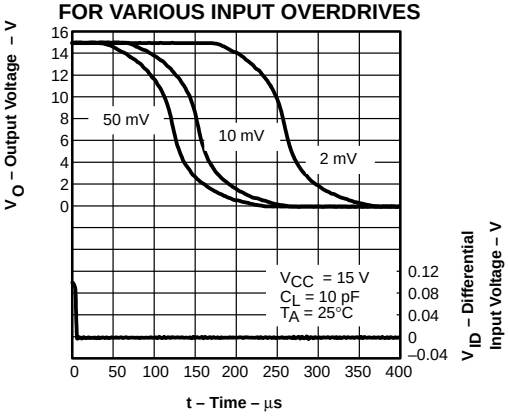



**Figure 17**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3701CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3701C | Samples |
| TLV3701CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBCC | Samples |
| TLV3701CDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBCC | Samples |
| TLV3701CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBCC | Samples |
| TLV3701CDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VBCC | Samples |
| TLV3701CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3701C | Samples |
| TLV3701ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3701I | Samples |
| TLV3701IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBCI | Samples |
| TLV3701IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBCI | Samples |
| TLV3701IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBCI | Samples |
| TLV3701IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBCI | Samples |
| TLV3701IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3701I | Samples |
| TLV3701IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3701I | Samples |
| TLV3701IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3701I | Samples |
| TLV3701IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3701I | Samples |
| TLV3701IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3701I | Samples |
| TLV3702CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3702C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3702CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3702C | Samples |
| TLV3702CDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AKC | Samples |
| TLV3702CDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AKC | Samples |
| TLV3702CDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AKC | Samples |
| TLV3702CDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AKC | Samples |
| TLV3702ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702I | Samples |
| TLV3702IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702I | Samples |
| TLV3702IDGK | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AKD | Samples |
| TLV3702IDGKG4 | ACTIVE | VSSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AKD | Samples |
| TLV3702IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AKD | Samples |
| TLV3702IDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AKD | Samples |
| TLV3702IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702I | Samples |
| TLV3702IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702I | Samples |
| TLV3702IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3702I | Samples |
| TLV3702IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3702I | Samples |
| TLV3704CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3704C | Samples |
| TLV3704CDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3704C | Samples |
| TLV3704CPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3704C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3704CPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 3704C | Samples |
| TLV3704ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |
| TLV3704IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |
| TLV3704IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |
| TLV3704IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |
| TLV3704IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3704I | Samples |
| TLV3704INE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV3704I | Samples |
| TLV3704IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |
| TLV3704IPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |
| TLV3704IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |
| TLV3704IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3704I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF TLV3701, TLV3702 :**

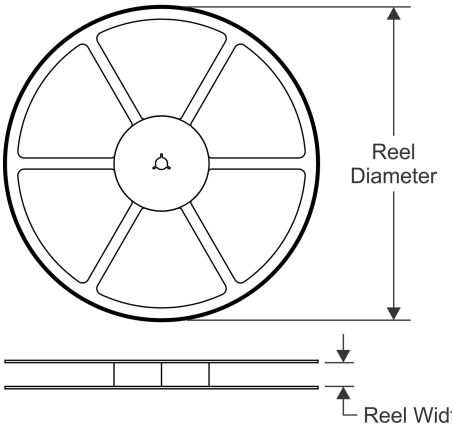
- Automotive: TLV3701-Q1, TLV3702-Q1
- Enhanced Product: TLV3701-EP

NOTE: Qualified Version Definitions:

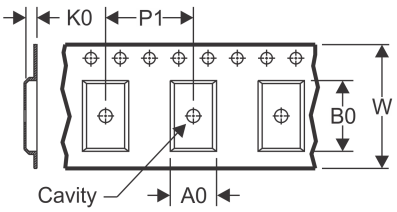
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

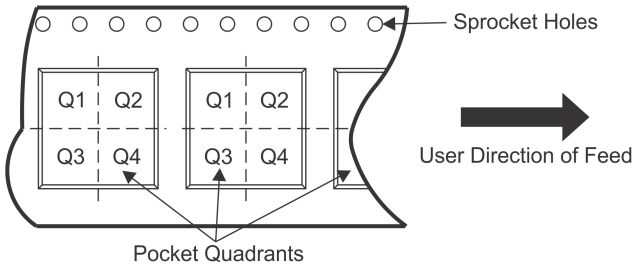



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

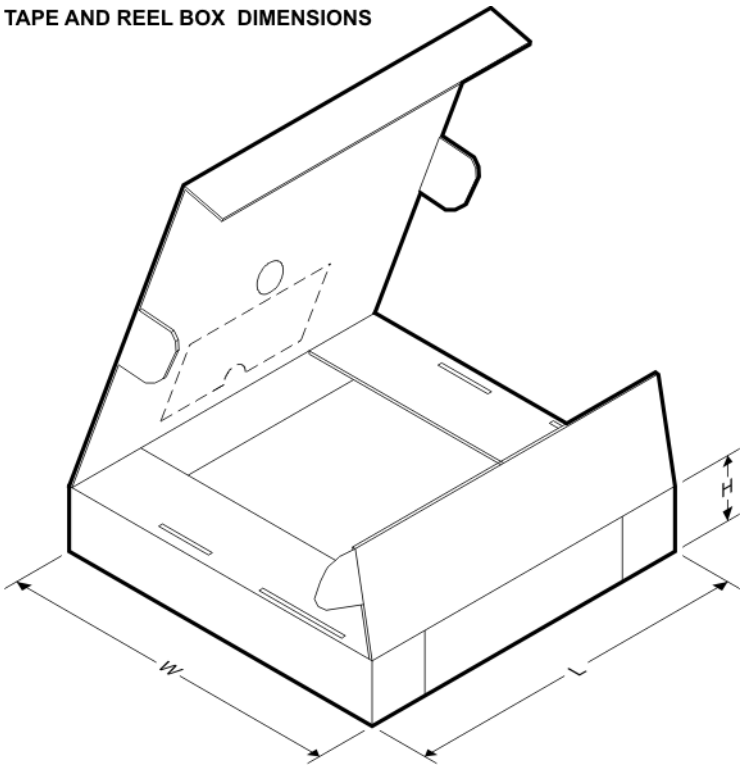
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV3701CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3701CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3701IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3701IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3701IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3702CDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV3702IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV3702IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3704IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV3704IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

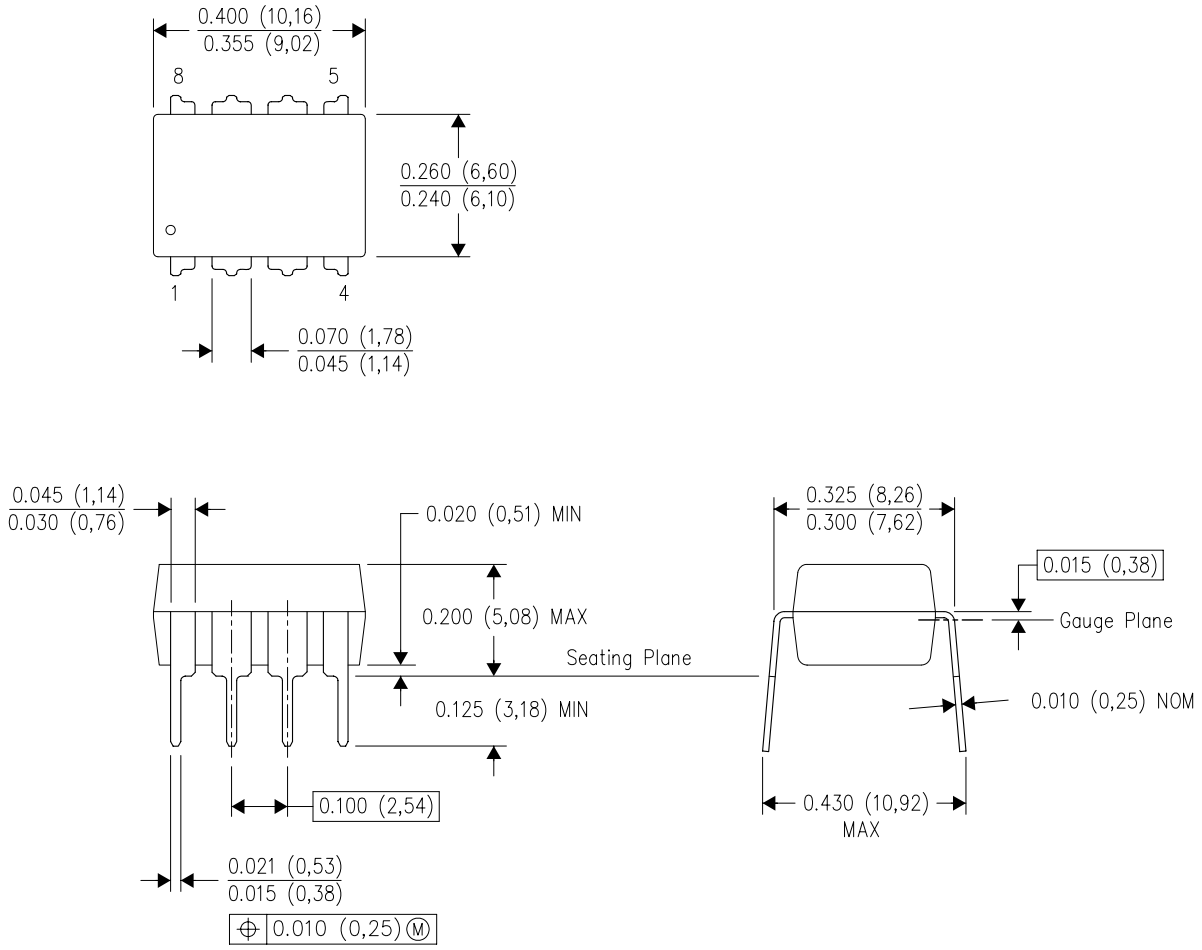
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

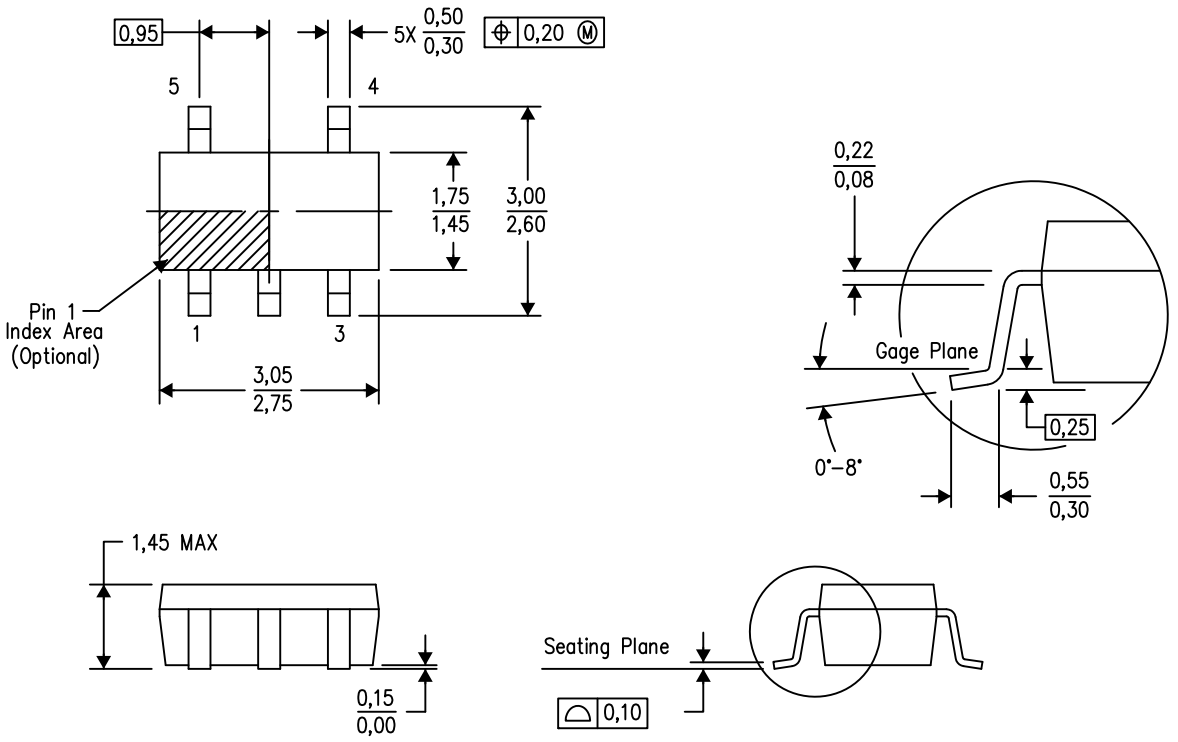
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV3701CDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV3701CDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV3701IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV3701IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV3701IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV3702CDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV3702IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV3702IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV3704IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV3704IPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

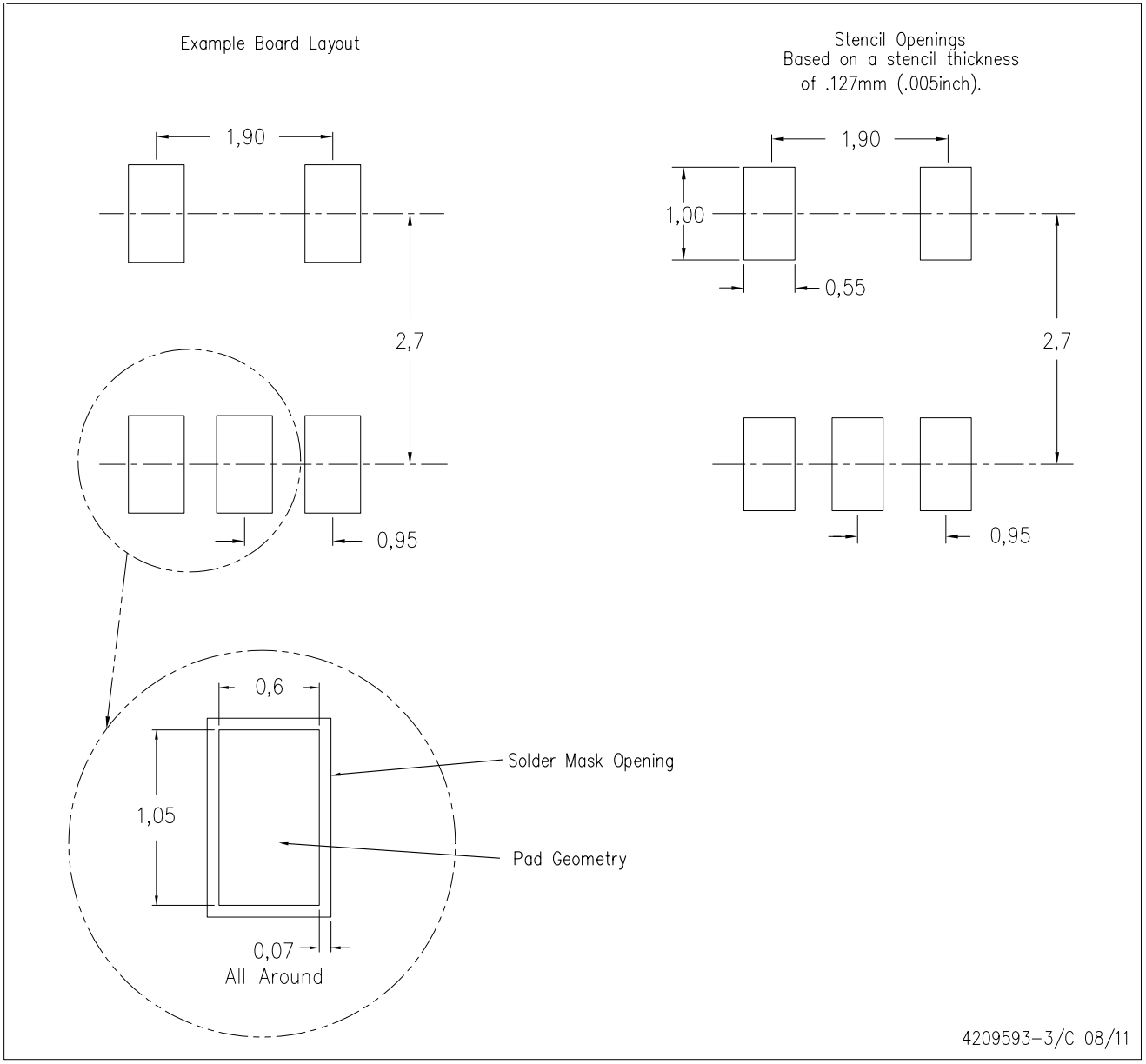
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/L 08/2013

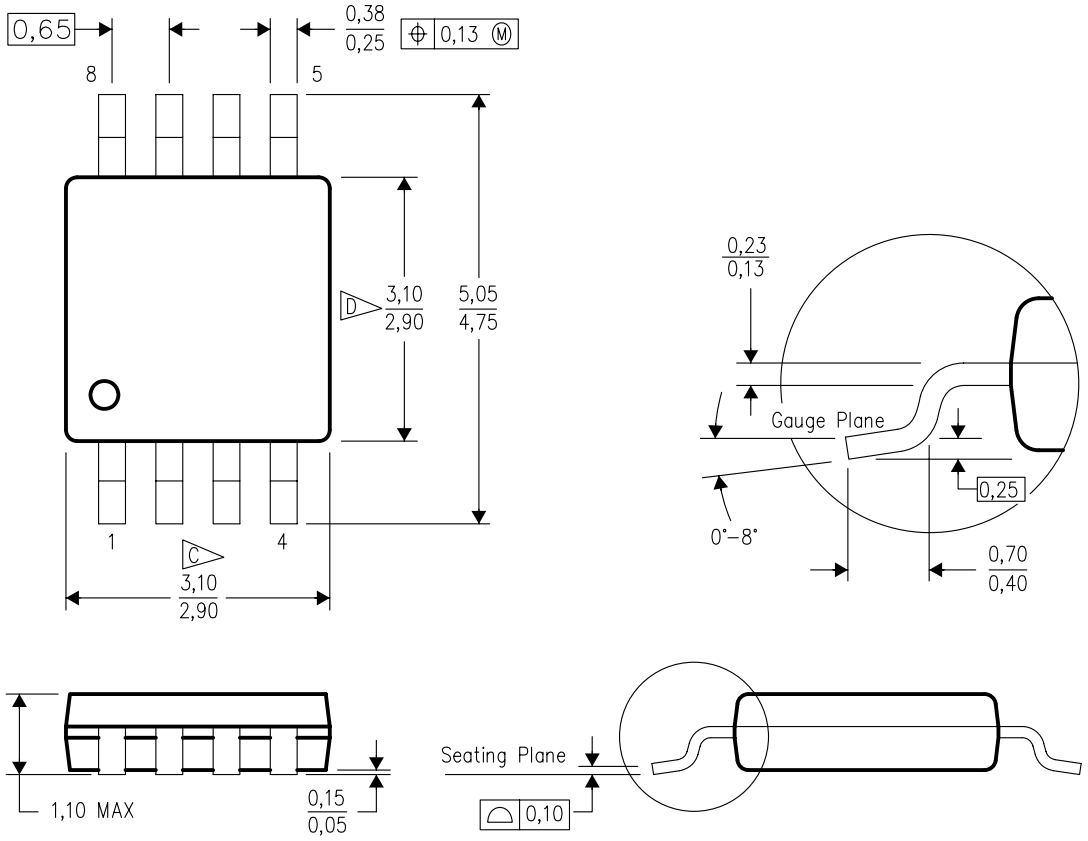
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

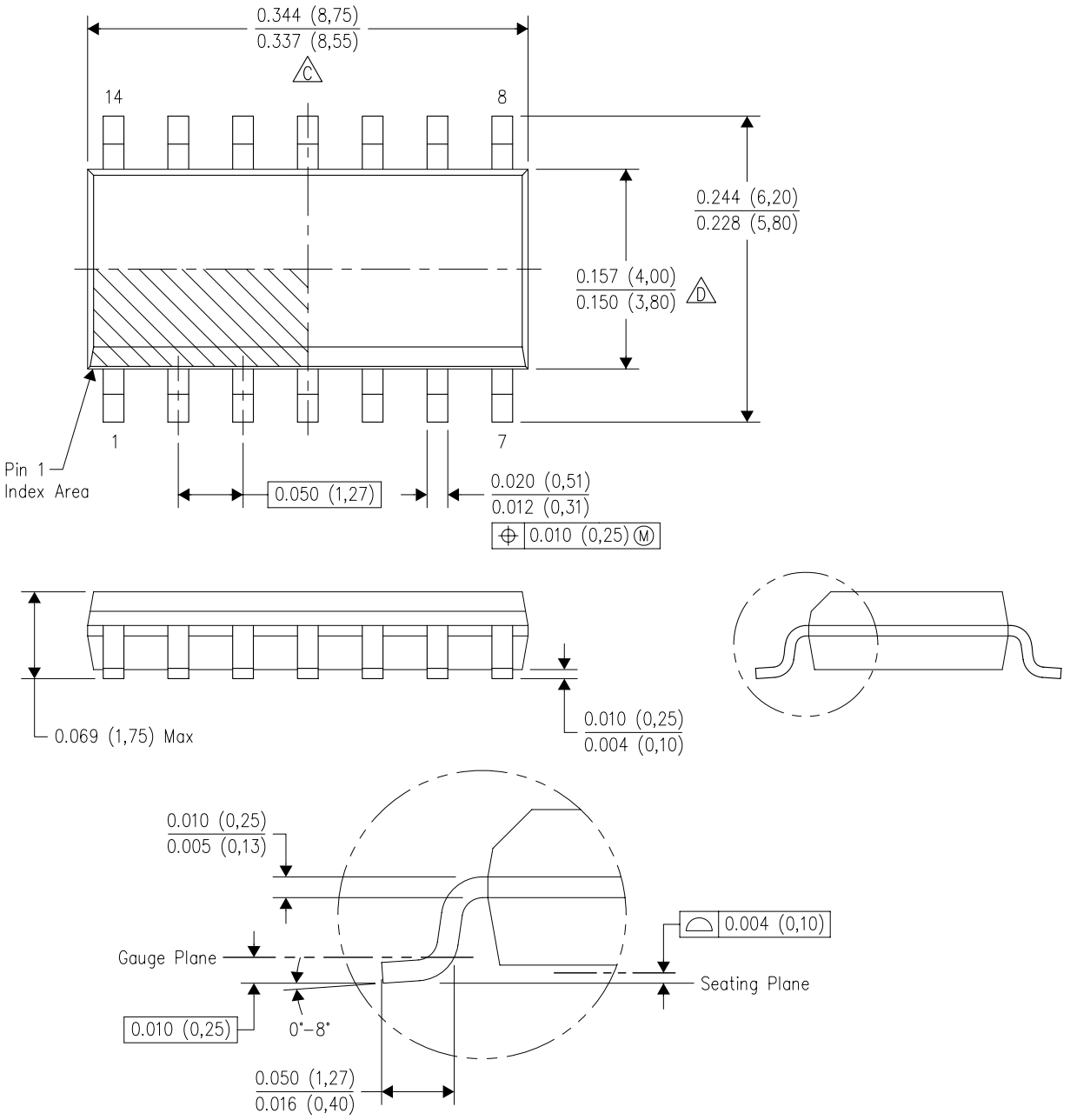
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

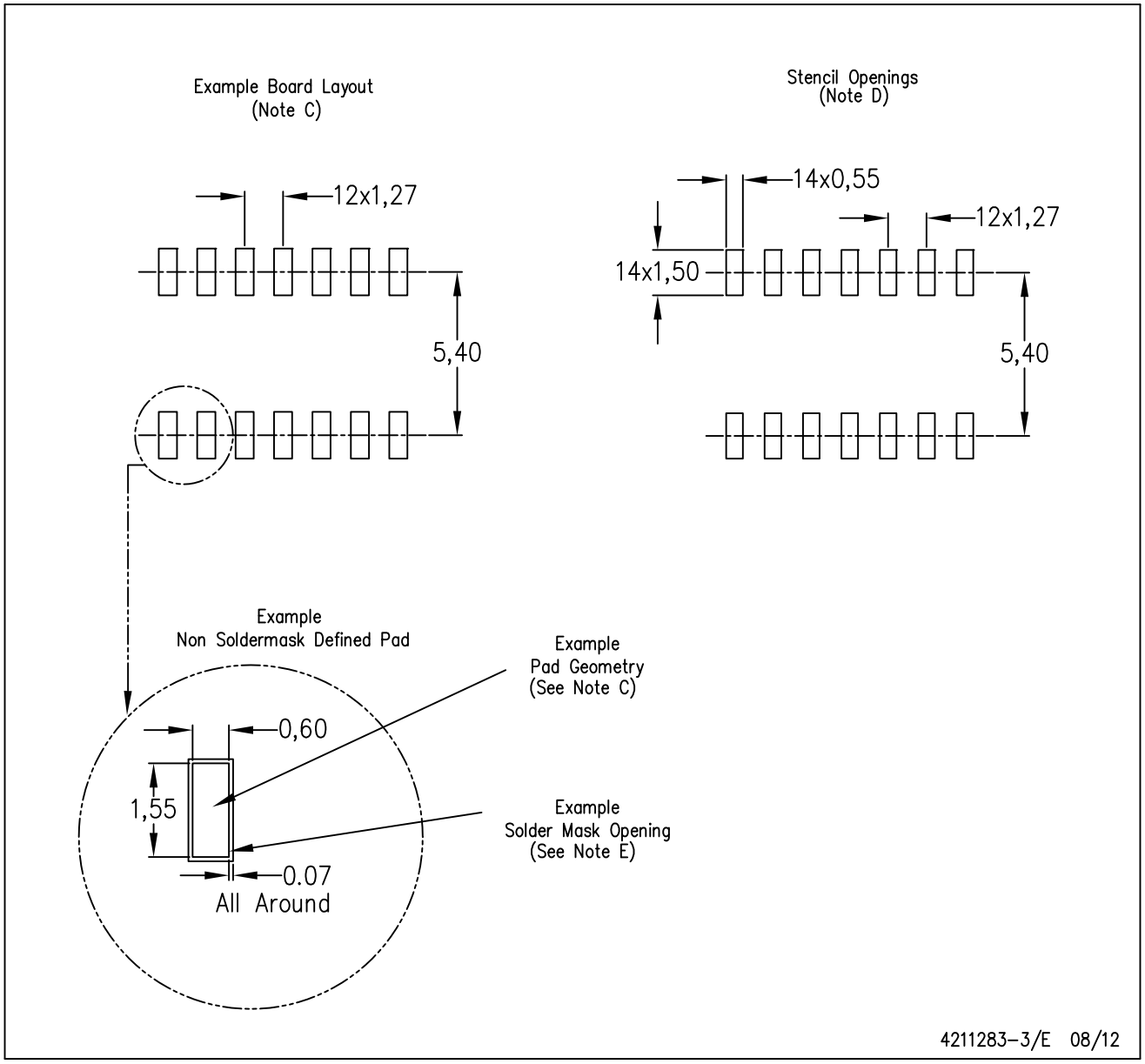
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

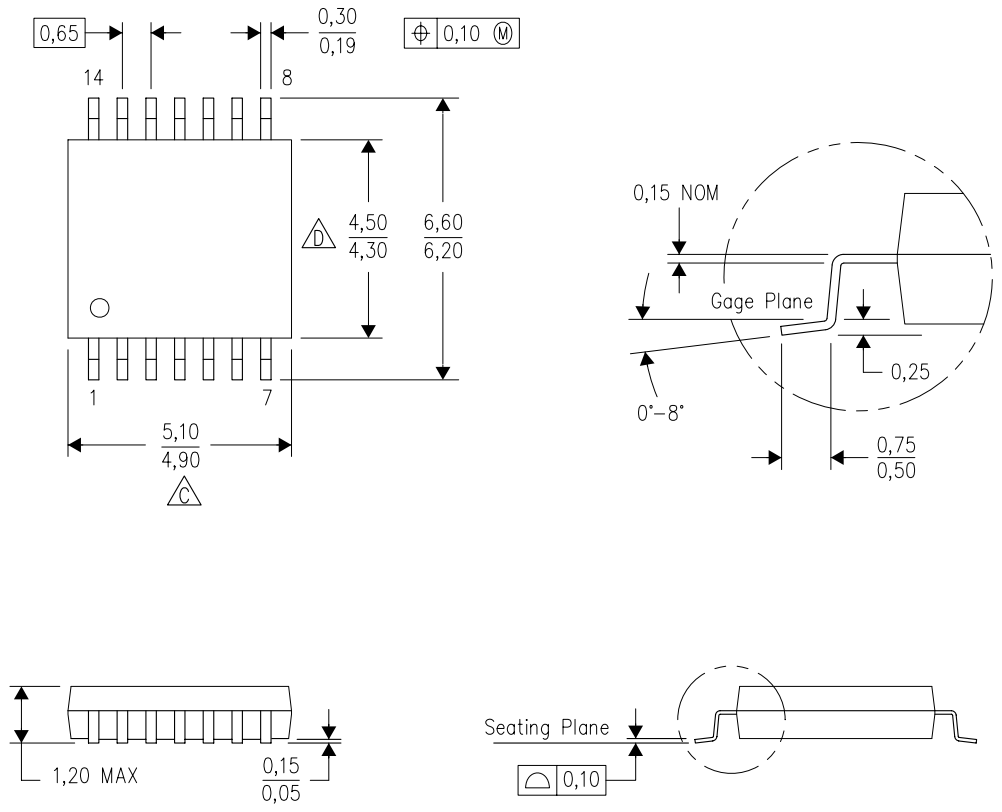
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

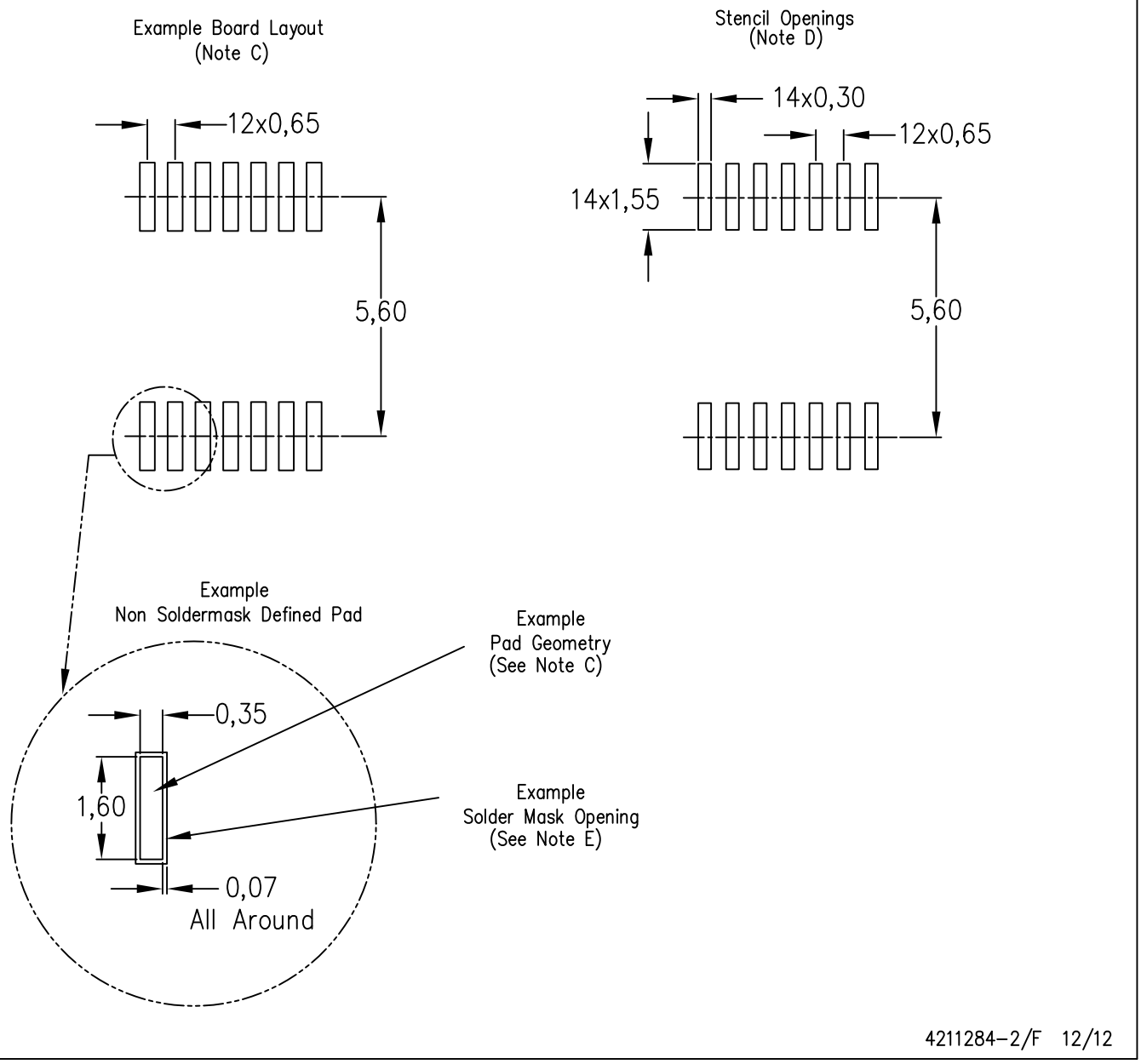
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

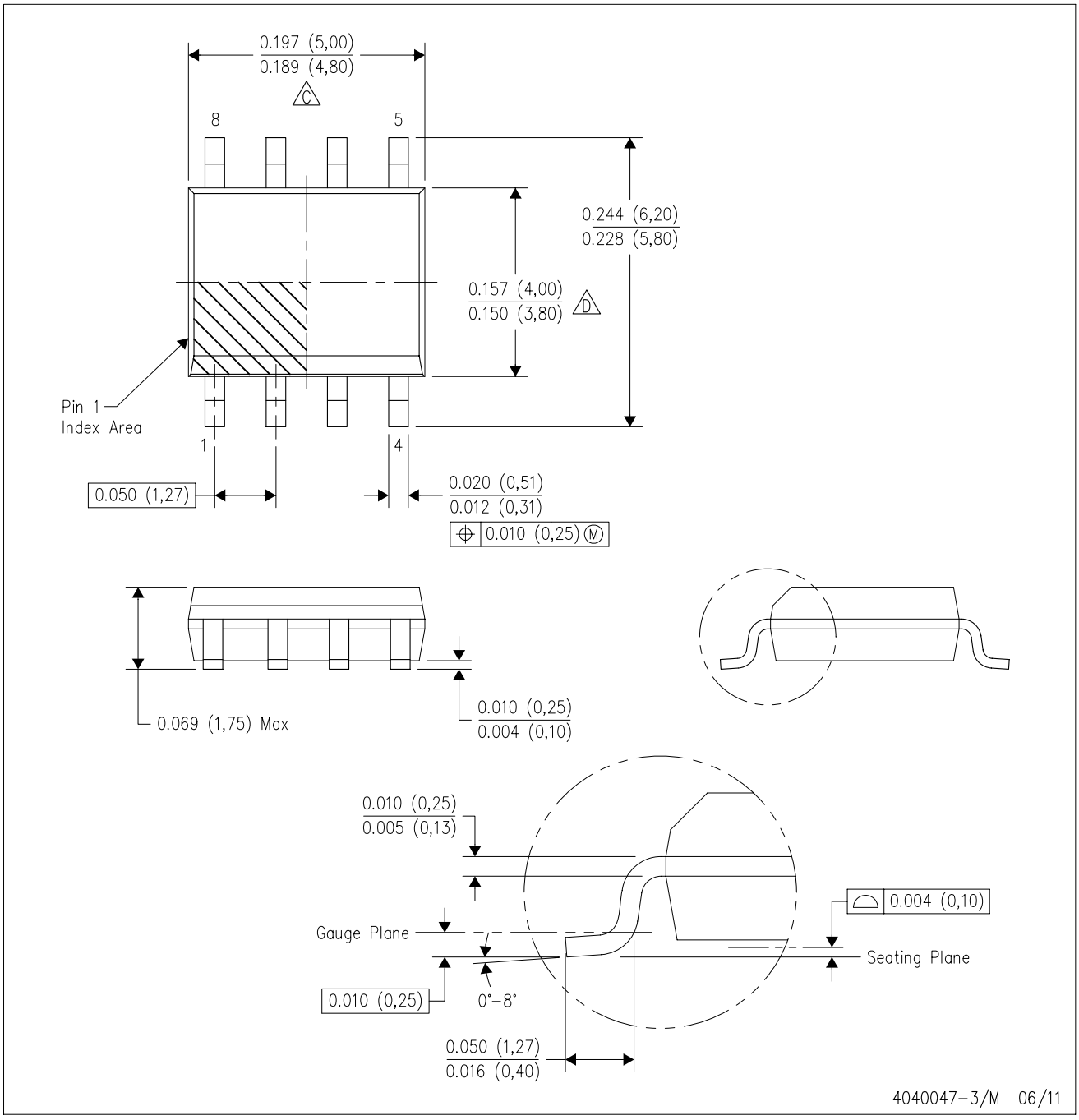
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



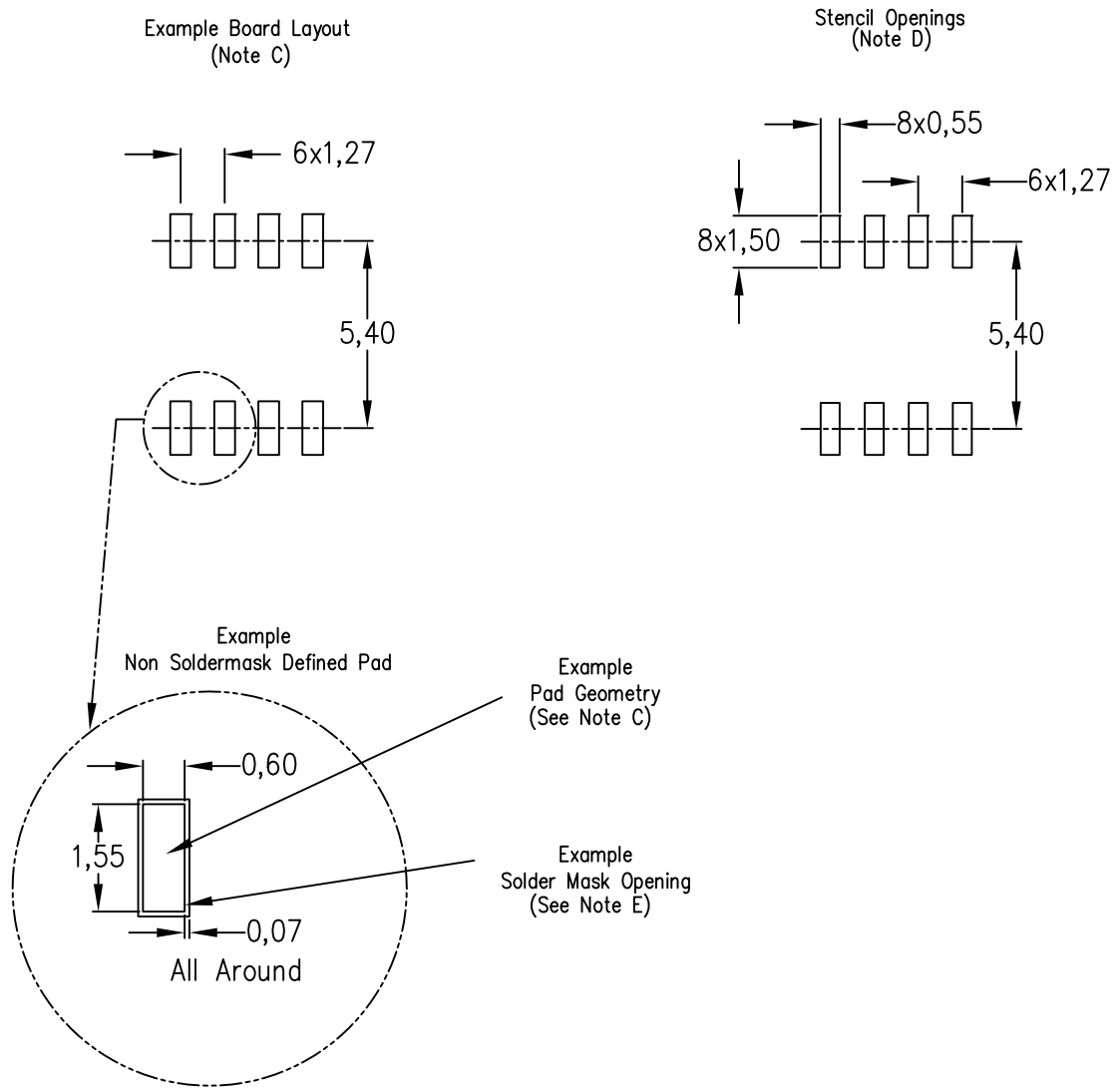

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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