TLV320DAC32EVM and TLV320DAC32EVM-PDK

This user's guide describes the characteristics, operation, and use of the TLV320DAC32EVM, both by itself and as part of the TLV320DAC32EVM-PDK. This evaluation module (EVM) is a complete stereo audio DAC with digital audio inputs, two line inputs and analog outputs, extensive audio routing, mixing and effects capabilities. A complete circuit description, schematic diagram and bill of materials are also included.

The following related documents are available through the Texas Instruments web site at www.ti.com.

EVM-Compatible Device Data Sheets

Device	Literature Number
TLV320DAC32	SLAS506
TAS1020B	SLES025
REG1117-3.3	SBVS001
TPS767D318	SLVS209
SN74LVC125A	SCAS290
SN74LVC1G125	SCES223
SN74LVC1G07	SCES296

Contents

1 EVM Overview 2
2 Analog Interface 3
3 Digital Interface 4
4 Power Supplies 5
5 EVM Operation 6
6 Kit Operation 7
7 EVM Bill of Materials 25
Appendix A TLV320DAC32EVM Schematic 28
Appendix B USB-MODEVM Schematic 29
Appendix C USB-MODEVM Communications Protocol 30

List of Figures

1 TLV320DAC32EVM-PDK Block Diagram 7
2 Digital Audio Data/DAC Tab 9
3 Clocks Tab 12
4 Filters Tab 13
5 Enabling Filters 14
6 Shelf Filters 14
7 EQ Filters 15
8 Analog Simulation Filters 16
9 Preset Filters 17
10 De-emphasis Filters 18

I^2S, I^2C are trademarks of Koninklijke Philips Electronics N.V.
Windows is a trademark of Microsoft Corporation.
SPI is a trademark of Motorola, Inc.
LabView is a trademark of National Instruments.

11 User Filters 19
12 3D Effect Settings 19
13 Output Stage Configuration Tab 20
14 High Power Output 21
15 Command Line Interface Tab 22
16 File Menu 23
17 Register Data Tab 24

List of Tables

1 Analog Interface Pin Out 3
2 Alternate Analog Connectors 3
3 Digital Interface Pin Out 4
4 Power Supply Pin Out 5
5 List of Jumpers 6
6 USB-MODEVM SW2 Settings 8
7 TLV320DAC32EVM Bill of Materials 25
8 USB-MODEVM Bill of Materials 27
C-1 USB Control Endpoint HIDSETREPORT Request 30
C-2 Data Packet Configuration 30
C-3 GPIO Pin Assignments 35

1 EVM Overview

1.1 Features

- Full-featured evaluation board for the TLV320DAC32 stereo audio codec.
- Modular design for use with a variety of digital signal processor (DSP) and microcontroller interface boards.

The TLV320DAC32EVM-PDK is a complete evaluation kit, which includes a universal serial bus (USB)-based motherboard and evaluation software for use with a personal computer running the Microsoft Windows™ operating system (Win2000 or XP).

1.2 Introduction

The TLV320DAC32EVM is in Texas Instruments' modular EVM form factor, which allows direct evaluation of the device performance and operating characteristics, and eases software development and system prototyping. This EVM is compatible with the 5-6K Interface Evaluation Module (SLAU104) and the HPA-MCUINTERFACE (SLAU106) from Texas Instruments and additional third-party boards which support TI's Modular EVM format.

The TLV320DAC32EVM-PDK is a complete evaluation/demonstration kit, which includes a USB-based motherboard called the USB-MODEVM Interface board and evaluation software for use with a personal computer running the Microsoft Windows operating systems.

2 Analog Interface

For maximum flexibility, the TLV320DAC32EVM is designed for easy interfacing to the input and outputs analog signals. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J1. These headers/sockets provide access to the analog input and output pins of the device. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 summarizes the analog interface pinout for the TLV320DAC32EVM.

Table 1. Analog Interface Pin Out

PIN NUMBER	SIGNAL	DESCRIPTION
J1.1	HPLCOM	High Power Output Driver (Left Minus or Multifunctional)
J1.2	HPLOUT	High Power Output Driver (Left Plus)
J1.3	HPRCOM	High Power Output Driver (Right Minus or Multifunctional)
J1.4	HPROUT	High Power Output Driver (Right Plus)
J1.5	NC	Not Connected
J1.6	NC	Not Connected
J1.7	LINE2L	LINE2 Analog Input (Left)
J1.8	LINE2R	LINE2 Analog Input (Right)
J1.9	AGND	Analog Ground
J1.10	NC	Not Connected
J1.11	AGND	Analog Ground
J1.12	NC	Not Connected
J1.13	AGND	Analog Ground
J1.14	MICBIAS	Microphone Bias Voltage Output
J1.15	NC	Not Connected
J1.16	NC	Not Connected
J1.17	AGND	Analog Ground
J1.18	NC	Not Connected
J1.19	AGND	Analog Ground
J1.20	NC	Not Connected

In addition to the analog headers, the analog inputs and outputs may also be accessed through alternate connectors, either screw terminals or audio jacks. The line input is connected via J8 and the stereo headphone output (the HP set of outputs) is available at J9.

Table 2 summarizes the screw terminals available on the TLV320DAC32EVM.

Table 2. Alternate Analog Connectors

DESIGNATOR	PIN 1	PIN 2	PIN3
J6	AGND	LINE2INR	LINE2INL
J12	(+) HPLOUT	(–) HPLCOM	AGND
J13	(+) HPROUT	(–) HPRCOM	AGND
J14	(+) HPLOUT MEASUREMENT	(–) HPLCOM MEASUREMENT	AGND
J15	(+) HPROUT MEASUREMENT	(–) HPRCOM MEASUREMENT	AGND

3 Digital Interface

The TLV320DAC32EVM is designed to interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J4 and J5. These headers/sockets provide access to the digital control and serial data pins of the device. Consult Samtec at www.samtec.com or call 1-800- SAMTEC-9 for a variety of mating connector options. Table 3 summarizes the digital interface pinout for the TLV320DAC32EVM.

Table 3. Digital Interface Pin Out

PIN NUMBER	SIGNAL	DESCRIPTION
J4.1	NC	Not Connected
J4.2	GPIO1	General Purpose Input/Output #1
J4.3	SCLK	SPI Serial Clock
J4.4	DGND	Digital Ground
J4.5	NC	Not Connected
J4.6	GPIO2	General Purpose Input/Output #2
J4.7	$\overline{SS}$	SPI Chip Select
J4.8	RESET INPUT	Reset signal input to DAC32EVM
J4.9	NC	Not Connected
J4.10	DGND	Digital Ground
J4.11	MOSI	SPI MOSI Slave Serial Data Input
J4.12	SPI SELECT	Select Pin (SPI vs I^2C Control Mode)
J4.13	MISO	SPI MISO Slave Serial Data Output
J4.14	DAC32 $\overline{RESET}$	Reset
J4.15	NC	Not Connected
J4.16	SCL	I^2C Serial Clock
J4.17	NC	Not Connected
J4.18	DGND	Digital Ground
J4.19	NC	Not Connected
J4.20	SDA	I^2C Serial Data Input/Output
J5.1	NC	Not Connected
J5.2	NC	Not Connected
J5.3	BCLK	Audio Serial Data Bus Bit Clock (Input/Output)
J5.4	DGND	Digital Ground
J5.5	NC	Not Connected
J5.6	NC	Not Connected
J5.7	WCLK	Audio Serial Data Bus Word Clock (Input/Output)
J5.8	NC	Not Connected
J5.9	NC	Not Connected
J5.10	DGND	Digital Ground
J5.11	DIN	Audio Serial Data Bus Data Input (Input)
J5.12	NC	Not Connected
J5.13	DOUT	Audio Serial Data Bus Data Output (Output)
J5.14	NC	Not Connected
J5.15	NC	Not Connected
J5.16	SCL	I^2C Serial Clock
J5.17	MCLK	Master Clock Input
J5.18	DGND	Digital Ground
J5.19	NC	Not Connected
J5.20	SDA	I^2C Serial Data Input/Output

Note that J5 comprises the signals needed for an I²S™ serial digital audio interface; the control interface (I²C™ and $\overline{\text{RESET}}$) signals are routed to J4. I²C is actually routed to both connectors; however, the device is connected only to J4.

4 Power Supplies

J3 provides connection to the common power bus for the TLV320DAC32EVM. Power is supplied on the pins listed in Table 4.

Table 4. Power Supply Pin Out

SIGNAL	PIN NUMBER		SIGNAL
NC	J3.1	J3.2	NC
+5VA	J3.3	J3.4	NC
DGND	J3.5	J3.6	AGND
DVDD (1.8V)	J3.7	J3.8	NC
IOVDD (3.3V)	J3.9	J3.10	NC

The TLV320DAC32EVM-PDK motherboard (the USB-MODEVM Interface board) supplies power to J3 of the TLV320DAC32EVM. Power for the motherboard is supplied either through its USB connection or via terminal blocks on that board.

4.1 Stand-Alone Operation

When used as a stand-alone EVM, power can be applied to J3 directly, making sure to reference the supplies to the appropriate grounds on that connector.

CAUTION

Verify that all power supplies are within the safe operating limits shown on the TLV320DAC32 data sheet before applying power to the EVM.

4.2 USB-MODEVM Interface Power

The USB-MODEVM Interface board can be powered from several different sources:

- USB
- 6VDC-10VDC AC/DC external wall supply (not included)
- Lab power supply

When powered from the USB connection, JMP6 should have a shunt from pins 1–2 (this is the default factory configuration). When powered from 6V-10VDC, either through the J8 terminal block or J9 barrel jack, JMP6 should have a shunt installed on pins 2–3. If power is applied in any of these ways, onboard regulators generate the required supply voltages and no further power supplies are necessary.

If lab supplies are used to provide the individual voltages required by the USB-MODEVM Interface, JMP6 should have no shunt installed. Voltages are then applied to J2 (+5VA), J3 (+5VD), J4 (+1.8VD), and J5 (+3.3VD). The +1.8VD and +3.3VD can also be generated on the board by the onboard regulators from the +5VD supply; to enable this configuration, the switches on SW1 need to be set to enable the regulators by placing them in the ON position (lower position, looking at the board with text reading right-side up). If +1.8VD and +3.3VD are supplied externally, disable the onboard regulators by placing SW1 switches in the OFF position.

Each power supply voltage has an LED (D1-D7) that lights when the power supplies are active.

5 EVM Operation

This section provides information on the analog input and output, digital control, and general operating conditions of the TLV320DAC32EVM.

5.1 Analog Input

The analog input sources can be applied directly to J1 (top or bottom side) or through signal conditioning modules available for the modular EVM system.

The analog inputs may also be accessed through J8 and and screw terminal, J6.

5.2 Analog Output

The analog outputs from the TLV320DAC32 are available on screw terminals, J12 and J13. They also may be accessed at the test points on the EVM with the corresponding label. When measuring the performance of the device, the outputs can be routed through an RC low-pass filter to reduce the out-of-band noise which can cause incorrect readings from the measurement equipment. These filtered outputs can be accessed on screw terminals J14 and J15.

5.3 Digital Control

The digital control signals can be applied directly to J4 and J5 (top or bottom side). The modular TLV320DAC32EVM can also be connected directly to a DSP interface board, such as the 5-6KINTERFACE or HPA-MCUINTERFACE, or to the USB-MODEVM Interface board if purchased as part of the TLV320DAC32EVM-PDK. See the product folder for this EVM or the TLV320DAC32 for a current list of compatible interface and/or accessory boards.

5.4 Default Jumper Locations

Table 5 provides a list of jumpers found on the EVM and their factory default conditions.

Table 5. List of Jumpers

JUMPER	DEFAULT POSITION	JUMPER DESCRIPTION
JMP1	Installed	Connects Analog and Digital Grounds.
JMP2	Open	Selects on-board EEPROM as Firmware Source.
JMP5	1-2	Connects the IOVDD supply of the codec to IOVDD or DVDD. It also provides a means of measuring IOVDD current.
JMP6	Installed	Provides a means of measuring DVDD current.
JMP7	Installed	Provides a means of measuring DRVDD current.
JMP8	Installed	Provides a means of measuring AVDD_DAC current.
JMP9	Open	When installed, allows the USB-MODEVM to hardware reset the device under user control
JMP11	Installed	When installed, shorts across the output capacitor on HPLOUT; remove this jumper if using AC-coupled output drive
JMP12	Installed	When installed, shorts HPLCOM and HPRCOM. Use only if these signals are set to constant VCM.
JMP13	Installed	When installed, shorts across the output capacitor on HPLCOM; remove this jumper if using AC-coupled output drive
JMP14	Installed	When installed, shorts across the output capacitor on HPROUT; remove this jumper if using AC-coupled output drive
JMP15	Installed	When installed, shorts across the output capacitor on HPRCOM; remove this jumper if using AC-coupled output drive

6 Kit Operation

The following section provides information on using the TLV320DAC32EVM-PDK, including set up, program installation, and program usage.

6.1 TLV320DAC32EVM-PDK Block Diagram change

A block diagram of the TLV320DAC32EVM-PDK is shown in Figure 1. The evaluation kit consists of two circuit boards connected together. The motherboard is designated as the USB-MODEVM Interface board, while the daughtercard is the TLV320DAC32EVM described previously in this manual.

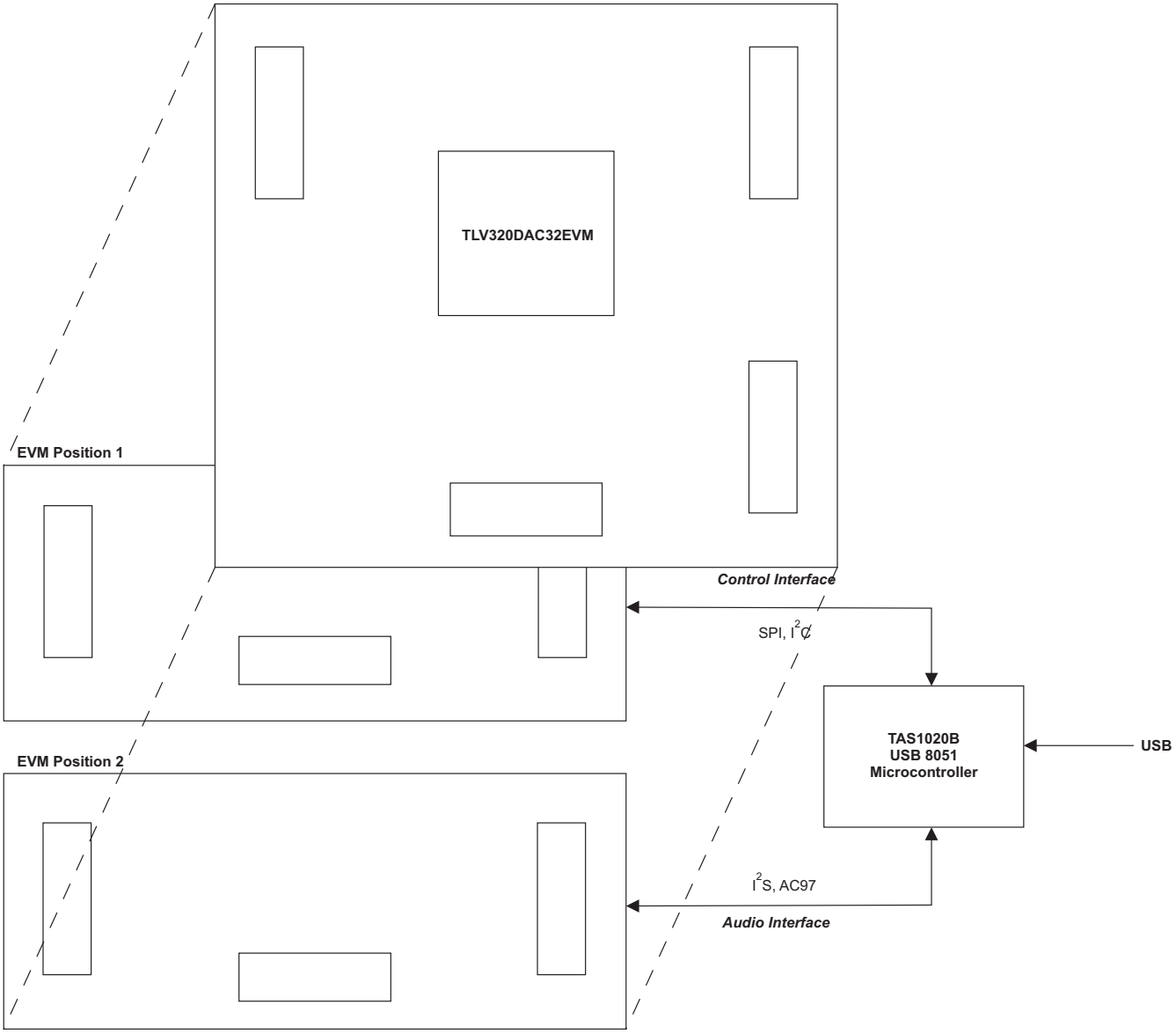


Figure 1. TLV320DAC32EVM-PDK Block Diagram

The USB-MODEVM Interface board is intended to be used in USB mode, where control of the installed EVM is accomplished using the onboard USB controller device. However, a provision is made for driving all the data buses (I^2C, SPI™, I^2S/AC97) externally. The source of these signals is controlled by SW2 on the USB-MODEVM. See Table 6 for details on the switch settings.

Table 6. USB-MODEVM SW2 Settings

SW-2 SWITCH NUMBER	LABEL	SWITCH DESCRIPTION
1	A0	USB-MODEVM EEPROM I²C Address A0 ON: A0 = 0 OFF: A0 = 1
2	A1	USB-MODEVM EEPROM I²C Address A1 ON: A1 = 0 OFF: A1 = 1
3	A2	USB-MODEVM EEPROM I²C Address A2 ON: A2 = 0 OFF: A2 = 1
4	USB I²S	I²S Bus Source Selection ON: I²S Bus connects to TAS1020B OFF: I²S Bus connects to USB-MODEVM J14
5	USB MCK	I²S Bus MCLK Source Selection ON: MCLK connects to TAS1020B OFF: MCLK connects to USB-MODEVM J14
6	USB SPI	SPI Bus Source Selection ON: SPI Bus connects to TAS1020B OFF: SPI Bus connects to USB-MODEVM J15
7	USB RST	RST Source Selection ON: EVM Reset Signal comes from TAS1020B OFF: EVM Reset Signal comes from USB-MODEVM J15
8	EXT MCK	External MCLK Selection ON: MCLK Signal is provided from USB-MODEVM J10 OFF: MCLK Signal comes from either selection of SW2-5

For use with the TLV320DAC32EVM, SW-2 positions 1 through 7 should be set to ON, while SW-2.8 should be set to OFF.

6.2 Installation

Ensure that the TLV320DAC32EVM is installed on the USB-MODEVM Interface board, aligning J1, J3, J4, and J5 with the corresponding connectors on the USB-MODEVM.

Place the CD-ROM into your PC CD-ROM drive. Locate the **Setup** program on the disk, and run it. The Setup program will install the TLV320DAC32 Evaluation software on the user's PC. The software for NI-VISA Runtime will install automatically if it has not been previously installed. This software allows the program to communicate with USB.

When the installation completes, click *Finish* on the TLV320DAC32EVM installer window. The user may be prompted to restart the computer.

When installation is complete, attach a USB cable from the PC to the USB-MODEVM Interface board. As configured at the factory, the board will be powered from the USB interface, so the power indicator LEDs on the USB-MODEVM should light. At this time, the PC may go through an initialization of the drivers to properly operate the USB-MODEVM interface board. Once this connection is established and any driver configuration has completed, launch the TLV320DAC32EVM Evaluation software on the PC.

The software should automatically find the TLV320DAC32EVM, and a screen similar to the one in Figure 2 should appear.

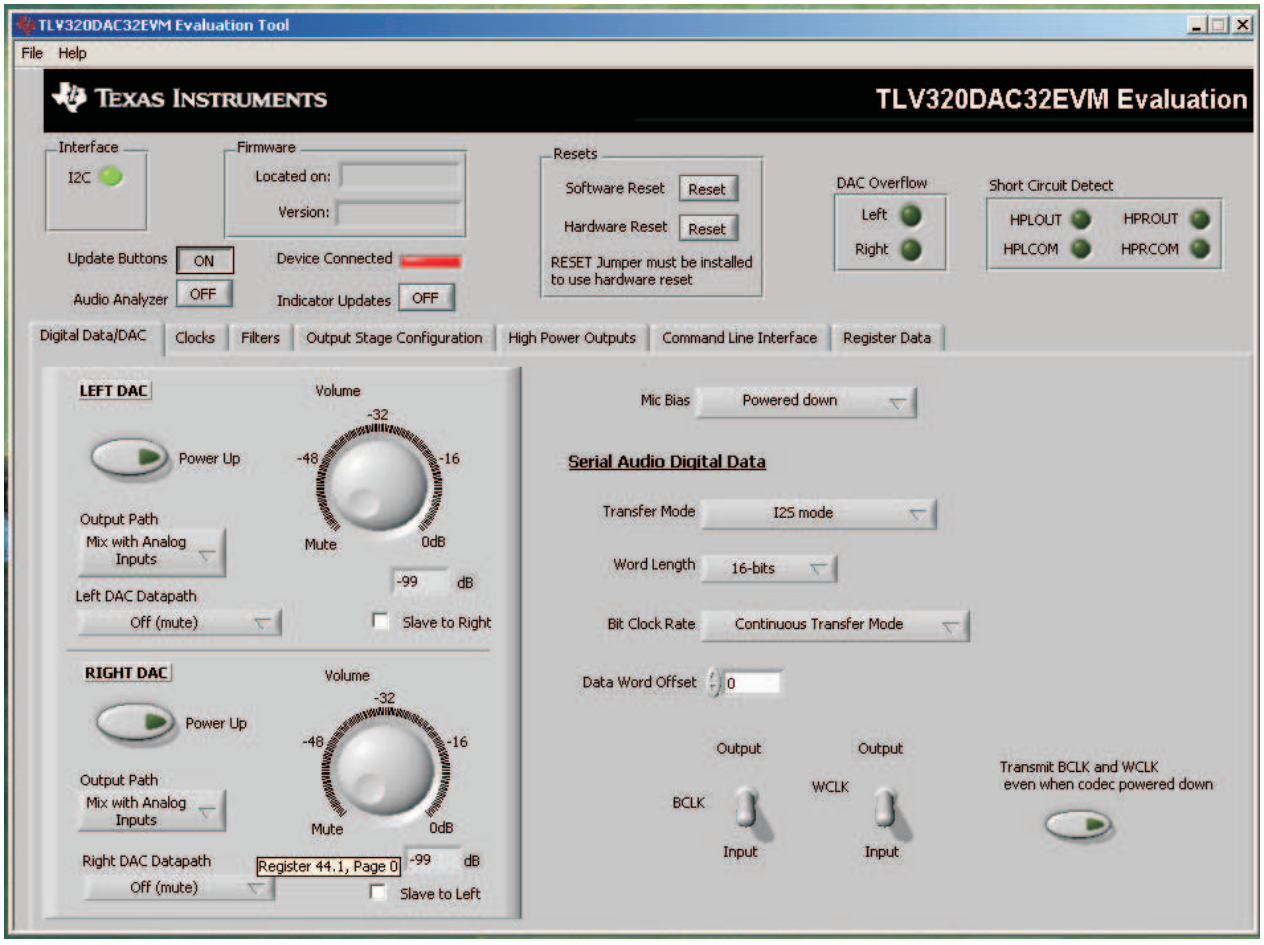


Figure 2. Digital Audio Data/DAC Tab

6.3 USB-MODEVM Interface Board

The diagram shown in Figure 1 displays only the basic features of the USB-MODEVM Interface board. The board is built around a TAS1020B streaming audio USB controller with an 8051-based core. The board features two positions for modular EVMs, or one double-wide serial modular EVM may be installed.

Since the TLV320DAC32EVM is a double-wide modular EVM, it is installed with connections to both EVM positions, which connects the TLV320DAC32 digital control interface to the I^2C port realized using the TAS1020B, as well as the TAS1020B digital audio interface..

In the factory configuration, the board is ready to use with the TLV320DAC32EVM. To view all the functions and configuration options available on the USB-MODEVM board, see the USB-MODEVM Interface Board schematic in Appendix B.

6.4 Indicators and Main Screen Controls

Figure 2 illustrates the indicators and controls near the top of the screen, and a large tabbed interface below. This section covers the controls above this tabbed section.

6.4.1 Interface Indicator

At the top left of the screen is an **Interface** indicator. The TLV320DAC32 has an I^2C interface. The indicator is lit after the program begins.

6.4.2 Firmware Information

To the right of the Interface indicator is a group box called **Firmware**. This box indicates where the firmware being used is operating from — in this release, the firmware is on the USB-MODEVM, so *USB-MODEVM* should be visible in the box labeled **Located On:**. The version of the firmware appears in the **Version** box below this.

6.4.3 Device Connected Indicator

Below the **Firmware** group box, an indicator labeled DEVICE CONNECTED shows the status of the USB connection. It the indicator is green, then the USB connection is good and the software is ready to use. If the indicator is red, then there is an error and the software is not recognizing the EVM.

6.4.4 Device Reset Controls

To the right, the next group box contains controls for resetting the TLV320DAC32. A software reset can be done by writing to a register in the TLV320DAC32, and this is accomplished by pushing the button labeled **Software Reset**. The TLV320DAC32 also may be reset by toggling a pin on the TLV320DAC32, which is done by pushing the **Hardware Reset** button.

CAUTION

In order to perform a hardware reset, the RESET jumper (JMP9) must be installed and SW2-7 on the USB-MODEVM must be turned OFF. Failure to do either of these steps results in not generating a hardware reset or causing unstable operation of the EVM, which may require cycling power to the USB-MODEVM.

The **DAC Overflow** indicator lights when the overflow flags are set in the TLV320DAC32. These indicators, as well as the other indicators on this panel, are updated only when the software's front panel is inactive, once every 20ms. To the far right on this screen, the short-circuit indicators show when a short-circuit condition is detected, if this feature has been enabled.

6.4.5 Update Buttons Control

Near the left side of the screen is a button labeled **Update Buttons**. This button defaults to ON and can be turned off it desired. The buttons allows for the software indicators (buttons, knobs, and dials) to be automatically updated to reflect the device status when the device is configured by means of the Command Line Interface (see Section 6.9.1).

6.5 Digital Audio Data/DAC Tab

The Audio Interface tab (Figure 2) sets up the audio data interface to the TLV320DAC32 and controls the operation of the DAC.

6.5.1 DAC Controls

On the left side of this tab are controls for the left and right DACs.

The DAC controls are set up to allow powering of each DAC individually, and setting the output level. Each channel's level can be set independently using the corresponding **Volume** knob. Alternately, by checking the **Slave to Right** box, the left channel Volume can be made to track the right channel Volume knob setting; checking the **Slave to Left** box causes the right channel Volume knob to track the left Volume knob setting.

Data going to the DACs is selected using the drop-down boxes under the **Left and Right Datapath**. Each DAC channel can be selected to be off, use left channel data, use right channel data, or use a mono mix of the left and right data.

Analog audio coming from the DACs is routed to outputs using the **Output Path** controls in each DAC control panel. The DAC outputs can be mixed with the analog inputs (LINE2L, LINE2R) and routed to the high power outputs using the mixer controls on the **High Power Outputs** tab. If the DAC is to be routed directly to HP outputs, this can be selected as choices in the Output Path control. Note that if "HP Output Driver" option is selected as the output path, the mixer controls on the **High Power Output** tabs have no effect.

6.5.2 MICBIAS Control

The microphone bias can either be powered down or set to 2.0V, 2.5V, or the power supply voltage of the DAC (AVDD).

6.5.3 Digital Audio Data Controls

The DAC32 allows for multiple serial audio digital data configurations to provide maximum flexibility.

For use with the PC software and the USB-MODEVM, the default settings should be used. If using an external I^2S source, or other data source, the interface mode may be selected using the **Transfer Mode** control—selecting either I^2S mode, DSP mode, or Right- or Left-Justified modes. Word length can be selected using the **Word Length** control, and the bit clock rate can also be selected using the **Bit Clock** rate control. The **Data Word Offset**, used in TDM mode (see the SLAS506 product data sheet) can also be selected on this tab.

Along the bottom of this tab are controls for choosing the **BLCK** and **WCLK** as being either inputs or outputs. When the codec is desired to be a master, **BLCK** and **WCLK** should be set to Output. When the codec is desired to be a slave, the default settings of Input are correct. An indicator that allows for transmitting BLCK and WCLK when the codec is powered down is also located at the bottom of this tab.

6.6 Clocks Tab

The TLV320DAC32 has a very flexible scheme for generating the clock sources for the DAC sample rate. The Clocks tab allows access to set the different options for setting up these clocks. Refer to the Audio Clock Generation Processing figure in the TLV320DAC32 data sheet.

For use with the PC software and the USB-MODEVM, the clock settings must be set a certain way. These settings are not the default settings of the TLV320DAC32. The EVM-required settings can be loaded automatically by pushing the **Load EVM Clock Settings** button at the bottom of this tab. Note that changing any of the clock settings from the values loaded when this button is pushed may result in the EVM not working properly with the PC software or USB interface. If an external audio bus is used (audio not driven over the USB bus), then settings may be changed to any valid combination. See Figure 3.

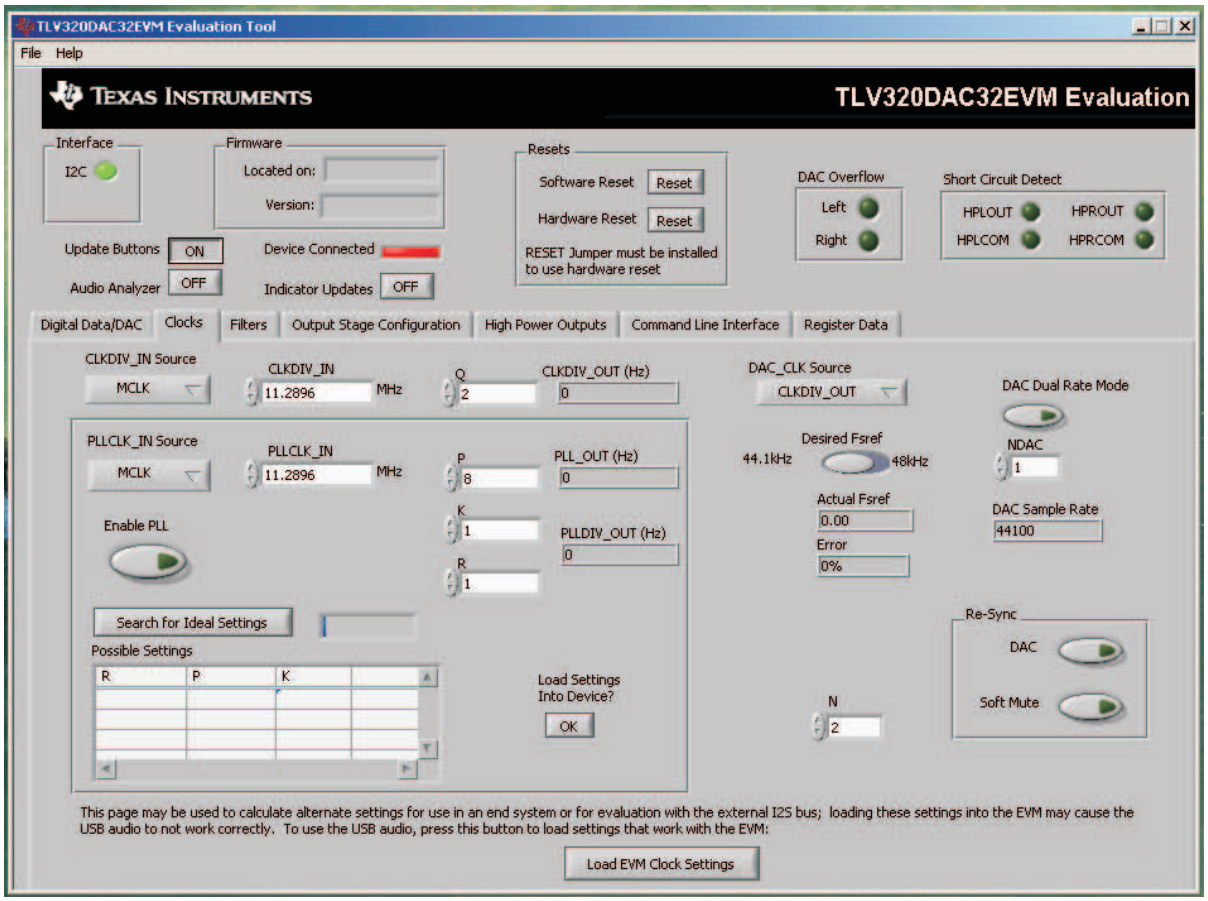


Figure 3. Clocks Tab

The codec clock source is chosen by the **DAC_CLK Source** control. When this control is set to *CLKDIV_OUT*, the PLL is not used; when set to *PLLDIV_OUT*, the PLL is used to generate the clocks.

6.6.1 Use Without PLL

Setting up the TLV320DAC32 for clocking without using the PLL is straightforward. The **CLKDIV_IN** source can be selected as either *MCLK* or *BCLK*, the default is MCLK. The CLKDIV_IN frequency is then entered into the **CLKDIV_IN** box, in megahertz (MHz). The default value shown, 11.2896MHz, is the frequency used on the USB-MODEVM board. This value is then divided by the value of Q, which can be set from 2 to 17; the resulting *CLKDIV_OUT* frequency is shown in the indicator next to the **Q** control.

This frequency will then be used to calculate the actual Fsref frequency, and the DAC sample rate, after the **NADC** factor is applied to the Fsref. If dual rate mode is desired, this option can be enabled for the DAC by pressing the corresponding **Dual Rate Mode** button.

6.6.2 Use With The PLL

When PLLDIV_OUT is selected as the codec clock source, the PLL will be used. The PLL clock source is chosen using the **PLLCLK_IN** control, and may be set to either *MCLK* or *BCLK*. The PLLCLK_IN frequency is then entered into the **PLLCLK_IN Source** box.

The *PLL_OUT* and *PLLDIV_OUT* indicators show the resulting PLL output frequencies with the values set for the P, K, and R parameters of the PLL. See the TLV320DAC32 data sheet for an explanation of these parameters. The parameters can be set by clicking on the up/down arrows of the **P**, **K**, and **R** combo boxes, or they can be typed into these boxes. The values can also be calculated by the PC software.

To use the PC software to find the ideal values of P, K, and R for a given PLL input frequency and desired Fsref, the **Fsref** must be set using the switch on this tab; it can be set to either 44.1kHz or 48kHz. Once the Fsref and PLLCLK_IN values are correctly set, pushing the **Search for Ideal Settings** button starts the software searching for ideal combinations of P, K, and R which achieve the desired Fsref. The possible settings for these parameters are displayed in the spreadsheet-like table labeled *Possible Settings*. Clicking on a row in this table sets the P, K, and R values in the software and updates the PLL_OUT and PLLDIV_OUT readings, as well as the *Actual Fsref* and Error displays. This process does not actually load the values into the TLV320DAC32, however; it only updates the displays in the software. This allows for different possible solutions to be selected and the error evaluated before loading into the device.

When a suitable combination of P,K, and R have been chosen, pressing the **Load Settings into Device?** button will download these values into the appropriate registers on the TLV320DAC32.

Re-sync of the audio bus is enabled using the controls in the lower right corner of this screen. Re-sync is done if the group delay changes by more than ±FS/4 for the ADC or DAC sample rates (see the TLV320DAC32 data sheet). The channels can be soft muted when doing the re-sync if the **Soft Mute** button is enabled.

6.7 Filters Tab

The TLV320DAC32 has a very rich feature set for applying digital filtering to audio signals. This tab (Figure 4) controls all of the filter features of the TLV320DAC32. In order to use this tab and have plotting of filter responses correct, the DAC sample rate must be set correctly. Therefore, the clocks must be set up correctly in the software following the discussion in Section 6.6.

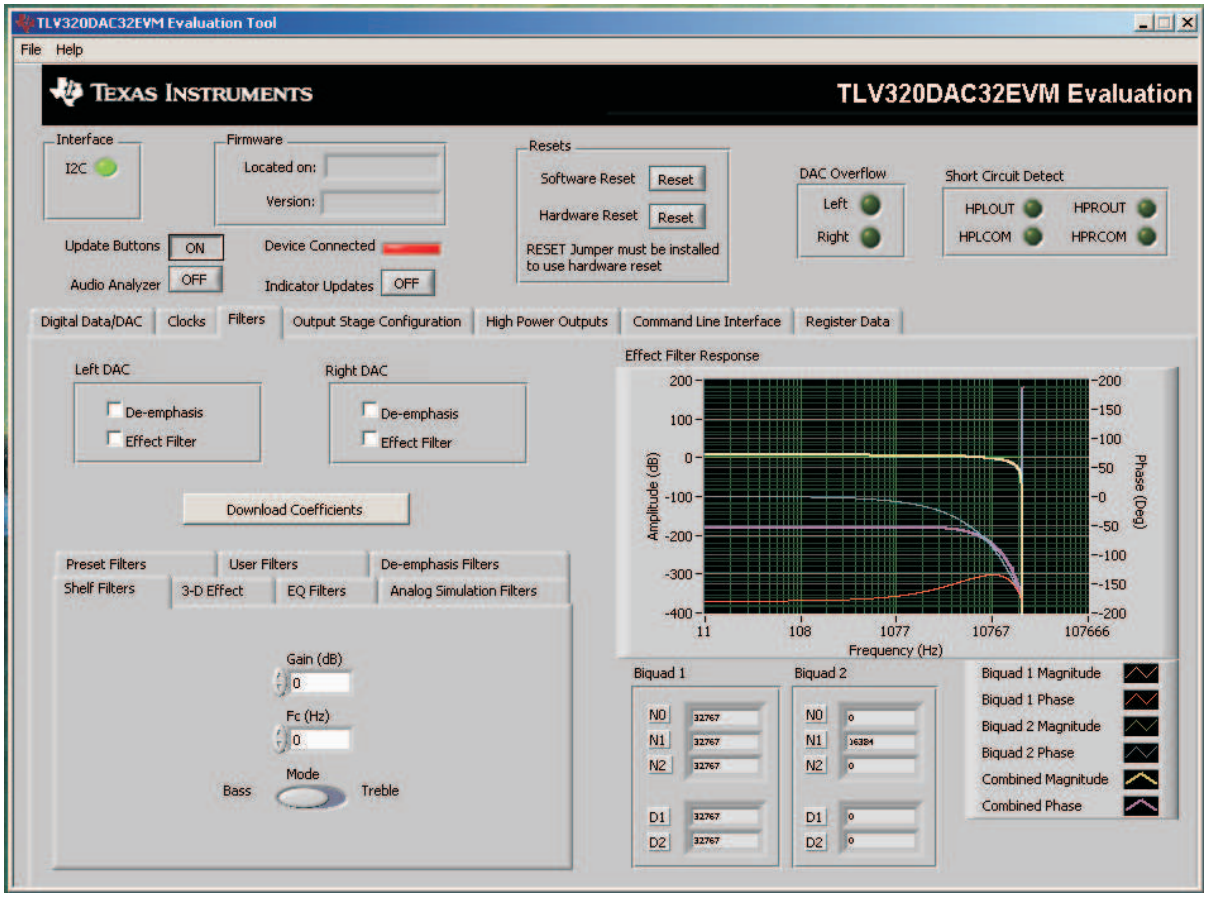


Figure 4. Filters Tab

The right-hand side of this tab shows a display that plots the magnitude and phase response of each biquad section, plus the combined responses of the two biquad sections. The coefficients used for the plotted responses are shown below the graph for both Biquad 1 and Biquad 2. Note that the plot shows only the responses of the effect filters, not the combined response of those filter along with the de-emphasis filters.

6.7.1 Enabling Filters

The de-emphasis and effect filters (the biquad filters) of the TLV320DAC32 are selected using the check boxes shown in Figure 5. The De-emphasis filters are described in the TLV320DAC32 data sheet, and their coefficients may be changed (see Section 6.7.6).



Figure 5. Enabling Filters

When designing filters for use with TLV320DAC32, the software allows for several different filter types to be used. These options are shown on a tab control in the lower left corner of the screen. When a filter type is selected, and suitable input parameters defined, the response will be shown in the *Effect Filter Response* graph. Regardless of the setting for enabling the Effect Filter, the filter coefficients are not loaded into the TLV320DAC32 until the **Download Coefficients** button is pressed. To avoid noise during the update of coefficients, it is recommended that the user uncheck the **Effect Filter enable** check boxes before downloading coefficients. Once the desired coefficients are in the TLV320DAC32, enable the Effect Filters by checking the boxes again.

6.7.2 Shelf Filters

A shelf filter is a simple filter that applies a gain (positive or negative) to frequencies above or below a certain corner frequency. As shown in Figure 6, in *Bass* mode a shelf filter applies a gain to frequencies below the corner frequency; in *Treble* mode the gain is applied to frequencies above the corner frequency.

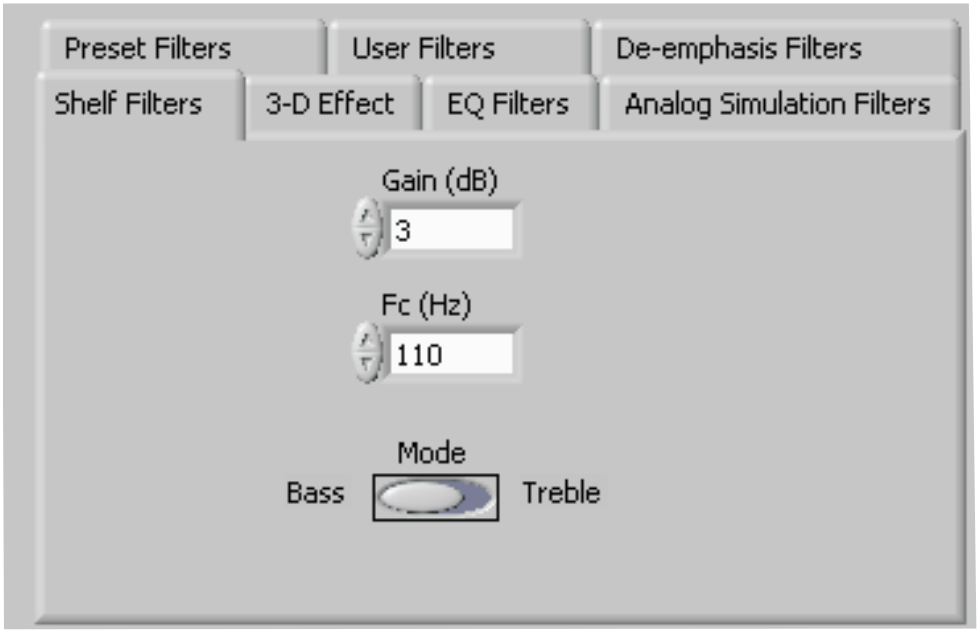


Figure 6. Shelf Filters

To use these filters, enter the gain desired and the corner frequency. Choose the mode to use (*Bass* or *Treble*); the response will be plotted on the *Effect Filter Response* graph.

6.7.3 EQ Filters

EQ, or parametric, filters can be designed on this tab (see Figure 7). Enter a gain, bandwidth, and a center frequency (Fc). Either bandpass (positive gain) or band-reject (negative gain) filters can be created

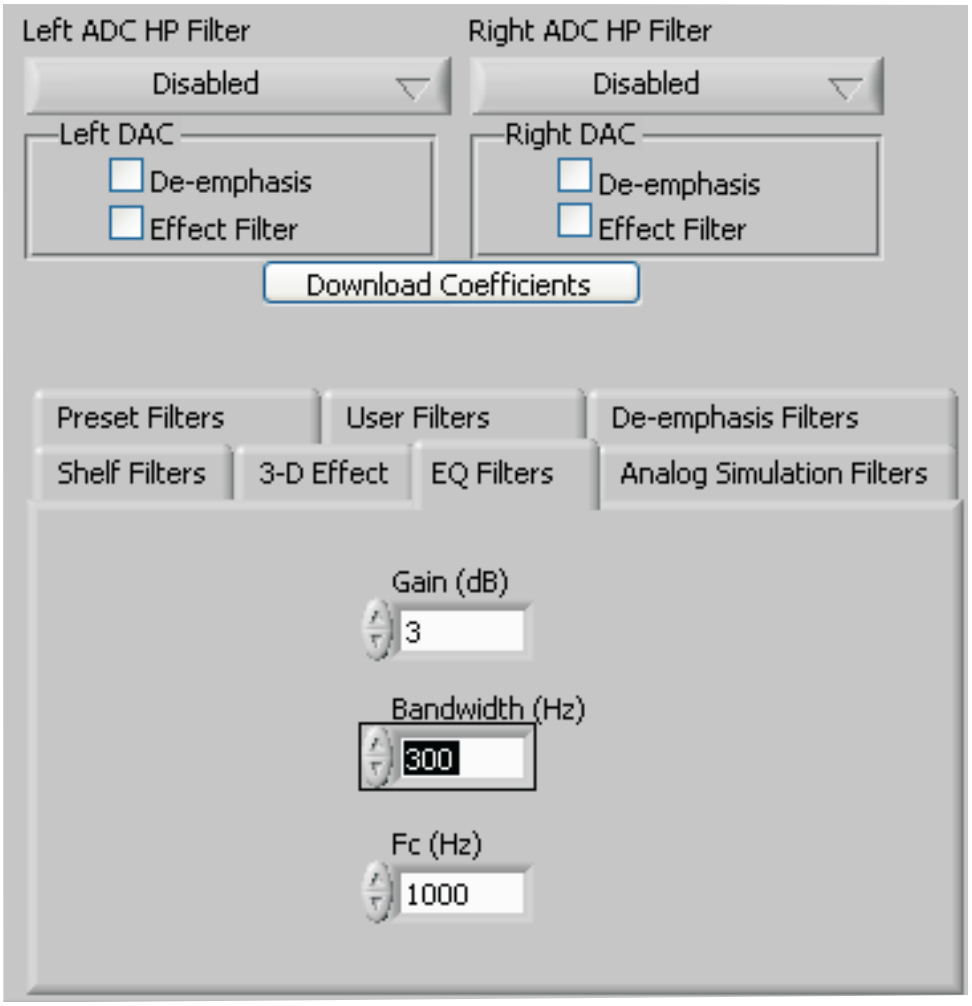


Figure 7. EQ Filters

6.7.4 Analog Simulation Filters

Biquads are quite good at simulating analog filter designs. For each biquad section on this tab, enter the desired analog filter type to simulate (Butterworth, Chebyshev, Inverse Chebyshev, Elliptic or Bessel). Parameter entry boxes appropriate to the filter type will be shown (ripple, for example, with Chebyshev filters, etc.). Enter the desired design parameters and the response will be shown (see Figure 8.)

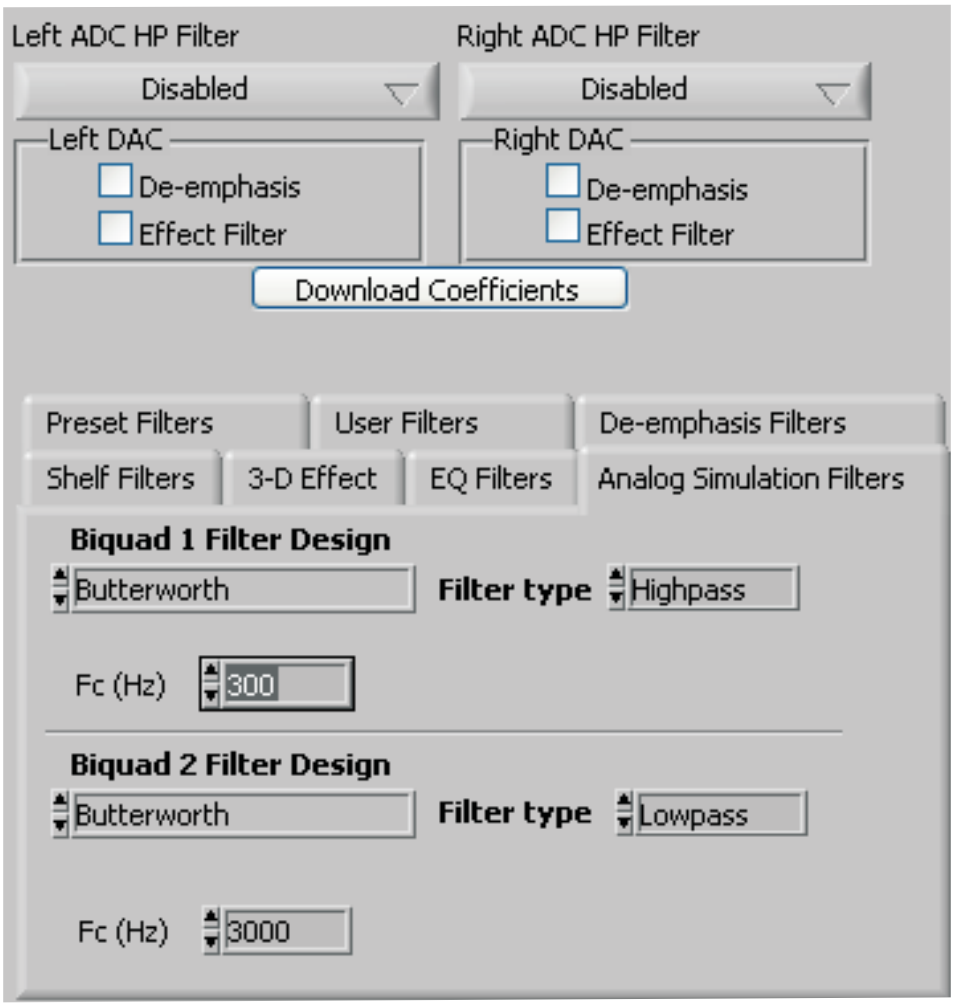


Figure 8. Analog Simulation Filters

6.7.5 Preset Filters

Many applications are designed to provide preset filters common for certain types of program material. This tab (Figure 9) allows selection of one of four preset filter responses - Rock, Jazz, Classical, or Pop.

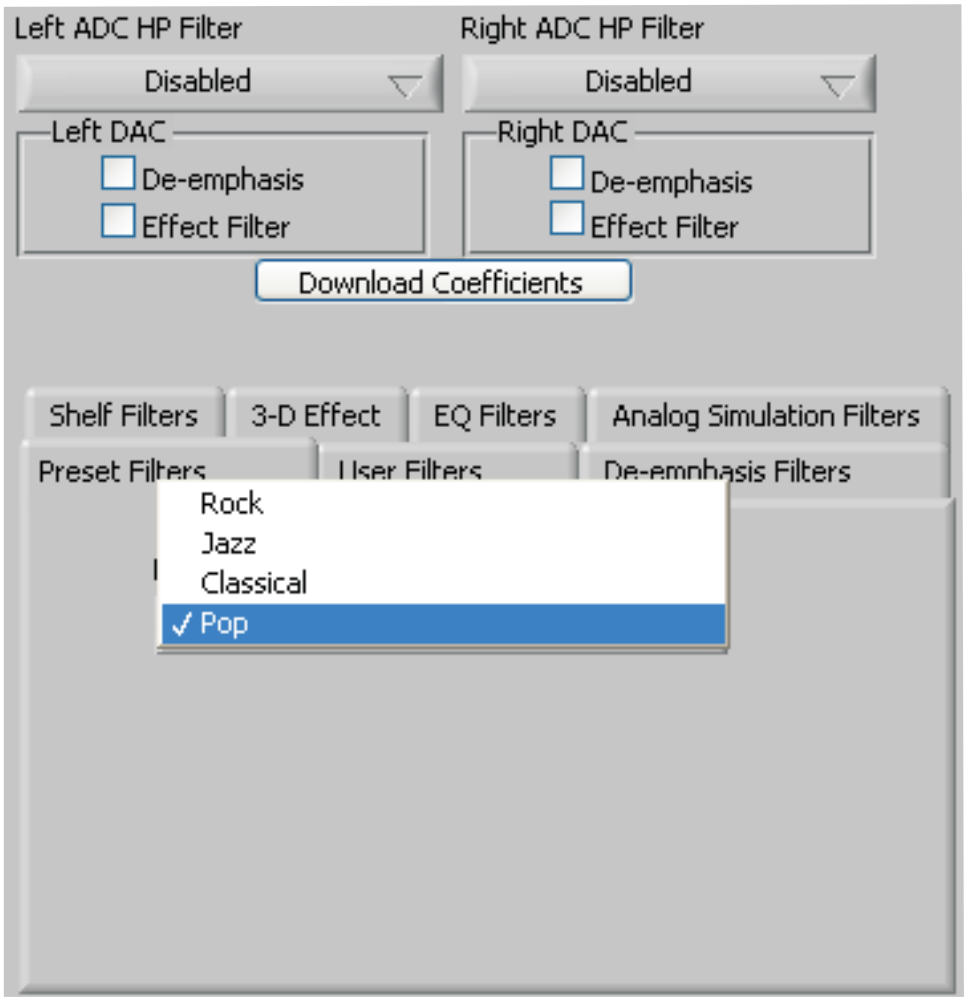


Figure 9. Preset Filters

6.7.6 De-emphasis Filters

The de-emphasis filters used in the TLV320DAC32 can be programmed as described in the TLV320DAC32 data sheet, using this tab (Figure 10). Enter the coefficients for the de-emphasis filter response desired. While on this tab, the de-emphasis response will be shown on the *Effect Filter Response* graph; however, note that this response is not included in graphs of other effect responses when on the other filter design tabs.

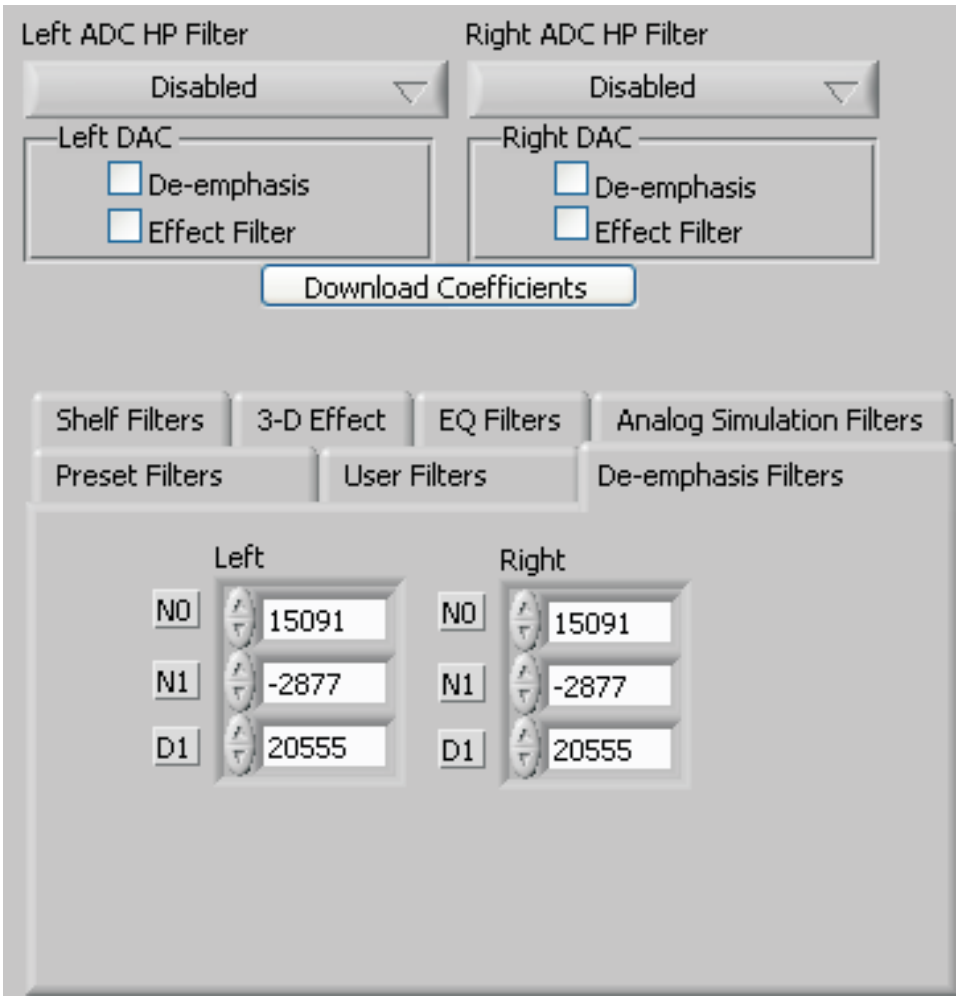


Figure 10. De-emphasis Filters

6.7.7 User Filters

If filter coefficients are known, they can be entered directly on this tab (Figure 11) for both biquads for both left and right channels. The filter response will ***not*** be shown on the *Effect Filter Response* graph for user filters.

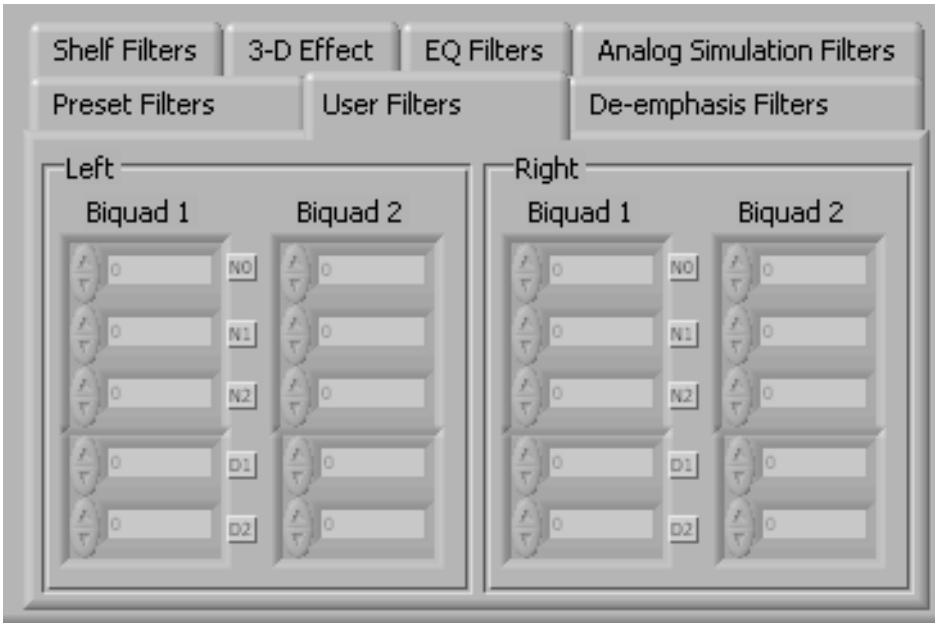


Figure 11. User Filters

6.7.8 3D Effect

The 3D effect is described in the TLV320DAC32 data sheet. It uses the two biquad sections differently than most other effect filter settings. To use this effect properly, make sure the appropriate coefficients are already loaded into the two biquad sections. The User Filters tab may be used to load the coefficients (Figure 12).

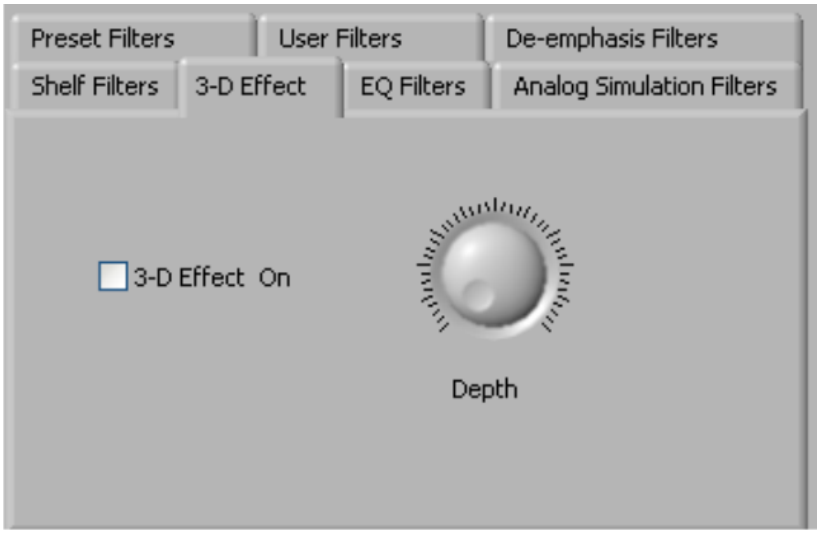


Figure 12. 3D Effect Settings

To enable the 3D effect, check the **3D Effect On** box. The **Depth** knob controls the value of the 3D Attenuation Coefficient.

6.8 Output Stage Configuration Tab

The Output Stage Configuration tab (Figure 13) allows for setting several features of the output drivers. The **Configuration** may be set as either *Fully-Differential* or *Pseudo-Differential*. The output coupling can be chosen as either capless or AC-coupled. This setting should correspond to the setting of the hardware switch (SW1) on the TLV320DAC32EVM.

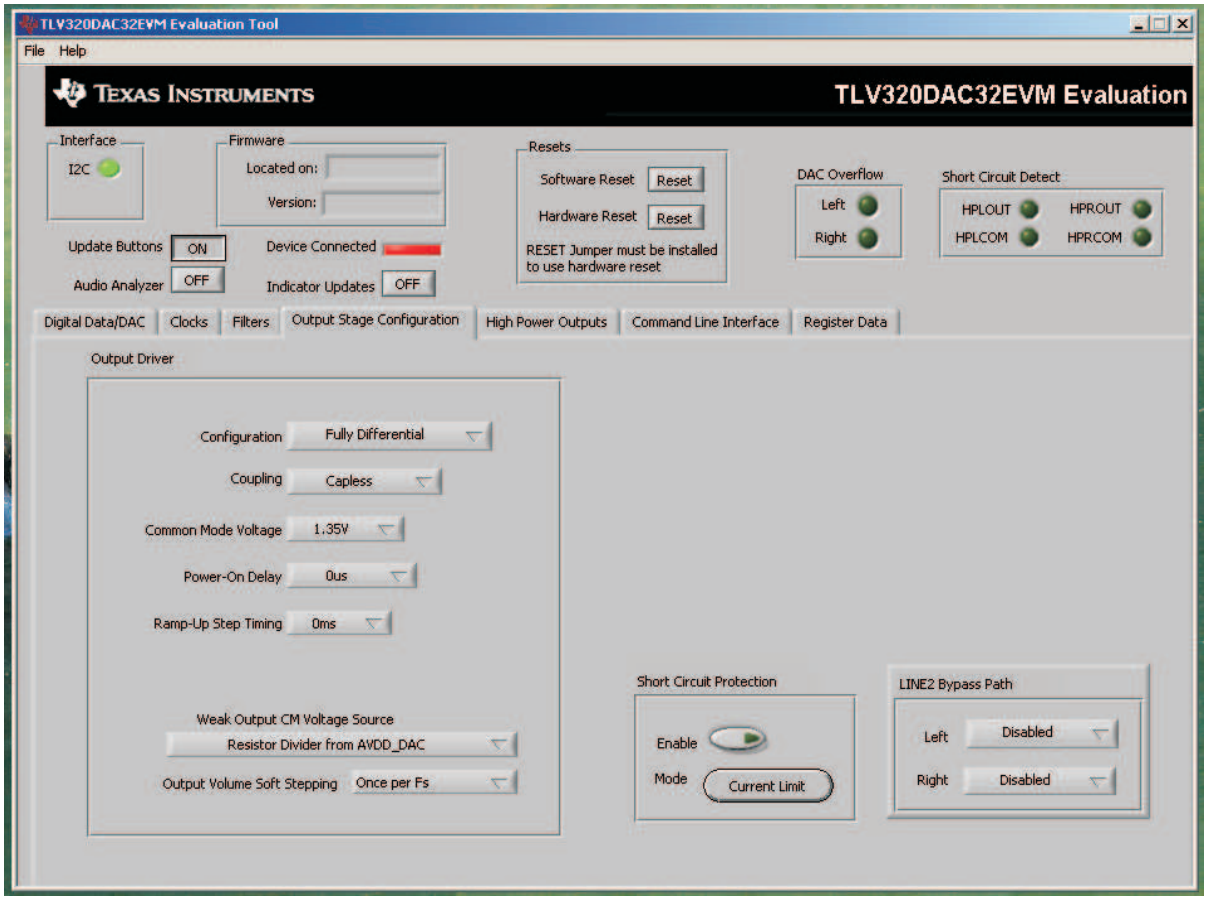


Figure 13. Output Stage Configuration Tab

The Common Mode Voltage of the outputs may be set to 1.35V, 1.5V, 1.65V, or 1.8V using the **Common Mode Voltage** control. The **Power-On Delay** of the output drivers can be set using the corresponding control from 0µs up to 4 seconds. **Ramp-Up Step Timing** can also be adjusted from 0ms to 4ms.

The high power outputs of the TLV320DAC32 can be configured to go to a weak common-mode voltage when powered down. The source of this weak common-mode voltage can be set on this tab with the **Weak Output CM Voltage Source** drop-down. Choices for the source are either a resistor divider off the AVDD_DAC supply, or a bandgap reference. See the data sheet for more details on this option.

The outputs can be set to soft-step their volume changes, using the **Output Volume Soft Stepping** control, and set to step once per Fs period, once per two Fs periods, or soft-stepping can be disabled altogether.

Output short-circuit protection can be enabled in the **Short Circuit Protection** group box. Short Circuit Protection can use a current-limit mode, where the drivers will limit current output if a short-circuit condition is detected, or in a mode where the drivers will power down when such a condition exists.

The LINE2 Bypass Path group box has controls that allow disabling or routing the LINE2 input to the output stage directly.

6.9 High Power Outputs Tab

This tab contains four groupings of controls, one for each of the high power outputs. Each output has a mixer to mix the LINE2L, LINE2R, DAC_L and DAC_R signals, assuming that the DACs are not routed directly to the high power outputs (see Section 6.5.1).

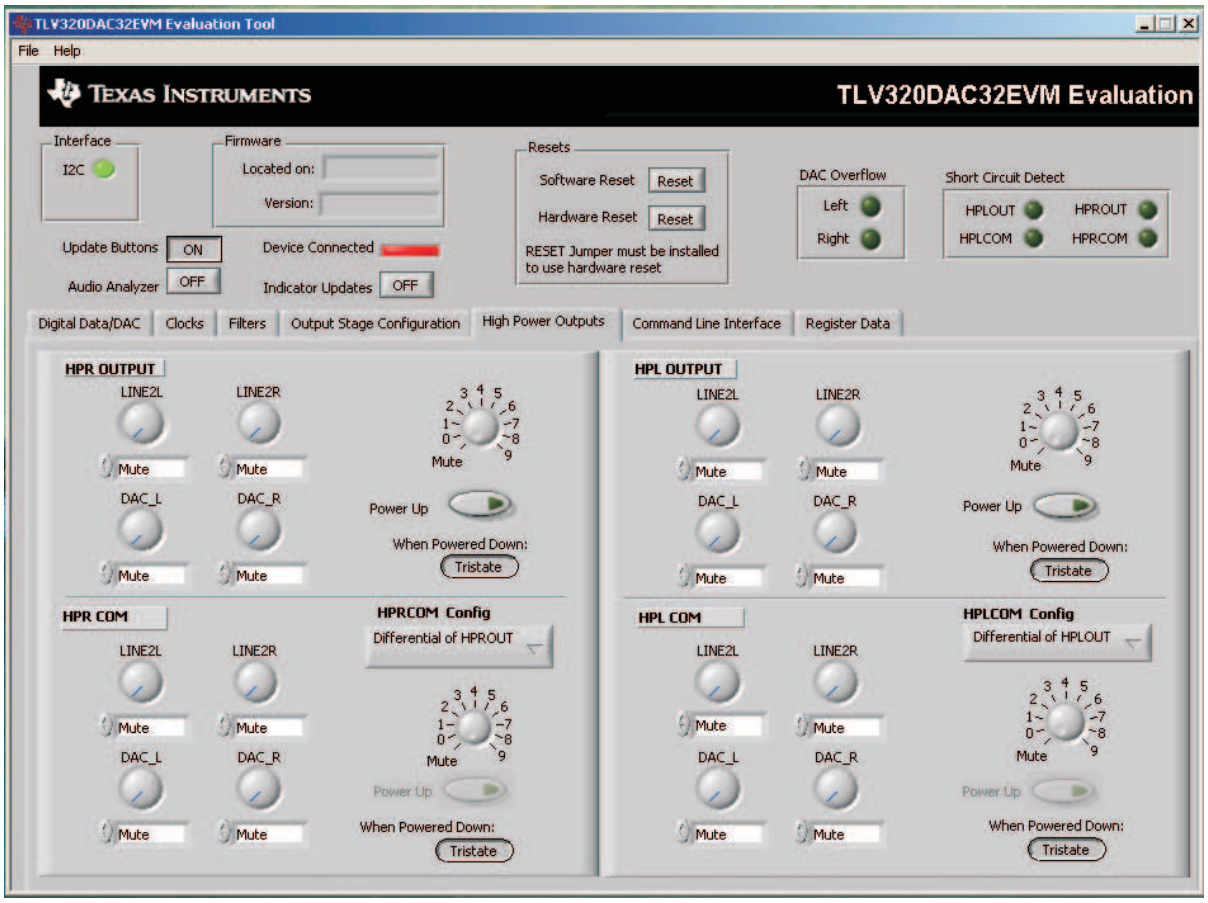


Figure 14. High Power Output

The controls are divided such that the right channel controls are on the left side of the tab and the left channel controls are on the right side of the tab. Each output group contains a power button, 3-state control button, four mixer volume controls and a output amplifier volume control.

At the right side of the output strip is a master volume knob for that output, which allows muting the output or applying gain up to 9dB.

The mixer control volume controls allow for each of four input sources to be independently controlled to allow volume adjustment and summing. Each of these controls allow adjustment of the volume from –78.3dB to 0dB, including mute.

The power button controls whether the corresponding output is powered up or not. When powered down, the outputs can be 3-stated or driven weakly to a the output common mode voltage; this option is selected using the button below the power button.

The **COM** outputs (*HPLCOM* and *HPRCOM*) can be used as independent output channels or can be used as complementary signals to the HPL and HPR outputs. In these complementary configurations, the COM outputs can be selected as differential signals to the corresponding outputs or may be set to be a common mode voltage. When used in these configurations, the power button for the COM output is disabled, as the power mode for that output will track the power status of the HPL or HPR output that the COM output is tracking.

6.9.1 Command Line Interface Tab

A scripting language controls the TAS1020B on the USB-MODEVM from the LabView™-based PC software. The main program controls, described previously, only write a script which is then transferred to an interpreter that sends the appropriate data to the correct USB endpoint. Because this system is script-based, provisions are made in this tab for the user to view the scripting commands created as the controls are manipulated, as well as load and execute other scripts that have been written and saved (see Figure 15). This design allows the software to be used as a test tool, or to provide troubleshooting information in the event that the user encounters a problem with this EVM.

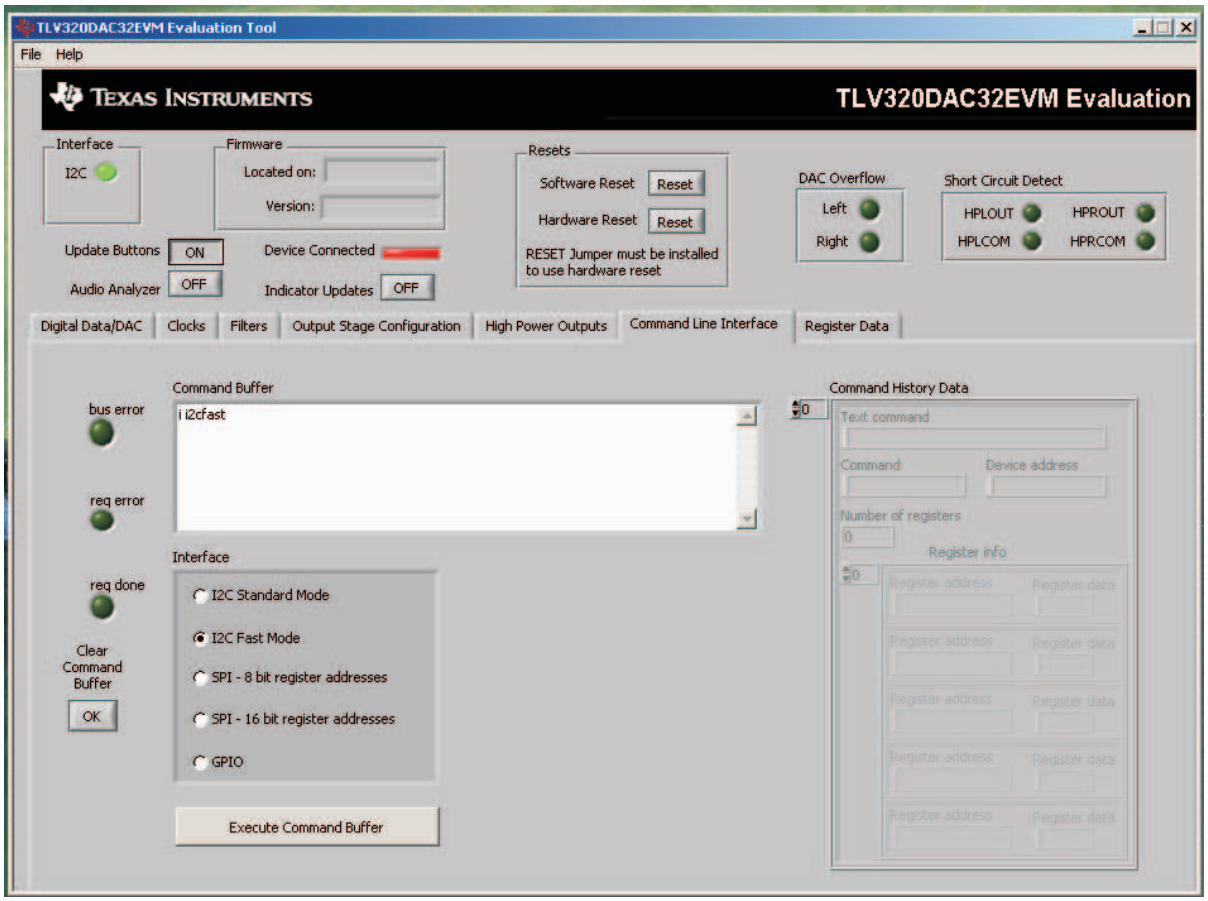


Figure 15. Command Line Interface Tab

A script is loaded into the command buffer, either by operating the controls on the other tabs or by loading a script file. When executed, the return packets of data which result from each command is displayed in the **Command History Data** array control. When executing several commands, the Command History Data control only shows the results of the last command. To see the results after every executed command, use the logging function described below.

The File menu (Figure 16) provides some options for working with scripts. The first option, *Open Command File...*, loads a command file script into the command buffer. This script is then executed by pressing the **Execute Command Buffer** button.

The second option is *Log Script and Results...*, which opens a file save dialog box. Choose a location for a log file to be written using this file save dialog. When the Execute Command Buffer button is pressed, the script runs, and the script, along with resulting data read back during the script, is saved to the file specified. The log file is a standard text file that can be opened with any text editor, and looks much like the source script file, but with the additional information of the result of each script command executed.

The third menu item is a submenu of *Recently Opened Files*. This is a list of script files that have previously been opened, allowing fast access to commonly-used script files. The final menu item is *Exit*, which terminates the TLV320DAC32EVM software.

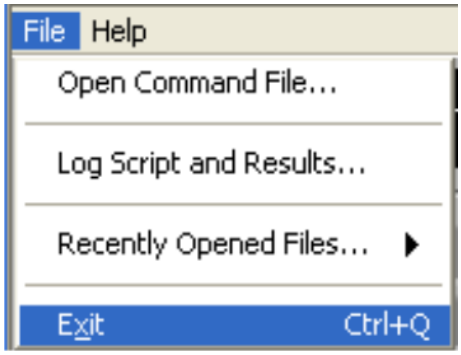


Figure 16. File Menu

Under the Help menu is an *About...* menu item which displays information about the TLV320DAC32EVM software.

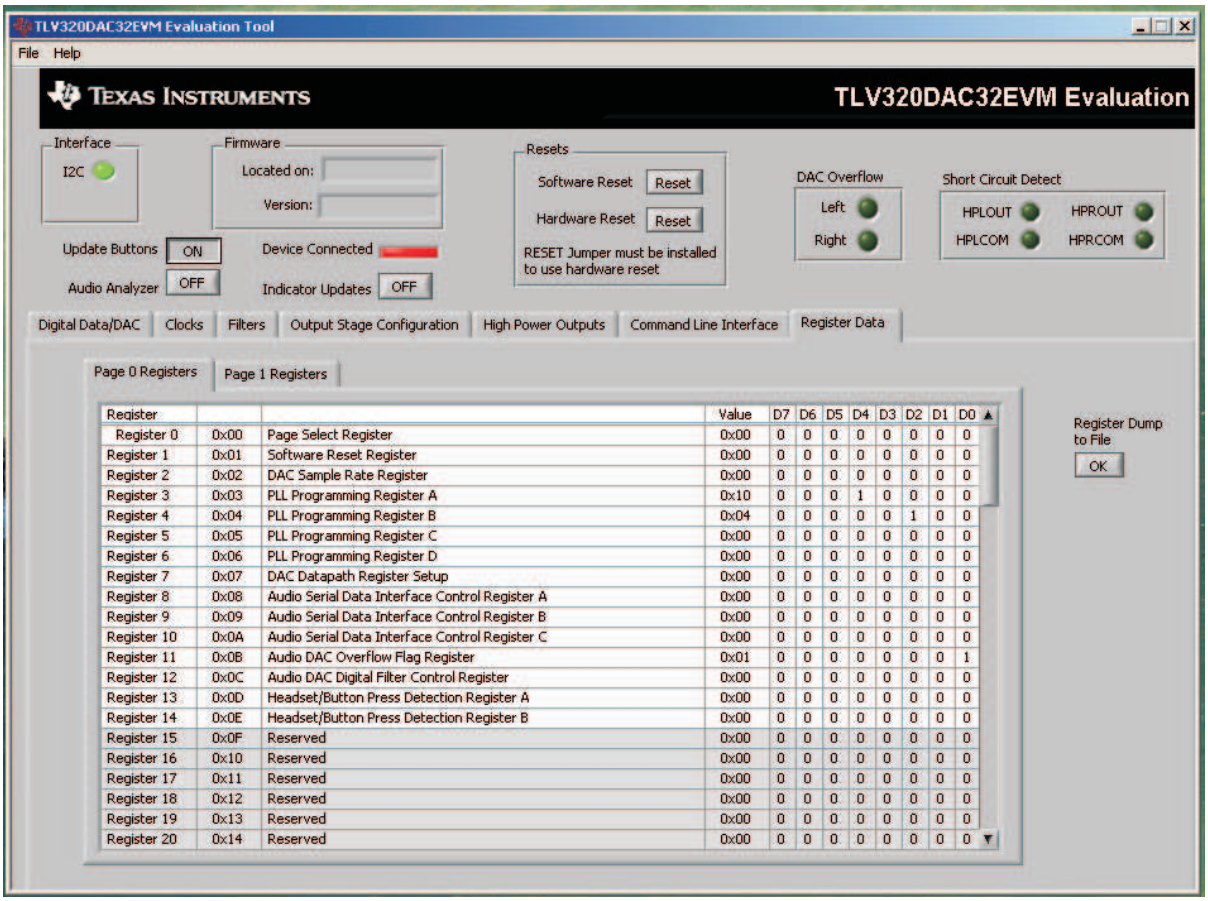
The actual USB protocol used as well as instructions on writing scripts are detailed in Section C.1. While it is not necessary to understand or use either the protocol or the scripts directly, understanding them may be helpful to some users.

6.9.2 Register Data Tab

The Register Data Tab contains two tabs labeled **Page 0 Registers** and **Page 1 Registers**. Each tab contains the current register settings of the codec in table format (see Figure 17).

The first three columns contain the register number and name information. The register number is displayed in decimal format in the first column and hexadecimal format in the second column. The third column contains the name of the register. Reserved registers are highlighted gray and should not be read or written. The remaining columns display the register data in hexadecimal format and in binary format with bit D7 being the MSB.

The **Register Dump to File** button allows both pages of the register information to be saved as Excel files. Each page is saved as a separate file. The user is prompted for the name and location of the files to be saved.



Register			Value	D7	D6	D5	D4	D3	D2	D1	D0
Register 0	0x00	Page Select Register	0x00	0	0	0	0	0	0	0	0
Register 1	0x01	Software Reset Register	0x00	0	0	0	0	0	0	0	0
Register 2	0x02	DAC Sample Rate Register	0x00	0	0	0	0	0	0	0	0
Register 3	0x03	PLL Programming Register A	0x10	0	0	0	1	0	0	0	0
Register 4	0x04	PLL Programming Register B	0x04	0	0	0	0	0	1	0	0
Register 5	0x05	PLL Programming Register C	0x00	0	0	0	0	0	0	0	0
Register 6	0x06	PLL Programming Register D	0x00	0	0	0	0	0	0	0	0
Register 7	0x07	DAC Datapath Register Setup	0x00	0	0	0	0	0	0	0	0
Register 8	0x08	Audio Serial Data Interface Control Register A	0x00	0	0	0	0	0	0	0	0
Register 9	0x09	Audio Serial Data Interface Control Register B	0x00	0	0	0	0	0	0	0	0
Register 10	0x0A	Audio Serial Data Interface Control Register C	0x00	0	0	0	0	0	0	0	0
Register 11	0x0B	Audio DAC Overflow Flag Register	0x01	0	0	0	0	0	0	0	1
Register 12	0x0C	Audio DAC Digital Filter Control Register	0x00	0	0	0	0	0	0	0	0
Register 13	0x0D	Headset/Button Press Detection Register A	0x00	0	0	0	0	0	0	0	0
Register 14	0x0E	Headset/Button Press Detection Register B	0x00	0	0	0	0	0	0	0	0
Register 15	0x0F	Reserved	0x00	0	0	0	0	0	0	0	0
Register 16	0x10	Reserved	0x00	0	0	0	0	0	0	0	0
Register 17	0x11	Reserved	0x00	0	0	0	0	0	0	0	0
Register 18	0x12	Reserved	0x00	0	0	0	0	0	0	0	0
Register 19	0x13	Reserved	0x00	0	0	0	0	0	0	0	0
Register 20	0x14	Reserved	0x00	0	0	0	0	0	0	0	0

Figure 17. Register Data Tab

7 EVM Bill of Materials

Table 7 and Table 8 contain a complete bill of materials for the modular TLV320DAC32EVM and the USB-MODEVM Interface Board (included only in the TLV320DAC32EVM-PDK).

Table 7. TLV320DAC32EVM Bill of Materials

REF DES	Install	Value	Size	Description	MFG	MFG P/N	Digi-Key P/N
C1–C4	√	10µF	1206	6.3V Ceramic Chip Capacitor, ±10%, X5R	TDK	C3216X5R0J106K	
C5, C6	√	0.1µF	0603	16V Ceramic Chip Capacitor, ±10%, X7R	TDK	C1608X7R1C104K	
C9–C12		0.1µF	0603	16V Ceramic Chip Capacitor, ±10%, X7R	TDK	C1608X7R1C104K	
C14	√	10µF	1206	6.3V Ceramic Chip Capacitor, ±10%, X5R	TDK	C3216X5R0J106K	
C15		NI	1210				
C16, C17		NI	1206				
C18, C19	√	0.1µF	1206	100V Ceramic Chip Capacitor, ±10%, X7R	TDK	C3216X7R2A104K	
C20	√	10µF	1206	6.3V Ceramic Chip Capacitor, ±10%, X5R	TDK	C3216X5R0J106K	
C21–C26	√	47µF	1210	6.3V Ceramic Chip Capacitor, ±20%, X5R	TDK	C3225X5R0J476M	
C27–C30	√	47nF	0603	50V Ceramic Chip Capacitor, ±10%, X7R	TDK	C1608X7R1H473K	445-1313-2
C31		0.1µF	0603	16V Ceramic Chip Capacitor, ±10%, X7R	TDK	C1608X7R1C104K	
R1–R3	√	2.7K	0603	1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ272V	P2.7KGCT-ND
R7, R8	√	0	1206	1/4W 5% Chip Resistor	Panasonic	ERJ-8GEY0R00V	P0.0ECT-ND
R9	√	100K	0603	1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ101V	P100GCT-ND
R10–R13	√	100	0603	1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ101V	P100GCT-ND
R14	√	10	0603	1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ100V	P10GCT-ND
R15		0	0603	1/10W 5% Chip Resistor	Panasonic	ERJ-3GEY0R00V	P0.0GCT-ND
SW1	√			4PDT Right Angle Switch	E-Switch	EG4208	EG1914-ND
SW2	√			2PDT Slide Switch	E-Switch	EG4209	EG1907-ND
J1	√		Plug 2X10	20 Pin SMT Plug	Samtec	TSM-110-01-L-DV-P	
			Socket 2X10	20 Pin SMT Socket	Samtec	SSW-110-22-F-D-VS-K	
J3	√		Plug 2X5	10 Pin SMT Plug	Samtec	TSM-105-01-L-DV-P	
			Socket 2X5	10 Pin SMT Socket	Samtec	SSW-105-22-F-D-VS-K	
J4	√		Plug 2X10	20 Pin SMT Plug	Samtec	TSM-110-01-L-DV-P	
			Socket 2X10	20 Pin SMT Socket	Samtec	SSW-110-22-F-D-VS-K	
J5	√		Plug 2X10	20 Pin SMT Plug	Samtec	TSM-110-01-L-DV-P	
			Socket 2X10	20 Pin SMT Socket	Samtec	SSW-110-22-F-D-VS-K	
J6	√			Screw Terminal Block, 3 Position	On Shore	1ED555/3DS	ED1515-ND
J8	√		3,5 mm	3,5 mm Audio Jack, T-R-S, SMD	CUI Inc	SJ1-3515-SMT	CP1-3515SJCT-ND
					KobiConn	161-3335	
J9	√		3,5 mm	3,5 mm Audio Jack, T-R-S, SMD	CUI Inc	SJ1-3515-SMT	CP1-3515SJCT-ND
					KobiConn	161-3515-SMT	CP1-3515SJCT-ND
J12–15	√			Screw Terminal Block, 3 Position	On Shore	1ED555/3DS	ED1515-ND
		Jumper Function					
JMP1	√	AGND/DGND	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP2	√	EEPROM enable	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP5	√	IOVDD select	Header 1X3	3 Postion Jumper, 0.1" spacing	Samtec	TSW-103-07-L-S	
JMP6	√	DVDD	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP7	√	DRVDD	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP8	√	AVDD	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP9	√	RESET	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP11	√	HPLOUT direct	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP12	√	HPLCOM/ HPRCOM	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP13	√	HPLCOM direct	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP14	√	HPROUT direct	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
JMP15	√	HPRCOM direct	Header 1X2	2 Postion Jumper, 0.1" spacing	Samtec	TSW-102-07-L-S	
			Jumper Block	Header Shorting Block	Samtec	SNT-100-BK-T	
		Alternate Label					
TP1	√	AGND		Test Point	Keystone	E5011	5011K-ND
TP2	√	DGND		Test Point	Keystone	E5011	5011K-ND
TP5	√	MICBIAS		Miniature Test point Terminal	Keystone	E5000	5000K-ND

Table 7. TLV320DAC32EVM Bill of Materials (continued)

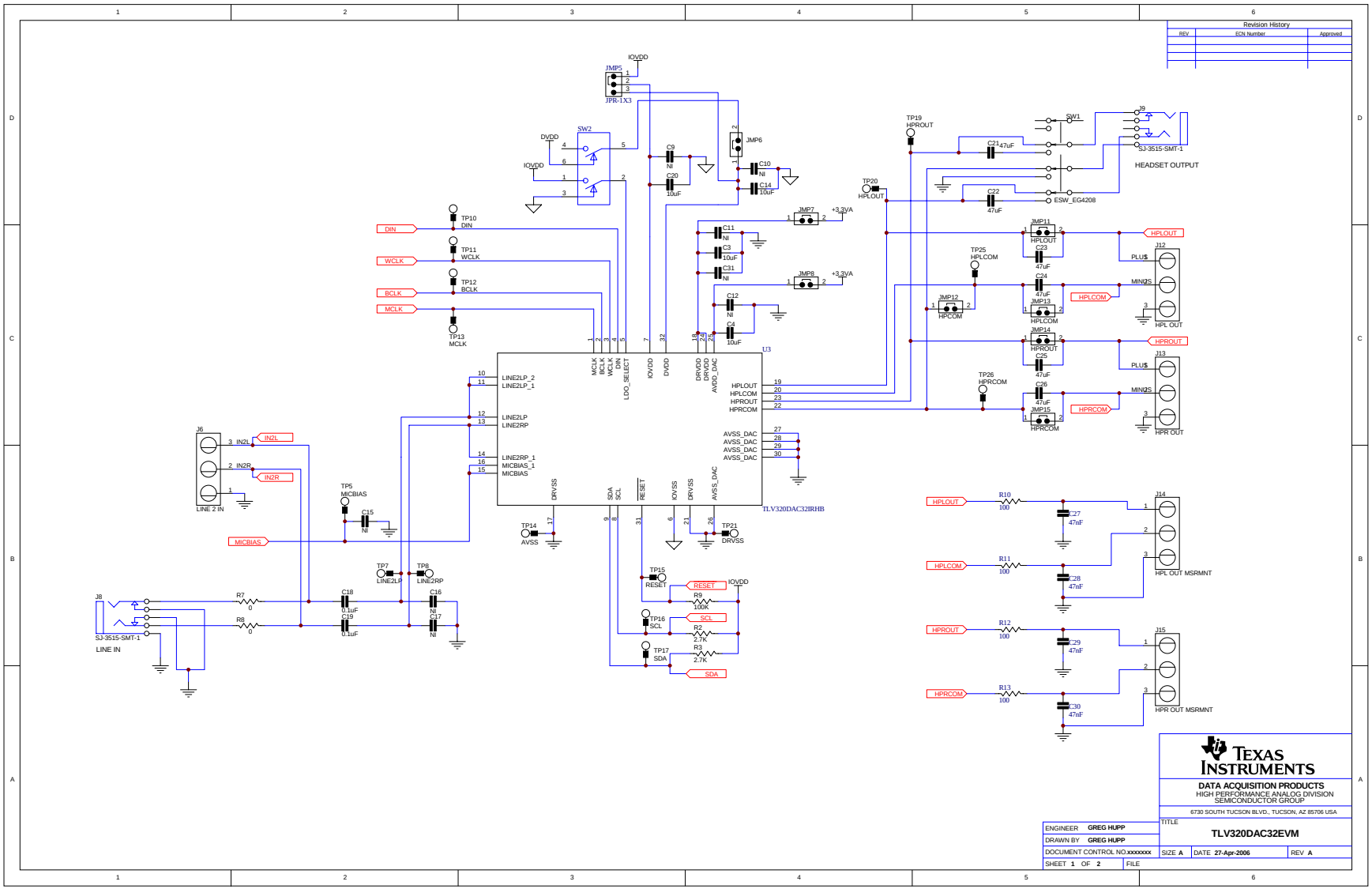
REF DES	Install	Value	Size	Description	MFG	MFG P/N	Digi-Key P/N
TP7	√	LINE2LP		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP8	√	LINE2RP		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP10	√	DIN		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP11	√	WCLK		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP12	√	BCLK		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP13	√	MCLK		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP14	√	AVSS		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP15	√	RESET		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP16	√	SCL		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP17	√	SDA		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP19	√	HPROUT		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP20	√	HPLOUT		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP21	√	DRVSS		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP25	√	HPLCOM		Miniature Test point Terminal	Keystone	E5000	5000K-ND
TP26	√	HPRCOM		Miniature Test point Terminal	Keystone	E5000	5000K-ND
U1	√		SOT-223	3.3V LDO	TI	REG1117-3.3	
U2	√		MCP SN-8	64K I2C EEPROM	Microchip	24LC64I/SN	
U3	√		RGZ-48	Audio DAC	TI	TLV320DAC32IRHB	

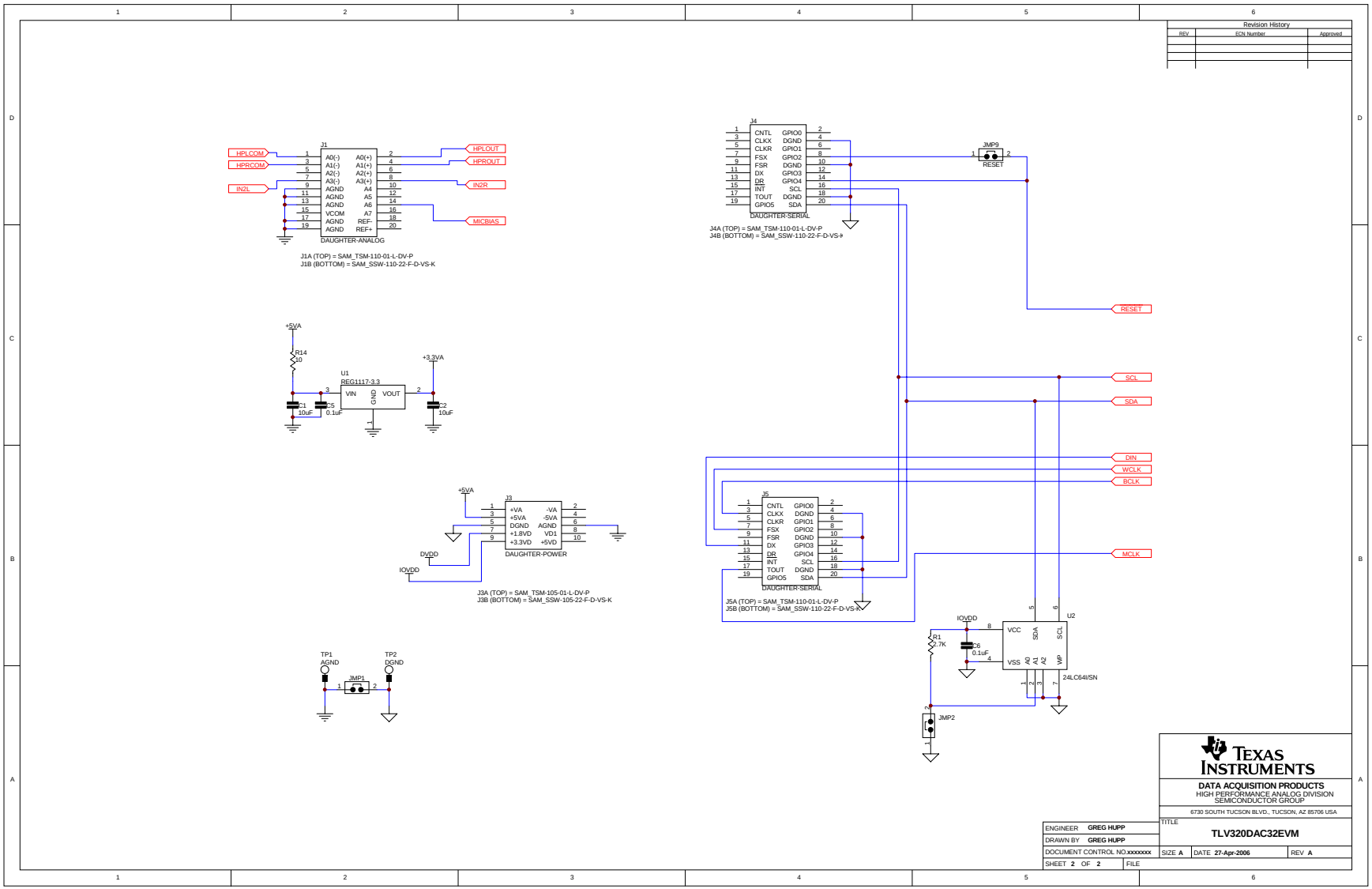
Table 8. USB-MODEVM Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
R4	10Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1300V
R10, R11	27.4Ω 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF27R4V
R20	75Ω 1/4W 1% Chip Resistor	Panasonic	ERJ-14NF75R0U
R19	220Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ221V
R14, R21, R22	390Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ391V
R13	649Ω 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF6490V
R9	1.5kΩ 1/10W 5%, Chip Resistor	Panasonic	ERJ-3GEYJ1352V
R1–R3, R5–R8	2.7kΩ 1/10W 5%, Chip Resistor	Panasonic	ERJ-3GEYJ272V
R12	3.09kΩ 1/16W 1%, Chip Resistor	Panasonic	ERJ-3EKF3091V
R15, R16	10kΩ 1/10W 5%, Chip Resistor	Panasonic	ERJ-3GEYJ1303V
R17, R18	100kΩ 1/10W 5%, Chip Resistor	Panasonic	ERJ-3GEYJ1304V
RA1	10kΩ 1/8W Octal Isolated Resistor Array	CTS Corporation	742C163103JTR
C18, C19	33pF 50V Ceramic, Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H330J
C13, C14	47pF 50V Ceramic, Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H470J
C20	100pF 50V Ceramic, Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H101J
C21	1000pF 50V Ceramic, Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H102J
C15	0.1µF 16V Ceramic, Chip Capacitor, ±10%,X7R	TDK	C1608X7R1C104K
C16, C17	0.33 µF 16V Ceramic, Chip Capacitor, ±20%,Y5V	TDK	C1608X5R1C334K
C9–C12, C22–C28	1µF 6.3V Ceramic, Chip Capacitor, ±10%, X5R	TDK	C1608X5R0J1305K
C1–C8	10 µF 6.3V Ceramic, Chip Capacitor, ±10%, X5R	TDK	C3216X5R0J1306K
D1	50V, 1A, Diode MELF SMD	Micro Commercial Components	DL4001
D2	Yellow Light Emitting Diode	Lumex	SML-LX0603YW-TR
D3–D7	Green Light Emitting Diode	Lumex	SML-LX0603GW-TR
D5	Red Light Emitting Diode	Lumex	SML-LX0603IW-TR
Q1, Q2	N-Channel MOSFET	Zetex	ZXMN6A07F
X1	6MHz Crystal SMD	Epson	MA-505 6.000M-C0
U8	USB Streaming Controller	Texas Instruments	TAS1020BPFB
U2	5V LDO Regulator	Texas Instruments	REG1117-5
U9	3.3V/1.8V Dual Output LDO Regulator	Texas Instruments	TPS767D318PWP
U3, U4	Quad, 3-State Buffers	Texas Instruments	SN74LVC125APW
U5–U7	Single IC Buffer Driver with Open Drain o/p	Texas Instruments	SN74LVC1G07DBVR
U10	Single 3-State Buffer	Texas Instruments	SN74LVC1G125DBVR
U1	64K 2-Wire Serial EEPROM I^2C	Microchip	24LC64I/SN
	USB-MODEVM PCB	Texas Instruments	6463995
TP1–TP6, TP9–TP11	Miniature test point terminal	Keystone Electronics	5000
TP7, TP8	Multipurpose test point terminal	Keystone Electronics	5011
J7	USB Type B Slave Connector Thru-Hole	Mill-Max	897-30-004-90-000000
J13, J2–J5, J8	2-position terminal block	On Shore Technology	ED555/2DS
J9	2.5mm power connector	CUI Stack	PJ-102B
J130	BNC connector, female, PC mount	AMP/Tyco	414305-1
J131A, J132A, J21A, J22A	20-pin SMT plug	Samtec	TSM-110-01-L-DV-P
J131B, J132B, J21B, J22B	20-pin SMT socket	Samtec	SSW-110-22-F-D-VS-K
J133A, J23A	10-pin SMT plug	Samtec	TSM-105-01-L-DV-P
J133B, J23B	10-pin SMT socket	Samtec	SSW-105-22-F-D-VS-K
J6	4-pin double row header (2x2) 0.1"	Samtec	TSW-102-07-L-D
J134, J135	12-pin double row header (2x6) 0.1"	Samtec	TSW-106-07-L-D
JMP1–JMP4, JMP8–JMP14	2-position jumper, 0.1" spacing	Samtec	TSW-102-07-L-S
JMP5, JMP6	3-position jumper, 0.1" spacing	Samtec	TSW-103-07-L-S
JMP7	3-position dual row jumper, 0.1" spacing	Samtec	TSW-103-07-L-D
SW1	SMT, half-pitch 2-position switch	C&K Division, ITT	TDA02H0SK1
SW2	SMT, half-pitch 8-position switch	C&K Division, ITT	TDA08H0SK1
	Jumper plug	Samtec	SNT-100-BK-T

Appendix A TLV320DAC32EVM Schematic

The schematic diagram is provided as a reference.


Revision History
REV.
ECN Number
Approved
IOVDD
JMP5
JPR-1X3
DVDD
SW2
JMP6
C9
NI
C20
10uF
C10
NI
C14
10uF
TP19
HPROUT
SW1
J9
C21 47uF
SJ-3515-SMT-1
HEADSET OUTPUT
TP20
HPLOUT
C22
47uF
ESW_EG4208
DIN
WCLK
BCLK
MCLK
TP10
DIN
TP11
WCLK
TP12
BCLK
TP13
MCLK
JMP7
+3.3VA
C11
NI
C3
10uF
C31
NI
JMP8
+3.3VA
C12
NI
C4
10uF
U3
MCLK
BCLK
WCLK
DIN
LDO_SELECT
IOVDD
DVDD
DRVDD
DRVDD
AVDD_DAC
LINE2LP_2
LINE2LP_1
LINE2LP
LINE2RP
LINE2RP_1
MICBIAS_1
MICBIAS
HPLOUT
HPLCOM
HPROUT
HPRCOM
AVSS_DAC
AVSS_DAC
AVSS_DAC
AVSS_DAC
DRVSS
SDA
SCL
RESET
IOVSS
DRVSS
AVSS_DAC
TLV320DAC32IRHB
TP14
AVSS
TP21
DRVSS
TP25
HPLCOM
JMP11
HPLOUT
C23
47uF
JMP12
HPCOM
C24
47uF
JMP13
HPLCOM
HPLOUT
PLUS
MINUS
J12
HPL OUT
TP26
HPRCOM
JMP14
HPROUT
C25
47uF
C26
47uF
JMP15
HPRCOM
HPROUT
PLUS
MINUS
J13
HPR OUT
J6
IN2L
IN2R
LINE 2 IN
TP5
MICBIAS
C15
NI
MICBIAS
TP7
LINE2LP
TP8
LINE2RP
J8
SJ-3515-SMT-1
LINE IN
R7
0
R8
0
C18
0.1uF
C19
0.1uF
C16
NI
C17
NI
TP15
RESET
RESET
IOVDD
R9
100K
TP16
SCL
SCL
R2
2.7K
TP17
SDA
R3
2.7K
SDA
HPLOUT
R10
100
C27
47nF
HPLCOM
R11
100
C28
47nF
J14
HPL OUT MSRMNT
HPROUT
R12
100
C29
47nF
HPRCOM
R13
100
C30
47nF
J15
HPR OUT MSRMNT
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA
TITLE
TLV320DAC32EVM
ENGINEER GREG HUPP
DRAWN BY: GREG HUPP
DOCUMENT CONTROL NO.xxxxxxx
SIZE A
DATE 27-Apr-2006
REV A
SHEET 1 OF 2
FILE


Revision History
REV
ECN Number
Approved
HPLCOM
HPRCOM
IN2L
HPLOUT
HPROUT
IN2R
MICBIAS
J1
A0(-) A0(+)
A1(-) A1(+)
A2(-) A2(+)
A3(-) A3(+)
AGND A4
AGND A5
AGND A6
VCOM A7
AGND REF-
AGND REF+
DAUGHTER-ANALOG
J1A (TOP) = SAM_TSM-110-01-L-DV-P
J1B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K
J4
CNTL GPIO0
CLKX DGND
CLKR GPIO1
FSX GPIO2
FSR DGND
DX GPIO3
DR GPIO4
INT SCL
TOUT DGND
GPIO5 SDA
DAUGHTER-SERIAL
J4A (TOP) = SAM_TSM-110-01-L-DV-P
J4B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K
JMP9
RESET
RESET
SCL
SDA
DIN
WCLK
BCLK
MCLK
+5VA
R14
10
U1
REG1117-3.3
VIN GND VOUT
+3.3VA
C1
10uF
C5
0.1uF
C2
10uF
J3
+VA -VA
+5VA -5VA
DGND AGND
+1.8VD VD1
+3.3VD +5VD
DAUGHTER-POWER
DVDD
IOVDD
J3A (TOP) = SAM_TSM-105-01-L-DV-P
J3B (BOTTOM) = SAM_SSW-105-22-F-D-VS-K
J5
CNTL GPIO0
CLKX DGND
CLKR GPIO1
FSX GPIO2
FSR DGND
DX GPIO3
DR GPIO4
INT SCL
TOUT DGND
GPIO5 SDA
DAUGHTER-SERIAL
J5A (TOP) = SAM_TSM-110-01-L-DV-P
J5B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K
IOVDD
R1
2.7K
C6
0.1uF
U2
VCC SDA SCL
VSS A0 A1 A2 WP
24LC64I/SN
JMP2
TP1
AGND
TP2
DGND
JMP1
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA
TITLE
TLV320DAC32EVM
ENGINEER GREG HUPP
DRAWN BY: GREG HUPP
DOCUMENT CONTROL NO.xxxxxxx
SIZE A
DATE 27-Apr-2006
REV A
SHEET 2 OF 2
FILE

Appendix B USB-MODEVM Schematic

The schematic diagram is provided as a reference.

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

IOVDD
Q1 ZXMN6A07F
SDA
J6
EXTERNAL I2C
SCL
Q2 ZXMN6A07F
TP10
+3.3VD
TP9
R3 2.7K
R5 2.7K
+3.3VD
U1
VCC SDA SCL
VSS A0 A1 A2 WP
C9 1uF
24LC64I/SN
C18 33pF
X1
MA-505 6.000M-C0
6.00 MHZ
C19 33pF
J7 USB SLAVE CONN
GND D+ D- VCC
897-30-004-90-000000
R9 1.5K
R10 27.4
R11 27.4
C13 47pF
C14 47pF
C20 100pF
C21 .001uF
R12 3.09K
U8
TAS1020BPFB
SCL SDA VREN RESET MCLKO2 MCLKO1 CSCLK CDATO CDATI CSYNC CRESET CSCHNE
XTALO XTALI PLLFILI PLLFILO MCLKI PUR DP DM DVSS DVSS DVSS AVSS
P1.7 P1.6 P1.5 P1.4 P1.3 P1.2 P1.1 P1.0 DVDD DVDD DVDD AVDD
MRESET TEST EXTEN RSTO P3.0 P3.1 P3.2/XINT P3.3 P3.4 P3.5 NC NC
TP11 MRESET
+3.3VD
R13 649
USB ACTIVE
D2 SML-LX0603YW-TR YELLOW
JMP8 P1.3
JMP9 P1.2
JMP10 P1.1
JMP11 P1.0
JMP12 P3.5
JMP13 P3.4
JMP14 P3.3
C24 1uF
C10 1uF
C11 1uF
C12 1uF
+3.3VD
U3
SN74LVC125APW
1A 2A 3A 4A 1OE 2OE 3OE 4OE VCC 1Y 2Y 3Y 4Y GND
USB MCK
USB I2S
C22 1uF
IOVDD
C28 1uF
U10
SN74LVC1G125DBV
J10 EXT MCLK
R20 75
MCLK
I2SDIN
BCLK
LRCLK
I2SDOUT
+3.3VD
RA1 10K
SW2
A0 A1 A2 USB I2S USB MCK USB SPI USB RST EXT MCK
SW DIP-8
+3.3VD
R6 2.7K
U5
SN74LVC1G07DBV
C23 1uF
IOVDD
J14
EXTERNAL AUDIO DATA
PWR_DWN
+3.3VD
R7 2.7K
U7
SN74LVC1G07DBV
C26 1uF
IOVDD
MISO
MOSI
SS
SCLK
RESET
C27 1uF
IOVDD
U4
SN74LVC125APW
1A 2A 3A 4A 1OE 2OE 3OE 4OE VCC 1Y 2Y 3Y 4Y GND
J15
EXTERNAL SPI
USB RST
USB SPI
INT
+3.3VD
R8 2.7K
C25 1uF
IOVDD
U6
SN74LVC1G07DBV
J8
ED555/2DS
EXT PWR IN
6VDC-10VDC IN
JMP6
PWR SELECT
+5VD
R14 390
D3 SML-LX0603GW-TR GREEN
U2
REG1117-5
VIN GND VOUT
D1 DL4001
C15 0.1uF
C16 0.33uF
C6 10uF
J9
CUI-STACK PJ102-B
2.5 MM
SW1
1.8VD ENABLE
3.3VD ENABLE
REGULATOR ENABLE
R15 10K
R16 10K
U9
TPS767D318PWP
1IN 1IN 1EN 1GND 2GND 2EN 2IN 2IN 1RESET 1OUT 1OUT 2RESET 2OUT 2OUT
R17 100K
R18 100K
C7 10uF
C8 10uF
C17 0.33uF
+1.8VD
R4 10
D5 SML-LX0603IW-TR RED
+3.3VD
R19 220
D4 SML-LX0603GW-TR GREEN
+5VD
+3.3VD
+1.8VD
JMP7
IOVDD SELECT
IOVDD
TP6

ENGINEER	**RICK DOWNS**
DRAWN BY	**ROBERT BENJAMIN**
DOCUMENT CONTROL NO.	**6463996**
SHEET	**1** OF **2**

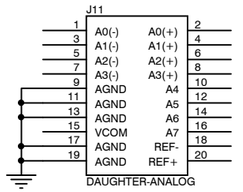
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

TITLE
USB-MODEVM INTERFACE

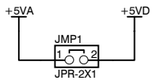
SIZE **B** | DATE **28-Oct-2004** | REV **B**

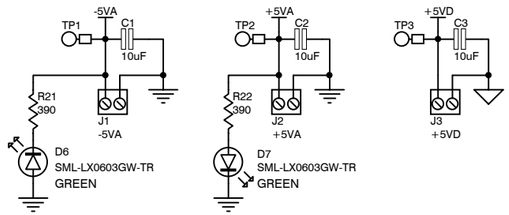
FILE **D:\USB-MODEVM\USB Motherboard - ModEvm.ddb - Documents\USB Interface**

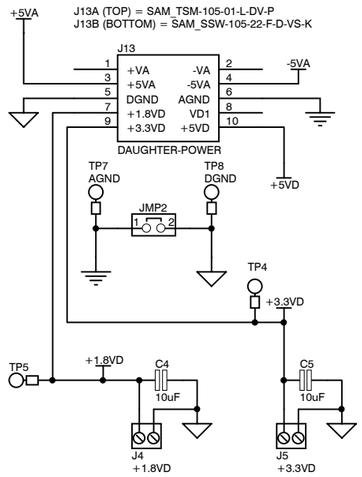
REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED



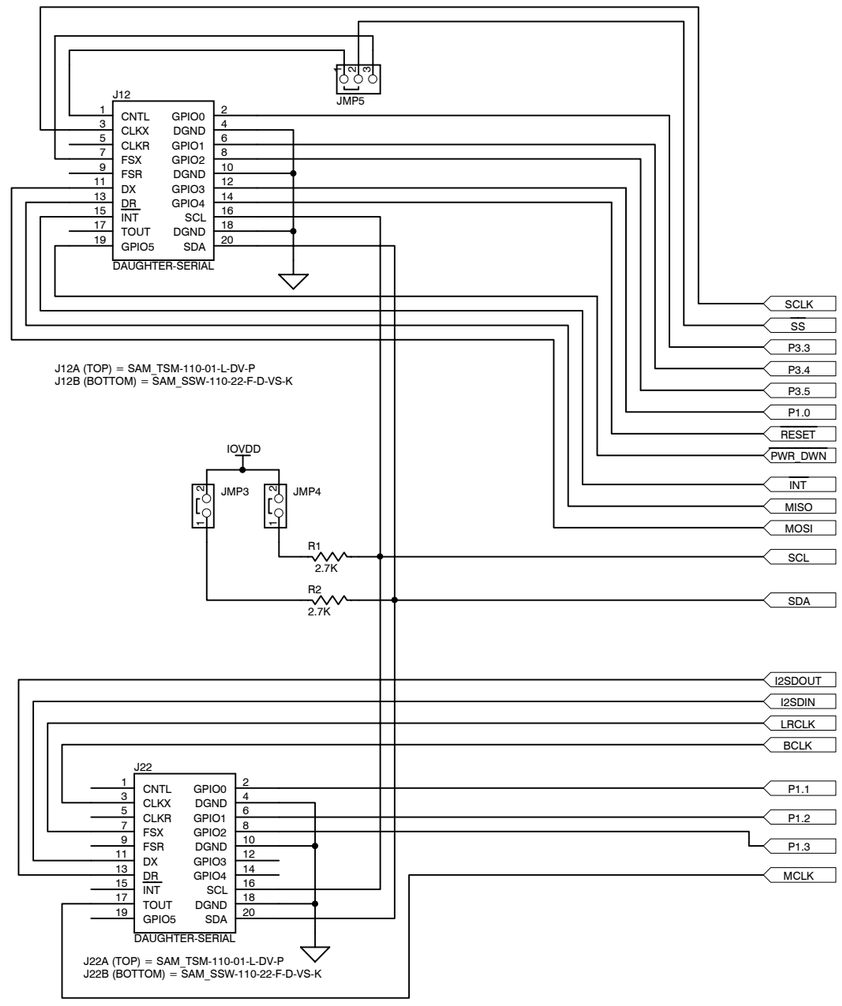
J11A (TOP) = SAM_TSM-110-01-L-DV-P
J11B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K





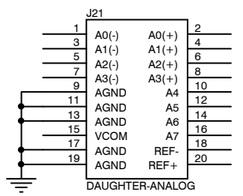


J13A (TOP) = SAM_TSM-105-01-L-DV-P
J13B (BOTTOM) = SAM_SSW-105-22-F-D-VS-K

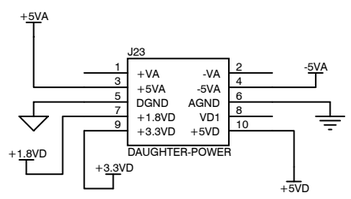


J12A (TOP) = SAM_TSM-110-01-L-DV-P
J12B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K

J22A (TOP) = SAM_TSM-110-01-L-DV-P
J22B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K



J21A (TOP) = SAM_TSM-110-01-L-DV-P
J21B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K



J23A (TOP) = SAM_TSM-105-01-L-DV-P
J23B (BOTTOM) = SAM_SSW-105-22-F-D-VS-K

TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

TITLE **USB-MODEVM INTERFACE**

ENGINEER **RICK DOWNS**			
DRAWN BY **ROBERT BENJAMIN**			
DOCUMENT CONTROL NO. **6463996**	SIZE **B**	DATE **28-Oct-2004**	REV **B**
SHEET **2** OF **2**	FILE **D:\USB-MODEVM\USB Motherboard - ModEvm.ddb - Documents\Daughtercard Interface**		

Appendix C USB-MODEVM Communications Protocol

The communications protocol used by the USB-MODEVM is provided as a reference.

C.1 USB-MODEVM Protocol

The USB-MODEVM is defined to be a Vendor-Specific class, and is identified on the PC system as an NI-VISA device. Because the TAS1020B has several routines in its ROM which are designed for use with HID-class devices, HID-like structures are used, even though the USB-MODEVM is not an HID-class device. Data is passed from the PC to the TAS1020B using the control endpoint.

Data is sent in an HIDSETREPORT (see Table C-1):

Table C-1. USB Control Endpoint HIDSETREPORT Request

Part	Value	Description
bmRequestType	0x21	00100001
bRequest	0x09	SET_REPORT
wValue	0x00	Don't care
wIndex	0x03	HID interface is index 3
wLength	calculated by host	
Data		Data packet as described below

The data packet consists of the following bytes, shown in Table C-2:

Table C-2. Data Packet Configuration

BYTE NUMBER	TYPE	DESCRIPTION
0	Interface	Specifies serial interface and operation. The two values are logically OR'd. Operation: READ 0x00 WRITE 0x10 Interface: GPIO 0x08 SPI_16 0x04 I2C_FAST 0x02 T 0x01 I2C_STD 0x00 SPI_8
1	I^2C Slave Address	Slave address of I^2C device or MSB of 16-bit reg addr for SPI
2	Length	Length of data to write/read (number of bytes)
3	Register address	Address of register for I^2C or 8-bit SPI; LSB of 16-bit address for SPI
4..64	Data	Up to 60 data bytes could be written at a time. EP0 maximum length is 64. The return packet is limited to 42 bytes, so advise only sending 32 bytes at any one time.

Example usage:
Write two bytes (AA, 55) to device starting at register 5 of an I^2C device with address A0:

```
[0]    0x11
[1]    0xA0
[2]    0x02
[3]    0x05
[4]    0xAA
[5]    0x55
```

Do the same with a fast mode I²C device:

```
[0]    0x12
[1]    0xA0
[2]    0x02
[3]    0x05
[4]    0xAA
[5]    0x55
```

Do the same with an SPI device which uses an 8-bit register address:

```
[0]    0x10
[1]    0xA0
[2]    0x02
[3]    0x05
[4]    0xAA
[5]    0x55
```

Do the same with a 16-bit register address, as found on parts like the TSC2101. Assume the register address (command word) is **0x10E0**:

```
[0]    0x14
[1]    0x10→Note: the I²C address now serves as MSB of reg addr.
[2]    0x02
[3]    0xE0
[4]    0xAA
[5]    0x55
```

In each case, the TAS1020B will return, in an HID interrupt packet, the following:

[0] interface byte | status

status:

`REQ_ERROR 0x80`

`INTF_ERROR 0x40`

`REQ_DONE 0x20`

[1] for I²C interfaces, the I²C address as sent

for SPI interfaces, the read back data from SPI line for transmission of the corresponding byte

[2] length as sent

[3] for I²C interfaces, the reg address as sent

for SPI interfaces, the read back data from SPI line for transmission of the corresponding byte

[4..60] echo of data packet sent

If the command is sent with no problem, the returning byte [0] should be the same as the sent one logically OR'd with 0x20 – in our first example above, the returning packet should be:

```
[0]    0x31
[1]    0xA0
[2]    0x02
[3]    0x05
[4]    0xAA
[5]    0x55
```

If the interface fails (for example, the I^2C device does not acknowledge), it would come back as:

```
[0]    0x51→ interface | INTF_ERROR
[1]    0xA0
[2]    0x02
[3]    0x05
[4]    0xAA
[5]    0x55
```

If the request is malformed, that is, the interface byte (byte [0]) takes on a value which is not described above, the return packet would be:

```
[0]    0x93→ you sent 0x13, which is not valid, so 0x93 returned
[1]    0xA0
[2]    0x02
[3]    0x05
[4]    0xAA
[5]    0x55
```

Examples above used writes. Reading is similar:
Read two bytes from device starting at register 5 of an I^2C device with address A0:

```
[0]    0x01
[1]    0xA0
[2]    0x02
[3]    0x05
```

The return packet should be

```
[0]    0x21
[1]    0xA0
[2]    0x02
[3]    0x05
[4]    0xAA
[5]    0x55
```

assuming that the values we wrote above starting at Register 5 were actually written to the device.

C.2 Writing Scripts

A script is a text file that contains data to send to the serial control buses. The scripting language is the parser for the language; therefore, the program is not tolerate mistakes made in the source script file. However, the formatting of the file is simple.

Each line in a script file is one command. There is no provision for extending lines beyond one line. A line is terminated by a carriage return.

The first character of a line is the command. Commands are:

i Set interface bus to use
r Read from the serial control bus
w Write to the serial control bus
Comment
b Break
d Delay

The first command, **i**, sets the interface to use for the commands to follow. This command must be followed by one of the following parameters:

i2cstd	Standard mode I^2C Bus
i2cfast	Fast mode I^2C bus
spi8	SPI bus with 8-bit register addressing
spi16	SPI bus with 16-bit register addressing
gpio	Use the USB-MODEVM GPIO capability

For example, if a fast mode I^2C bus is to be used, the script would begin with:

i i2cfast

No data follows the break command. Anything following a comment command is ignored by the parser, provided that it is on the same line. The delay command allows the user to specify a time, in milliseconds, that the script will pause before proceeding.

Note: UNLIKE ALL OTHER NUMBERS USED IN THE SCRIPT COMMANDS, THE DELAY TIME IS ENTERED IN A DECIMAL FORMAT. Also, note that because of latency in the USB bus as well as the time it takes the processor on the USB-MODEVM to handle requests, the delay time may not be precise.

A series of byte values follows either a read or write command. Each byte value is expressed in hexadecimal, and each byte must be separated by a space. Commands are interpreted and sent to the TAS1020B by the program using the protocol described in Section C.1.

The first byte following a read or write command is the I^2C slave address of the device (if I^2C is used) or the first data byte to write (if SPI is used — note that SPI interfaces are not standardized on protocols, so the meaning of this byte will vary with the device being addressed on the SPI bus). The second byte is the starting register address that data will be written to (again, with I^2C; SPI varies — see Section C.1 for additional information about what variations may be necessary for a particular SPI mode). Following these two bytes are data, if writing; if reading, the third byte value is the number of bytes to read, (expressed in hexadecimal).

For example, to write the values 0xAA 0x55 to an I^2C device with a slave address of 0x90, starting at a register address of 0x03, one would write:

```
#example script
i i2cfast
w 90 03 AA 55
r 90 03 2
```

This script begins with a comment which specifies that a fast I²C bus is used, then writes *0xAA 0x55* to the I²C slave device at address 0x90. The values are written into registers 0x03 and 0x04. The script then reads back two bytes from the same device starting at register address 0x03. Note that the slave device value does not change. It is not necessary to set the R/$\overline{W}$ bit for I²C devices in the script; this is done by the read or write commands.

Here is an example of using an SPI device that requires 16-bit register addresses:

```
# setup TSC2101 for input and output
# uses SPI16 interface
# this script sets up DAC and ADC at full volume, input from onboard mic
#
# Page 2: Audio control registers
w 10 00 00 00 80 00 00 00 45 31 44 FD 40 00 31 C4
w 13 60 11 20 00 00 00 80 7F 00 C5 FE 31 40 7C 00 02 00 C4 00 00 00 23 10 FE 00 FE 00
```

Note that blank lines are allowed. However, be sure that the script does not end with a blank line. While ending with a blank line does not cause the script to fail, the program executes that line, and may prevent the user from seeing data that was written or read back on the previous command.

In this example, the first two bytes of each command are the command word to send to the TSC2101 (0x1000, 0x1360); these are followed by data to write to the device starting at the address specified in the command word. The second line may wrap in the viewer used and appear as more than one line. Careful examination shows that there is only one carriage return on the line, following the last **00**.

Any text editor may be used to write these scripts; Jedit is an editor that is recommended for general usage. For more information, go to: http://www.jedit.org.

Once the script is written, it can be used in the command window by running the program, and then selecting *Open Command File...* from the File menu. Locate and open the script. The script is then displayed in the command buffer. The user may also edit the script once it is in the buffer, but saving of the command buffer is not possible at this time.

Once the script is in the command buffer, it may be executed by pressing the *Execute Command Buffer* button. If breakpoints are placed in the script, the script executes to that point. The user is presented with a dialog box containing a button to press to continue executing the script. When the user is ready to proceed, push the button and the script will continue.

Here an example of a (partial) script with breakpoints:

```
# setup DAC32 for input and output
# uses I2C                          interface
i i2cfast
# reg 07 - codec datapath
w 30 07 8A
r 30 07 1
d 1000
# regs 15/16 - ADC volume, unmute and set to 0dB
w 30 0F 00 00
r 30 0F 2
b
```

This script writes the value 8A at register 7, then reads it back to verify that the write was good. A delay of 1000ms (one second) is placed after the read to pause the script operation. When the script continues, the values **00 00** is written starting at register 0F. This output is verified by reading two bytes, and pausing the script again, this time with a break. The script would not continue until the user allows it to by pressing *OK* in the dialog box that will be displayed due to the break.

C.3 GPIO Capability

The USB-MODEVM has seven GPIO lines. Access the lines by specifying the interface to be 0x08, and then using the standard format for packets—but addresses are unnecessary. The GPIO lines are mapped into one byte (see Table C-3):

Table C-3. GPIO Pin Assignments

7	6	5	4	3	2	1	0
x	P3.5	P3.4	P3.3	P1.3	P1.2	P1.1	P1.0

Example: write P3.5 to a 1, set all others to 0:

```
[0]   0x18→ write, GPIO
[1]   0x00→ this value is ignored
[2]   0x01→ length - ALWAYS a 1
[3]   0x00→ this value is ignored
[4]   0x40→ 01000000
```

The user may also read back from the GPIO to see the state of the pins. If the user just wrote the previous example to the port pins.

Example: read the GPIO

```
[0]   0x08→ read, GPIO
[1]   0x00→ this value is ignored
[2]   0x01→ length - ALWAYS a 1
[3]   0x00→ this value is ignored
```

The return packet should be:

```
[0]   0x28
[1]   0x00
[2]   0x01
[3]   0x00
[4]   0x40
```

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2006, Texas Instruments Incorporated

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.3 V to 5 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2006, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated