TEXAS INSTRUMENTS

TLV320AIC28

Audio Codec Evaluation Module

User's Guide

February 2004

Data Acquisition − Industrial Audio

SLAU127

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Preface

Read This First

About This Manual

This user's guide describes the function and operation of the TLV320AIC28, or simply AIC28, audio codec evaluation module. This manual helps the user quickly set up the evaluation board and its accompanying software, to rapidly test and evaluate the AIC28. A complete circuit description, schematic diagram, and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- ❏ Introduction
- ❏ Getting Started
- ❏ Operation
- ❏ Physical Description

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Data Sheets	Literature Number
TLV320AIC28	SLAS418
TAS1020B	SLES025A
TPS767D301/318	SLVS209D
SN74LVC125A	SCAS290M

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Chapter 1

Introduction

The AIC28 is a low power, high performance audio codec with mono input and stereo output. There are two digital interface buses on the AIC28 that communicate with a host processor: the SPI interface and the I^2S interface. The SPI serial interface is for a host processor to control the AIC28, and the audio data is communicated to the AIC28 over an I^2S bus. The AIC28EVM accesses both of these buses through the use of a USB microcontroller, which provides a way to generate data for both buses from a PC running Windows 98SE, 2000, or XP.

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1.1 Device Characteristics

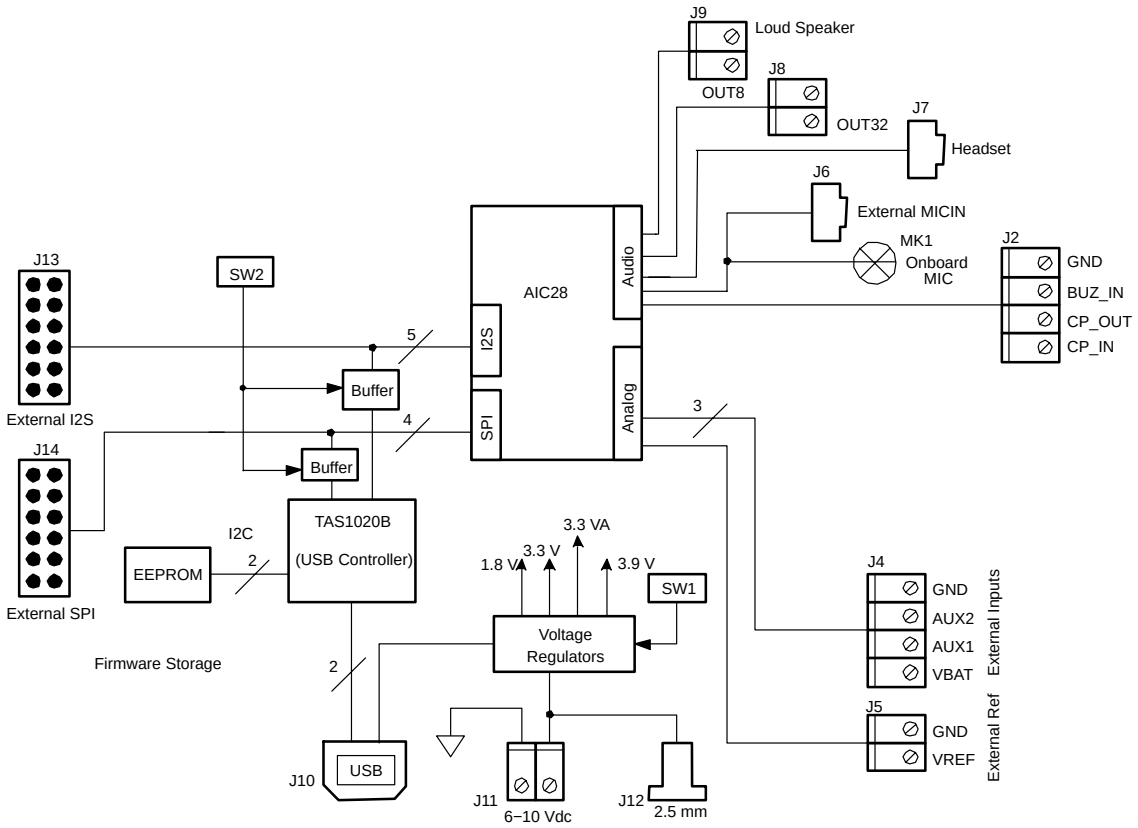
The AIC28 has a high performance audio codec. Access to the audio DAC and ADC sections of the AIC28 is through an I²S interface. For more detail about AIC28 device, refer to the AIC28 data sheet.

The AIC28 interfaces to the host controller through a standard SPI serial interface. The AIC28 offers two auxiliary analog inputs and one battery voltage measurements. The battery measurement is capable of reading battery voltages up to 6 V, while operating with only a 2.7-V supply. It also has an on-chip temperature sensor capable of reading 1°C resolution.

1.2 EVM Block Diagram

A block diagram of the AIC28 evaluation kit is shown in Figure 1−1.

Figure 1−1. AIC28 Evaluation Kit Block Diagram



The digital control interface is through either the USB bus or an external SPI bus, selectable through the SW2. While the SW2 is not at the *USB*-controlled position, the onboard SPI bus from the onboard microprocessor is disabled, allowing the external SPI bus to control the AIC28.

Power supplies are derived from the *USB* bus, or may be provided to the kit through external connectors from an external user-supplied laboratory power supply.

1.3 Analog Inputs/Outputs

There are various audio input/output connectors or plugs that allow the onboard microphone (MK1) or external microphone (J6) signal, and a cell phone input signal or a *BUZZ* input (J2), into the device. The J8 output terminal provides a connector to a 32-Ω speaker; and the J9 output terminal provides a connector to an 8-Ω speaker. Also, a headset can be directly connected into the EVM board through the J7 audio plug.

The other analog inputs are brought onto the board through the J4 terminal block. The AUX inputs must be between 0 V and 3.3 V, whereas the battery input VBAT can range from 0 V to 6 V.

1.4 External Voltage Reference

If the external voltage reference is used, the reference can be input to the AIC28 device through the J5 terminal block.

1.5 Power Requirements

The AIC28EVM can be powered from either the USB port or an external 6-Vdc to 10-Vdc power supply.

1.6 Computer Requirements

The AIC28EVM software is designed for a Windows based platform PC that supports USB (Windows 98SE, 2000, XP, etc).

Minimum requirements include:

- ❏ IBM-compatible Pentium PC or higher
- ❏ Windows 98SE/2000/XP
- ❏ 64-MByte RAM minimum
- ❏ 20-MByte available hard disk space
- ❏ CD-ROM drive
- ❏ USB port

Chapter 2

Getting Started

This chapter guides you through unpacking your EVM and setting it up so you can begin working with it immediately.

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2.1 Unpacking the EVM

When unpacking the AIC28EVM, check the material in the box. The EVM kit includes the following:

- ❑ AIC28EVM board, PWB 6444330
- ❑ CD−ROM, 6458792

If any of these components is missing, contact Texas Instruments for a replacement.

2.2 Default Configuration

The AIC28EVM features a few simple means of configuring its operation. The default settings are shown in Table 2−1. When you unpack your AIC28EVM, ensure that the board is initially configured as listed in Table 2−1.

Table 2−1. Default Configuration Settings

Board Identifier	Description		Default Setting
SW1	Onboard power supply enables:	1.8 V Enable	SW1_1 ON (Enabled)
		3.9 V Enable	SW1_2 ON (Enabled)
		3.3 V Enable	SW1_3 ON (Enabled)
		Spare	SW1_4 OFF
SW2	On/OFF board control selection:	Onboard I2S	SW1_1 ON (Onboard)
		Onboard MCLK	SW1_2 ON (Onboard)
		Onboard SPI	SW1_3 ON (Onboard)
		USB Reset	SW1_4 ON (Enabled)
SW3	Headset cap/cap-less selection:		Cap-Less Output
JMP3	MIC BIAS source from (3.3 V or AIC28)		2 to 3 (AIC28)
JMP4	Differential MIC input selection		Removed (Single-ended)
JMP5	FW Boot source selection		Installed (EEPROM)
JMP6	Power Supply (USB or external) selection		1 to 2 (USB)
JMP7	AIC28 IOVDD (3.3 V or 1.8 V) power selection		1 to 2 (3.3 V)
JMP8	AUX2 resistance measurement		Removed
JMP9	AUX1 resistance measurement		Removed

Notes: 1) For more detail about the onboard configurations, refer to the next chapter.

Notes: 2) JMP1, JMP2, and JMP10 through JMP13 are installed by default. These jumpers can be replaced by current meters for evaluating or testing the corresponding power consumption.

2.3 Quick Start

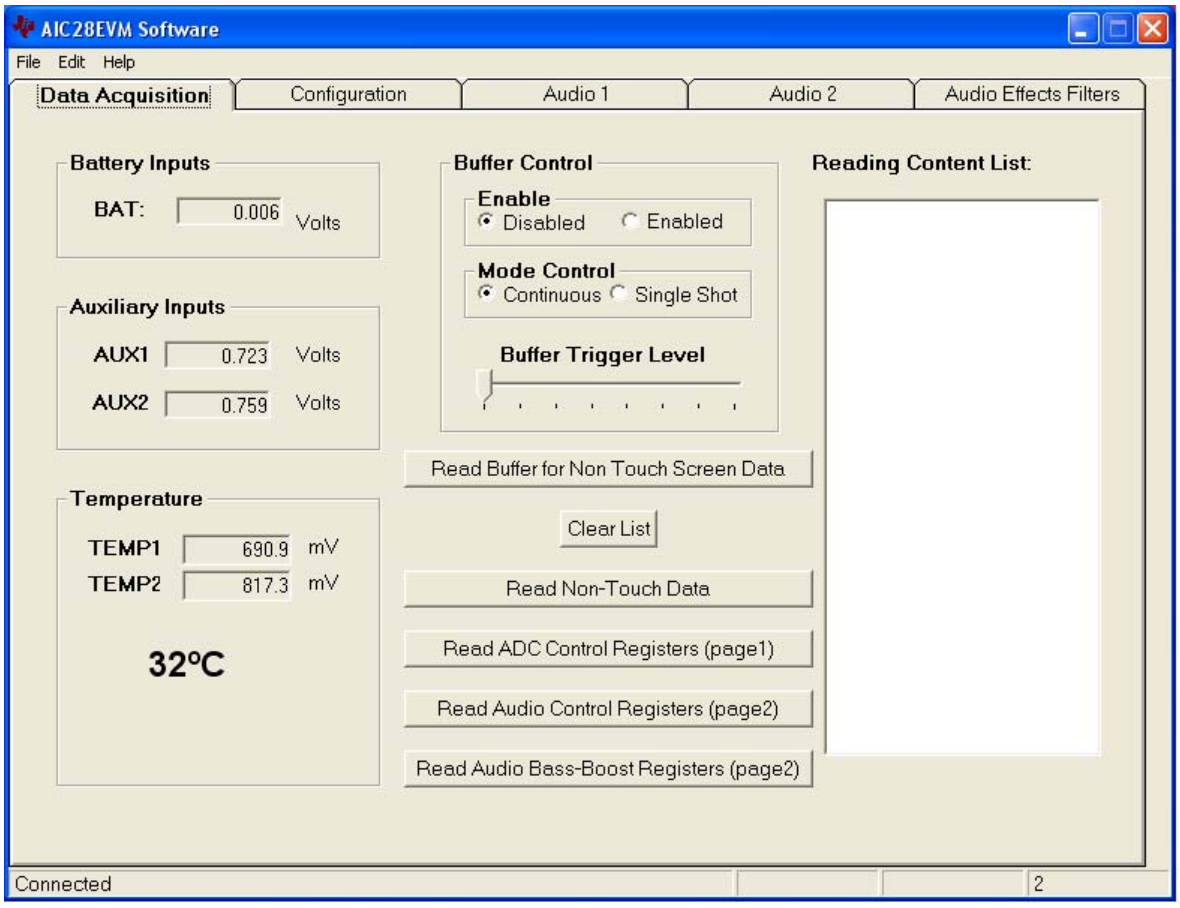
Once the AIC28EVM has been unpacked and you have verified that the board is configured as shown in Table 2−1, install the software.

Place the CD-ROM into the CD-ROM drive of the PC. Locate and run the Setup program on the disk. The Setup program installs the AIC28EVM software on your PC. Note that if you are running Windows 2000 or XP, you need administrator privileges to install the software. Follow the instructions provided by the installer.

When the installation is complete, connect a USB cable from the PC to the AIC28EVM. When the AIC28EVM is connected to the PC the first time, the user may see a message that a Human Interface / Audio Device has been connected. Once this connection has been made, launch the AIC28EVM software on the PC.

The software should automatically find the AIC28EVM. If the board is found, the screen shown in Figure 2−1 appears.

Figure 2−1. Default Software Screen



If a speaker is connected to J9 (the loud speaker connection terminal), a *ding* sound is heard when the USB cable from the PC is plugged into J10 of the EVM. Additional *dings* are heard when launching the software.

The EVM is set to default with the side-tone function enabled. Therefore, when powered up, signals to the onboard mini-microphone (MX1) are heard through the speaker connected to J9.

Chapter 3

Operation

This chapter describes each function of the AIC28 evaluation kit and how to use the accompanying software to control and use the AIC28.

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3.1 Switches

Table 3−1 shows the function of each switch on the EVM.

Table 3−1. Switch Function Reference

Reference Designator		Setting	Function	Factory Default	Subsection
SW1	SW1−1	ON	1.8-V power supply enabled	ON	3.1.1
		OFF	1.8-V power supply disabled		
	SW1−2	ON	3.9-V power supply enabled		
		OFF	3.9-V power supply disabled		
	SW1−3	ON	3.3-V power supply enabled		
		OFF	3.3-V power supply disabled		
SW2	SW2−1	ON	Onboard I2S selected	ON	3.1.3
		OFF	External I2S selected		
	SW2−2	ON	Onboard MCLK selected	ON	3.1.4
		OFF	External MCLK selected		
	SW2−3	ON	Onboard SPI selected	ON	3.1.2
		OFF	External SPI selected		
	SW2−4	ON	USB reset connected to the AIC28	ON	3.1.5
		OFF	USB reset is not connected to the AIC28		
SW3		CAP	Output to headset jack with CAPs	CAPLESS	3.1.6
		CAPLESS	Output to headset jack without CAPs		

3.1.1 Power Supply Selection

SW1 enables or disables the onboard power supplies, including the 1.8 V, the 3.3 VA, and the 3.9 V, so that the power up/down performance of the AIC28 can be evaluated. The 1.8 V provides the 1.8-V digital core power for the AIC28; the 3.3 VA provides the analog power supply for the AIC28; and the 3.9 V gives the analog driver power for the AIC28.

Note that the EVM board has four regulated power supplies. In addition to the 1.8 V, 3.3 VA and 3.9 V supplies, the forth power supply 3.3 V cannot be disabled. This power supply provides the power for the AIC28's digital I/Os, when selected, and the power for the USB control device TAS1020B.

3.1.2 SPI Selection

The SPI bus on the AIC28 provides the main interface between a host processor and the AIC28 device. The onboard TAS1020B plays the role of the host processor, if the SW2−3 is set ON. If an external processor or SPI device is used, set the SW2−3 to the OFF position so as to disable the onboard SPI interface and open the AIC28 SPI port to the external SPI bus.

3.1.3 I²S Selection

The I²S bus on the AIC28 can interface with the onboard host processor, the TAS1020B USB controller, or with other offboard external I²S processor or devices. When the SW2−1 is set to *ON*, the manufacture default, the AIC28 I²S is connected to the TAS1020B's I²S. Otherwise, if the SW2−1 is shifted to *OFF*, the buffer between the onboard I²S ports is disabled so that an external I²S can communicate with the AIC28 I²S port.

3.1.4 MCLK Selection

The AIC28 needs a proper MCLK for the basic audio ADC/DAC functions. The onboard processor, TAS1020B, generates an 11.2896-MHz frequency to provide the MCLK. If an external MCLK is preferred, turn off the SW2−2.

3.1.5 USB Reset

A reset signal output from the onboard TAS1020B processor can be used to reset the AIC28 whenever the TAS1020B is resetting. SW2−4 enables/disables the connection. By default, the connection is enabled. If the processor is not active, the connection to AIC28 should be disabled by turning off the SW2−4.

3.1.6 Cap or Capless Headset Interface

Corresponding to the onchip cap or capless headset interface selection, the EVM has the SW3 built in for use with the different headset interface configurations. For more details, refer to the AIC28 data sheet.

3.2 Jumpers

Table 3−2 shows the function of each jumper on the EVM.

Table 3−2. Jumper Function Reference

Reference Designator	Setting	Function	Factory Default	Subsection
JMP1, JMP2, JMP10, JMP11, JMP12, JMP13	Removed	Power is not provided to the AIC28	Installed	3.2.1
	Installed	Power is provided to the AIC28		
JMP3	1 to 2	MIC BIAS from fixed resistor	2 to 3	3.2.2
	2 to 3	MIC BIAS from AIC28		
JMP4		Differential MIC input selection	Removed	3.2.3
JMP5	Removed	FW boot from external resources	Installed	3.2.4
	Installed	FW boot from EEPROM		
JMP6	1 to 2	EVM board power supply by USB	1 to 2	3.2.5
	2 to 3	EVM board power supply externally		
JMP7	1 to 2	AIC28 uses 3.3 V IOVDD	1 to 2	3.2.6
	2 to 3	AIC28 uses 1.8 V IOVDD		
JMP8	Removed	AUX2 as voltage measurement	Removed	3.2.7
	Installed	AUX2 as resistance measurement		
JMP9	Removed	AUX1 as voltage measurement	Removed	
	Installed	AUX1 as resistance measurement		

3.2.1 Power Supply Current Measurement

Six jumpers are on the front of the six power supply pins of the AIC28. The jumpers can be replaced by current meters that measure and monitor the currents to the corresponding power supply pins. Refer to Table 2−1, Note 2.

3.2.2 MIC BIAS Selection

JMP3 selects the handset microphone bias to come from the AIC28 (MICBIAS_HND pin) or from an external resistor, R14, which is not installed on the AIC28EVM board. If an external bias is needed, the appropriate size resistor can be soldered into the R14 location on the board, and JMP3 is set to connect between positions 1 and 2. If the microphone bias is not required, do not install the jumper top for JMP3 in any position.

3.2.3 MIC Input Selection

The headset microphone input MICIN_HED and the handset microphone input MICIN_HND can be connected to the AIC28 device in single-ended mode.

Differential microphone input is selected using pins MICIN_HED and AUX1/AUX2 as a differential input pair; and/or by using the pins MICIN_HND and AUX1/AUX2 as differential input pair, selected through bits 5 to 7 (D5, D6, D7) in the AIC28 control register page 02 and address 0x03. If a differential microphone input is selected, the JMP4 must be set to provide the AUX1/AUX2 with microphone bias. Table 3−3 gives the JMP4 settings corresponding to the selected differential inputs.

Table 3−3. JUMP4 Settings Reference

Reference Designator	Setting	MICIN Selection
JMP4	All removed	Single-Ended MICINs
	4 to 6	MICIN_HED and AUX1 differential pair
	4 to 2	MICIN_HED and AUX2 differential pair
	3 to 5	MICIN_HND and AUX1 differential pair
	3 to 1	MICIN_HND and AUX2 differential pair

3.2.4 EEPROM A1 Select

The AIC28EVM loads its firmware from an onboard EEPROM. In order to use the firmware in this EEPROM, its A1 address line must be pulled low; therefore, JMP5 should stay installed for normal use.

This jumper can be removed when firmware updates are to be made.

3.2.5 Power Supply Selection

The AIC28EVM can be powered from the USB port directly, or an external power supply can be provided through J11 or J12. JMP6 allows the user to select either the USB or external power sources.

3.2.6 IOVDD Voltage Selection

One of the features of the AIC28 device is that the digital IO power supply for the AIC28 device is flexible, ranging from 1.1 V to 3.6 V. To evaluate the feature, the EVM has the JMP7 for the selection of the IOVDD, either 3.3 V (JMP7 to 1 and 2 position), or 1.8 V (JMP7 to 2 and 3 position).

3.2.7 AUX Input Selection

The auxiliary analog input pins, AUX1 and AUX2, can be used to measure the voltages applied on the pins or the resistance on the pins, selectable in the AIC28 control register page 1 and address 0x0C. Also, under the resistance measurement mode, there are two operation modes, either internal bias or external bias resistance measurement. When AUX1 is used for the external bias resistance measurement, install the JMP9; when AUX2 is used for the external resistance measurement, install the JMP8. Otherwise, leave the jumper(s) uninstalled. Refer to the AIC28 data sheet for more details.

Additionally, the AUX1 or AUX2 can be paired with the MICIN−HED or MICIN−HND to be used as the AIC28 audio codec's differential microphone input port. Refer to section 3.2.3 and the AIC28 data sheet for more details.

3.3 I/O Connector and Signals

The various connectors on the AIC28EVM are described in this section.

3.3.1 Audio Connectors

The AIC28 audio inputs and outputs are routed through the 3,5-mm jacks or terminal blocks. Note the polarity of channel assignments for these connectors.

Table 3−4. Audio Connectors

Reference Designator	Name	Description	
J6	Mic In	Microphone input to handset microphone in (MICIN_HND)	Tip = mic input
			ring = mic bias voltage (or MICIN if differential)
			sleeve = ground
J7	HEADSET	Headset input/output connection	tip1 = headset microphone input
			tip2= headset right output channel
			ring = headset left output channel
			sleeve = audio common ground
J8	OUT32	Receiver driver (32-Ω output) connection	J8+ = OUT32P(SPK1)
			J8− = OUT32M
J9	OUT8	Loud speaker (8-Ω output) connection	J9+ = OUT8P
			J9− = OUT8M

Additionally, the cell-phone input and output signals can be brought to the EVM board through the terminal block J2. The buzz input is also routed to J2.

Table 3−5. Other Audio Inputs

Reference Designator	Description	Pin Number	Signal Name	Function
J2	Other audio inputs	1	CP IN	Cell-phone input
		2	CP OUT	Cell-phone output
		3	BUZZ IN	Buzz signal input
		4	GND	Ground

3.3.2 USB Interface Connector

Connection to a USB cable from a PC is made through J10, a standard USB type-B receptacle.

Table 3−6. USB Interface Connector

Reference Designator	Description	Pin Number	Signal Name	Function
J10	USB slave connection to PC	1	VCC	+5-V supply from USB
		2	D−	−Differential USB signal
		3	D+	+Differential USB signal
		4	GND	Ground

3.3.3 External Power Connectors

Whereas it is most convenient to power the AIC28EVM from the USB bus, external power supplies can be used. The two connectors detailed in Table 3−7 are provided for the external power.

Table 3−7. External Power Connectors

Reference Designator	Description	Pin Number	Signal Name
J11	External power	1	6-Vdc to 10-Vdc input
	Terminal block	2	Ground
J12	External power jack	—	6-Vdc to 10-Vdc input, positive center terminal

3.3.4 Audio Data (I^2S) Connector

The I^2S bus, which carries audio data to and from the AIC28, is connected to header J13. The I^2S signals from the on-board host processor (TAS1020B) can be disabled by turning off the SW2−1. Also refer to the previous section on switch settings.

Table 3−8. Audio Data Connector

Reference Designator	Description	Pin Number	Signal Name
J13	Audio data (I^2S) connector	1	MCLK
		3	BCLK
		5	LRCLK
		7	I2SDIN
		9	I2SDOUT
		11	Power down
		2, 4, 6, 8, 10, 12	Ground

3.3.5 External SPI Connector

The AIC28 SPI port is connected to header J14. It can be driven by an external source if the onboard microprocessor is disabled by turning off the SW2−3 and removing the A1 select jumper (JMP5). Also refer to the previous sections on switch and jumper settings.

Table 3−9. External SPI Connector

Reference Designator	Description	Pin Number	Signal Name	Function
J14	External SPI bus	1	RGSET	Reset line
		3	SS	Slave select for SPI bus
		5	SCLK	Serial clock for SPI bus
		7	MOSI	Master out, slave in data line
		9	MISO	Master in, slave out data line
		11	PENIRQ	Pen down or $\overline{\text{DAV}}$ interrupt line
		2, 4, 6, 8, 10, 12	GND	Ground

3.3.6 Analog Input Connector

The auxiliary and battery inputs to the AIC28 are brought onto the EVM board through terminal block J4. The pinout is shown in Table 3−10.

Table 3−10. Analog Input Connector

Reference Designator	Description	Pin Number	Signal Name	Function
J4	Battery and auxiliary inputs to the touch screen control	1	VBAT	Battery input, 0 V to 6 V
		2	AUX1	Auxiliary input 1, 0 V to VREF
		3	AUX2	Auxiliary input 2, 0 V to VREF
		4	GND	Ground

3.4 Circuit Description

The AIC28 evaluation kit circuitry consists of a USB microprocessor, power supply circuitry, analog input interfaces, and audio interface circuitry (both analog and digital). These circuits are described in the following sections.

3.4.1 USB Microprocessor

The AIC28EVM has a USB interface for connecting to a PC. This connection is made through a TAS1020B streaming audio processor, U10. The SPI interface to the AIC28 can be controlled from two sources: the external SPI header, J14, or through the onboard microprocessor (U10) via USB. The U10 outputs are enabled only when the supplied firmware is loaded, and the corresponding bus(es) is enabled, refer to switch description for SW2 in section 3.1.

The firmware resides in the serial EEPROM chip, U2. U10 only loads firmware from U2 when the U2 A1 address line is pulled low. To disable firmware loading, A1 must be high, by having JM5 removed. Refer to section 3.2.4.

When the firmware is loaded and active, D2 (a yellow LED) is lit. If no firmware is loaded, the U10 output should be in 3-state. In order to ensure that the onboard host processor does NOT effect the interface between the external SPI bus to drive the AIC28, turn OFF the SW2−3.

When the SW2−3 is ON and the firmware is loaded, the PC software enables the onboard microprocessor to control the SPI bus.

Caution

Do not drive the external SPI bus when the firmware is loaded and the onboard microprocessor is active. If you want to use the external SPI bus, disable the microprocessor by removing JMP5, turning OFF the SW2−3 to isolate the microprocessor SPI bus, and cycling power to the AIC28EVM.

Likewise, the I^2S signals for the digital audio can be driven either externally by J13 or by the USB audio controller.

Caution
Do not drive the external I²S bus when the firmware is loaded and the onboard microprocessor is active. If you want to use the external I²S bus, disable the microprocessor by removing JMP5, turning OFF the SW2−1 to isolate the microprocessor I²S bus, and cycling power to the AIC28EVM.

3.4.2 Power Supply

Power to the AIC28EVM can be derived directly from the USB interface or externally supplied through the J11 terminal block or the J12 barrel jack connector. Supply voltages of 6 Vdc to 10 Vdc must be supplied from an external supply. Because it is regulated on the AIC28EVM, this input voltage does not need to be regulated as long as it falls within this range. D1 prevents damage to the board in the event a power supply is connected in reverse polarity.

Two linear regulators are on the board. U3 regulates the digital power-supply voltage to provide 1.8 V for the AIC28 digital core, or the digital IO power supply if the IOVDD is selected as 1.8 V by JMP7. Also, U3 provides the 3.3-V digital power for all of other digital circuits. U4 regulates the analog power supplies. Its 3.9-V power supply is used for the AIC28 analog driver power DRVDD2; its 3.3 VA powers the rest of the analog circuits on the board.

The regulated supply voltages have LEDs attached that alert the user that the supply is working. D2 (red) is the indicator for the 1.8-V power supply; D4 (green) is the indicator for the 3.3-V power supply; D5 (green) is the indicator for the 3.9-V driver power; and D6 (green) is the indicator for the 3.3-VA analog power supply.

3.4.3 Analog Inputs

Terminal block J4 provides input connection points for the battery and auxiliary inputs. Battery input can range from 0 V to 6 V, and the auxiliary inputs can range from 0 V to V_{REF}.

Each of these three inputs has a provision for an RC filter to be placed in line with the signal. As shipped, all resistors are 0 V, and the capacitors are not installed. If noisy conditions prevent obtaining good readings from the AIC28, 0.1-µF capacitors can be installed in positions C1, C6, and C7. If more filtering is required, the 0-V resistors should be unsoldered from the board and replaced with small resistors.

3.4.4 Audio Interface Circuitry

A mono Electret microphone can be connected to J6. This jack provides both audio and bias connections. Bias for the microphone can be supplied either from the AIC28 mic bias circuitry or from an external resistor, R14. R14 is not installed on the AIC28EVM, but can be installed by the user. Internal or external bias is selected by JMP3.

A small onboard microphone is also on the EVM, parallel to the J6. Without an external electrical microphone, voice can be input to the AIC28 through this microphone.

The AIC28 has a built-in headset interface. J7 is the jack for connection to the headset where the microphone input is mono and the audio output can be stereo. The signal to the headset can be dc-decoupled through the capacitors (C21 and C22) or *capless*. Note that the switch SW3 must be used according to the software settings to work either at the *CAP* mode or the *CAPLESS* mode. Refer to the related description in the data sheet.

The audio output can also be connected to a 32-Ω speaker through J8, and the 8-Ω loud speaker through J9.

Additionally, the cell-phone input/output, and the buzz input, can be connected to the AIC28 device through the onboard terminal block J2.

3.5 Program Description

After installing the software for the AIC28EVM as described in section 2.3, the user can begin to evaluate and develop with the AIC28.

The program's interface is a simple, five-tab interface. Clicking on a tab takes you to the functions associated with that tab. The program begins on the Data Acquisition screen (the default) as shown in Figure 2−1.

The status bar at the bottom of the screen is divided into four sections and shows the status of communication between the PC and the EVM. Starting from the left, the first section shows the status of the connection. If an error in communication occurs, an error message appears here; otherwise, it looks as shown in Figure 2−1. The final section, on the right side of the status bar, shows the number of readings per second.

3.5.1 Data Acquisition Screen

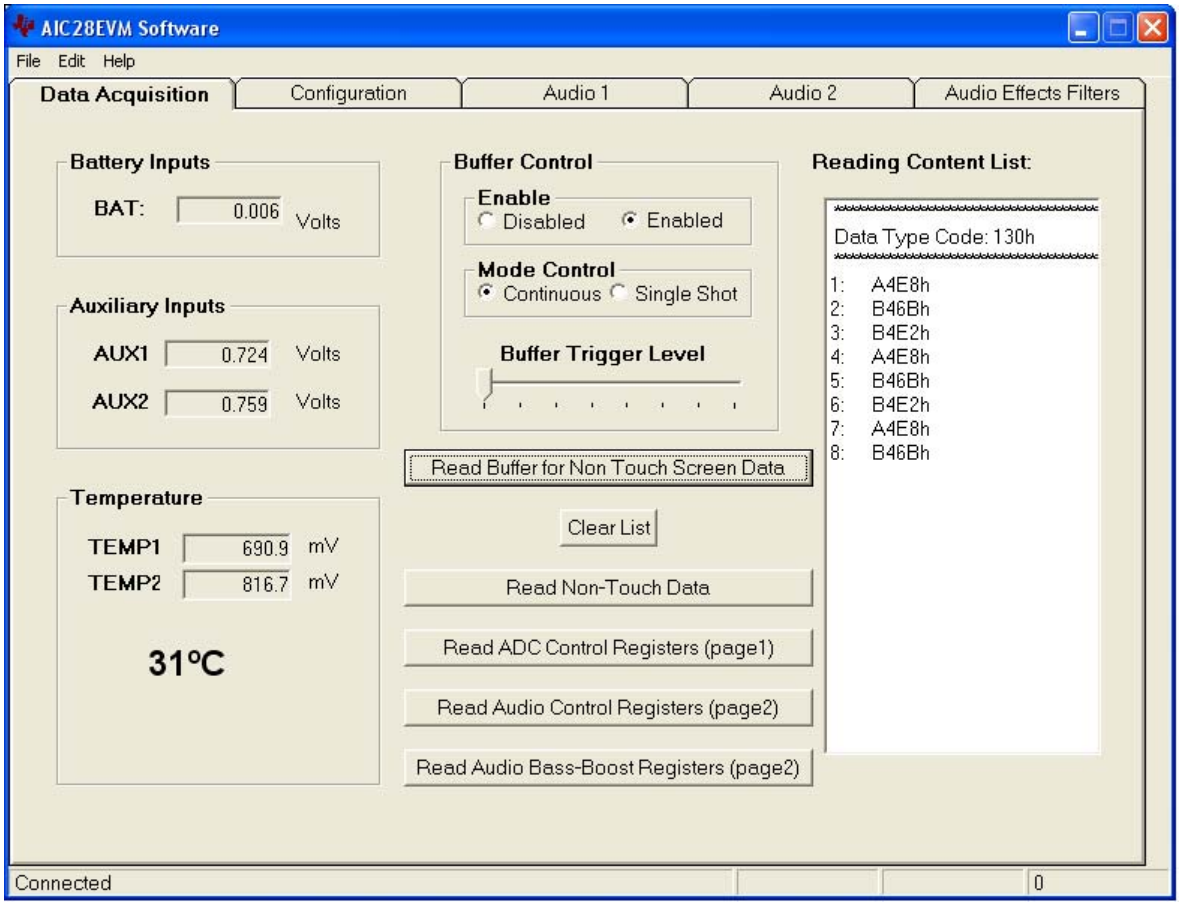
3.5.1.1 Analog Data Acquisition

At this screen with the buffer mode *NOT* enabled, the AIC28 is commanded to perform the battery and auxiliary input voltage readings, and then a TEMP1 and TEMP2 measurement. These measurements are all repeated twice every second, and the results are displayed on the three boxes at the left side of this screen.

3.5.1.2 Buffer Function

In the middle of the screen, the buffer mode settings can be accessed. By default, the buffer function is disabled and all analog data are converted and stored to the corresponding registers. When the *buffer* function is enabled, by checking the *Enable* option, as shown at Figure 3−1, the data is converted and saved to the *buffe*r registers in page 3 of the AIC28 memory space. Refer to the data sheet for the details of the *buffer function*.

Figure 3−1. Data Acquisition Screen With Enabled Buffer Function



When clicking on *Read Buffer for Non Touch Screen Data*, the AIC28 enters *auto-scan* mode to perform the auto scan on AUX1, AUX2, and TEMP1. These nontouch screen raw data are moved into the *Reading Content List* on the right

side of the Data Acquistion tab. The data in Figure3−1 is listed in this order: AUX1, AUX2, TEMP1, AUX1, AUX2, etc.

With this EVM, the buffer trigger level is either 8 or 16, selected by the *Buffer Trigger Level* selection slide. Even though the AIC28 can be set to a higher trigger level up to 64, this EVM allows only 8 or 16. The buffer function can be controlled in either Continuous or Single Shot mode, which is selected on the mode control option box. Refer to the data sheet for more on AIC28 buffer function.

The data in the list is cleared by clicking on the *Clear List* button on this screen.

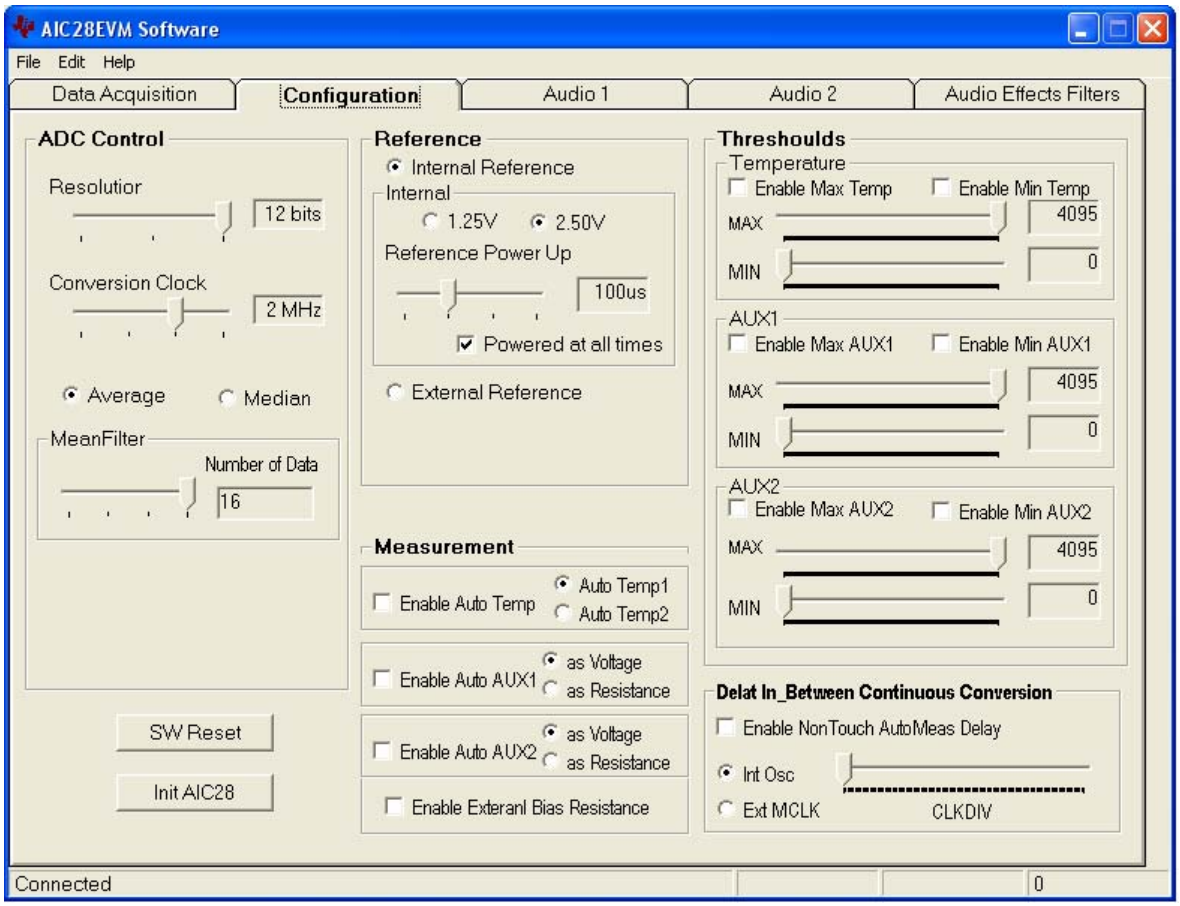
3.5.1.3 Register Readings

Four additional register reading buttons trigger the lead corresponding registers and move the raw data into the list. This is helpful for testing and debugging.

3.5.2 Configuration Screen

This screen accesses all the configurable settings for the AIC28 A/C converter and reference as shown in Figure 3−2.

Figure 3−2. Configuration Screen

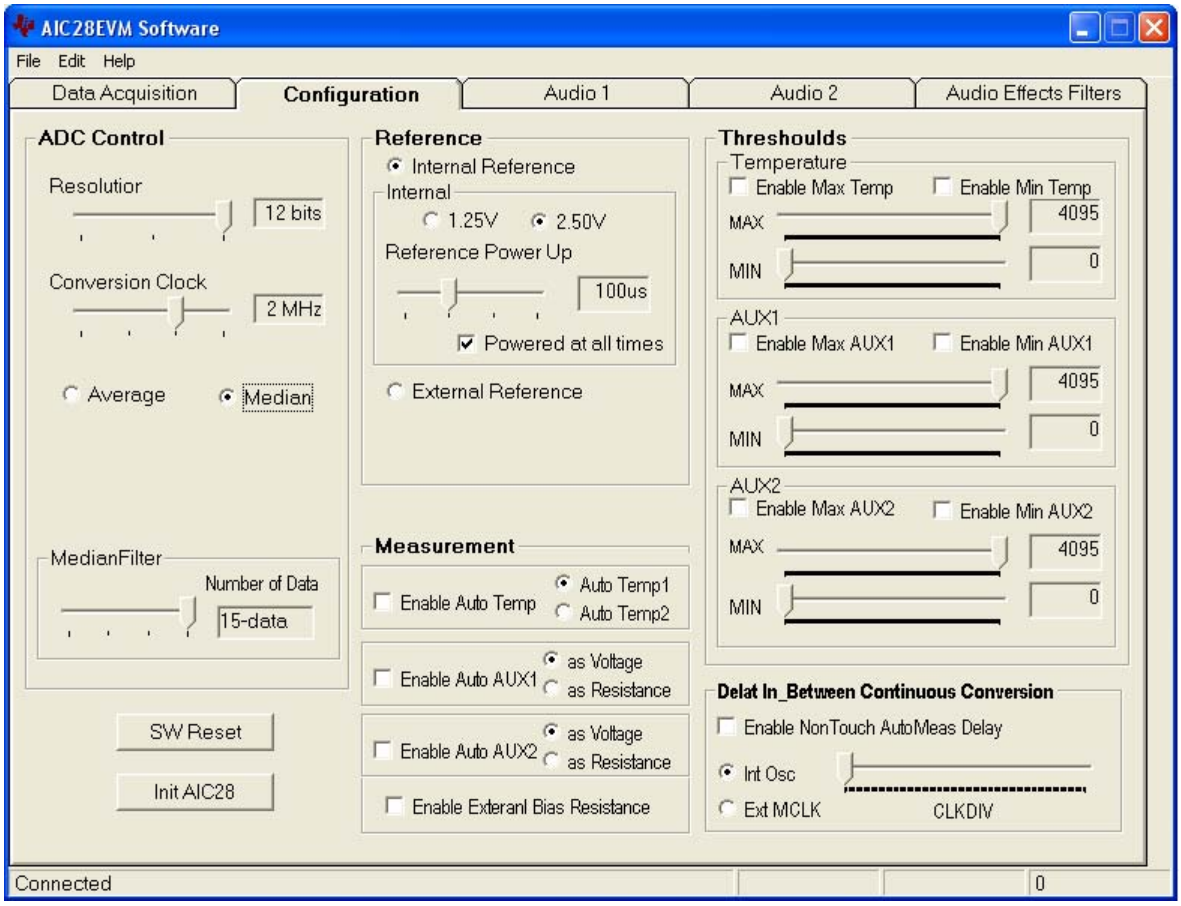


3.5.2.1 ADC Control Section

This section controls all of the parameters of the A/D converter. Each slider controls one parameter, whose value is shown next to the slider. Each slider is described as follows.

- **Resolution**—Selects between 8−, 10−, and 12−bit resolution.
- **Conversion Clock**—The internal clock which runs the A/D converter can run at 8, 4, 2, or 1 MHz. When running at 8 MHz, only 8-bit resolution is possible; when running at 4 MHz, 8- or 10-bit resolution is possible, but 12-bit is not. These restrictions are reflected in the operation of this program, because only 1- or 2-MHz clock rates allow 12-bit resolution to be chosen.
- **Average/Median**—There are two ways to reduce noise effect to the ADC result. One is averaging, where 4, 8, or 16 readings are averaged; another option is to find the median value among 5, 9, or 15 readings. The default is the average mode, as shown in Figure 3−2. When Median mode is selected, you see the configuration tab as shown in Figure 3−3.

Figure 3−3. Configuration Screen at Median Mode



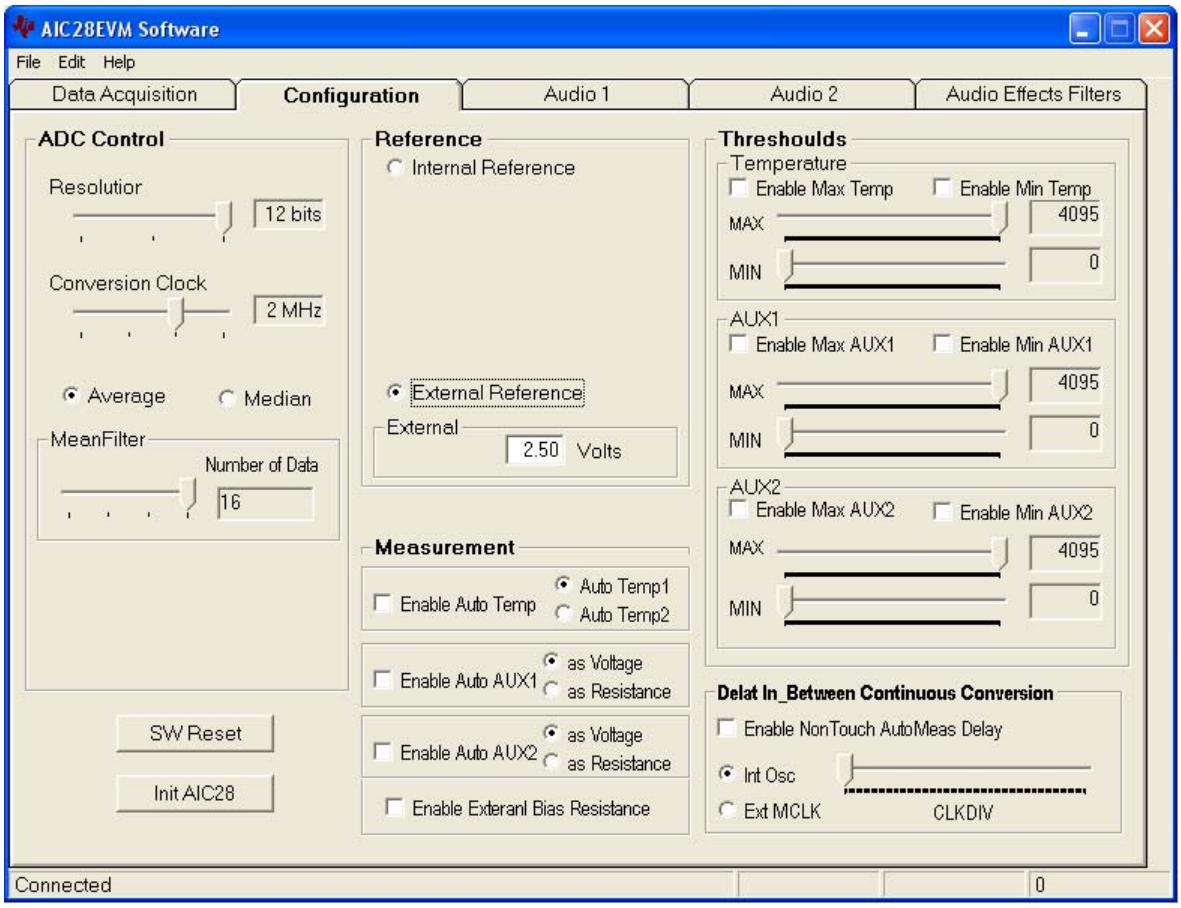
3.5.2.2 Reference Section

For the analog inputs, a reference voltage is needed for the A/D converter. Figure 3−2 and Figure 3−3 show this section with the AIC28 internal reference chosen.

The internal reference voltage can be set to either 1.25 V or 2.5 V. The internal reference powers down between conversions to save power if the *Powered at all times* checkbox is not checked. Using the *Powered at all times* checkbox, this can be overridden and the reference does not power down. If the reference is allowed to power down, the AIC28 must allow a delay time for the reference to power up when a conversion is to take place. This delay time can be set using the slider in this section.

If an external reference is to be used, it can be selected as shown in Figure 3−4. The value of the external reference should be entered in the text box shown.

Figure 3−4. Configuration Screen With External Reference Selection



3.5.2.3 Measurement Section

The AIC28 supports programmable auto-temperature and auto-auxiliary measurement mode. In the auto measurement mode, the AIC28 can auto start the TEMP1, TEMP2, AUX1, and/or AUX2 measurement after a programmable interval. The checkboxes in the Measurement section provide choices.

Additionally, the AUX1 and AUX2 can be configured to measure voltage or resistance. Under the resistance measurement, the bias can be configured as external or internal by checking or unchecking the box *Enable External Bias Resistance*.

3.5.2.4 Threshold Section

Another feature with the temperature and auxiliary input measurements in AIC28 is that the maximum and minimum of the analog input can be set up so that whenever the corresponding input signal goes outside the thresholds, the corresponding flags are set.

In this section, if the threshold function has not been enabled, that is the *Enable* checkbox has not been checked, the corresponding MAX/MIN slider does not move. Also note that the MAX value must be larger or equal to the MIN value.

3.5.2.5 Continuous Conversion Delay Section

In the auto measurement mode, the delays between the conversions are programmable. This section can be used to program to delays between the continuous conversions.

The nontouch and touch auto measurement delays can be programmed individually. Whenever the delay is enabled, by clicking on the corresponding checkbox, the delay-time option shows up for the selection.

The clock used here can be the internal oscillator or the external MCLK. The clock divider (CLKDIV) is used to get 1-MHz clock for the programmable delay. This sets the CLKDIV so that MCLK/CLKDIV = 1 MHz.

3.5.2.6 Reinitialization and Reset

Two buttons on this screen allow the user to reset and reinitialize the AIC28.

By clicking the button SW Reset , a software device reset is issued to the AIC28. By clicking the button Init AIC28 , the control registers (for ADC and audio) revert back to the startup (firmware) default settings.

To bring the AIC28 EVM back to its power-up status, you can click SW Reset, followed by Init AIC28 .

3.5.3 Audio Screens

Three tabs control the AIC28 audio functions: *Audio 1*, *Audio 2*, and *Audio Effects Filters* tabs.

Figure 3−5 shows the default condition of the Audio 1 tab with the following sections:

INTERFACE:	set up the audio I^2S port
PLL:	set up PLL parameters to get the desired FSref frequency
ADC:	set up the audio ADC, and select the ADC input source
DAC/Outputs:	set up the audio DAC and the all analog output features
GPIO1:	set up GPIO1 function/status
GPIO2:	set up GPIO2 function/status

Figure 3−5. Audio 1 Screen at Default

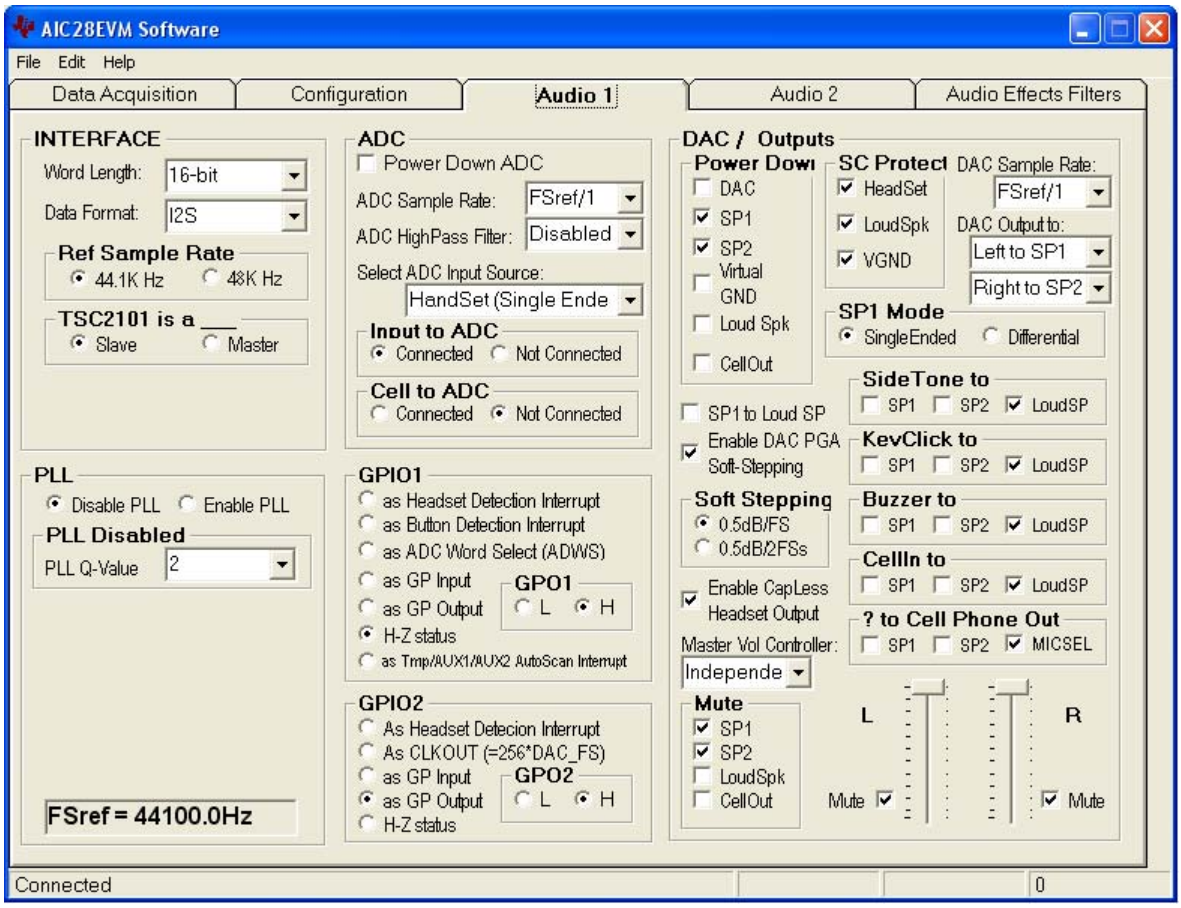


Figure 3−6 shows the default condition of the Audio 2 tab. The functions and setting on Audio 2 mainly control the audio analog inputs with the following sections:

HeadSet: set up the headset input power and gain control (PGA or AGC) function and other headset specified functions.

HandSet: set up the handset input power and gain control (PGA or AGC) function and other handset specified functions.

Cell Phone: set up the cell-phone input power and gain control (PGA or AGC) function.

SideTone: set up the sidetone power and gain.

KeyClick: set up the key-click tone.

Buzz Input: set up the power and gain for the input from the BUZZ_IN pin.

Figure 3−6. Audio 2 Screen at Default

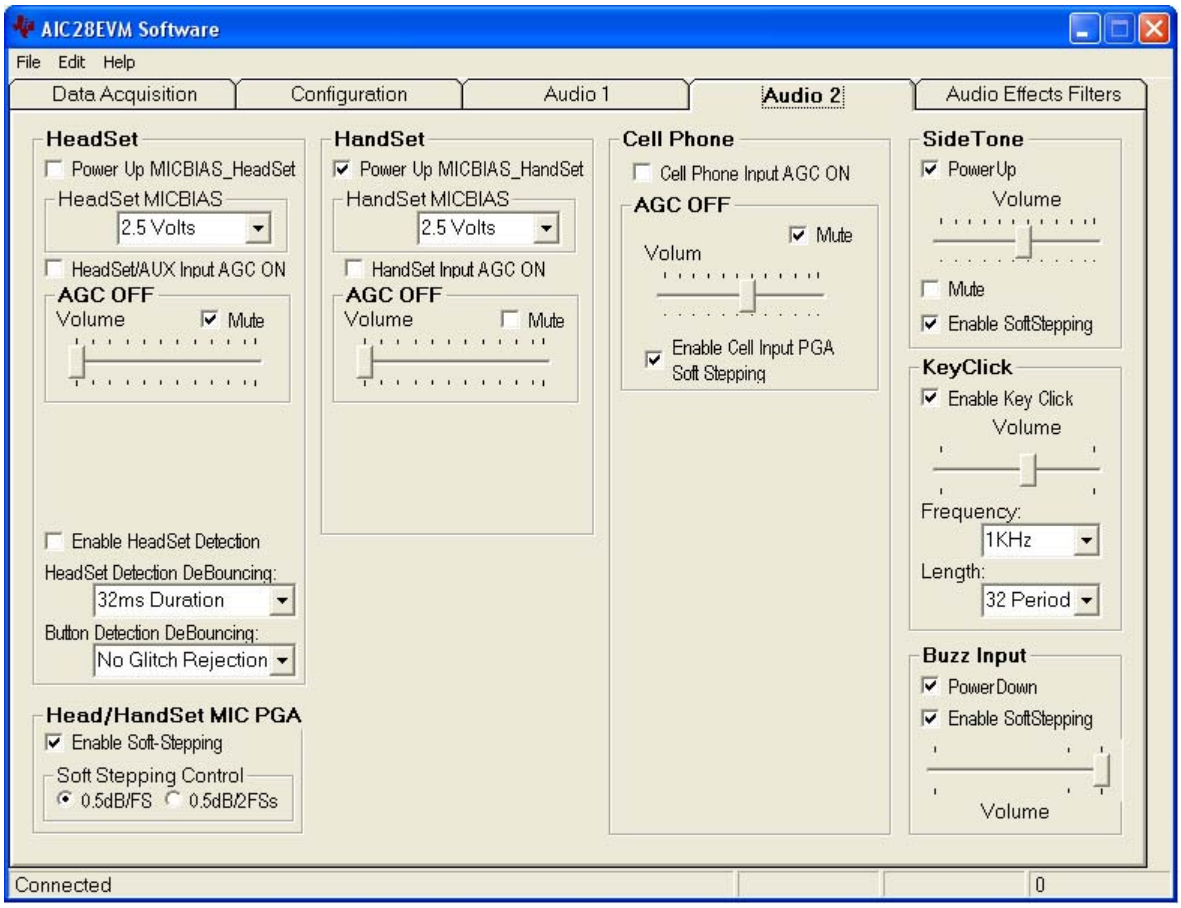
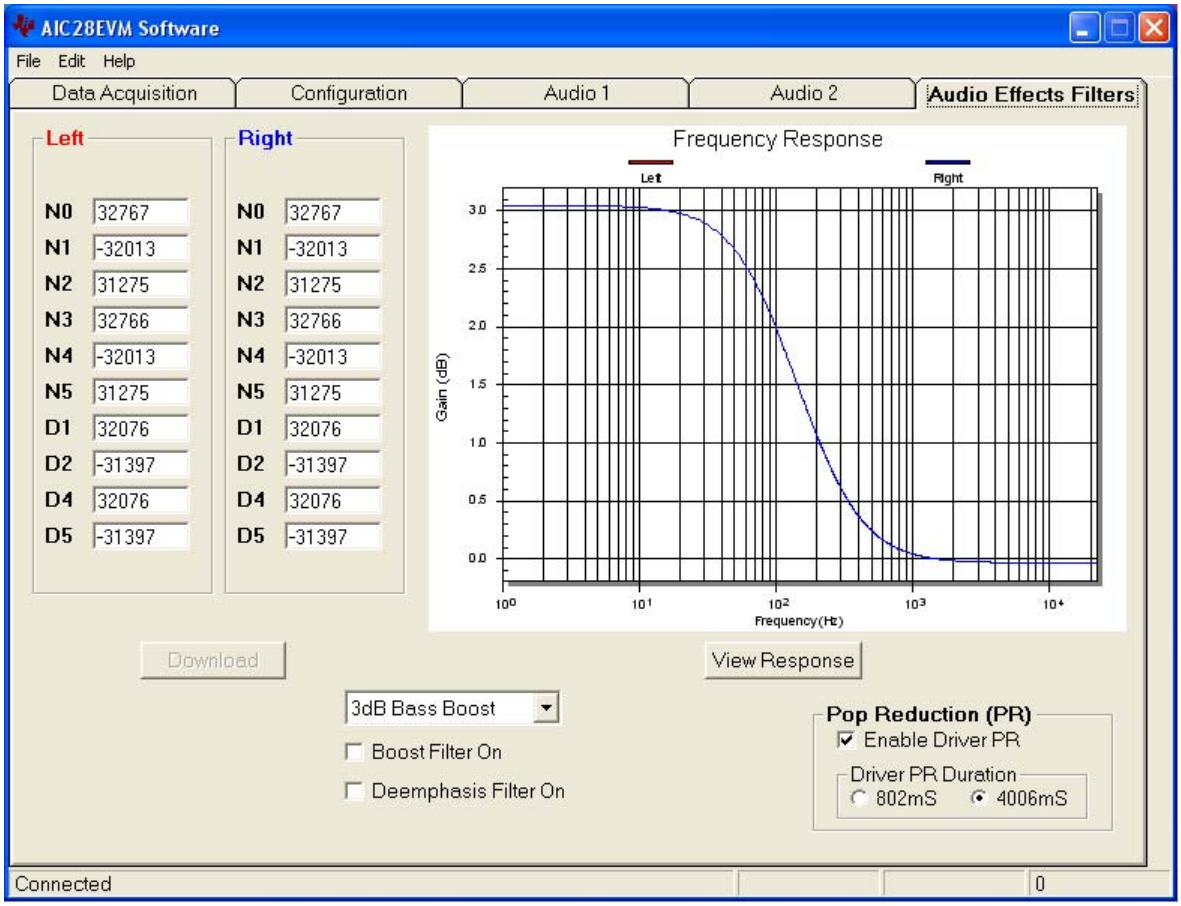


Figure 3−7 shows the default condition of the AudioEffects Filters tab. This tab displays the boost filters, the de-emphasis filter, and the output driver *pop* noise reduction function.

Figure 3−7. Audio Effects Filters Screen at Default



3.5.3.1 Interface Section

This section (refer to Figure 3−5) controls the behavior of the I^2S port (BCLK, LRCLK, DIN, and DOUT pins). In this EVM, the audio port transfers the 16 bit data in I^2S format, and the codec reference sample rate is at 44.1 kHz.

The AIC28 is programmed as a slave by default. The onboard processor TAS1020B is the *master,* which generates the BCLK and LRCLK signal.

If the AIC28 is used as a master, the onboard processor should be disabled and the I^2S port should be *detached* from the processor by turning OFF the onboard I^2S interface. Refer to the previous chapter for the hardware settings.

3.5.3.2 PLL Section

There is an on-chip phase-locked loop (PLL) on the audio codec part of the AIC28. The PLL can be enabled or disabled, based on the given master clock (MCLK) to the AIC28 and the required reference frequency (FSref) for the codec. For more details on the PLL, refer to the AIC28 data sheet. The PLL can be set on the PLL Secton of Audio 1 screen (Figure 3−5).

With the EVM board, the MCLK is at 11.2896 MHz, and the reference sample rate is at 44.1 kHz by default.

On the bottom of the section, the corresponding FSref frequency is shown based on the selection of:

1) the Q-value if the PLL has not been enabled; or

2) the P, J, D values if the PLL has been enabled.

3.5.3.3 ADC Section

This section (Audio 1 Tab, Figure 3−5) sets up the audio ADC power and the analog input source.

By default, the audio ADC has been powered up so that the audio recording function can start to run with any SW settings. By checking Power Down ADC, audio ADC power is disabled.

The ADC sample rate can be set as a divider frequency from the reference frequency, FSref. For example, when FSref = 44.1 kHz (set at the INTERFACE section of the same tab), an 8-K sample rate is achieved by setting the divider to 5.5 (44100/5.5 = 8018 Hz).

The audio ADC also has a high-pass filter, which is a submultiple of the sample rate, to remove dc or low frequency components from the input signal.

The input signal to the audio ADC can be obtained from different analog resources and under a different mode, selectable from the *Select ADC Input Source* option list. The microphone input from the headset or the handset can be selected; the single-ended or the differential input (paired with AUX1 or AUX2) can be used.

Also, there is the option to connect the above selected signal or the cell-phone input to the audio ADC.

3.5.3.4 DAC/Outputs Section

This section sets up the audio DAC power and all functions of the analog outputs, such as the power, the gain control, and the destination, which identifies the analog output pin or pins where the analog output signal is sent.

In the *Power Down* subsection, the DAC and the output driver circuits can be powered up/down individually. By checking a checkbox, the corresponding AIC28 circuit is powered down.

In the *SC Protect* subsection, the short-circuit (SC) protection function can be enabled or disabled. When the short-circuit protection functon is enabled and a short-circuit occurs, all analog outputs are disabled and the corresponding flag is set. For example, to set the headset SC protection, check the box. In the event of a headset short circuit, all analog outputs are disabled, and D1 of control registers in page 2 address 0x1D is set. The AIC28 requires hardware or software reset to return to normal operation.

Similar to the ADC, the DAC sample rate can be set as a divider frequency from the reference FSref frequency, through the *DAC Sample Rate* option list.

The AIC28 has the capability to route the stereo DAC output signals to any of the selected analog output. To route the signals to the headset drivers (SP1

and SP2 pins), select from the *DAC Output to* lists. By default, the left channel DAC output is routed to SP1 and the right channel to SP2.

The signal routed to SP1 can also be output to the loud speaker (OUT8P/OUT8N), if the *SP1 to Loud SP* checkbox is checked.

The SP1 can be used in single-ended or differential mode. In the single-ended mode, it is driven as one channel of the stereo headset outputs, and the audio sound is received through a headset that has been plugged into the jack J7 on the EVM. In the differential mode, the SP1 is paired with the OUT32N pin as the *receiver drive*r, and the audio sound is received through a speaker that has been connected to the terminal block J8 on the EVM. Note that the receiver driver and the headphone drivers are not allowed to be turned on at the same time. By default, the SP1 is set to single-ended mode.

Besides the DAC outputs, other inputs, such as the SideTone, KeyClick, CP_IN, and BUZZ_IN can be routed to speaker 1 (SP1), speaker 2 (SP2), and/or the loud speaker (LoudSP). The routing among these signals can be done on this section by clicking on the corresponding checkbox. The signals to SP1, SP2, or the ADC can be output to the TSC's cellphone output pin.

Like the audio ADC gain controls, the DAC PGA gain, can be set to soft-stepping mode. Under the soft-stepping mode, the *soft stepping* can be set to either 0.5−dB per one sample, or 0.5−dB per two samples.

The stereo DAC audio volumes is controlled three different ways by the left (L) and right (R) volume control slides, selectable through setting the master volume controller: 1) independent, 2) right channel controlled, or 3) left channel controlled.

In addition to the left and right DAC channel volume controls and mutes, the analog signals from the SPK1, SPK2, OUT8P/OUT8N (loud speaker), and CP_OUT pins can be individually muted or unmuted.

AIC28 supports both capacitor-coupled (cap) and capacitor-less (capless) interfaces for headset through software. Check the box *Enable Capless Headset Output* to turn on the capless outputs. Note that SW3 on the EVM board is associated with the software setting to have the proper cap or capless audio outputs on the EVM.

3.5.3.5 GPIO1 and GPIO2 Sections

The two GPIO pins on the AIC28 are programmed for several different functions, selectable through the GPIO1 or GPIO2 section. Refer to the data sheet for all of the functions. When a GPIO pin is used as a digital output, its status can be controlled by the *GPO Command* to either logic high or low. When not being used, the GPIO pin should be put on high impedance (Hi-Z) status.

3.5.3.6 Headset Section

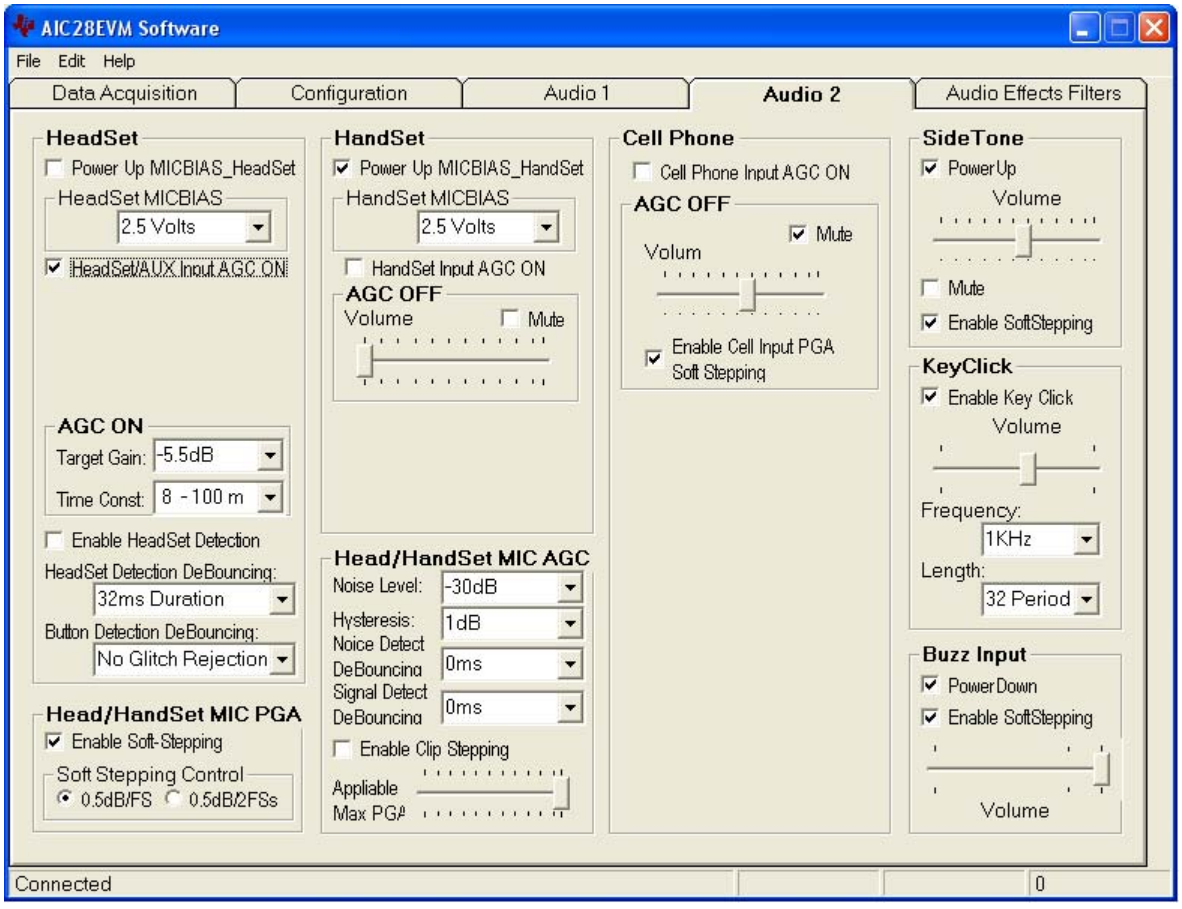
The headset section is in the Audio 2 tab, which is used mainly to set up the headset input gain through the headset PGA or the AGC, selectable by the *Headset/AUX Input AGC ON* checkbox.

By default, the AGC is OFF and the programmable gain amplifier (PGA) on the headset circuit is selected for the gain control, allowing analog input gain control from 0 dB to 59.5 dB. When the AGC is OFF, moving the volume slide on the *AGC OFF* subsection adjusts the PGA on the MICIN_HED path and checking the Mute box mutes the headset input signal.

When the PGA changes from the current value to a newly programmed value, the change rate can be controlled if the PGA Soft Stepping box is checked in the *Head/Handset MIC PGA* section, where the PGA changes 0.5 dB at either 1 step per sample or one step per two samples.

When the box by AGC ON is checked, the AGC is enabled and all of the options or settings for programming the AGC are now accessible, as shown in Figure 3−8. Refer to the TSC 2101 data sheet for setting and using the AGC.

Figure 3−8. Audio 2 Screen With Headset AGC On



In addition to the input gain control, the headset microphone bias can be selected. The programmable de-bounce features for the headset and button detect can also set up in this section. Refer to data sheet for the details on the detection and de-bounce.

3.5.3.7 Handset Section

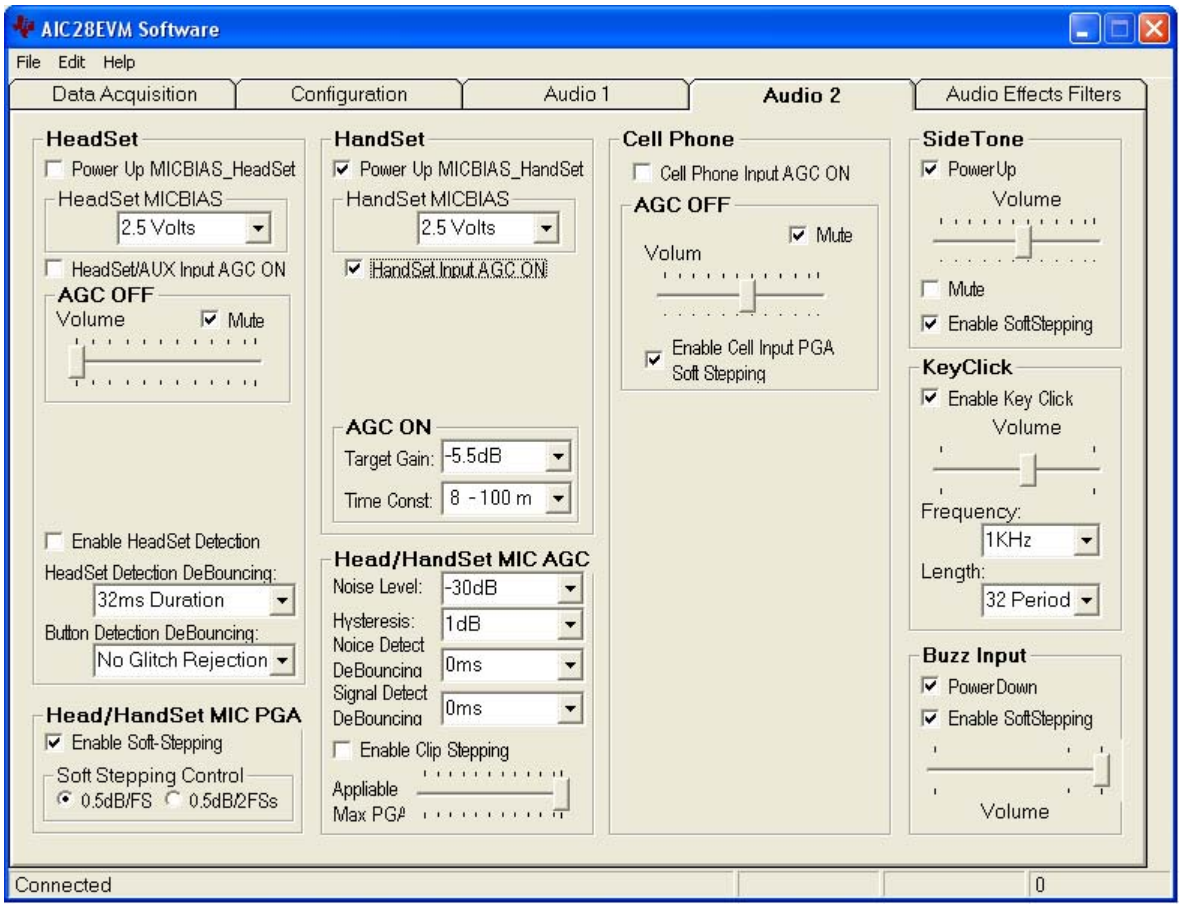
Similar to the headset section, the handset section is used mainly to set up the handset input gain through the handset PGA or the AGC, selectable by the *Handset Input AGC ON* checkbox.

By default, when the handset AGC is OFF, and the programmable gain amplifier (PGA) is selected for the input gain control, allowing analog input gain control from 0 dB to 59.5 dB. Under the case (AGC OFF), moving the volume slide on the *AGC OFF* subsection adjusts the PGA on the MICIN_HND path and checking the Mute box mutes the handset input signal.

The handset and headset share the soft-stepping settings. Refer to the explanation in the *Headset Section* for the feature and settings.

Similar to the headset, when the box by AGC ON is checked, the handset AGC is enabled, as shown in Figure 3−9. Refer to the TSC 2101 data sheet for setting and using the AGC.

Figure 3−9. Audio 2 Screen With Handset AGC On



In addition to the handset input gain control, the handset microphone bias can be selected inside the Handset Section, similar to that in the *Headset Section*.

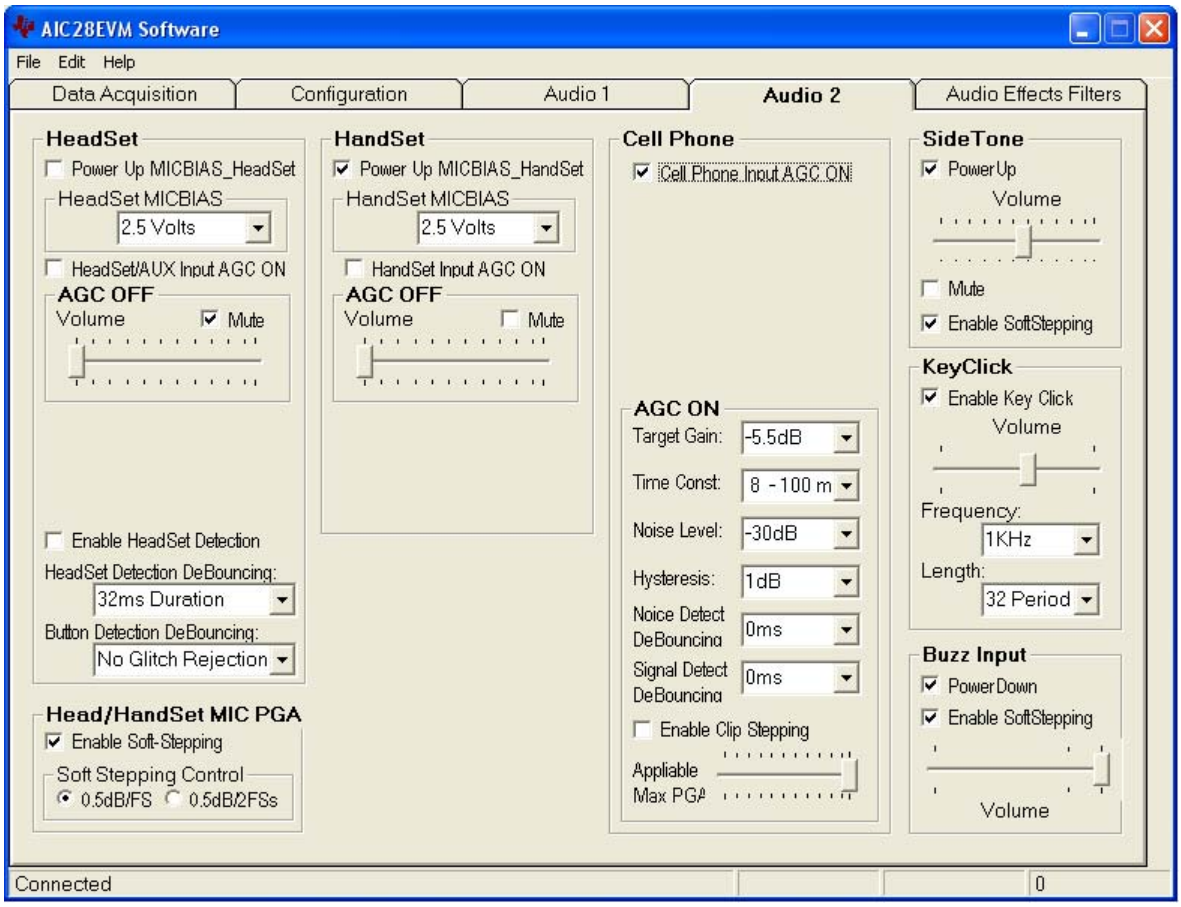
3.5.3.8 Cell-Phone Section

The cell-phone section is used to set up the cell-phone input gain, by using the CP_IN PGA or AGC.

When the checkbox by *Cell Phone Input AGC ON*, is not checked, the PGA controls the gain, from −34.5 dB to 12 dB, and in 0.5 dB steps if the soft-stepping option was selected. The cell-phone input is muted when the Mute box under the slider is checked.

When the box by AGC ON is checked, the cell-phone input AGC is enabled, as shown in Figure 3−10. Refer to the TSC 2101 data sheet for setting and using the AGC.

Figure 3−10. Audio 2 Screen With Cell-Phone AGC On



3.5.3.9 Sidetone Section

The AIC28 has an analog sidetone circuit. The audio outputs of the AIC28 includes a mix so that the sidetone can be mixed with the audio output signals, in proportion to their respective volume settings.

The sidetone is enabled when the PowerUp box is checked. Its volume can be adjusted by the analog volume control slider, ranging from −34.5 dB to12 dB, and in 0.5-dB steps if the soft-stepping option is used. The sidetone is muted when the Mute box under the slider is checked.

At the EVM power up, the sidetone is defaulted to power up.

3.5.3.10 Keyclick Section

When the *Enable Key Click* box is checked, a clicking sound is heard whenever an audio-related setting is selected or checked in the Audio 1, Audio 2 and the Audio Effects Filters screens.

The volume, frequency, and duration (length) of this keyclick can be adjusted using the corresponding slider and selectors.

At the EVM power up, the keyclick is enabled by default.

3.5.3.11 Buzz Input Section

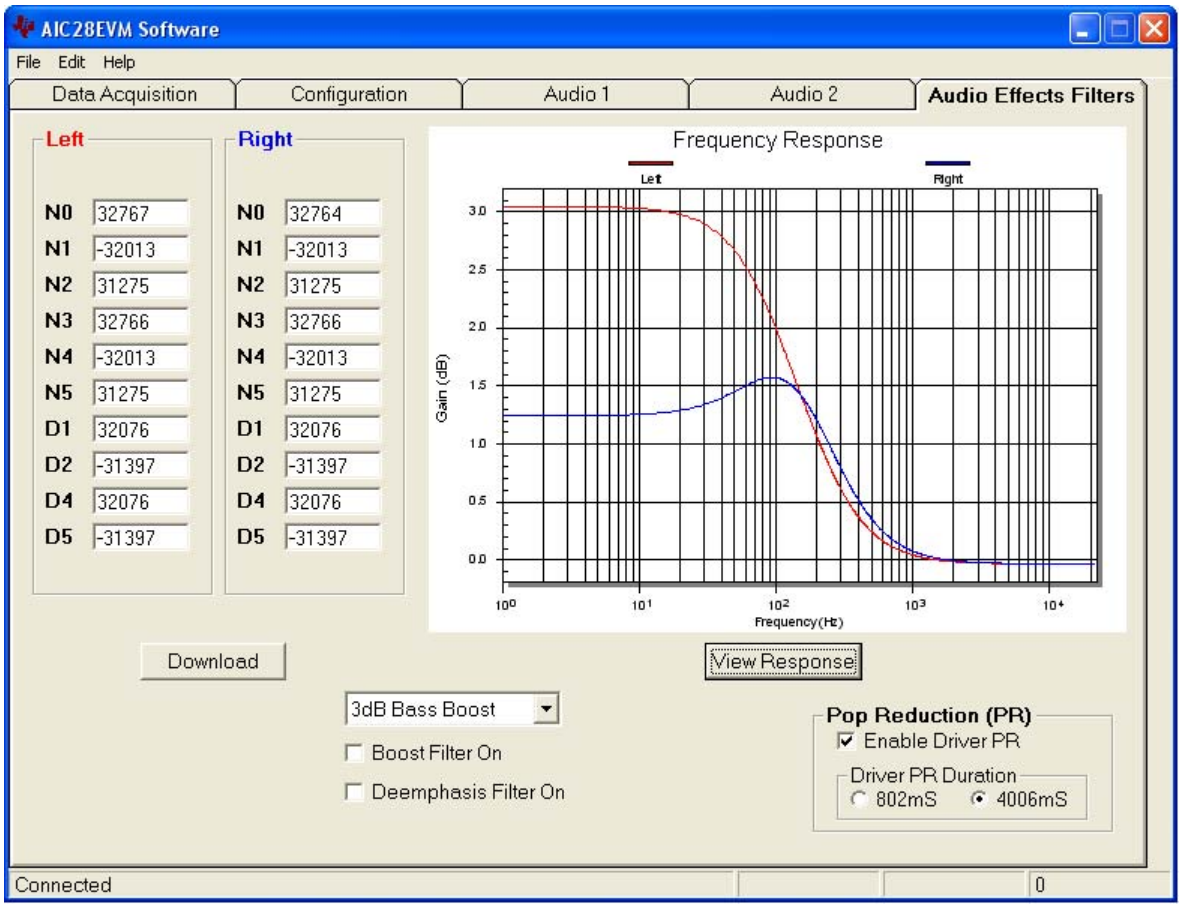
The buzzer input from the cell phone can be routed to AIC28 through the BUZZ_IN pin, if the checkbox by PowerDown is not selected. This input path supports the PGA range of from −45 dB to 0 dB, and in 3 dB steps if the soft-stepping option was chosen.

3.5.3.12 Audio Effects Filters Screen

The Audio Effects Filters screen displays all of the coefficients for the boost filter function of the AIC28. These coefficients are programmable. Refer to the default Audio Effects Filters Screen shown in Figure 3−7.

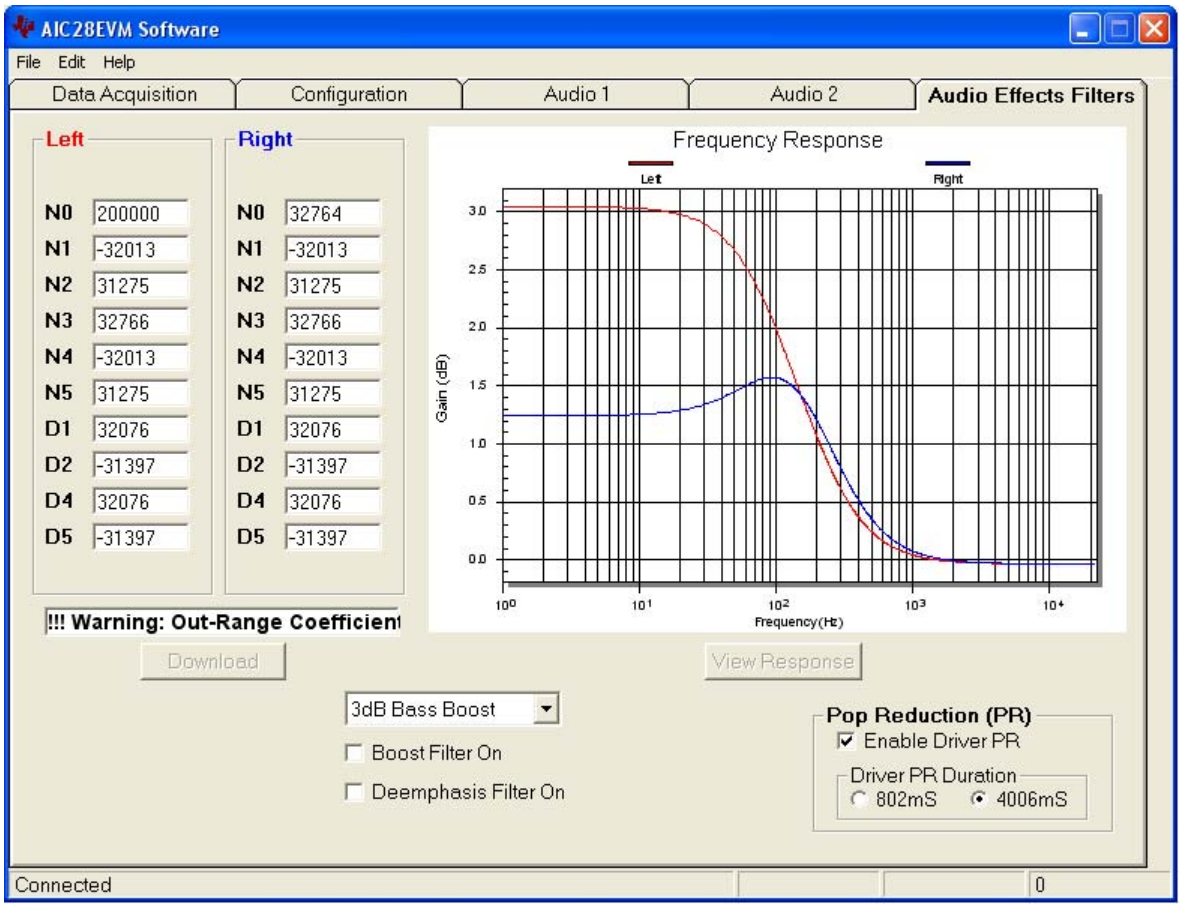
Different filter coefficients can be loaded for left and right channels, although usually these are set the same. Figure 3−11 shows an example with the different left and right channel filters.

Figure 3−11. Audio Effects Filters Screen With Different Left/Right Channels



If changes are made to coefficient values directly, the response can be viewed on the graph by pressing the *View Response* button. It is recommended that the user view the response before downloading values to the AIC28, as some values can cause clipping or oscillation of the filter. The filter equation is described in the AIC28 data sheet. When the entered data is outside the range, a warning window appears to indicate the improper coefficient entered, as shown in Figure 3−12.

Figure 3−12. Audio Effects Filters Screen With Bad Data



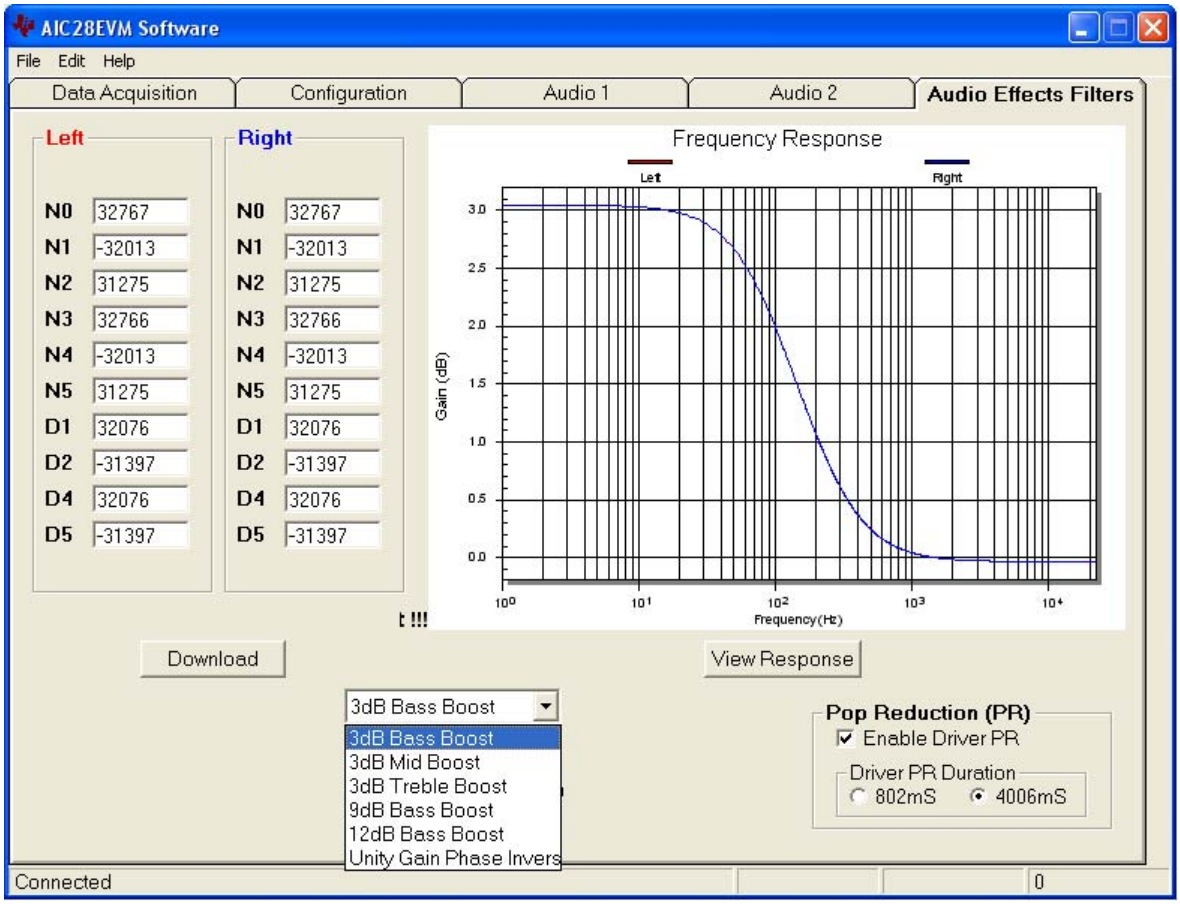
In addition to the direct coefficient settings previously described, there are six preconfigured filters designed with the EVM software, selectable using the drop-down list of this screen, refer to Figure 3−13. On selection, the coefficients are updated along with the graph of the filter response to the selection. However, nothing is loaded into the AIC28 until the Download button is pressed.

Checking the *Boost Filter* box enables the filter selected.

In addition to the boost filter, is another digital filter, the de-emphasis filter is provided by AIC28 for the audio DAC. Checking the *Deemphasis Filter On* box enables the filter.

Settings on this tab can reduce the *pop* noise heard at the moment the power supply (-ies) is brought up to the AIC28. The pop noise reduction can be set on the analog output driver circuit. Click on the *Enable Driver PR* checkbox to enable the output driver pop reduction feature. Set the *Clock* duration to change and optimize the noise reduction effect.

Figure 3−13. Audio Effects Filters Screen With Boost Filter Selection



Chapter 4

Physical Description

This chapter contains the bill of materials, the EVM board silk screen/top layer, and the schematics.

Topic **Page**

4.1	Bill of Materials	4-2
4.2	EVM Silk Screen/Top Layer	4-5
4.3	Schematics	4-6

4.1 Bill of Materials

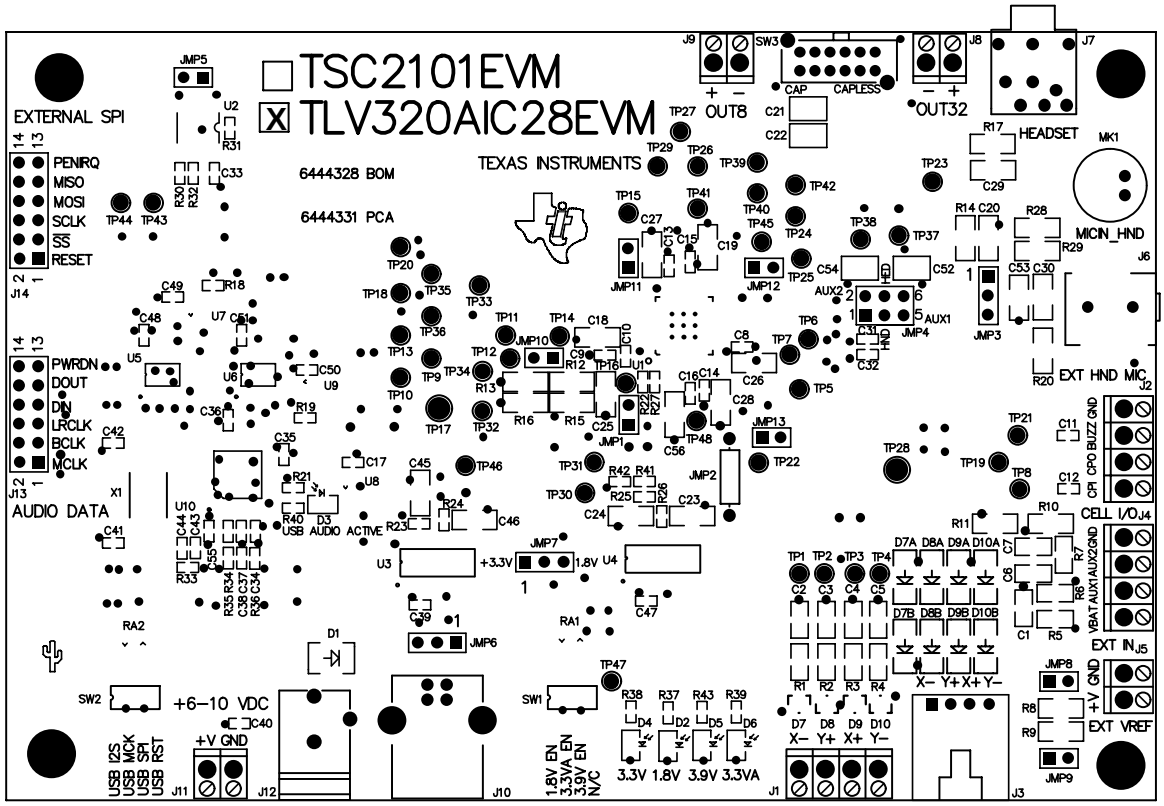
Item No.	Qty	Value	Ref Des	Description	Vendor	Part Number
1	62	0	R6, R7	1/8W 5% Chip resistor	Panasonic	ERJ−6GEY0R00V
Not Installed	4		R1−R4	1/8W 5% Chip resistor	Panasonic	ERJ−6GEY0R00V
2	1	0	R20	1/4W 5% Chip resistor	Panasonic	ERJ−8GEY0R00V
3	1	10	R37	1/16W 1% Chip resistor	Panasonic	ERJ−3EKF10R0V
4	2	27.4	R35, R36	1/16W 1% Chip resistor	Panasonic	ERJ−3EKF27R4V
5	2	220	R38, R39	1/10W 5% Chip resistor	Panasonic	ERJ−3GEYJ221V
6	1	220	R5	1/8W 5% Chip resistor	Panasonic	ERJ−6GEYJ221V
7	1	270	R43	1/10W 5% Chip resistor	Panasonic	ERJ−3GEYJ271V
8	1	649	R40	1/16W 1% Chip resistor	Panasonic	ERJ−3EKF6490V
9	1	680	R28	1/4W 5% Chip resistor	Panasonic	ERJ−8GEYJ681V
10	1	1.5 k	R34	1/10W 5% Chip resistor	Panasonic	ERJ−3GEYJ152V
11	1	2.2 k	R29	1/4W 5% Chip resistor	Panasonic	ERJ−8GEYJ222V
12	3	2.7 k	R18, R19, R21	1/10W 5% Chip resistor	Panasonic	ERJ−3GEYJ272V
13	1	2.7 k	R17	1/4W 5% Chip resistor	Panasonic	ERJ−8GEYJ272V
14	4	3.09 k	R30−R33	1/16W 1% Chip resistor	Panasonic	ERJ−3EKF3091V
15	1	30.1 k	R42	1/16W 1% Chip resistor	Panasonic	ERJ−3EKF3012V
16	1	69.8 k	R41	1/16W 1% Chip resistor	Panasonic	ERJ−3EKF6982V
17	6	100 k	R22−R27	1/10W 5% Chip resistor	Panasonic	ERJ−3GEYJ104V
18	2	10 k	RA1, RA2	1/16W 5% 4-resistor array, 8 terminal	CTS Corporation	742C083103JTR
Not Installed	9		R8−R16			
19	2	33 pF	C41, C42	50-V Ceramic chip capacitor, ±5%, NPO	Panasonic	ECJ−1VC1H330J
20	2	47 pF	C37, C38	50-V Ceramic chip capacitor, ±5%, NPO	Panasonic	ECJ−1VC1H470J
21	1	100 pF	C43	50-V Ceramic chip capacitor, ±5%, NPO	Panasonic	ECJ−1VC1H101J
22	1	1000 pF	C44	50-V Ceramic chip capacitor, ±10%, X7R	Panasonic	ECJ−1VB1H102K
23	12	0.1 µF	C8−C16, C31, C32, C40	16-V Ceramic chip capacitor, ±10%, X7R	Panasonic	ECJ−1VB1C104K
Not Installed	7	0.1 µF	C1−C7	16-V Ceramic chip capacitor, ±10%, X7R	Panasonic	ECJ−2VB1C104K
24	2	0.1 µF	C29, C30	16-V Ceramic chip capacitor, ±10%, X7R	Panasonic	ECJ−3VB1C104K
25	2	0.33 µF	C39, C47	10-V Ceramic chip capacitor, ±10%, X5R	Panasonic	ECJ−1VB1A334K
26	10	1 µF	C17, C33−C36, C48−C51, C55	16-V Ceramic chip capacitor, ±10%, X5R	Panasonic	ECJ−1VB1C105K
27	12	10 µF	C18−C20, C23−C28, C45, C46, C56	6.3-V Ceramic chip capacitor, ±10%, X5R	Panasonic	ECJ−3YB0J106K

Item No.	Qty	Value	Ref Des	Description	Vendor	Part Number
28	2	47 µF	C21, C22	6.3-V Ceramic chip capacitor, ±20%, X5R	Panasonic	ECJ−4YB0J476M
Not Installed	3		C52, C53, C54			
29	1		D1	50-V, 1-A diode SMD	Micro Commercial Corp.	DL4001
30	1		D2	Red LED, SMD	Lumex	SML−LX0603IW−TR
31	1		D3	Yellow LED, SMD	Lumex	SML−LX0603YW−TR
32	3		D4−D6	Green LED, SMD	Lumex	SML−LX0603GW−TR
Not Installed	4		D7−D10	Schottky barrier diode, series configuration	Zetex	BAT54STA
33	1		MK1	Omnidirectional microphone cartridge	Knowles Acoustics	MD9745APZ−F
34	1		X1	6-MHz crystal, SMD	Epson	MA−505 6.000M−C0
35	1		U1	Audio codec	Texas Instruments	TLV320AIC28RGZ
36	1		U2	64K, I^2C EEPROM	Microchip	24LC64−I/SN
37	1		U3	Dual output LDO voltage regulator	Texas Instruments	TPS767D318PWP
38	1		U4	Dual output LDO voltage regulator	Texas Instruments	TPS767D301PWP
39	2		U5, U6	Quad IC buffer driver with 3-state output	Texas Instruments	SN74LVC125APW
40	3		U7, U8, U9	Single IC buffer driver with open drain o/p	Texas Instruments	SN74LVC1G07DBVR
41	1		U10	USB Interface to SPI™/I^2S™	Texas Instruments	TAS1020BPFB
42	1		N/A	TLC320AIC28EVM PWB	Texas Instruments	6444330
43	2		J2, J4	Screw terminal block, 4 position	On Shore Technology	ED555/4DS
Not Installed	1		J1	Screw terminal block, 4 position	On Shore Technology	ED555/4DS
44	4		J5, J8, J9, J11	Screw terminal block, 2 position	On Shore Technology	ED555/2DS
Not Installed	1		J3	Right angle 4 position socket	AMP/Tyco Electronics	103634−3
45	1		J6	3,5 mm audio jack, T−R−S, SMD	CUI Inc.	SJ−3515−SMT−1
46	1		J7	3,5 mm audio jack, T−R−S−G, Thru−Hole	CUI Inc.	SJ−43514
47	1		J12	2,5 mm Power Jack	CUI Inc.	PJ−102B
48	1		J10	USB type B socket, thru−hole	Mill−Max	897-30-004-90-000000
49	2		J13, J14	6 × 2 Position header, 0.1” spacing	Samtec	TSW−106−07−L−D
50	3		JMP5, JMP8, JMP9	2 Position jumper, 0.1” spacing	Samtec	TSW−102−07−L−S

Item No.	Qty	Value	Ref Des	Description	Vendor	Part Number
51	3		JMP3, JMP6, JMP7	3 Position jumper, 0.1” spacing	Samtec	TSW−103−07−L−S
52	1		JMP4	3 X 2 Position header, 0.1” spacing	Samtec	TSW−103−07−L−D
53	1		JMP2	Bus wire		
54	5		JMP1, JMP10, JMP11, JMP12, JMP13	Bus wire		
55	2		SW1, SW2	4 Position DIP switch, SMD half pitch	C&K	TDA04H0SK1
56	1		SW3	4 PDT right angle switch	E−Switch	EG4208
Not Installed	46		TP1−TP16, TP18−TP27, TP29−TP48	Miniature test point terminal	Keystone Electronics	5000
57	2		TP17, TP28	Miniature test point large loop terminal	Keystone Electronics	5011
58	8		N/A	Jumper top	Samtec	SNT−100−BK−T
59	4		N/A	0.25” × 0.625” Hex 4−40 threaded standoff	Keystone Electronics	1808
60	4		N/A	Pan head machine screw 4−40 × 1/2” phillips	Building Fasteners	PMS 440 0050 PH

4.2 EVM Board Silk Screen/Top Layer

Figure 4−1. Top Board Layer Silk Screen



4.3 Schematics

Schematic diagrams of the AIC28EVM showing the AIC28 connections and the USB and connectors are shown on the following pages.

Revision History		
REV	ECN Number	Approved

PLEASE NOTE:
Components within dashed box are not included on the AIC28 version of the board.

D7 through D10 are not installed, but can be added for extra ESD protection, or for reducing touch panel noise.

C1 through C7 are not installed, but can be added for noise filtering.

R8 through R11, JMP8 and JMP9 are not installed, but can be used for resistance measurements on the AUX pins.

C52, C53, and C54 are not installed, but can be used to filter noise on microphone bias outputs.

JMP4 is used to select AUX inputs for differential microphone input mode.

R12, R13, R15 and R16 are not installed, but can be used as pull ups or pull downs on the GPIO lines.

TSC2101RGZ/TLV320AIC28RGZ

ENGINEER **BOB BENJAMIN**			
DRAWN BY **BOB BENJAMIN**			
DOCUMENT CONTROL NO. **6444329**	SIZE **A**	DATE **12-Jan-2004**	REV **A**
SHEET **1** OF **2**	FILE G:\TSC2101EVM\Schematic\TSC2101EVM.ddb - Documents\TSC2101		

TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

TITLE **TSC2101-AIC28EVM**
TOUCH SCREEN CONTROLLER/AUDIO CODEC

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

TP43
TP44
R30 3.09K
R32 3.09K
+3.3V
U2
VCC SDA SCL
VSS A0 A1 A2 WP
24LC64I/SN
C33 1uF
R31 3.09K
JMP5
A1 SELECT
C41 33pF
C42 33pF
X1
MA-505 6.000M-C0
6.00 MHZ
C43 100pF
C44 .001uF
R33 3.09K
U10
SCL SDA VREN RESET MCLKO2 MCLKO1 CSCLK CDATO CDATI CSYNC CRESET CSCHNE
XTALO XTALI PLLFILI PLLFILO MCLKI PUR DP DM DVSS DVSS DVSS AVSS
P1.7 P1.6 P1.5 P1.4 P1.3 P1.2 P1.1 P1.0 DVDD DVDD DVDD AVDD
MRESET TEST EXTEN RSTO P3.0 P3.1 P3.2/XINT P3.3 P3.4 P3.5 NC NC
TAS1020BPFB
J10 USB SLAVE CONN
GND D+ D- VCC
897-30-004-90-000000
R34 1.5K
R35 27.4
R36 27.4
C37 47pF
C38 47pF
TP46
MRESET
C55 1uF
C34 1uF
C35 1uF
C36 1uF
U5
1A 2A 3A 4A 1OE 2OE 3OE 4OE VCC 1Y 2Y 3Y 4Y GND
SN74LVC125APW
USB MCK
USB I2S
MCLK
I2SDIN
BCLK
I2SDOUT
LRCLK
C48 1uF
IOVDD
+3.3V
RA2 10K
SW2
USB I2S
USB MCK
USB SPI
USB RST
TAS ENABLE
J13
AUDIO DATA
PWR_DWN
R18 2.7K
U7
SN74LVC1G07DBV
C49 1uF
R19 2.7K
U9
SN74LVC1G07DBV
C50 1uF
C51 1uF
MISO
MOSI
SS
SCLK
RESET
J14
EXTERNAL SPI
U6
SN74LVC125APW
USB RST
USB SPI
U3
1IN 1EN 1GND 2GND 2EN 2IN 2IN 1RESET 1OUT 1OUT 2RESET 2OUT 2OUT
TPS767D318PWP
R23 100K
R24 100K
+1.8V
C45 10uF
C46 10uF
C39 0.33uF
R38 220
D4
SML-LX0603GW-TR
GREEN
+3.3V
USB AUDIO ACTIVE
R40 649
D3
SML-LX0603YW-TR
YELLOW
R21 2.7K
C17 1uF
U8
SN74LVC1G07DBV
PENIRQ
J11
ED555/2DS
EXT PWR IN
6VDC-10VDC IN
J12
CUI-STACK PJ102-B
2.5 MM
C40 0.1uF
D1
DL4001
JMP6
PWR SELECT
U4
1IN 1EN 1GND 2GND 2EN 2IN 2IN 1RESET 1FB 1OUT 1OUT 2RESET 2OUT 2OUT
TPS767D301PWP
R25 100K
R41 69.8K
R42 30.1K
R26 100K
R39 220
+3.3VA
+3.9V
C24 10uF
R43 270
D5
SML-LX0603GW-TR
GREEN
D6
SML-LX0603GW-TR
GREEN
D2
SML-LX0603IW-TR
RED
R37 10
C47 0.33uF
C23 10uF
RA1 10K
SW1
1.8V ENABLE
3.3VA ENABLE
3.9V ENABLE
TSC PWR ENABLE
TP47
TESTPOINT
JMP7
IOVDD SELECT

ENGINEER	BOB BENJAMIN
DRAWN BY	BOB BENJAMIN
DOCUMENT CONTROL NO.	6444329
SHEET	2 OF 2

TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

TITLE: TSC2101-AIC28EVM USB INTERFACE

SIZE B | DATE 12-Jan-2004 | REV A

FILE G:\TSC2101EVM\Schematic\TSC2101EVM.ddb - Documents\TSCUSB