

NANOPOWER 1.8-V SOT23 COMPARATORS WITH VOLTAGE REFERENCE

FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site
 - One Fabrication Site
- **Extended Temperature Performance of**
–55°C to 125°C
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree⁽¹⁾**
- **Low Quiescent Current = 5 μ A (Max)**
- **Integrated Voltage Reference = 1.242 V**
- **Input Common-Mode Range = 200 mV Beyond Rails**
- **Voltage Reference Initial Accuracy = 1%**
- **Open-Drain Logic Compatible Output (TLV3011)**
- **Push-Pull Output (TLV3012)**
- **Low Supply Voltage = 1.8 V to 5.5 V**
- **Fast Response Time = 6- μ s Propagation Delay With 100-mV Overdrive (TLV3011: R_{PULLUP} = 10 k Ω)**
- **Microsize Package: SOT23-6**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

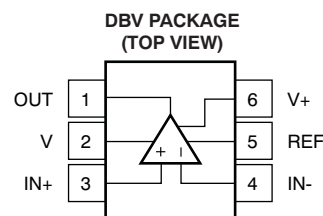
APPLICATIONS

- **Battery-Powered Level Detection**
- **Data Acquisition**
- **System Monitoring**
- **Oscillators**
- **Sensor Systems**
 - Smoke Detectors
 - Light Sensors
 - Alarms

DESCRIPTION

The TLV3011 and TLV3012 are low-power, open-drain output comparators. The devices feature an uncommitted on-chip voltage reference, have 5- μ A (max) quiescent current, input common-mode range 200 mV beyond the supply rails, and single-supply operation from 1.8 V to 5.5 V. The integrated 1.242-V series voltage reference offers low 100-ppm/°C (max) drift, is stable with up to 10-nF capacitive load, and can provide up to 0.5 mA (typ) of output current.

The TLV3011 and TLV3012 are available in the tiny SOT23-6 package for space-conservative designs. The devices are specified for the temperature range of –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PACKAGE ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP SIDE MARKING
-55°C TO 125°C	DBV-SOT	TLV3011AMDBVREP	BTv
	DBV-SOT	TLV3012AMDBVREP ⁽²⁾	TBD

- ## Pin Configurations

The figure shows the pin configurations for two comparators in a 6-pin SOT23-6 package. The left comparator is the TLV3011AMDBV, which has a 'BTV' internal symbol. Its pins are: 1 (OUT), 2 (V-), 3 (IN+), 4 (IN-), 5 (REF), and 6 (V+). The right comparator is the TLV3012AMDBV(1), which has a 'TBD' internal symbol. Its pins are: 1 (OUT), 2 (V-), 3 (IN+), 4 (IN-), 5 (REF), and 6 (V+).

(1) Product Preview

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage			7	V
Signal input terminals	Voltage ⁽²⁾	−0.5	(V+) +0.5	V
	Current ⁽²⁾		±10	mA
Output short circuit ⁽³⁾		Continuous		
Operating temperature range		−55	125	°C
T _{stg}	Storage temperature range	−65	150	°C
T _J	Junction temperature		150	°C
Lead ambient temperature (soldering, 10 s)			300	°C
ESD rating (Human-Body Model)			2000	V

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.
- (3) Short circuit to ground

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Offset Voltage								
V _{OS}	Input offset voltage		V _{CM} = 0 V, I _O = 0 V			0.5	15	mV
dV _{OS} /dT	Input offset voltage vs temperature		T _A = −55°C to 125°C			±12		μV/°C
PSRR	Power supply rejection ratio		V _S = 1.8 V to 5.5 V			100	1000	μV/V
Input Bias Current								
I _S	Input bias current		V _{CM} = V _S /2			±10		pA
I _{OS}	Input offset current		V _{CM} = V _S /2			±10		pA
Input Voltage Range								
V _{CM}	Common-mode voltage range				(V−) − 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio		V _{CM} = −0.2 V to (V+) − 1.5 V		60	74		dB
			V _{CM} = −0.2 V to (V+) + 0.2 V		54	62		
Input Impedance								
Common mode						10 ¹³ 2		Ω pF
Differential						10 ¹³ 4		Ω pF
Switching Characteristics								
Propagation delay time	Low to high	f = 10 kHz, V _{STEP} = 1 V, input overdrive = 10 mV		12		μs		
		f = 10 kHz, V _{STEP} = 1 V, input overdrive = 100 mV		6				
	High to low	f = 10 kHz, V _{STEP} = 1 V, input overdrive = 10 mV		13.5				
		f = 10 kHz, V _{STEP} = 1 V, input overdrive = 100 mV		6.5				
t _r	Rise time	TLV3011			See ⁽¹⁾		ns	
		TLV3012 ⁽²⁾	C _L = 10 pF		100			
t _f	Fall time			C _L = 10 pF		100		ns
Output								
V _{OL}	Voltage output low from rail		V _S = 5 V		160		200	mV
	Voltage output high from rail	TLV3012 ⁽²⁾	I _{OUT} = −5 mA		90		200	mV
	Short-circuit current	TLV3012 ⁽²⁾	I _{OUT} = 5 mA		See Typical Characteristics			
Voltage Reference								
V _{OUT}	Output voltage				1.208	1.242	1.276	V
	Initial accuracy				±1%			
dV _{OUT} /dT	Temperature drift		−55°C ≤ T _A ≤ 125°C		40		100	ppm/°C
dV _{OUT} /dI _{LOAD}	Load regulation	Sourcing	0 mA < I _{SOURCE} ≤ 0.5 mA		0.36		1	mV/mA
		Sinking	0 mA < I _{SINK} ≤ 0.5 mA		6.6			
I _{LOAD}	Output current				0.5			mA
dV _{OUT} /dV _{IN}	Line regulation		1.8 V ≤ V _{IN} ≤ 5.5 V		10		100	μV/V
Noise								
	Reference voltage noise		f = 0.1 Hz to 10 Hz		0.2			mV _{PP}
Power Supply								
V _S	Specified voltage				1.8		5.5	V
	Operating voltage range				1.8		5.5	V
I _O	Quiescent current		V _S = 5 V, V _O = High		2.8		5	μA

(1) t_r dependent on R_{PULLUP} and C_{LOAD} .

(2) Product Preview

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature						
Operating range			-55		125	°C
Storage range			-65		150	°C
Thermal resistance	SOT23-6			200		°C/W

TYPICAL CHARACTERISTICS

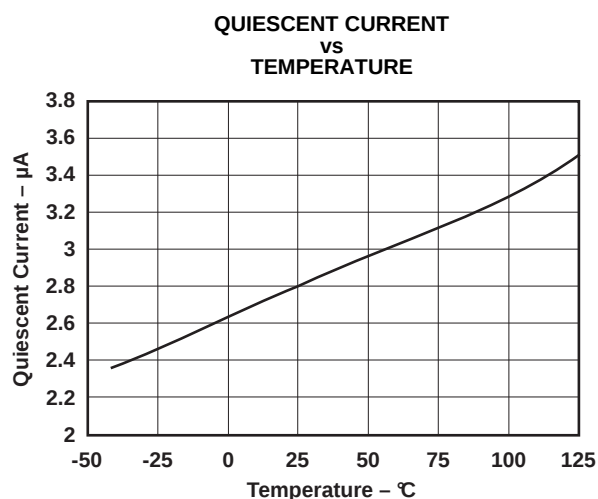


Figure 1.

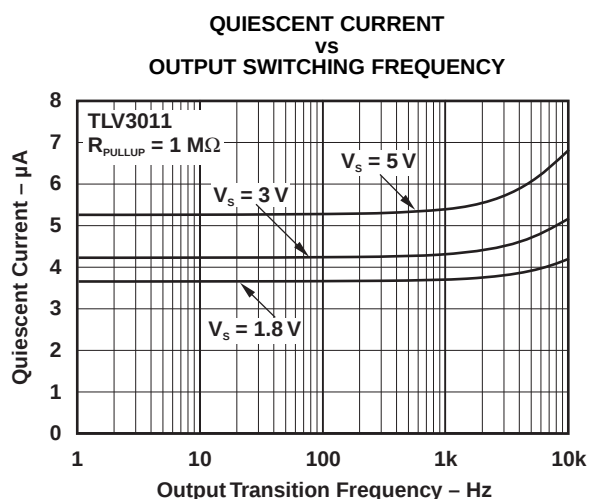


Figure 2.

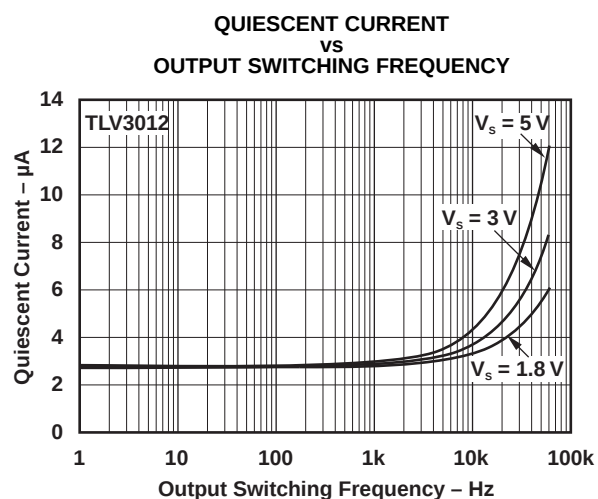


Figure 3.

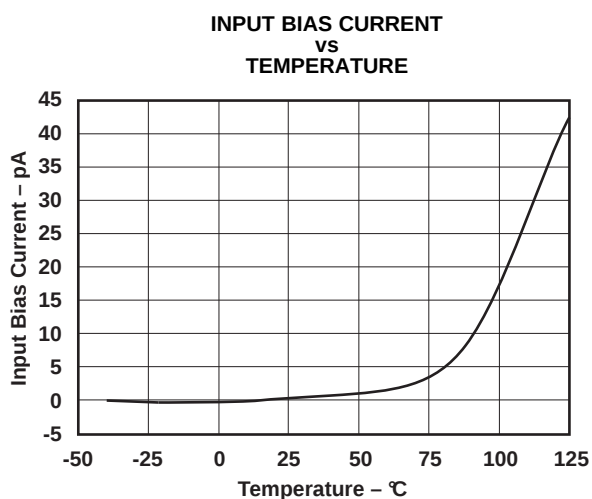


Figure 4.

TYPICAL CHARACTERISTICS (continued)

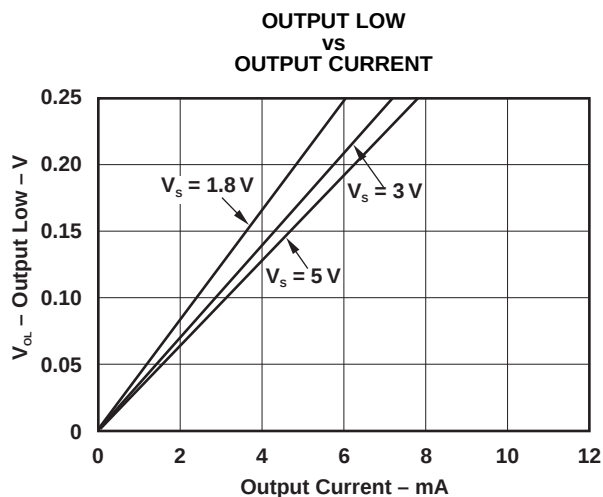


Figure 5.

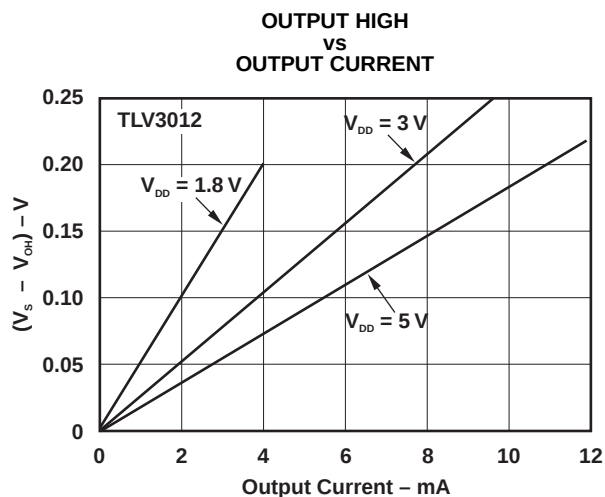


Figure 6.

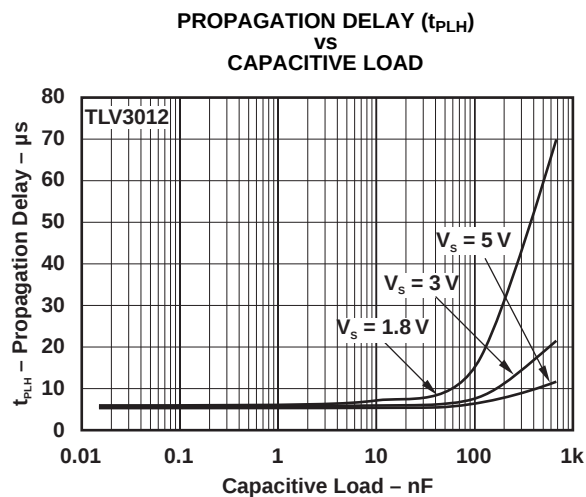


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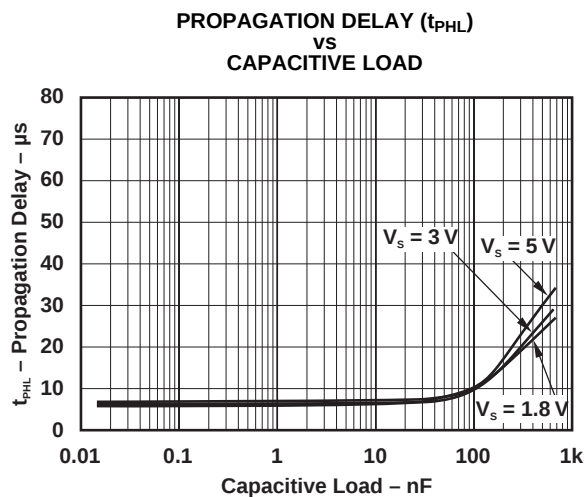


Figure 8.

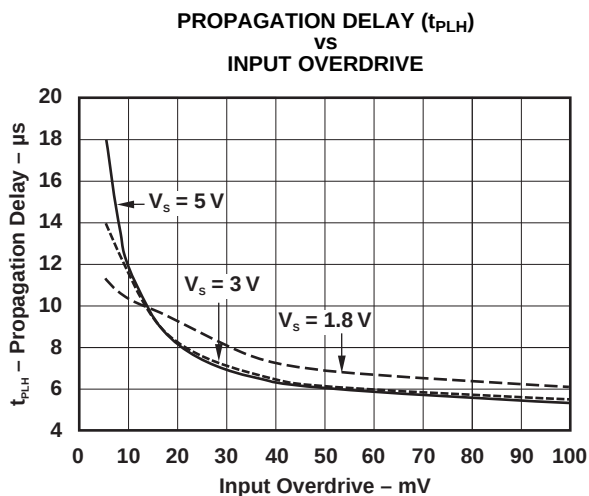


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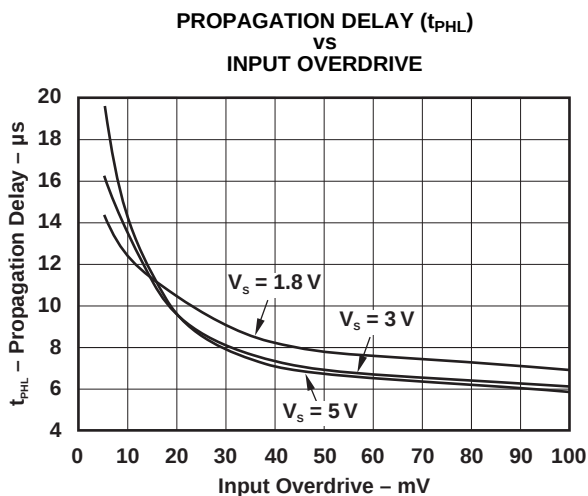


Figure 10.

TYPICAL CHARACTERISTICS (continued)

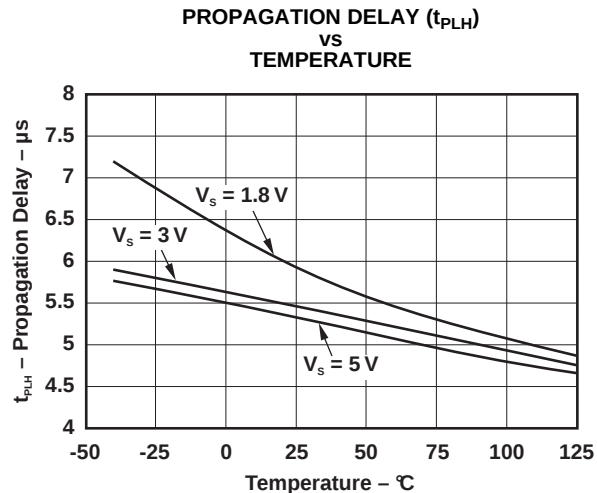


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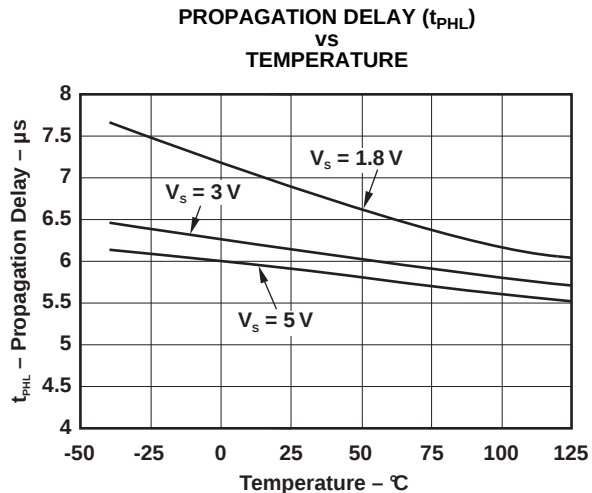


Figure 12.

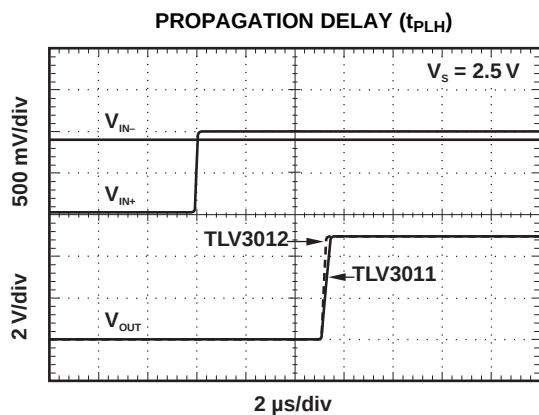


Figure 13.

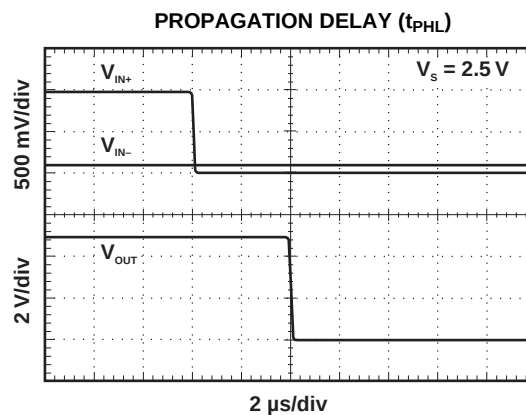


Figure 14.

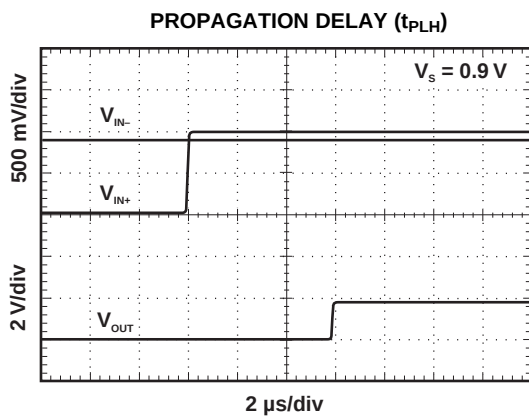


Figure 15.

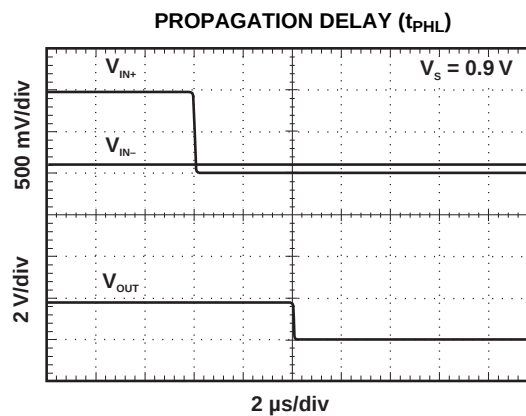


Figure 16.

TYPICAL CHARACTERISTICS (continued)

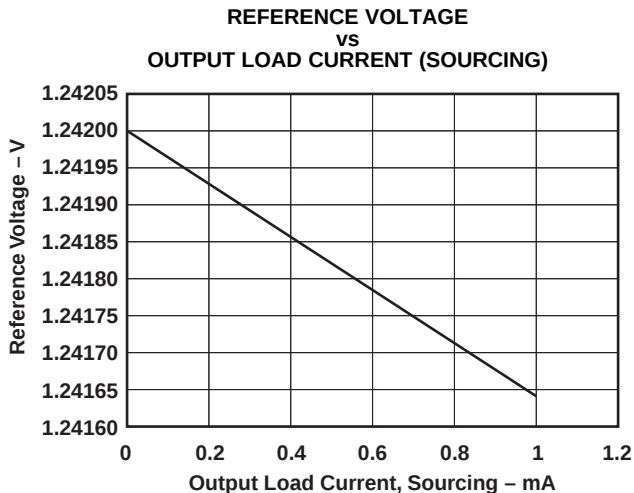


Figure 17.

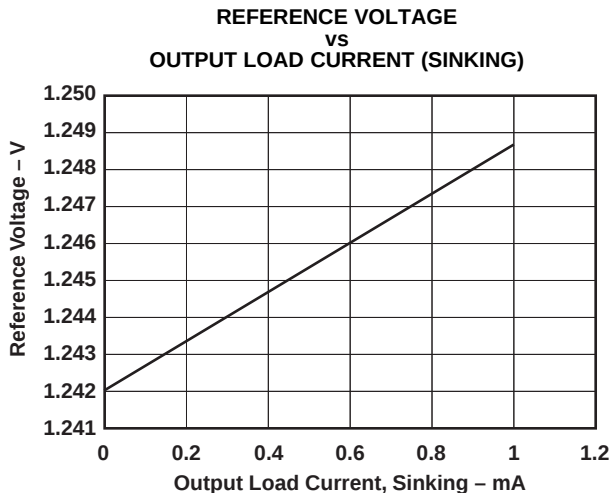


Figure 18.

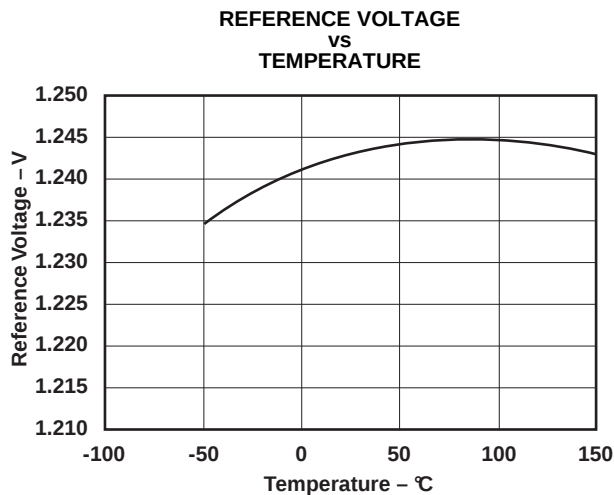


Figure 19.

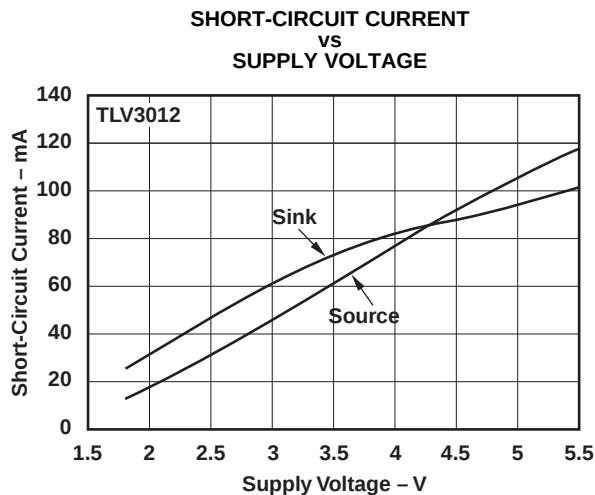


Figure 20.

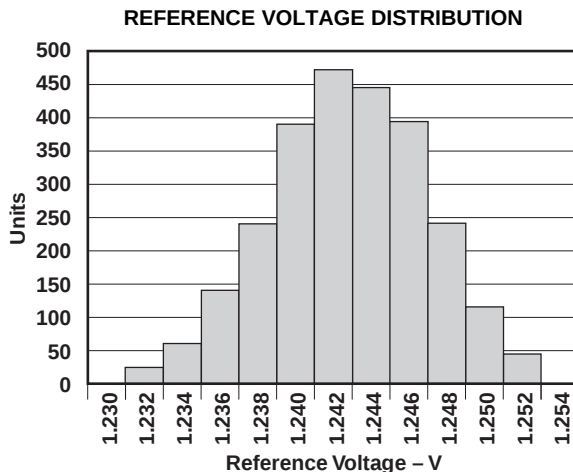


Figure 21.

APPLICATION INFORMATION

The TLV3011 is a low-power, open-drain comparator with on-chip 1.242-V series reference. The open-drain output allows multiple devices to be driven by a single pullup resistor to accomplish an OR function, making the TLV3011 useful for logic applications.

The TLV3012 comparator with on-chip 1.242-V series reference has a push-pull output stage optimal for reduced power budget applications and features no shoot-through current.

A typical supply current of 2.8 μA and small packaging combine with 1.8-V supply requirements to make the TLV3011 and TLV3012 optimal for battery and portable designs.

Board Layout

Typical connections for the TLV3011 and TLV3012 are shown in Figure 22. The TLV3011 is an open-drain output device. A pullup resistor must be connected between the comparator output and supply to enable operation.

To minimize supply noise, power supplies should be capacitively decoupled by a 0.01- μF ceramic capacitor in parallel with a 1- μF electrolytic capacitor. Comparators are sensitive to input noise and precautions such as proper grounding (use of ground plane), supply bypassing, and guarding of high-impedance nodes minimize the effects of noise and help to ensure specified performance.

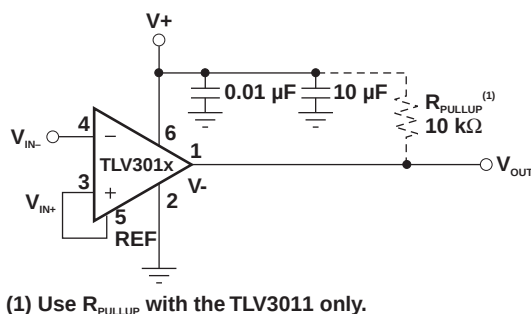


Figure 22. Basic Connections of the TLV3011 and TLV3012

Open-Drain Output (TLV3011)

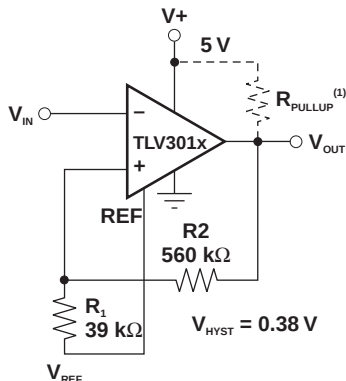
The open-drain output of the TLV3011 is useful in logic applications. The value of the pullup resistor and supply voltage used affects current consumption due to additional current drawn when the output is in a low state. This effect can be seen in Figure 3.

External Hysteresis

Comparator inputs have no noise immunity within the range of specified offset voltage (± 12 mV). For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV3011 and TLV3012 is ± 0.5 mV. To prevent multiple switching within the comparator threshold of the TLV3011 or TLV3012, external hysteresis may be added by connecting a small amount of feedback to the positive input. Figure 23 shows a typical topology used to introduce hysteresis, described by this equation:

$$V_{\text{HYST}} = \frac{V_+ \times R_1}{R_1 + R_2}$$

APPLICATION INFORMATION (continued)



(1) Use R_{PULLUP} with the TLV3011 only.

Figure 23. Adding Hysteresis

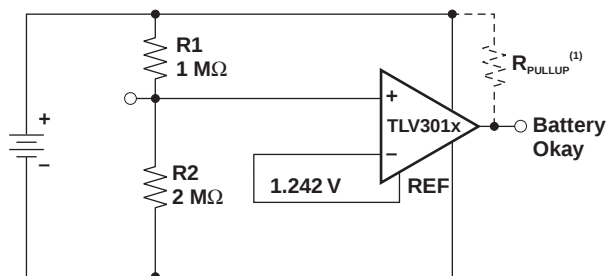
V_{HYST} sets the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

Applications

Battery-Level Detect

The low power consumption and 1.8-V supply voltage of the TLV3011 make it an excellent candidate for battery-powered applications. Figure 24 shows the TLV3011 configured as a low battery level detector for a 3-V battery.

$$\text{Battery Okay trip voltage} = 1.242 \frac{R_1 + R_2}{R_2}$$



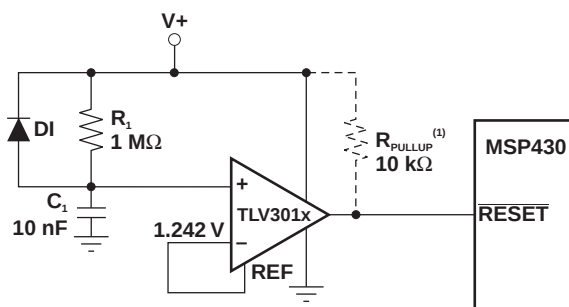
When the battery voltage drops below 1.9 V, the Battery Okay output goes low.

(1) Use R_{PULLUP} with the TLV3011 only.

Figure 24. TLV3011 Configured as Low Battery Level Detector

APPLICATION INFORMATION (continued)**Power-On Reset**

The reset circuit shown in [Figure 25](#) provides a time-delayed release of reset to the MSP430 microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by the internal voltage reference. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state, releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit does not increase current consumption, because no current flows through the RC circuit after the supply has stabilized.



(1) Use R_{PULLUP} with the TLV3011 only.

Figure 25. TLV3011 or TLV3012 Configured as Power-Up Reset Circuit for the MSP430

The reset delay needed depends on the power-up characteristics of the system power supply. R_1 and C_1 are selected to allow enough time for the power supply to stabilize. D_1 provides rapid reset if power is lost. In this example, the $R_1 \times C_1$ time constant is 10 ms.

Relaxation Oscillator

The TLV3012 can be configured as a relaxation oscillator to provide a simple and inexpensive clock output (see [Figure 26](#)). The capacitor is charged at a rate of $T = 0.69RC$ and discharges at a rate of $0.69RC$. Therefore, the period is $T = 1.38RC$. R_1 may be a different value than R_2 .

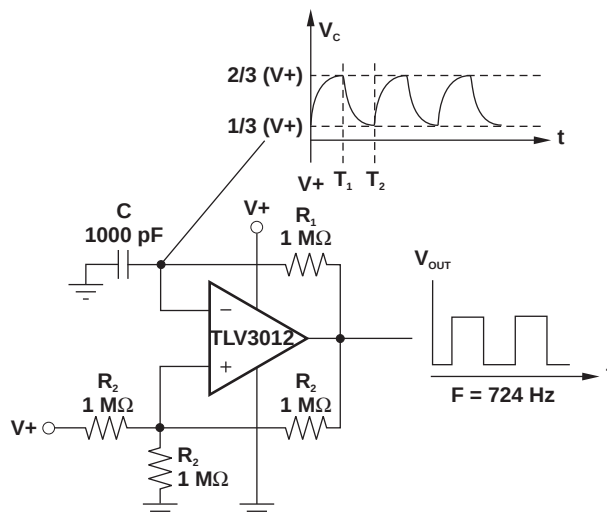


Figure 26. TLV3012 Configured as Relaxation Oscillator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3011AMDBVREP	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTV	Samples
V62/07604-01XE	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	BTV	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV3011-EP :

- Catalog: [TLV3011](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3011AMDBVREP	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

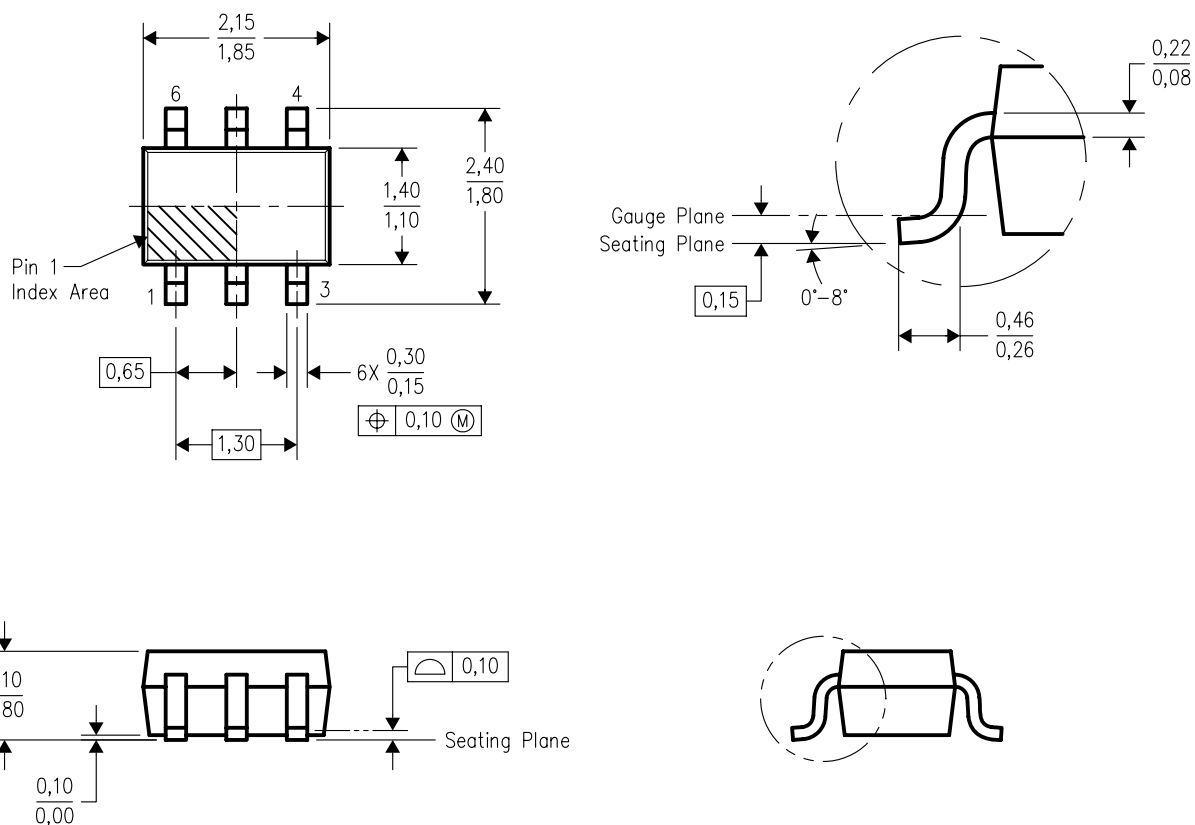


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3011AMDBVREP	SOT-23	DBV	6	3000	203.0	203.0	35.0

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

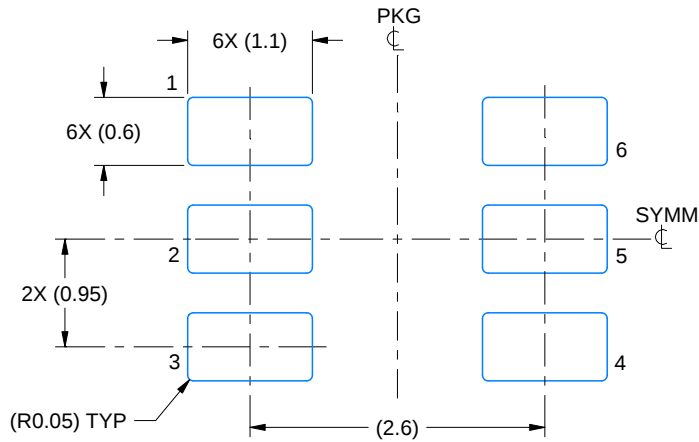
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

EXAMPLE BOARD LAYOUT

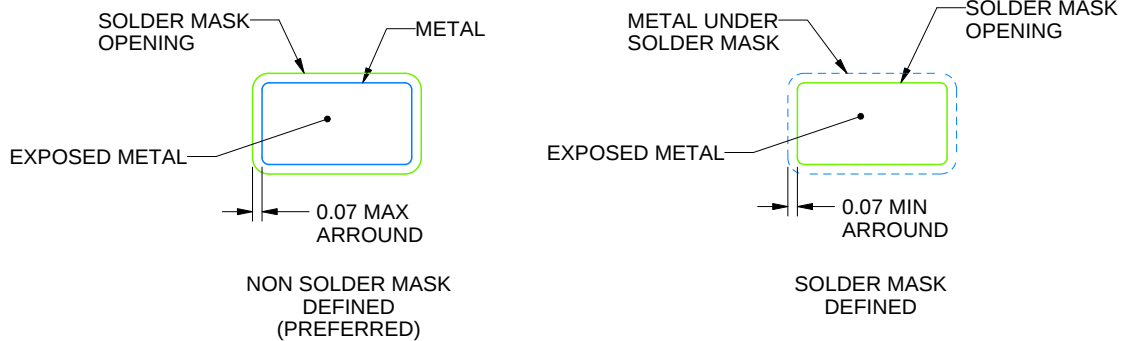
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

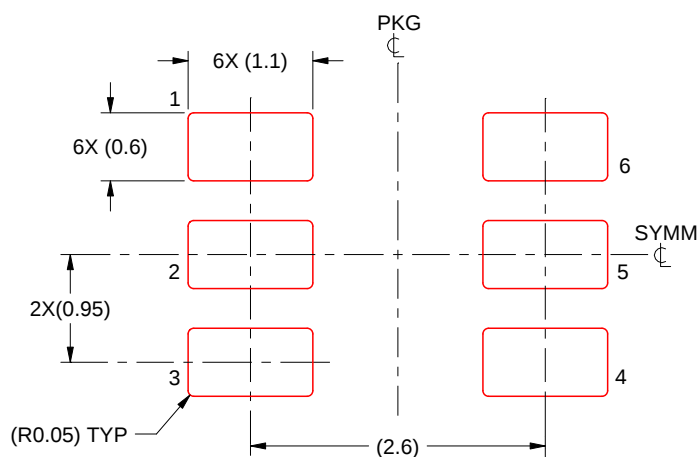
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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