Differential Two-Wire Hall Effect Sensor-IC for Wheel Speed Applications with Direction Detection

TLE4942-1C in PG-SSO2-4

Sensors

Never stop thinking.

Edition 2010-02-25

Published by
Infineon Technologies AG
81726 München, Germany

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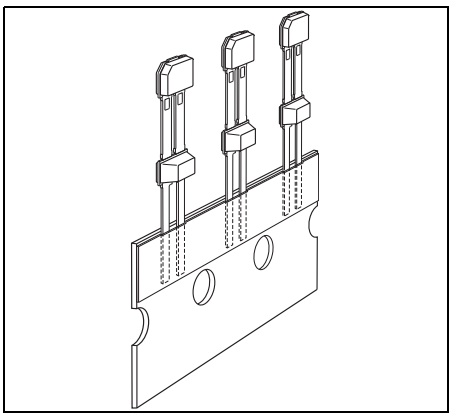
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Differential Two-Wire Hall Effect Sensor IC in PG-SSO2-4

TLE4942-1C

Features



- Two-wire PWM current interface
- Detection of rotation direction
- Airgap diagnosis
- Assembly position diagnosis
- Dynamic self-calibration principle
- Single chip solution
- No external components needed
- High sensitivity
- South and north pole pre-induction possible
- High resistance to piezo effects
- Large operating air-gaps
- Wide operating temperature range
- TLE4942-1C: 1.8 nF overmolded capacitor

Type	Marking	Ordering Code	Package
TLE4942-1C	42C1R4	SP000710676	PG-SSO-2-4

The Hall Effect sensor IC TLE4942-1C is designed to provide information about rotational speed, direction of rotation, assembly position and limit airgap to modern vehicle dynamics control systems and ABS. The output has been designed as a two wire current interface based on a Pulse Width Modulation principle. The sensor operates without external components and combines a fast power-up time with a low cut-off frequency. Excellent accuracy and sensitivity is specified for harsh automotive requirements as a wide temperature range, high ESD robustness and high EMC resilience. State-of-the-art BiCMOS technology is used for monolithic integration of the active sensor areas and the signal conditioning.

Finally, the optimized piezo compensation and the integrated dynamic offset compensation enable easy manufacturing and elimination of magnet offsets. The TLE4942-1C is additionally provided with an overmolded 1.8 nF capacitor for improved EMI performance.

Pin Configuration
(top view)

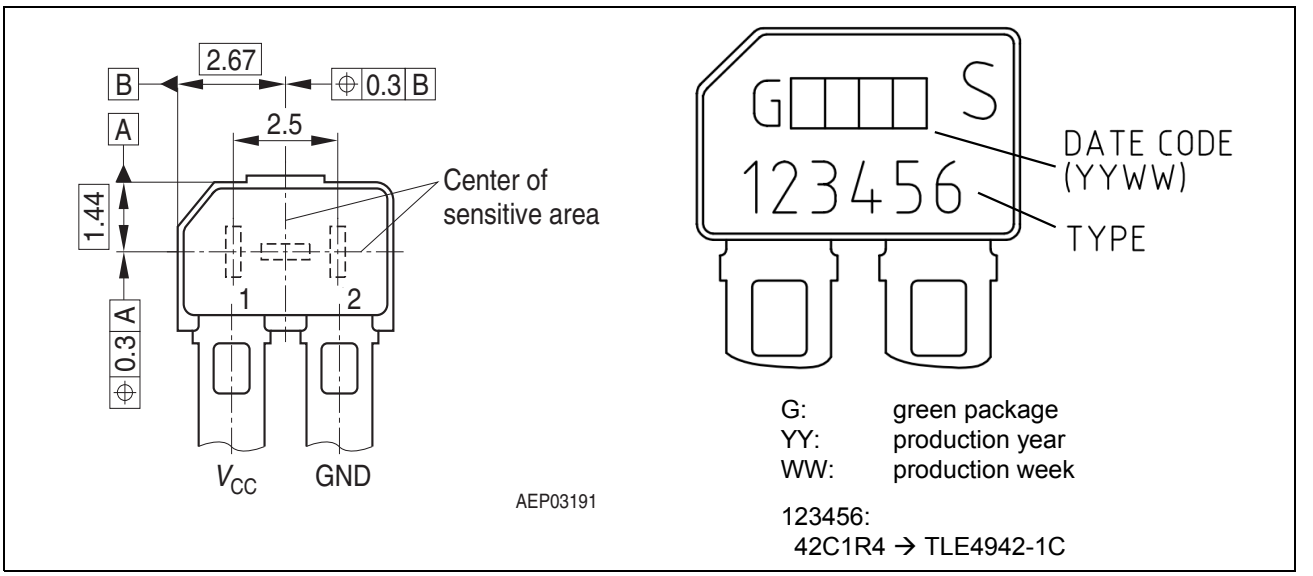


Figure 1

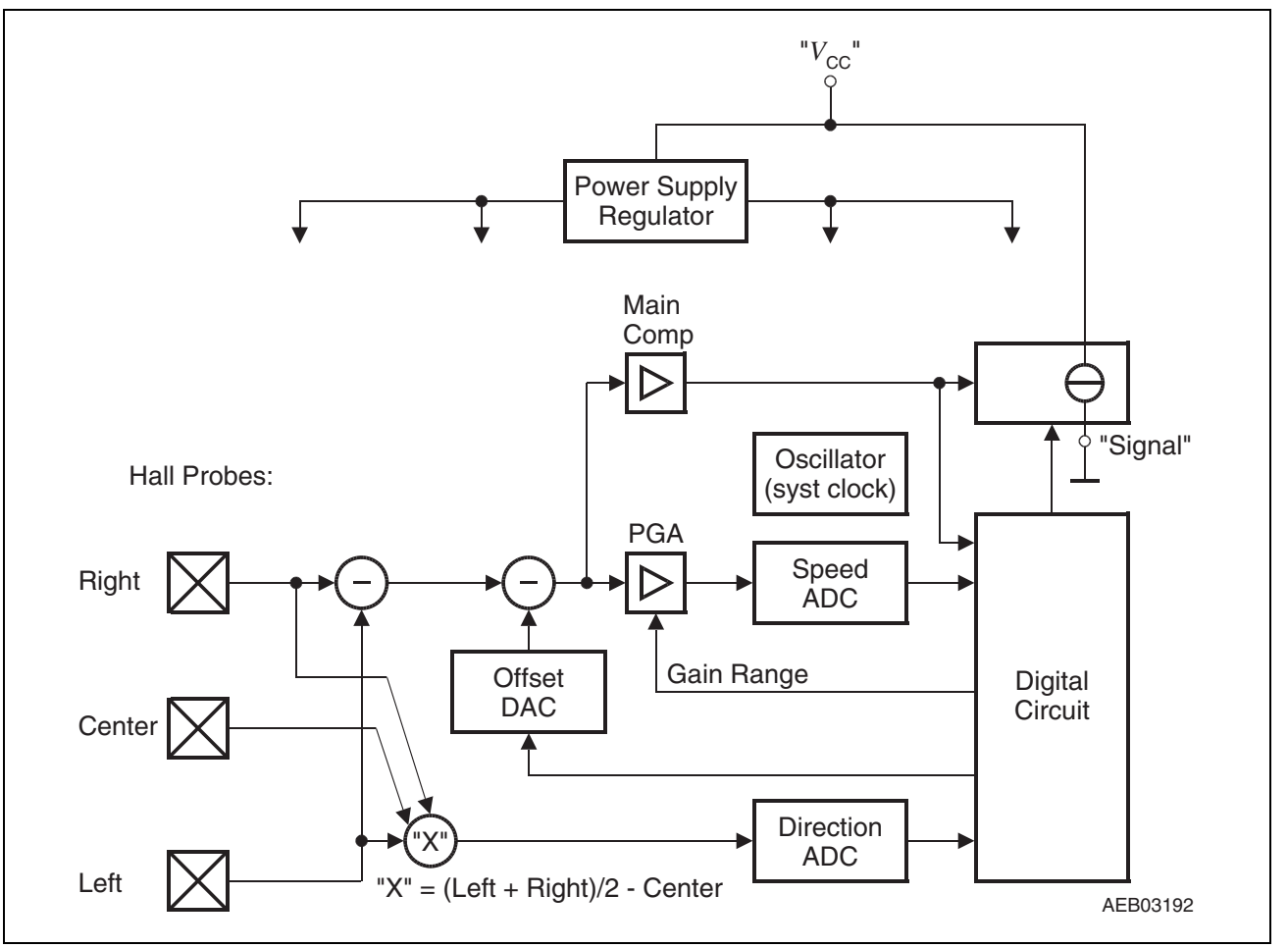


Figure 2 Block Diagram

Functional Description

The differential Hall Effect IC detects the motion of ferromagnetic or permanent magnet structures by measuring the differential flux density of the magnetic field. To detect the motion of ferromagnetic objects the magnetic field must be provided by a backbiasing permanent magnet. Either the South or North pole of the magnet can be attached to the rear, unmarked side of the IC package.

Magnetic offsets of up to ± 20 mT and mechanical offsets are cancelled out through a self-calibration algorithm. Only a few transitions are necessary for the self-calibration procedure. After the initial self-calibration sequence switching occurs when the input signal crosses the arithmetic mean of its max. and min. values (e.g. zero-crossing for sinusoidal signals).

The ON and OFF state of the IC are indicated by ***High*** and ***Low*** current consumption. Each zero crossing of the magnetic input signal triggers an output pulse.

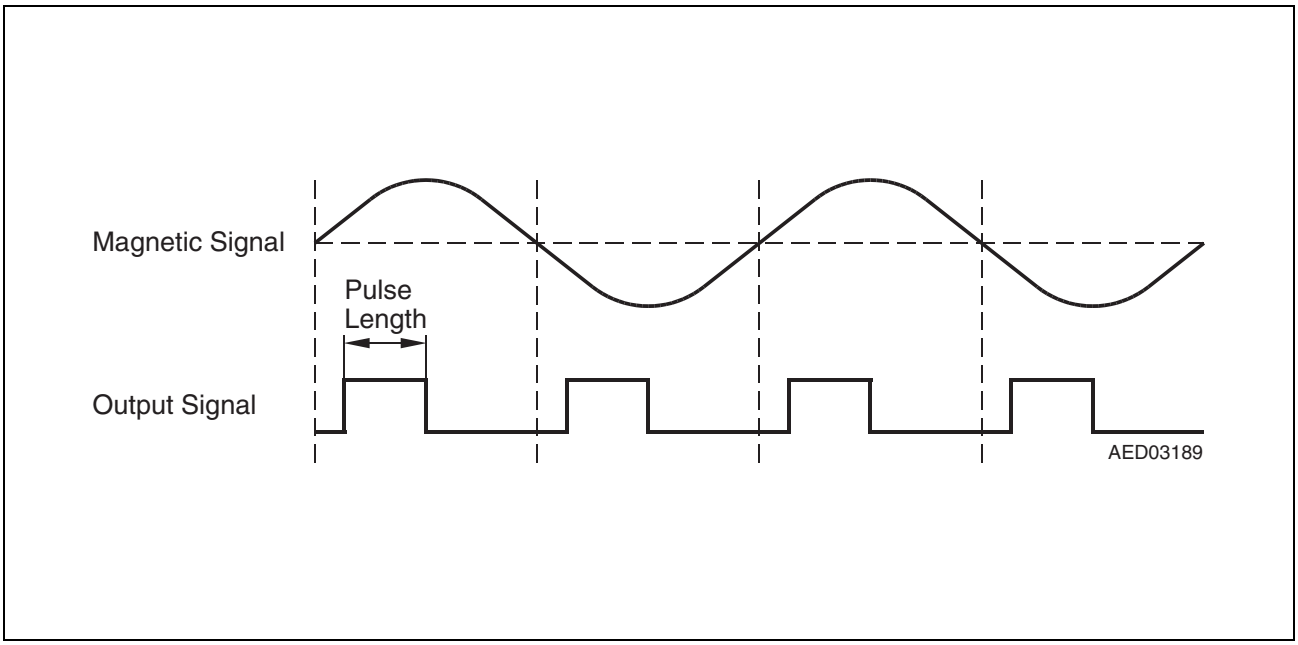


Figure 3 Zero-Crossing Principle and Corresponding Output Pulses

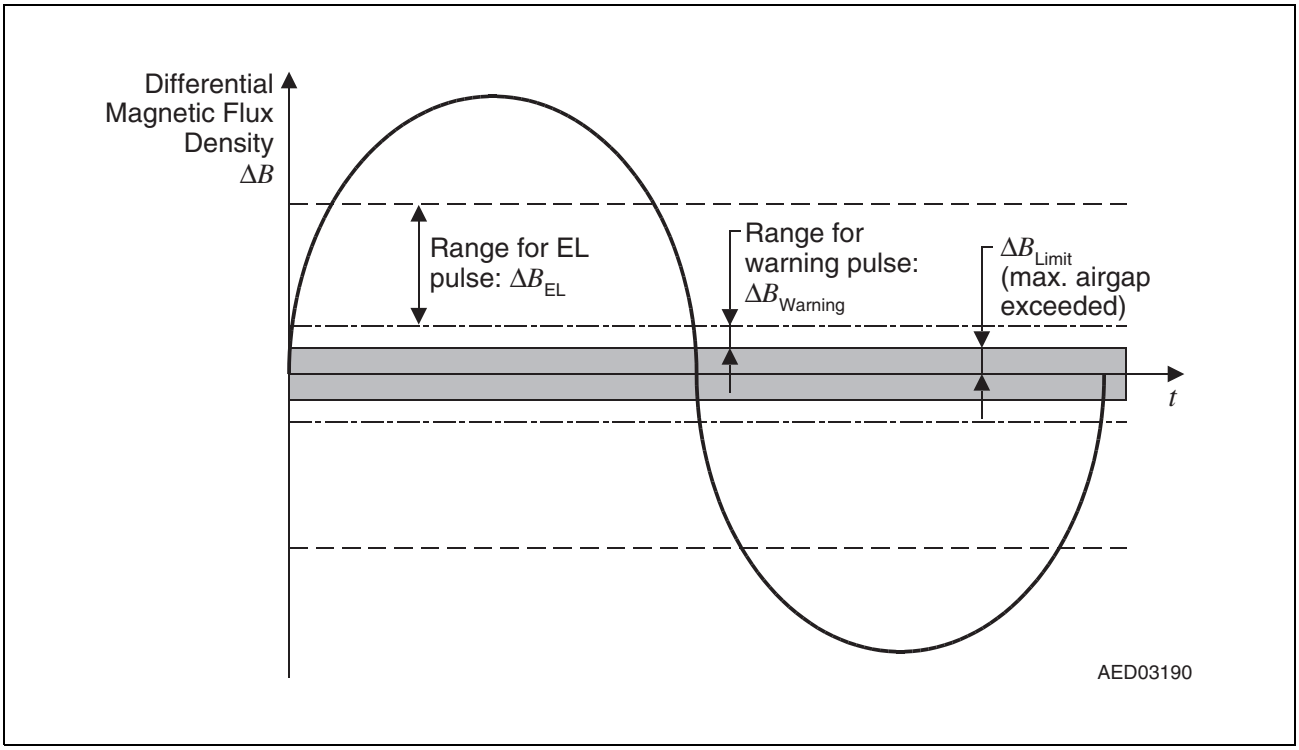


Figure 4 Definition of Differential Magnetic Flux Density Ranges

In addition to the speed signal, the following information is provided by varying the length of the output pulses in **Figure 3** (PWM modulation):

Airgap Warning range = **Warning**

Warning information is issued in the output pulse length when the magnetic field is below a critical value (e. g. the airgap between the Hall Effect IC and the target wheel exceeds a critical value). The device works with reduced functionality. Warning information is given only in calibrated mode.

Assembly position range = **EL**

EL information is issued in the output pulse length when the magnetic field is below a predefined value (the airgap between the Hall Effect IC and the target wheel exceeds a predefined value). The device works with full functionality.

Direction of rotation right = **DR-R**

DR-R information is issued in the output pulse length when the target wheel in front of the Hall Effect IC moves from the pin GND to the pin V_{CC}.

Direction of rotation left = **DR-L**

DR-L information is issued in the output pulse length when the target wheel in front of the Hall Effect IC moves from the pin V_{CC} to the pin GND. At sufficient magnetic field the direction information will be corrected already during uncalibrated mode after 2 pulses.

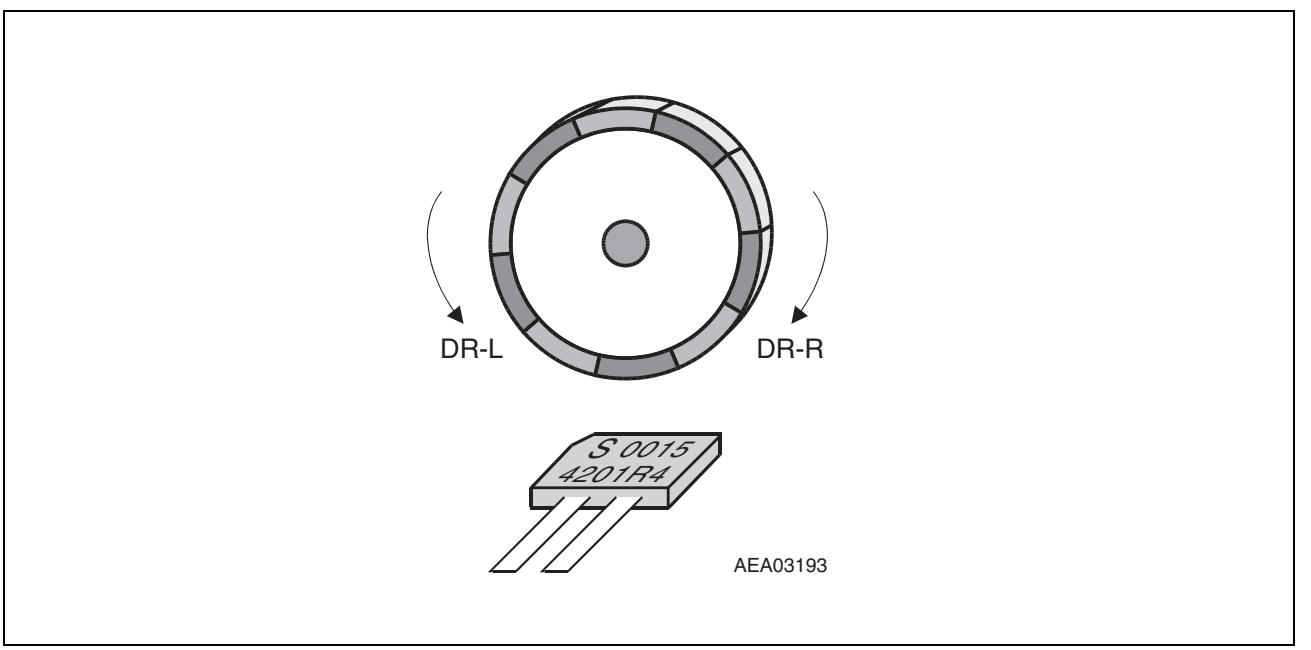


Figure 5 Definition of Rotation Direction

Circuit Description

The circuit is supplied internally by a voltage regulator. An on-chip oscillator serves as a clock generator for the DSP and the output encoder.

Speed Signal Circuitry

TLE4942-1C speed signal path comprises of a pair of Hall Effect probes, separated from each other by 2.5 mm, a differential amplifier including noise limiting low-pass filter, and a comparator triggering a switched current output stage. An offset cancellation feedback loop is provided through a signal-tracking A/D converter, a digital signal processor (DSP), and an offset cancellation D/A converter.

During the power-up phase the output is disabled (low state).

Uncalibrated Mode

Occasionally a short initial offset settling time $t_{d,input}$ might delay the detection of the input signal (the sensor is “blind”). This happens at power on or when a stop pulse is issued.

The magnetic input signal is tracked by the speed ADC and monitored within the digital circuit. For detection of a magnetic edge the signal transient needs to exceed a threshold (digital noise constant, $\Delta \hat{B}_{\text{Limit, early startup}}$). Only the first edge is suppressed internally. With the second detected edge pulses are issued at the output. When the signal slope is identified as a rising edge (or falling edge), a comparator is triggered. The comparator is triggered again as soon as a falling edge (or rising edge respectively) is detected (and vice versa). The minimum and maximum values of the input signal are extracted and their corresponding arithmetic mean value is calculated. The offset of this mean value is determined and fed into the offset cancellation DAC.

Between the startup of the magnetic input signal and the time when its second extreme is reached, the PGA (programmable gain amplifier) will switch to its appropriate position. This value is determined by the signal amplitude and initial offset value. The digital noise constant value is increased, leading to a change in phase shift between magnetic input signal and output signal. After that consecutive output pulses should have a nominal delay of about 180°.

Transition to Calibrated Mode

In the calibrated mode the phase shift between input and output signal is no longer determined by the ratio between digital noise constant and signal amplitude. Therefore a sudden change in the phase shift may occur during the transition from uncalibrated to calibrated mode.

Calibrated Mode

During the uncalibrated mode the offset value is calculated by the peak detection algorithm. In running mode (calibrated mode) the offset correction algorithm of the DSP

is switched into a low-jitter mode, thereby avoiding oscillation of the offset DAC LSB. Switching occurs at zero-crossover of the differential magnetic signal. It is only affected by the small residual offset of the comparator and by the propagation delay time of the signal path, which is mainly determined by the noise limiting filter. Signals which are below a predefined threshold ΔB_{Limit} are not detected. This prevents unwanted switching.

The comparator also detects whether the signal amplitude exceeds $\Delta B_{\text{Warning}}$ or ΔB_{EL}. This information is fed into the DSP and the output encoder. The pulse length of the High output current is generated according to the rotational speed, the direction of rotation and the magnetic field strength.

Direction Signal Circuitry

The differential signal between a third Hall probe and the mean of the differential Hall probe pair is obtained from the direction input amplifier. This signal is digitized by the direction ADC and fed into the DSP circuitry. There, the phase of the signal referring to the speed signal is analyzed and the direction information is forwarded to the output encoder.

Additional Notes

Typically the phase error due to PGA-transition reduces the error caused by switching the mode from uncalibrated to calibrated.

In very rare cases a further PGA switching can occur during the calibration process. It can take place when the signal is extremely close to a PGA switching threshold. This additional switching might delay the transition to calibrated mode by two more pulses. The probability of this case is mainly depending on variations of magnetic amplitude under real automotive conditions (see Appendix B)

The direction detection feature is also active in the uncalibrated mode but only at substantial magnetic signal. The correct direction information is worst case available after the first two output pulses in calibrated mode. Regarding the rare case mentioned before combined with other initial conditions this may lead to a worst case of 9 pulses before correct direction information is guaranteed.

Package Information

Pure tin covering (green lead plating) is used. Leadframe material is Wieland K62 (UNS: C18090) and contains CuSn1CrNiTi. Product is ROHS compliant and may contain a data matrix code on the rear side of the package.

Table 1 Absolute Maximum Ratings
T_j = – 40°C to 150°C, 4.5 V ≤ V_{CC} ≤ 16.5 V

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	– 0.3	–	V	T_j < 80°C
		–	16.5		T_j = 170°C
		–	20		T_j = 150°C
		–	22		t = 10 × 5 min
		–	24		t = 10 × 5 min, $R_M \geq 75\ \Omega$ included in V_{CC}
		–	27		t = 400 ms, $R_M \geq 75\ \Omega$ included in V_{CC}
Reverse polarity current	I_{rev}	–	200	mA	External current limitation required, t < 4 h
Junction temperature	T_j	–	150	°C	5000 h, V_{CC} < 16.5 V
		–	160		2500 h, V_{CC} < 16.5 V (not additive)
		–	170		500 h, V_{CC} < 16.5 V (not additive)
		–	190		4 h, V_{CC} < 16.5 V
Active lifetime	$t_{B,active}$	10000	–	h	
Storage temperature	T_S	– 40	150	°C	
Thermal resistance PG-SSO-2-4	R_{thJA}	–	190	K/W	1)

1) Can be improved significantly by further processing like overmolding

Note: Stresses in excess of those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2 ESD Protection
Human Body Model (HBM) tests according to:
Standard EIA/JESD22-A114-B HBM (covers MIL STD 883D)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD-Protection TLE4942-1C	V_{ESD}	–	± 12	kV	R = 1.5 kΩ, C = 100 pF

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	4.5	20	V	Directly on IC leads includes not the R_M voltage drop
Supply voltage ripple	V_{AC}	–	6	Vpp	V_{CC} = 13 V 0 < f < 50 kHz
Junction temperature	T_j	– 40	150	°C	
		–	170		500 h $V_{CC} \leq$ 16.5 V, increased jitter permissible
Pre-induction	B_0	– 500	+ 500	mT	
Pre-induction offset between outer probes	$\Delta B_{stat.,l/r}$	– 20	+ 20	mT	
Pre-induction offset between mean of outer probes and center probe	$\Delta B_{stat.,m/o}$	– 20	+ 20	mT	
Differential Induction	ΔB	– 120	+ 120	mT	

Note: Within the operating range the functions given in the circuit description are fulfilled.

Table 4 Electrical Characteristics

All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified.
Typical values correspond to V_{CC} = 12 V and T_A = 25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Supply current	I_{LOW}	5.9	7	8.4	mA	
Supply current	I_{HIGH}	11.8	14	16.8	mA	
Supply current ratio	I_{HIGH} / I_{LOW}	1.9	–	–		
Output rise/fall slew rate TLE4942-1C	t_r, t_f	 8 8	 – –	 22 26	mA/µs	R_M = 75 Ω T < 125°C T < 170°C See **Figure 6**
Current ripple dI_X/dV_{CC}	I_X	–	–	90	µA/V	1)8)
Limit threshold 1 Hz < f < 2500 Hz 2500 Hz < f < 5000 Hz	ΔB_{Limit}	 0.35 –	 0.8 –	 1.5 1.6	mT	2)
Airgap warning threshold 1 Hz < f < 2500 Hz 2500 Hz < f < 5000 Hz	$\Delta B_{Warning}$	 0.9 –	 1.6 –	 2.6 2.8	mT	2)
Limit - Airgap warning threshold ratio	$\Delta B_{Warning}$ / ΔB_{Limit}	1.3	2	2.7		
Assembly position threshold	ΔB_{EL}	5.2	7.2	9.6	mT	2) At room temp
Magnetic differential field change necessary to detect magnetic edge in uncalibrated mode $\Delta \hat{B}_{Limit, early startup}$	$\Delta \hat{B}_{Limit, early startup}$	– 0.7	– 1.76	– 3.3	 mT	First detected magnetic edge is suppressed (nonvalid)
Initial calibration delay time	$t_{d,input}$	255	300	345	µs	Additional to n_{start}
Magnetic edges suppressed until output switching	$n_{DZ\text{-}start}$	–	–	1 3)	magn. edges	After power on and stop pulse
Magnetic edges required for offset calibration 3)	$n_{DZ\text{-}calibration}$	–	–	6 3)	magn. edges	7th edge correct 4)

Table 4 Electrical Characteristics (cont'd)
All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified.
Typical values correspond to V_{CC} = 12 V and T_A = 25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
in rare cases (see Appendix B)	$n_{DZ\text{-}calibration\text{-}rare}$	–	–	8	edges	
Number of pulses in uncalibrated mode	$n_{DZ\text{-}Startup}$	–	–	5	pulses	
in rare cases (see Appendix B)	$n_{DZ\text{-}Startup\text{-}rare}$	–	–	7	pulses	
Number of pulses with invalid direction information $\Delta B < \Delta B_{EL}$ $\Delta B > \Delta B_{EL}$	$n_{DR\text{-}Startup}$	 – –	 – –	 7 2 [5)]	pulses	After $n_{DR\text{-}Startup}$ pulses + 1 the direction information is correct
Number of pulses with invalid assembly bit information	$n_{EL\text{-}Startup}$	–	–	7	pulses	After $n_{EL\text{-}Startup}$ pulses + 1 the assembly bit information is correct
Number of pulses where the airgap warning information is suppressed	$n_{LR\text{-}Startup}$	–	–	5	pulses	LR information is provided only in calibrated mode
Signal behavior after undervoltage or standstill > t_{Stop} Number of magnetic edges where the first pulse in given.	$n_{DZ\text{-}Start}$	–	–	2	edges	Magnetic edge according to $\Delta\hat{B}_{Limit,\ early\ startup}$ $t_{d,input}$ has to be taken into account
Shortest time delay between pulse 0 (stop pulse) and pulse 1		293	345	397	µs	Reference rising edges, includes pre low length
Shortest time delay between wheel speed pulse 1 and 2 and all further pulses		38	45	52	µs	Falling to rising edge - identical with pre low bit length

Table 4 Electrical Characteristics (cont'd)
All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified.
Typical values correspond to V_{CC} = 12 V and T_A = 25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Phase shift change during PGA switching		0	–	80	°	
Phase shift change during transition from uncalibrated to calibrated mode	$\Delta\Phi_{switch}$	– 90	–	+ 90	°	
Frequency	f	1 2500	– –	2500 5000	Hz	6)
Frequency changes	df/dt	–	–	± 100	Hz/ms	
Duty cycle	duty	40	50	60	%	7) Measured @ΔB = 2 mT sine wave Def. **Figure 7**
Jitter, T_j < 150°C T_j < 170°C 1 Hz < f < 2500 Hz	$S_{Jit\text{-}close}$	– –	– –	± 2 ± 3	%	8) 1σ value V_{CC} = 12 V $\Delta B \geq$ 2 mT
Jitter, T_j < 150°C T_j < 170°C 2500 Hz < f < 5000 Hz	$S_{Jit\text{-}close}$	– –	– –	± 3 ± 4.5	%	8) 1σ value V_{CC} = 12 V $\Delta B \geq$ 2 mT
Jitter, T_j < 150°C T_j < 170°C 1 Hz < f < 2500 Hz	$S_{Jit\text{-}far}$	– –	– –	± 4 ± 6	%	8) 1σ value V_{CC} = 12 V 2 mT $\geq \Delta B >$ ΔB_{Limit}
Jitter, T_j < 150°C T_j < 170°C 2500 Hz < f < 5000 Hz	$S_{Jit\text{-}far}$	– –	– –	± 6 ± 9	%	8) 1σ value V_{CC} = 12 V 2 mT $\geq \Delta B >$ ΔB_{Limit}
Jitter during startup and uncalibrated mode	$S_{Jit\text{-}close}$ (1σ-value)	– –	– –	± 3 ± 4	%	8) – 40°C ≤ T_{amb} ≤ 150°C 150°C ≤ T_{amb} ≤ 170°C
	$S_{Jit\text{-}far}$ (1σ-value)	– –	– –	± 5 ± 7	%	8) – 40°C ≤ T_{amb} ≤ 150°C 150°C ≤ T_{amb} ≤ 170°C

Table 4 Electrical Characteristics (cont'd)
All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified.
Typical values correspond to V_{CC} = 12 V and T_A = 25°C

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Jitter at board net ripple	$S_{Jit\text{-}AC}$	–	–	± 2	%	[8] V_{CC} = 13 V ± 6 Vpp 0 < f < 50 kHz ΔB = 15 mT
Jitter at board net ripple in uncalibrated mode	$S_{Jit\text{-}AC}$ (1σ-value)	–	–	± 3	%	[8] V_{CC} = 13 V ± 6 Vpp 0 < f < 50 kHz ΔB = 15 mT

1) higher values occure due to R_m-C combination
2) Magnetic amplitude values, sine magnetic field, Limits refer to the 50% critera. 50% of pulses are missing or wrong. Valid in calibrated mode only.
3) The sensor requires up to n_{start} magnetic switching edges for valid speed information after power-up or after a stand still condition. During that phase the output is disabled.
4) One magnetic edge is defined as a montonic signal change of more than 3.3 mT
5) Direction signal is given already during uncalibrated mode. Assembly Bit information is only provided in calibrated mode
6) High frequency behavior not subject to production test - verified by design/characterization. Frequency above 2500 Hz may have influence on jitter performance and magnetic thresholds. DR-R pulse length will be cut off above app. 3.3 kHz Therefore direction detection may not be possible anymore at high frequency.
7) During fast offset alterations, due to the calibration algorithm, exceeding the specified duty cycle is permitted for short time periods
8) Not subject to production test- verified by design/characterization

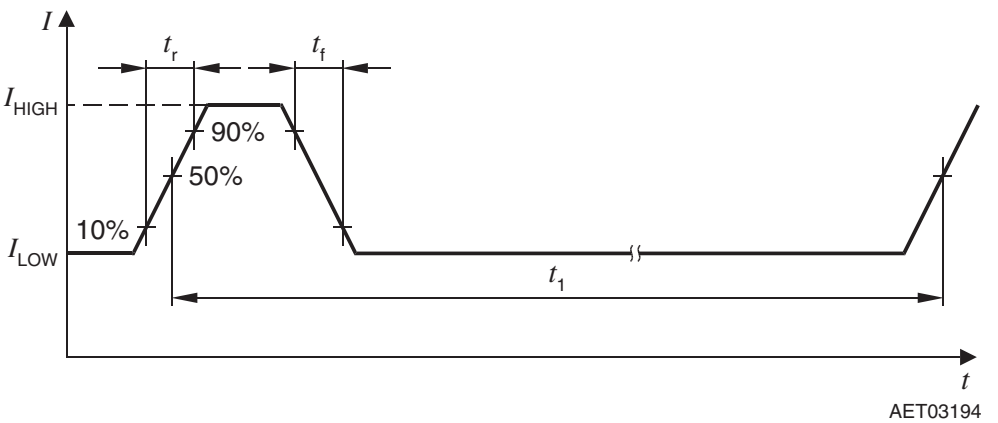


Figure 6 Definition of Rise and Fall Time

Table 5 Timing Characteristics

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Pre-low length	$t_{pre\text{-}low}$	38	45	52	µs	
Length of Warning pulse	$t_{Warning}$	38	45	52	µs	
Length of DR-L pulse	$t_{DR\text{-}L}$	76	90	104	µs	
Length of DR-R pulse	$t_{DR\text{-}R}$	153	180	207	µs	
Length of DR-L & EL pulse	$t_{DR\text{-}L\&EL}$	306	360	414	µs	
Length of DR-R & EL pulse	$t_{DR\text{-}R\&EL}$	616	720	828	µs	
Output of EL pulse, maximum frequency	f_{ELmax}	–	117	–	Hz	
Length of stand still pulse	t_{Stop}	1.232	1.44	1.656	ms	See **Figure 9**
Stand still period [1]	T_{Stop}	590	737	848	ms	See **Figure 9**

1) If no magnetic switching edge is detected for a period longer than T_{stop}, the stand still pulse is issued

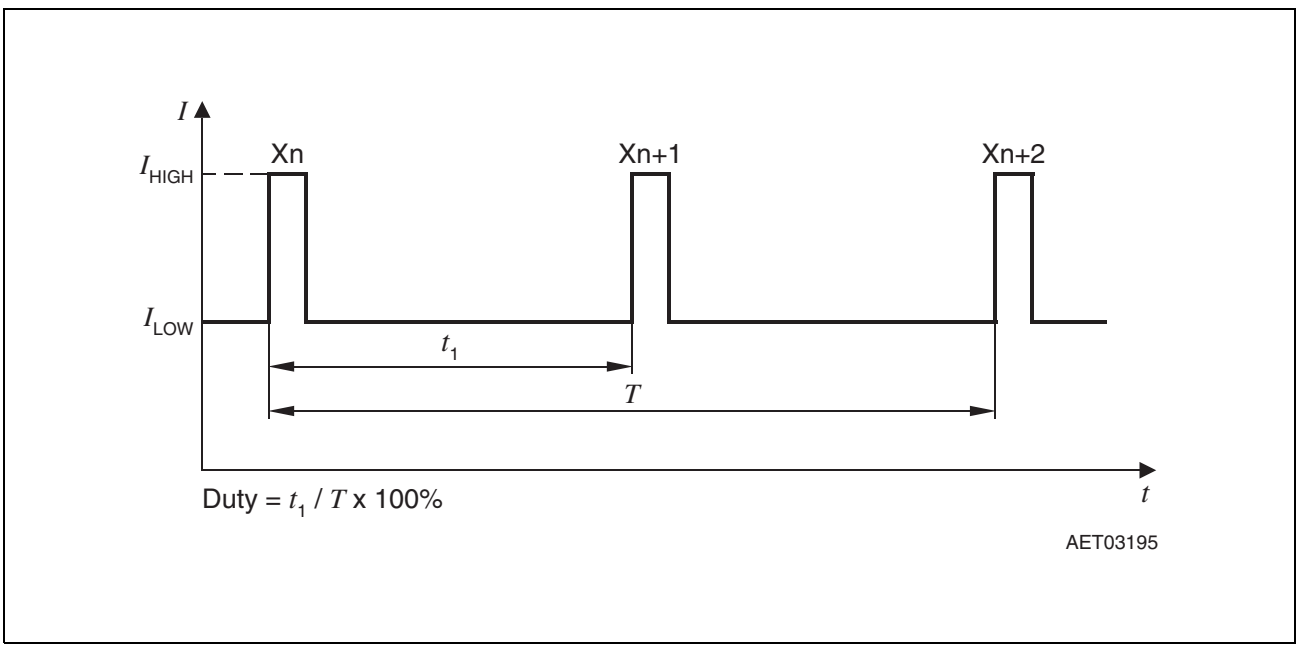


Figure 7 Definition of Duty Cycle

PWM Current Interface

Between each magnetic transition and the rising edge of the corresponding output pulse the output current is ***Low*** for $t_{pre\text{-}low}$ in order to allow reliable internal conveyance. Following the signal pulse (current is ***High***) is output.

If the magnetic differential field exceeds ΔB_{EL}, the output pulse lengths are 90 µs or 180 µs respectively, depending on the direction of rotation.

When the magnitude of the magnetic differential field is below ΔB_{EL}, the output pulse lengths are 360 µs and 720 µs respectively, depending on left or right rotation. Due to decreasing cycle times at higher frequencies, these longer pulses are only output up to frequencies of approximately 117 Hz. For higher frequencies and differential magnetic fields below ΔB_{EL}, the output pulse lengths are 90 µs or 180 µs respectively.

If the magnitude of the magnetic differential field is below $\Delta B_{Warning}$, the output pulse length is 45 µs. The warning output is dominant, this means that close to the limit airgap the direction and the assembly position information are disabled.

For magnitudes of the magnetic differential field below ΔB_{Limit}, signal is lost.

In case no magnetic differential signal is detected for a time longer than the stand still period T_{Stop}, the stop pulse is output. Typically with the first output stop pulse, the circuitry reverts to the uncalibrated mode.

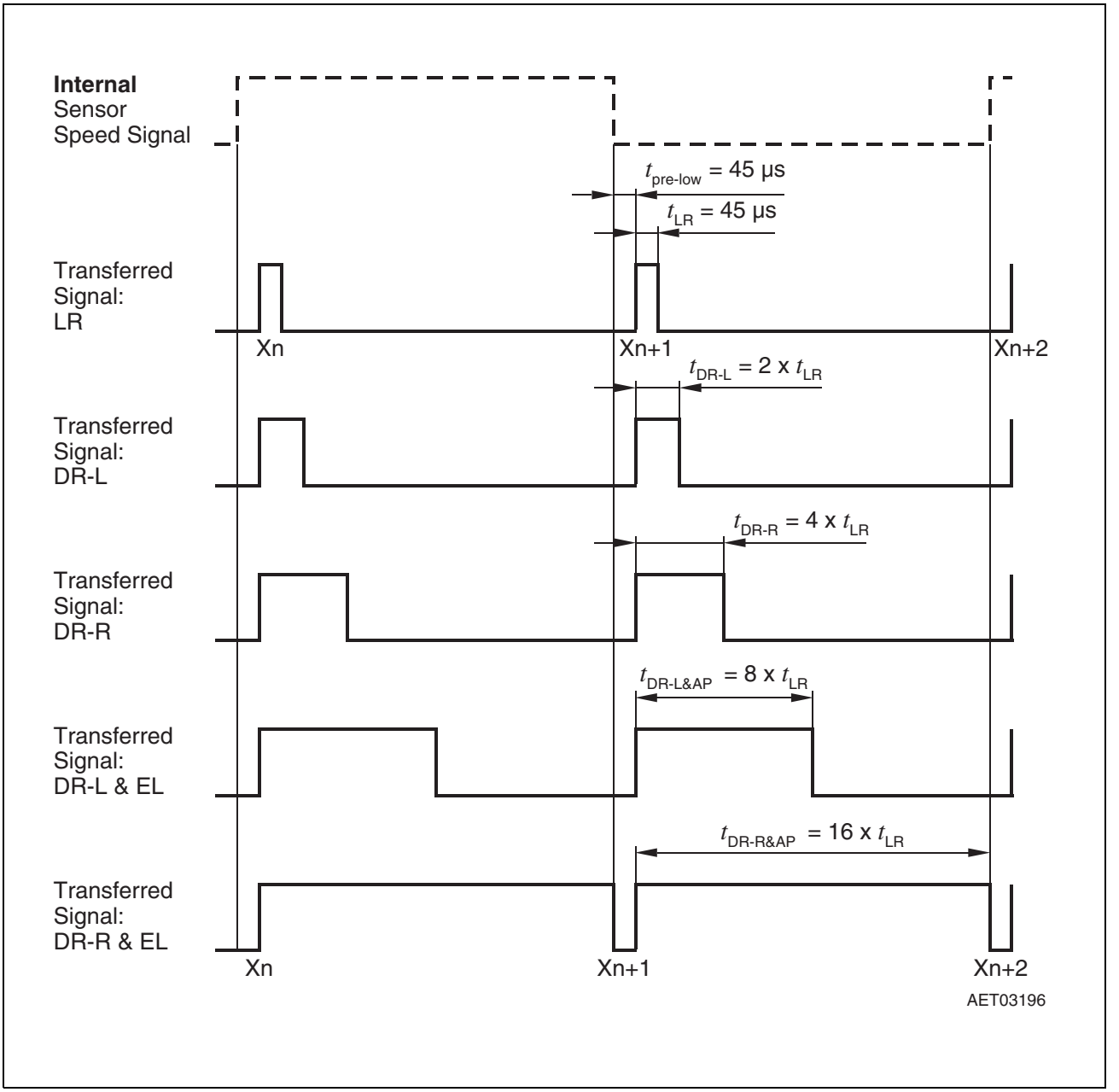


Figure 8 Definition of PWM Current Interface

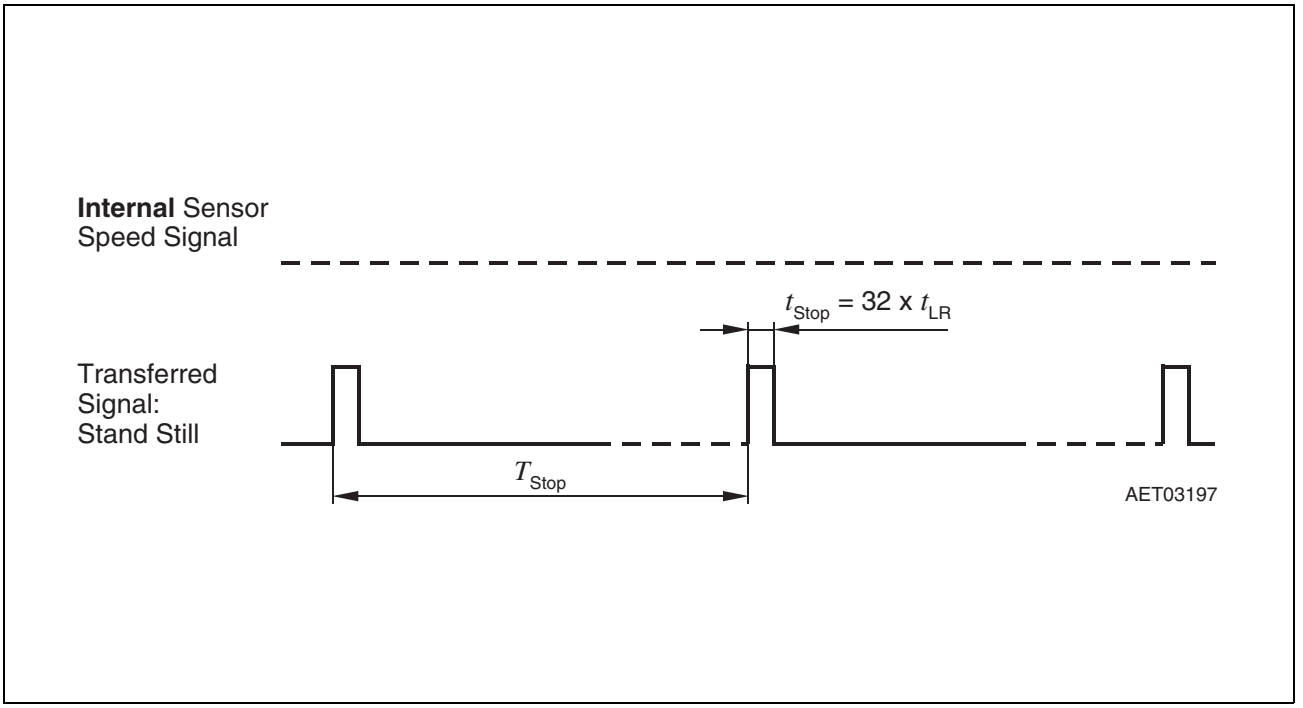


Figure 9 Definition of Stand Still Output Pulse

Duty Cycle at Fast Changing Frequencies

If the duty cycle deviates from 50%, it is possible that the present pulse length is output entirely once and cut once, within the same period, see **Figure 10**.

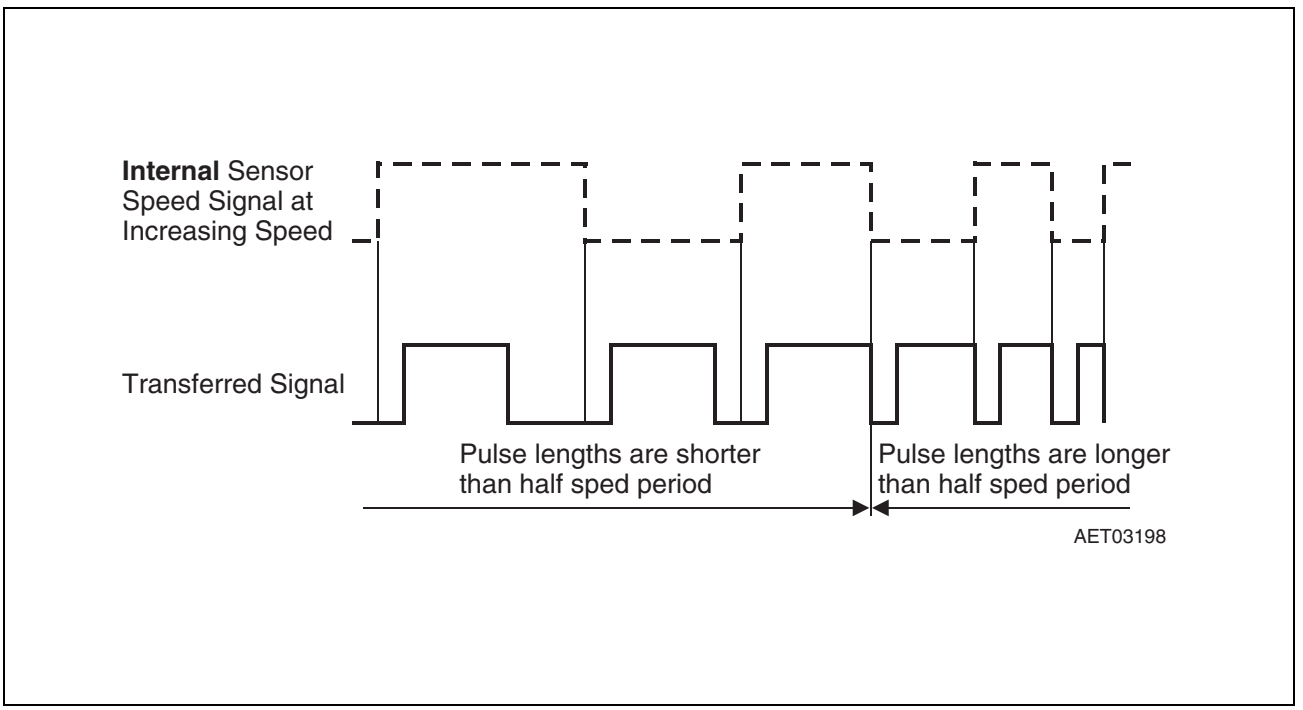


Figure 10 Deviation of Duty Cycle at Fast Changing Frequencies

Table 6 Electro Magnetic Compatibility (values depend on R_M!)

Ref. ISO 7637-1; test circuit 1;
ΔB = 2 mT (amplitude of sinus signal); V_{CC} = 13.5 V, f_B = 100 Hz; T = 25°C; $R_M \geq 75\ \Omega$

Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / – 100 V	C [1)]
Testpulse 2		IV / 100 V	C [1)]
Testpulse 3a		IV / – 150 V	A
Testpulse 3b		IV / 100 V	A
Testpulse 4		IV / – 7 V	B [2)]
Testpulse 5		IV / 86.5 [3)] V	C

1) According to 7637-1 the supply switched “OFF” for t = 200 ms
2) According to 7637-1 for test pulse 4 the test voltage shall be 12 V ± 0.2 V. Measured with R_M = 75 Ω only. Mainly the current consumption will decrease. Status C with test circuit 1.
3) Applying in the board net a suppressor diode with sufficient energy absorption capability

Note: Values are valid for all TLE4941C/42C types!

Ref. ISO 7637-3; test circuit 1;
ΔB = 2 mT (amplitude of sinus signal); V_{CC} = 13.5 V, f_B = 100 Hz; T = 25°C; $R_M \geq 75\ \Omega$

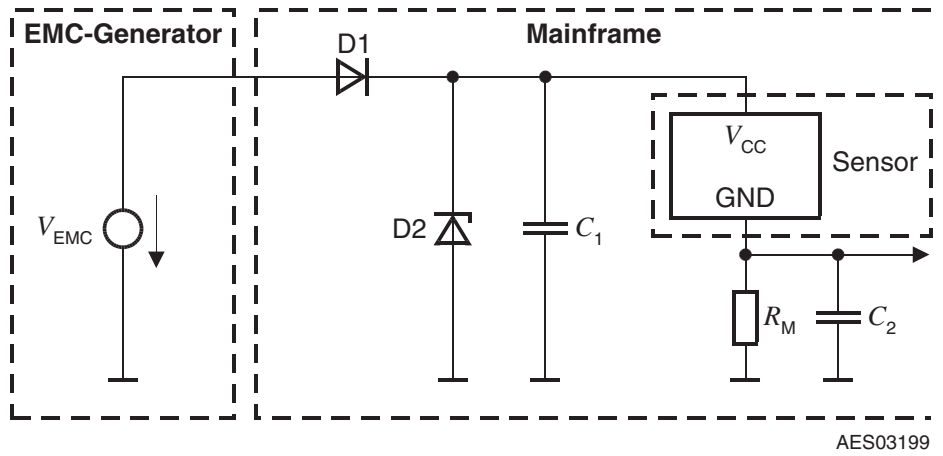
Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / – 30 V	A
Testpulse 2		IV / 30 V	A
Testpulse 3a		IV / – 60 V	A
Testpulse 3b		IV / 40 V	A

Note: Values are valid for all TLE4941C/42C types!

Ref. ISO 11452-3; test circuit 1; measured in TEM-cell
ΔB = 2 mT; V_{CC} = 13.5 V, f_B = 100 Hz; T = 25°C

Parameter	Symbol	Level/Typ	Remarks
EMC field strength	$E_{TEM\text{-}Cell}$	IV / 250 V/m	AM = 80%, f = 1 kHz

Note: Only valid for C-types!



Components: D1: 1N4007
D2: T 5Z27 1J
C_1: 10 µF / 35 V
C_2: 1 nF / 1000 V
R_M: 75 Ω / 5 W

Figure 11 Test Circuit 1

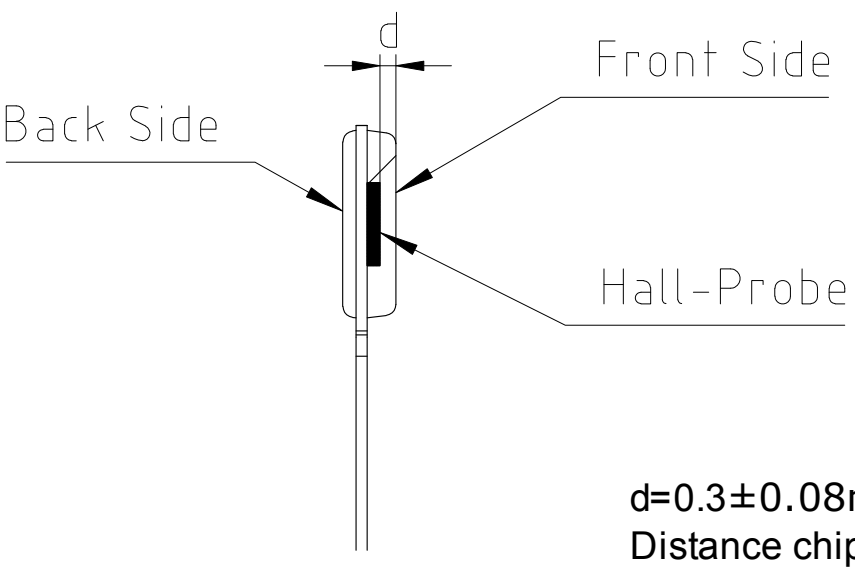
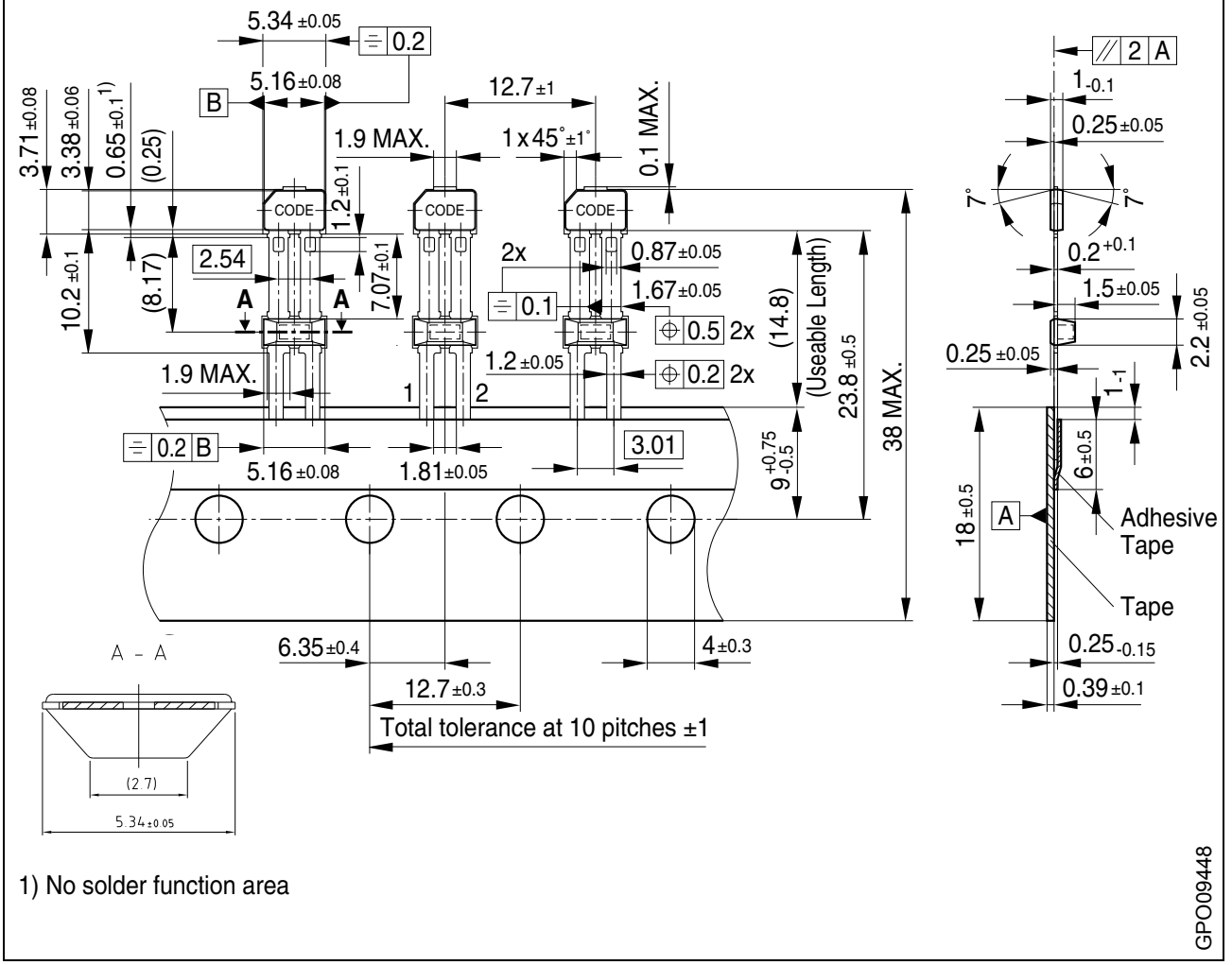


Figure 12 Distance Chip to Upper Side of IC

Package Outlines

PG-SSO-2-4
(Plastic Single Small Outline Package)



1) No solder function area

Figure 13

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

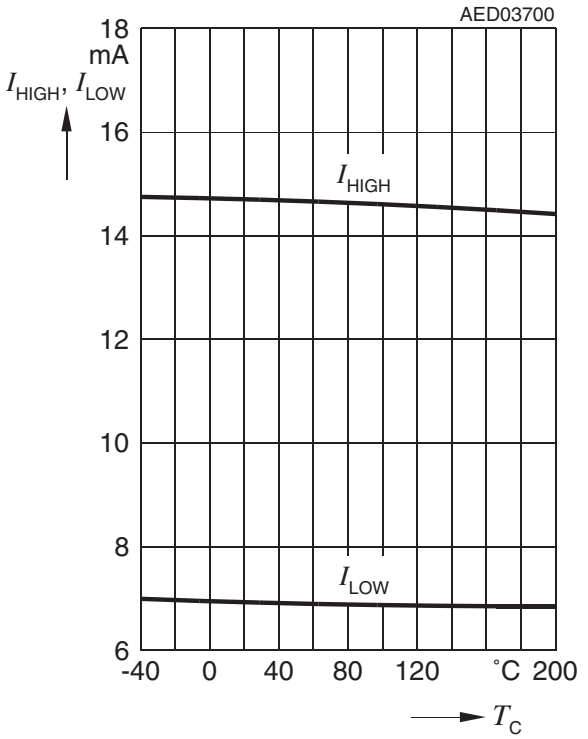
Dimensions in mm

Appendix A

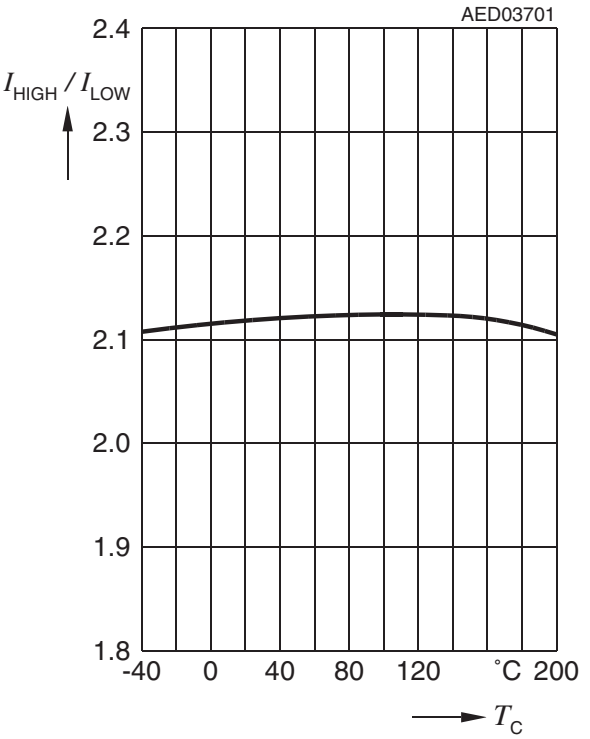
Typical Diagrams (measured performance)

T_C = $T_{case, IC}$ = approx. T_j - 5°C

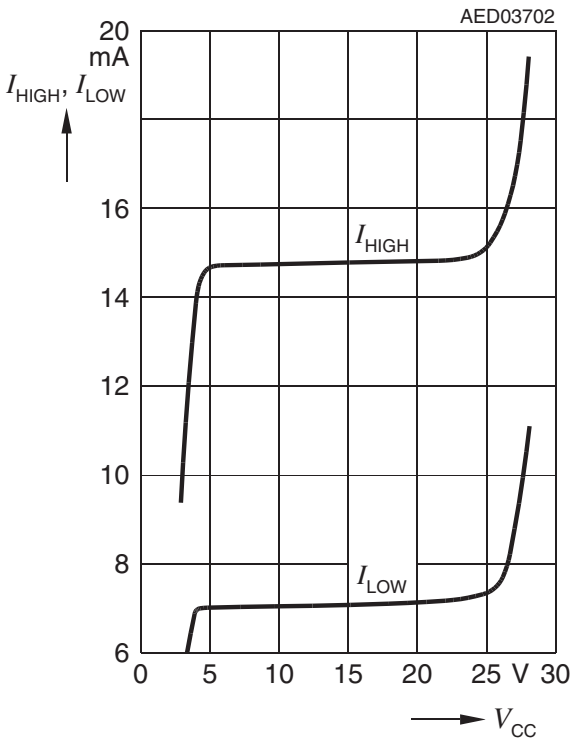
Supply Current



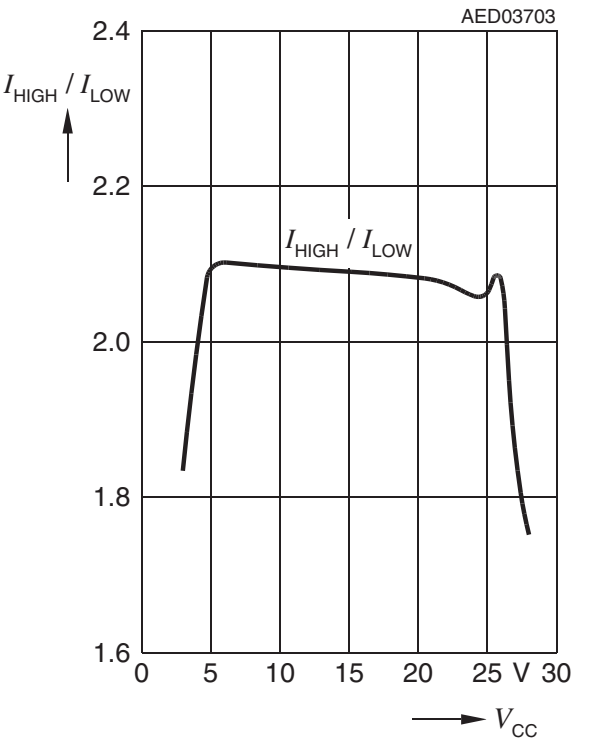
Supply Current Ratio I_{HIGH} / I_{LOW}



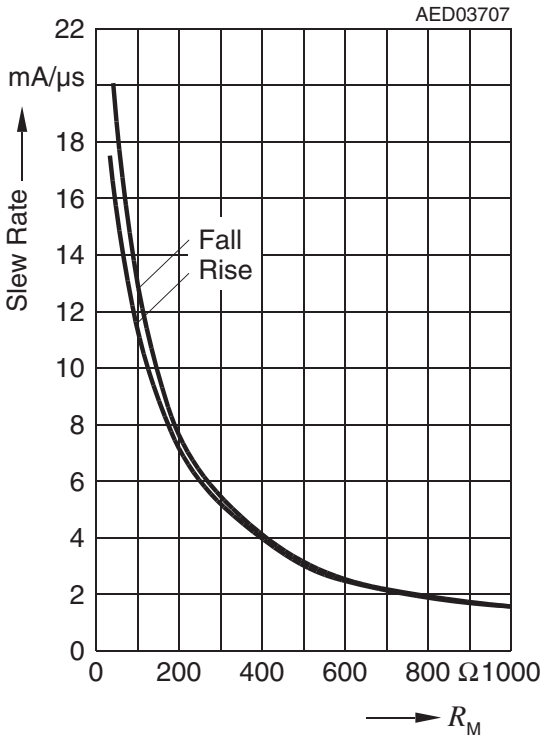
Supply Current = $f(V_{CC})$



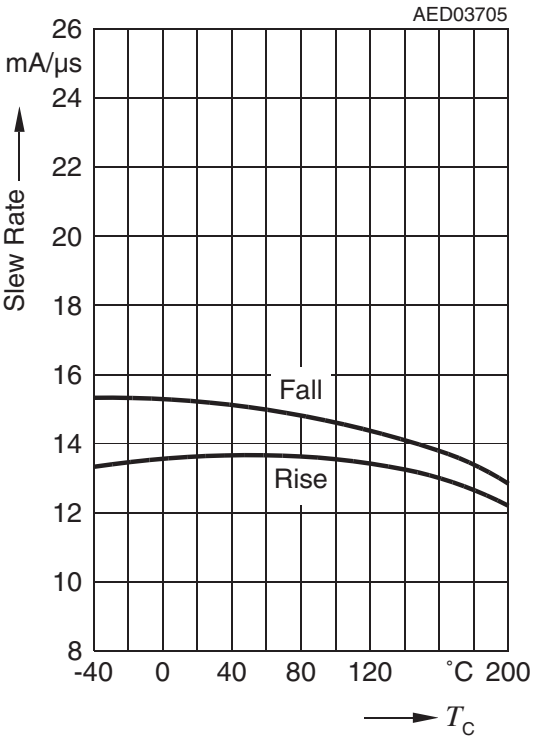
Supply Current Ratio I_{HIGH}/I_{LOW} = $f(V_{CC})$



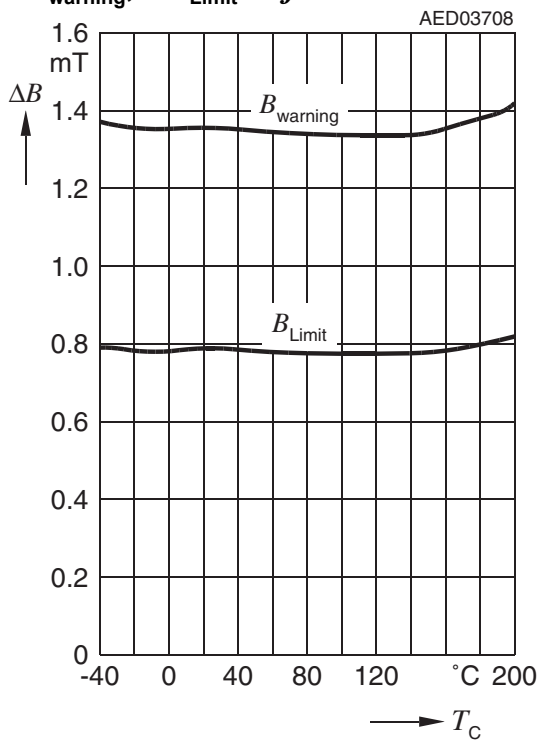
Slew Rate with C = 1.8 nF = $f(R_M)$



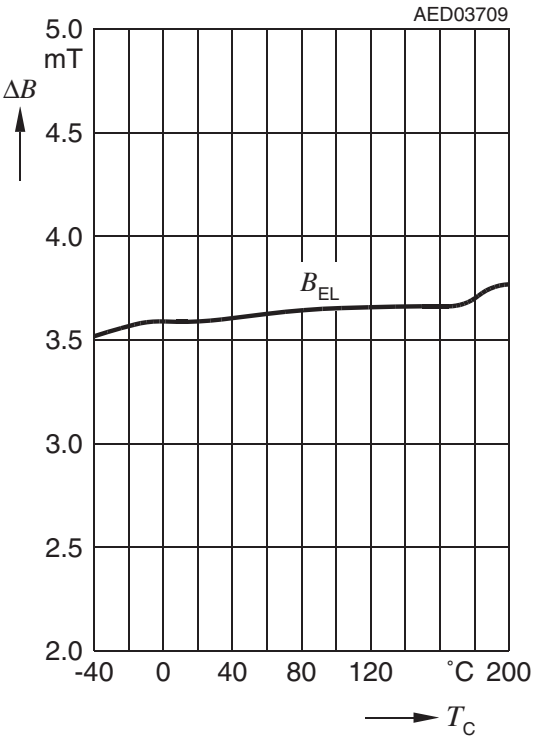
Slew Rate with C = 1.8 nF, R_M = 75 Ω



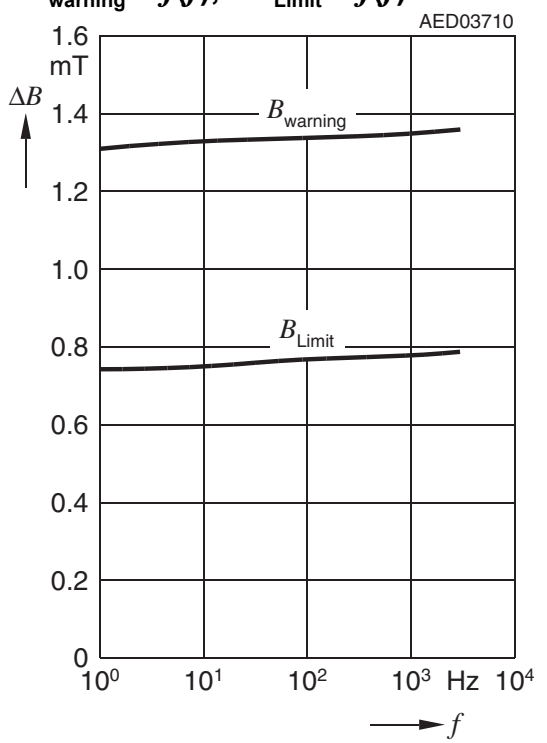
Magnetic Threshold
$\Delta B_{warning}$, ΔB_{Limit} at f = 1 kHz



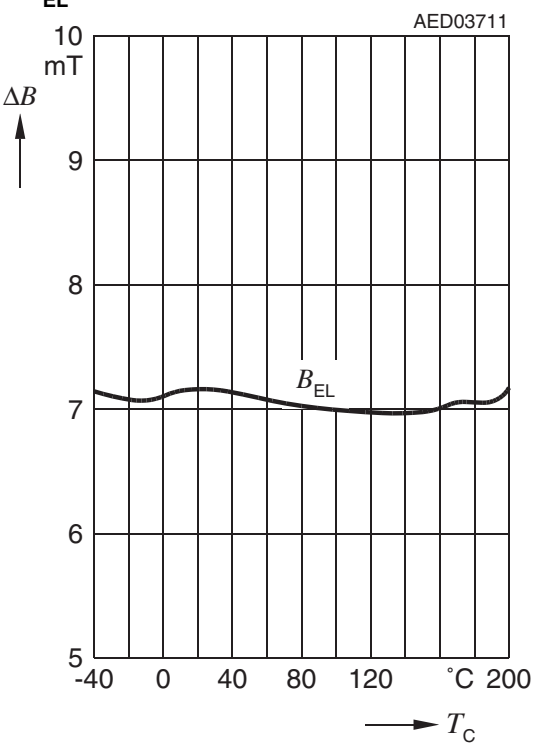
Magnetic Threshold
ΔB_{EL} 01



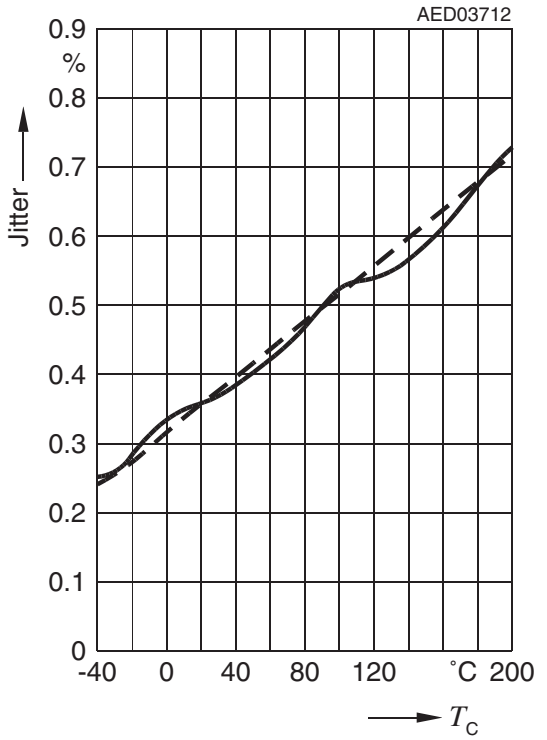
Magnetic Threshold
$\Delta B_{warning} = f(f)$, $\Delta B_{Limit} = f(f)$



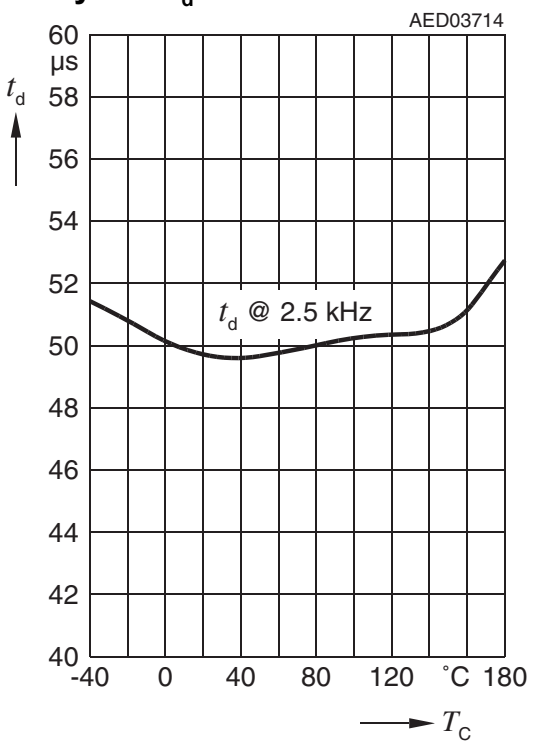
Magnetic Threshold
ΔB_{EL} 04



Jitter 1 at B = 2 mT, 1 kHz

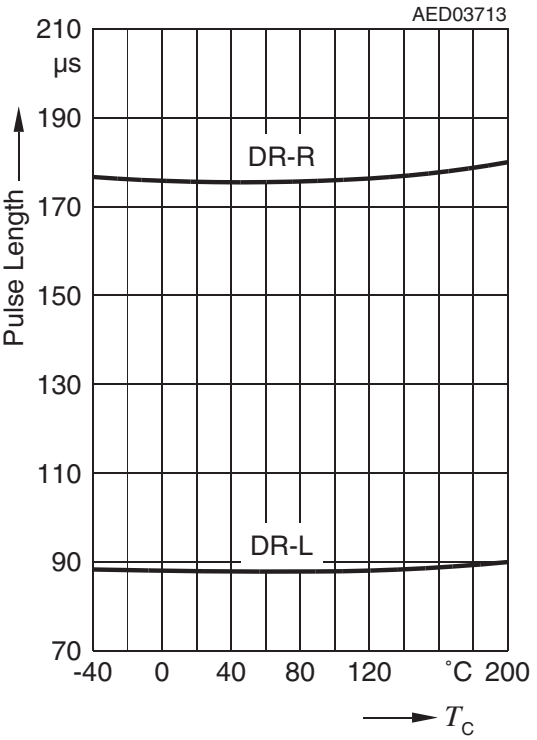


Delaytime t_d [1)]



1) t_d is the time between the zero crossing of ΔB = 2 mT sinusoidal input signal and the rising edge (50%) of the signal current.

Pulse Length of Direction Signal Left and Right (t_{DR-L}, t_{DR-R}) [2)]



2) Temp. Behaviour of Other Pulse Lengths are similar

Appendix B

Release 2.0

Occurrence of initial calibration delay time $t_{d,\ input}$

If there is no input signal (standstill), a new initial calibration is triggered each 0.7 s. This calibration has a duration $t_{d,\ input}$ of max. 300 µs. No input signal change is detected during that initial calibration time.

In normal operation (signal startup) the probability of $t_{d,\ input}$ to come into effect is:

$t_{d,\ input}$ /time frame for new calibration = 300 µs/700 ms = 0.05%.

After IC resets (e.g. after a significant undervoltage) $t_{d,\ input}$ will always come into effect.

Magnetic input signal extremely close to a PGA switching threshold during signal startup

After signal startup normally all PGA switching into the appropriate gain state happens within less than one signal period. This is included in the calculation for $n_{DZ\text{-}Startup}$. For the very rare case that the signal amplitude is extremely close to a PGA switching threshold and the full range of the following speed ADC respectively, a slight change of the signal amplitude can cause one further PGA switching. It can be caused by non-perfect magnetic signal (amplitude modulation due to tolerances of polewheel, tooth wheel or air gap variation). This additional PGA switching can result in a further delay of the calibrated output signal up to two magnetic edges leading to a worst case edges of $n_{DZ\text{-}Start\ up\ rare}$ = 8.

For a more detailed explanation please refer to the document
"TLE4941/42 Application Notes - Frequently Asked Questions".

Fast change of direction signal at small fields:

The described behaviour can happen when rotation direction is changed in t < 0.7 s

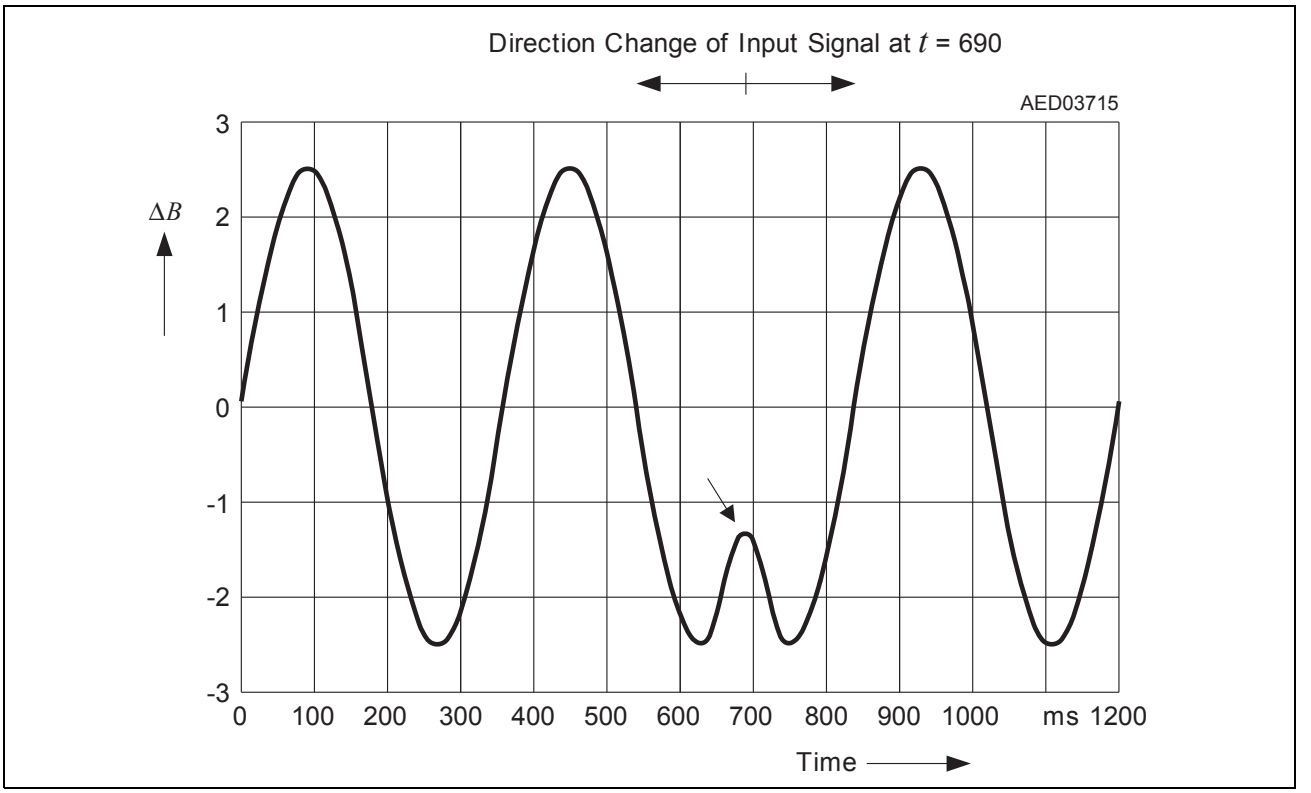


Figure 14

A local extremum (maximum or minimum) of the magnetic input signal can be caused during a reversal of rotation direction. In this case the local extremum can be detected by the IC and used for offset calibration. (E.g. the local maximum marked by an arrow in the above diagram.) Obviously the calculated offset value will be incorrect with respect to the following signal. As worst case a duty cycle up to max. 15% to 85% could occur for a few pulses. $B_{warning}$ and B_{EL} information can be incorrect during that short period. After a re-calibration, which typically takes place after 2...3 zero-crossings the offset will be correct again and hence the duty cycle, $B_{warning}$ and B_{EL} also.

As a result of "bad" duty cycle after fast direction reversal the sampling points for direction detection are at unusual signal phase angles also. At small magnetic input signals (ΔB < 1.7 x $\Delta B_{warning}$) this can lead to incorrect direction information. Duration: max. 7 pulses, in very rare cases (additional PGA transition during calibration similar to 2.) max. 9 pulses.

A local extremum close to the zero-crossing theoretically could lead to distances down to 45 µs of two consecutive output pulses at the point of direction reversal as well as a $B_{warning}$ pulse also.

Behaviour close to the magnetic thresholds $B_{warning}$, B_{Limit}, (B_{EL})

Real non-perfect magnetic signals and intrinsic thermal noise cause amplitude variations. Very close to the magnetic thresholds a mix of output pulse widths representing the referring magnetic values occur. For similar reasons pulse widths of 90, 180, 360, 720 µs can be observed occasionally for single pulses at B_{Limit}.

Behaviour close to speed v5 ($f_{EL\text{-}bit}$ = ca. 117 Hz)

Signal imperfections like duty cycle and jitter result in a mix of output pulses with and without assembly bit (EL) information. Input signal duty cycles apart from 50% increase the range where both pulse widths appear.

Dependency of direction detection on input signal pitch

The direction detection is optimized for a target wheel pitch of 5 mm where it will work down to $B_{warning}$. ($B_{warning}$ and direction detection thresholds meet at 5 mm pitch). For pitches other than 5 mm the magnetic input signal has to be increased to compensate for the inevitable signal attenuation.

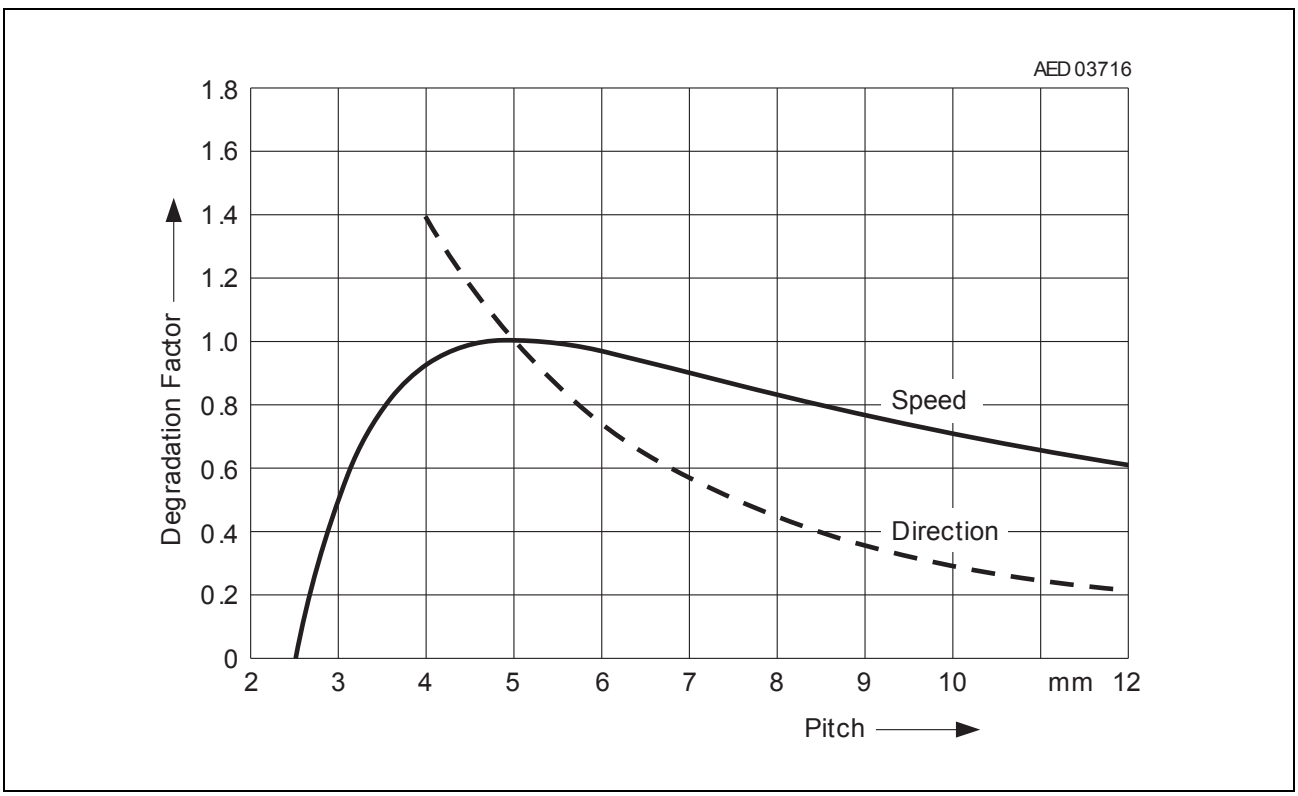


Figure 15 Degradation of speed and direction signal at sinusoidal input signals = $f_{(pitch)}$

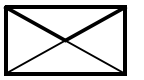
Revision History:February 2010, V4.0	
Previous Version: V3.1	
Page	Subjects (major changes since last revision)
all	Updated datasheet due to PCN No 2009-069-A

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