Freescale Semiconductor
Product Preview

Document Number: MC34830
Rev. 1.0, 9/2008

HD to SD Adjustable Bandwidth Video Buffer with DC Restore

34830

HD VIDEO BUFFER IC



Bottom View

EP SUFFIX (PB-FREE)
98ASA10819D
6-PIN UDFN

The 34830 is a very high performance video buffer that can handle HDTV bandwidths up to 1080p resolution. The integrated input clamp works with all sync formats and all types of video signals. The 34830 includes an innovative capability to set the bandwidth to the optimum trade-off of performance versus power dissipation. It can be adjusted all the way from HD frequencies to SD frequencies while benefiting from the lower power dissipation with lower bandwidths.

The 34830 can drive two standard video loads which are DC or AC coupled. Input signals can be DC or AC coupled. For the DC coupled case, the input sync should be close to ground. The 34830 can be disabled, with shutdown current being 0.12μA.

The 34830 is offered in an ultra thin UDFN package for space critical applications. It operates on a single 3.0 to 5.5V supply over a -40°C to 85°C temperature range.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
PC34830EP/R2	-40°C to 85°C	6-UDFN

Features

- 1080p / UXGA to 480i / VGA video buffer with 6dB gain
- Integrated input clamp
- Adjustable BW to save power
- Handles CV, Y, C, Pb, Pr, R, G, B signals
- Drives two video loads
- Single supply operation
- 3.0 to 5.5V range
- Rail to rail output
- 0.3% dG / 0.3% dθ for SD
- 0.6% THD for HD
- 0.12μA shutdown current
- Ultra thin UDFN package
- Pb-free packaging designated by suffix code EP

Applications

- Cellular phones
- DVD players
- Portable Game Players, Set-top boxes
- Laptop PCs, Desktop PCs,
- Projectors, Digital Cameras, Camcorders, Portable Media Players, Security Systems

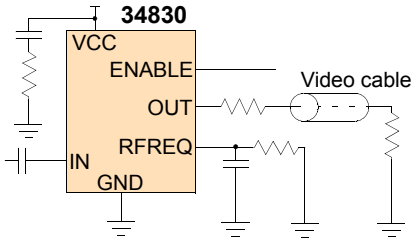


Figure 1. 34830 Simplified Application Diagram

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INTERNAL BLOCK DIAGRAM

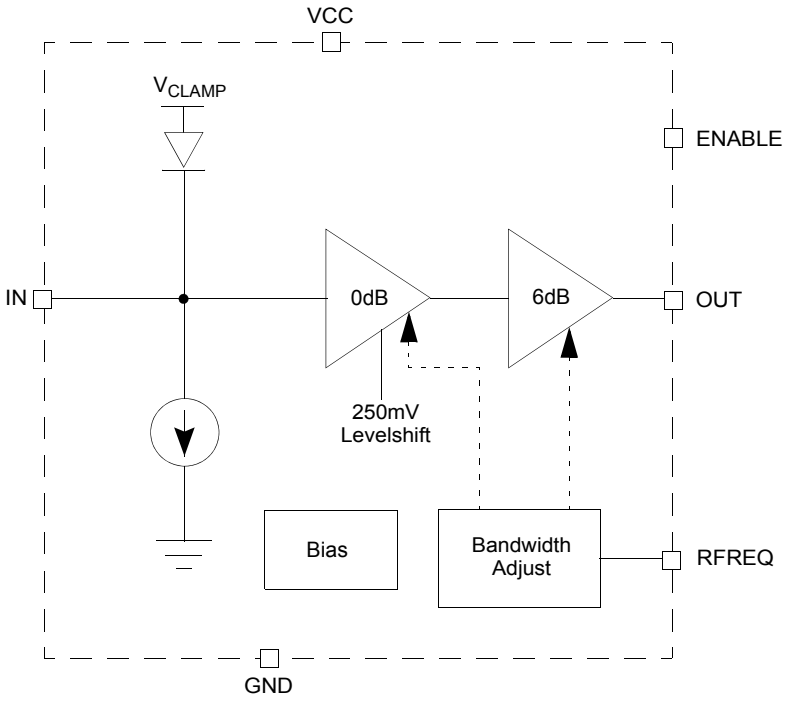


Figure 2. 34830 Simplified Internal Block Diagram

PIN CONNECTIONS

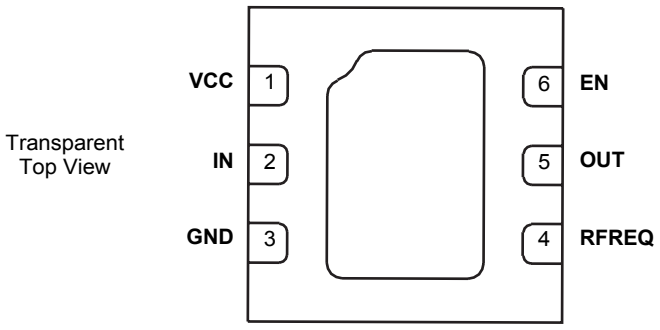


Figure 3. 34830 Pin Connections

Table 1. 34830 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	VCC	Power	VCC	Supply voltage input
2	IN	Input	Video Input	Video Input
3	GND	Ground	Ground	Ground return for the IC
4	RFREQ	Passive	Frequency Bandwidth Set	Connection for the resistor to GND to set operating bandwidth
5	OUT	Output	Video Output	Video output
6	EN	Input	Enable	Low = device disabled; High = device enabled
EP	-	Passive	Exposed Pad	Exposed pad for thermal dissipation. Connect the EP to GND or leave floating. The EP is electrically connected to ground.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Maximum Pin Voltage (Except as below) All other pins -0.3V to Vcc + 0.3V	V_{CC}	6.0	V
Maximum Current (into any pin)		±100	mA
THERMAL RATINGS			
Ambient Temperature Range	T_A	-40 to 85	°C
Operating Junction Temperature	T_J	-40 to 125	°C
Maximum Junction Temperature	T_{JMAX}	150	°C
Storage Temperature Range	T_{STORE}	-40 to 150	°C
Power Dissipation (UDFN package with EP soldered to ground plane) T_A = 25°C T_A = 70°C		 1790 1140	W
Thermal Resistance (6-LD UDFN)	 θ_{JA} θ_{JC}	 70 10	°C/W
Peak Package Soldering Temperature During Reflow[(2),(3)]	T_{PPRT}	260	°C

Notes

1. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100pF, R_{ZAP} = 1500Ω), the Machine Model (MM) (C_{ZAP} = 200pF, R_{ZAP} = 0Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0pF).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions V_{CC} = 3.0V to 5.5V, T_A = -40°C to 85°C, R_{FREQ} = 9.0kΩ, C_{IN} = 0.1µF, R_L = 150Ω, C_L = 5.0pF. Typical values are at T_A = 27°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range (inferred from gain) V_{CC} = 3V TO 3.4V V_{CC} = 3.4V TO 5.5V	V_{INP}	 $V_{INPCLAMP}$ $V_{INPCLAMP}$	 - -	 $(V_{CC}-1)/2$ 1.2	V
Input Clamping Level[4]	$V_{INPCLAMP}$	-50	0	+50	mV
Output Clamping Level[5]	$V_{OUTCLAMP}$	400	500	600	mV
Frequency Set Resistor Range	R_{FREQ}	9.0	-	108	kΩ
Supply Current measured with no load R_{FREQ} = 108kΩ R_{FREQ} = 9kΩ	I_{CC}	 - -	 4.5 17	 8 23	mA
Supply Current in Shutdown Mode (EN = 0.0V)	$I_{CCSHUTDOWN}$	-	0.12	5.0	µA
Output Short-circuit Current (Output shorted to V_{CC} or ground for <1s)	I_{SC}	-	100	-	mA
Input Leakage Current (V_{INP} = 1.0V)	I_{INP}	-	2.0	5.0	µA
Line-Time Distortion (100 IRE, 18µs)	H_{DIST}	-	0.1	0.2	%
Field-Time Distortion (100 IRE, 18µs, field lines)	V_{DIST}	-	0.2	0.4	%
Logic Low Input Voltage	V_{IL}	-	-	$0.3(V_{CC})$	V
Logic High Input Voltage	V_{IH}	$0.7(V_{CC})$	-	-	V
Logic Level Input Current (source and sink)	I_{ILH}	-	-	|1.0|	µA

Notes

4. Referenced to input. Input clamp not active for signals C, P_b, P_r, U, and V.
5. Establishes output sync level.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions V_{CC} = 3.0V to 5.5V, TA = -40°C to 85°C, R_{FREQ} = 9.0kΩ, C_{IN} = 0.1µs, R_L =150Ω, C_L = 5.0pF. Typical values are at T_A = 27°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Low Frequency Gain (@100kHz)	A	1.9	2.0	2.1	V/V
Small-signal 1.0 dB Bandwidth R_{FREQ} = 108kΩ R_{FREQ} = 9kΩ)	BW_{1SS}	 25 85	 37 130		MHz
Differential Gain (3-step measurement, R_{FREQ} = 108kΩ, f = 4.0MHz)	dG	-	0.3	1.0	%
Differential Phase (3-step measurement, R_{FREQ} = 108kΩ, f = 4.0MHz)	dθ	-	0.3	1.0	deg
Total Harmonic Distortion (V_{IN} = 0.65V + 700mV_{P-P} , 60MHz sine wave)	THD	-	0.65	-	%
DC Group Delay (at 100kHz)	t_G	-	2.8	-	ns
Group Delay Deviation (f = 100kHz to 60 MHz)	Δt_G	-	0.5	-	ns
Slew Rate (V_{OUT} = 2V step)	SR	-	450	-	V/µs
Settling Time to 10% (V_{OUT} = 2V_{PP})	t_S	-	4.0	-	ns
Peak Signal to Noise Ratio (V_{OUT} = 2.0Vp-p, f=100Hz to 200 MHz)	SNR	58	65	-	dB
Power Supply Rejection (Measured at 100kHz with 100mVpp sinewave ripple on V_{CC}.)	PSR	-	40	-	dB

ELECTRICAL PERFORMANCE CURVES

Plots are taken under conditions V_{CC} = 4.0V, R_{FREQ} = 9.0kΩ, R_L =150Ω, T_A = 27°C, unless otherwise noted.

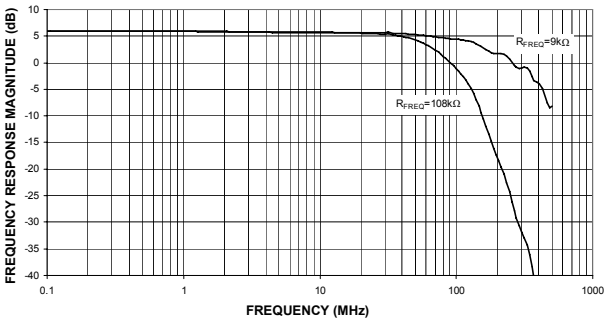


Figure 4. Frequency Response Magnitude

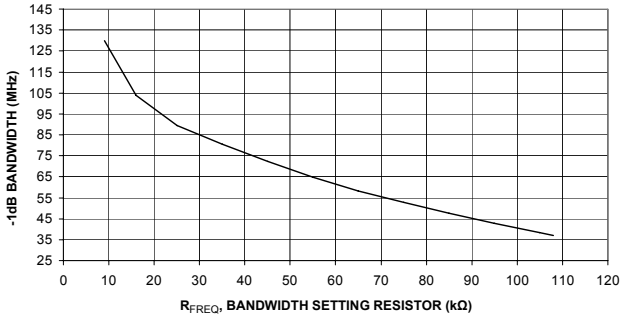


Figure 5. -1dB Bandwidth vs. R_{FREQ} (kΩ)

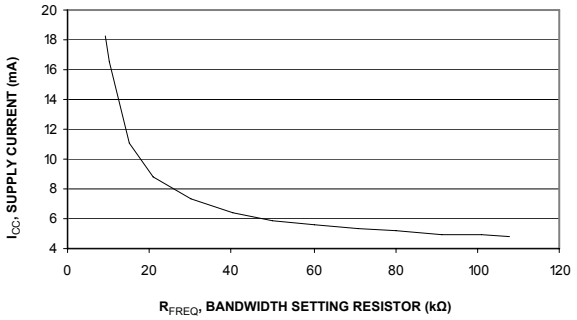


Figure 6. Supply Current vs. R_{FREQ} (kΩ)

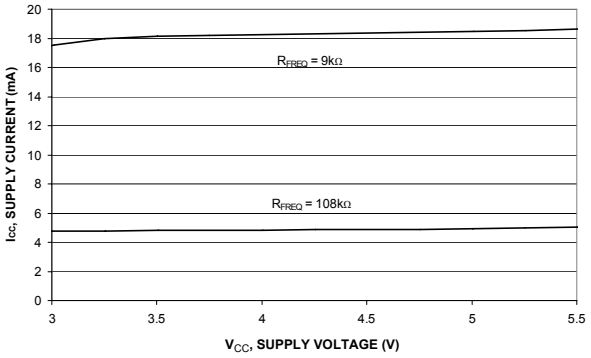


Figure 9. No Load Supply Current vs. Supply Voltage

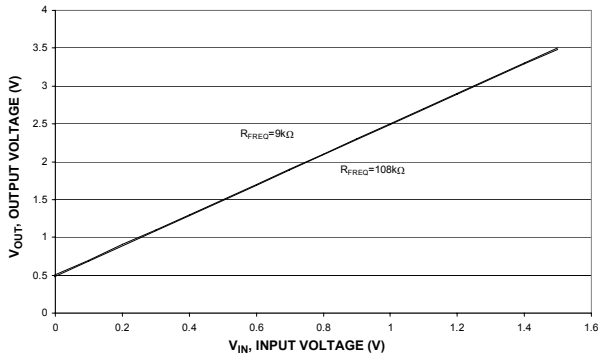


Figure 7. DC Output Voltage vs. Input Voltage

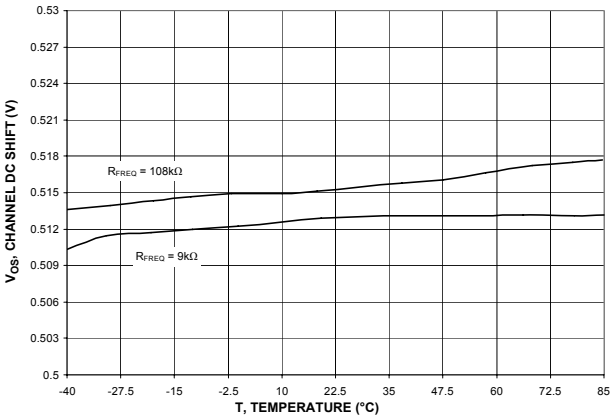


Figure 10. Channel DC Shift vs. Temperature

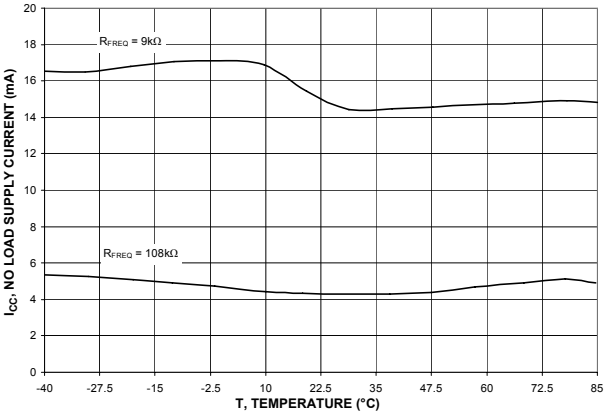


Figure 8. Supply Current vs. Temperature

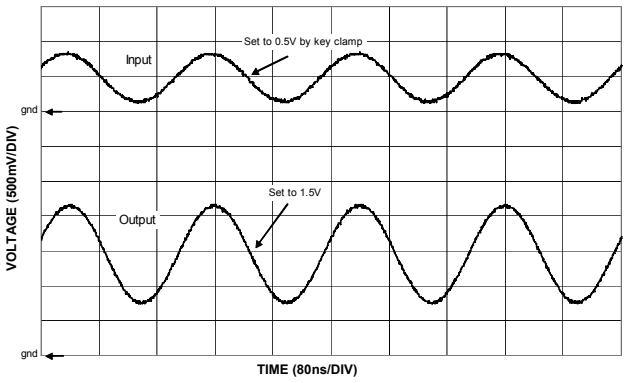


Figure 11. Sinusoidal Wave Response (External resistors setting clamp level to 0.5V, VCC= 3V, R_{FREQ} = 108kΩ for 5MHz sine input.)

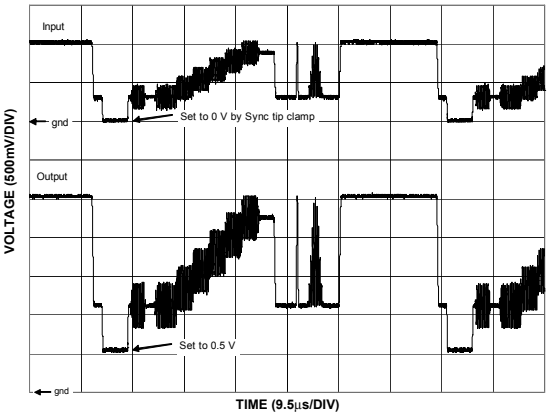


Figure 12. 480i Signal (R_{FREQ} = 108kΩ)

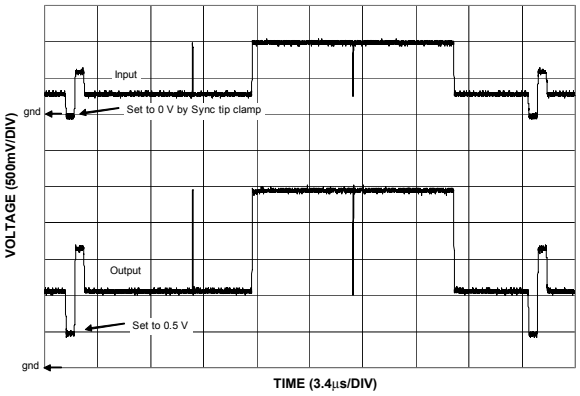


Figure 15. 1080i Signal

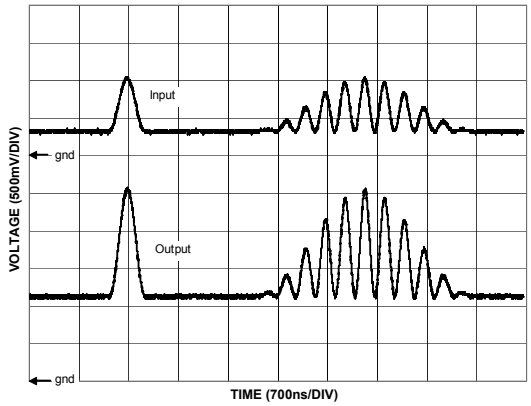


Figure 13. 480i 2T and Modulated 12.5T Response (R_{FREQ} = 108kΩ)

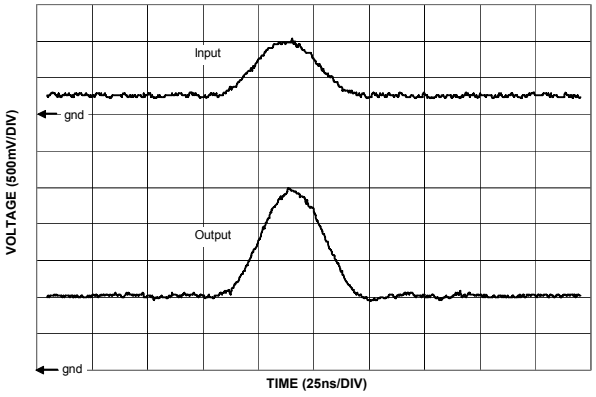


Figure 16. 1080i 2T Response

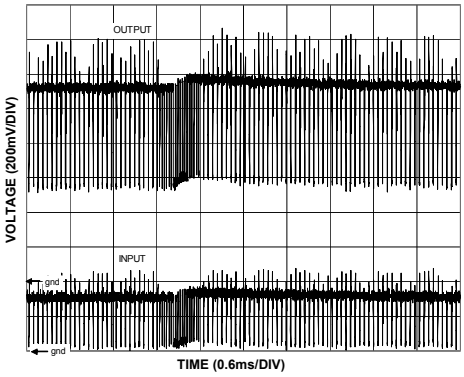


Figure 14. 480i Vertical/Horizontal Sync Levels (R_{FREQ} = 108kΩ)

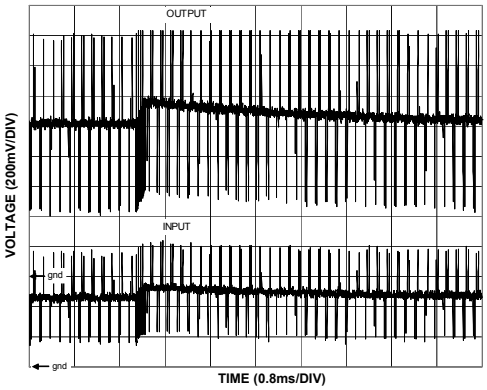


Figure 17. 1080i Vertical/Horizontal Sync Levels

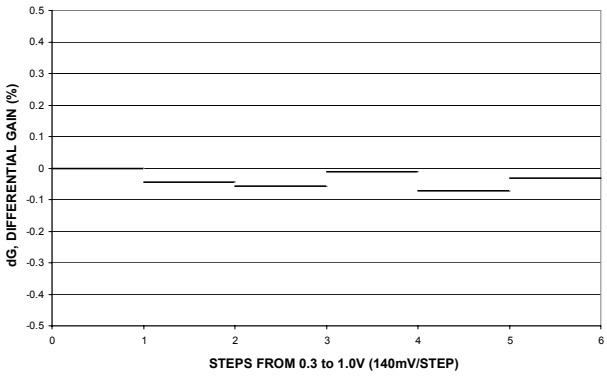


Figure 18. Differential Gain (R_{FREQ} = 108kΩ, measured at 4.0MHz)

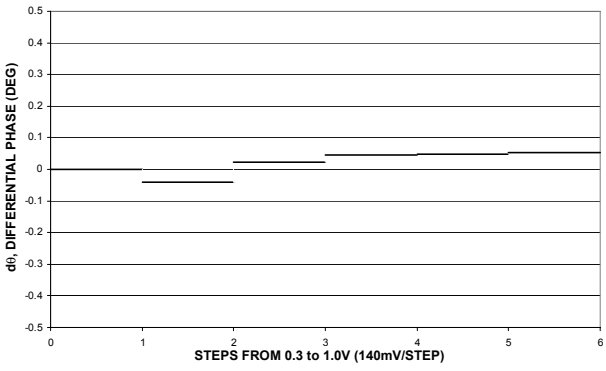


Figure 19. Differential Phase (R_{FREQ} = 108kΩ, measured at 4MHz)

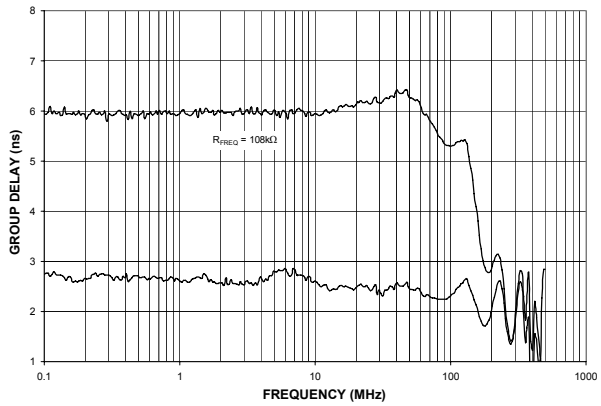


Figure 20. Group Delay Response

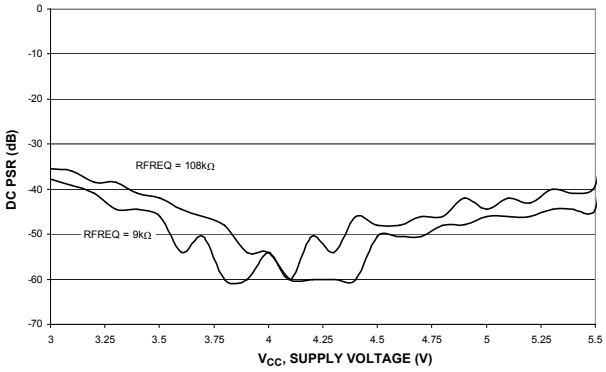


Figure 21. DC PSR vs. Supply Voltage

FUNCTIONAL DESCRIPTION

FUNCTIONAL PIN DESCRIPTION

VCC

VCC is the power input terminal for the IC. A 0.1μF bypass capacitor in series with a 4.7Ω resistor to ground should be connected as close as possible to this pin to provide noise immunity.

IN

IN is the video signal input terminal.

GND

GND is the ground terminal for the IC.

RFREQ

The operating bandwidth of the IC is set by the value of the resistor between this terminal and ground. By selecting a value for the RFREQ resistor between 9.0kΩ and 108kΩ,the bandwidth can be set for video applications ranging from 1080p to 480i.

OUT

OUT is the video signal output terminal.

EN

EN is a logic level enable input for the IC. EN = 1 turns the IC on, and EN = 0 turns it off.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

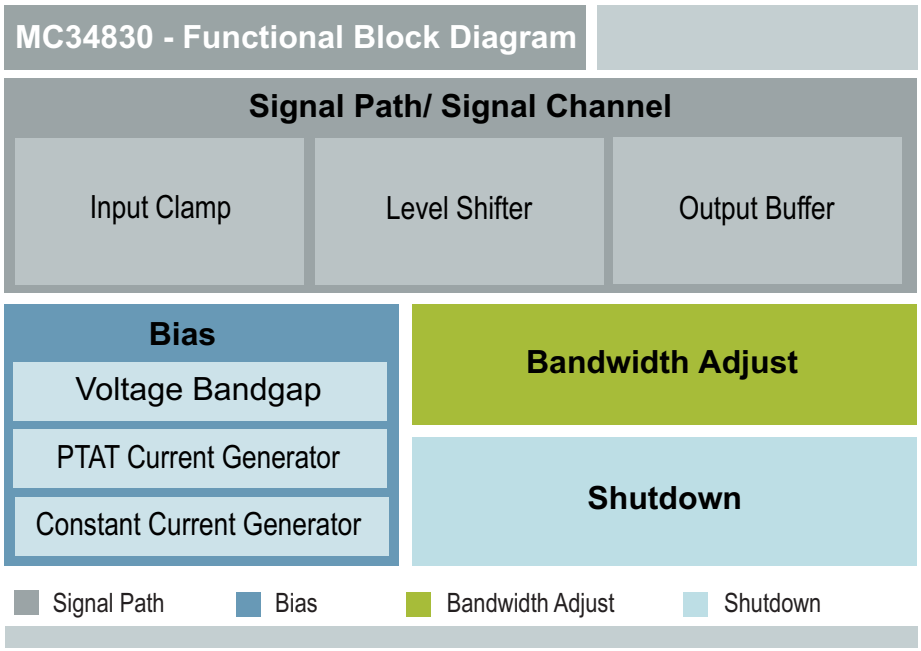


Figure 22. Functional Internal Block Diagram

SIGNAL PATH/SIGNAL CHANNEL

INPUT CLAMP

This sets the DC level of the signal at the input if the input is AC-coupled.

LEVELSHIFTER

The Level Shifter provides +250mV DC shift to the input signal. This positions the signal within the input compliance of the output buffer.

OUTPUT BUFFER

It provides gain of two as well as the current to drive the load.

BIAS CIRCUITRY

The Bias Circuitry sets the operating points for the internal blocks of the 34830. It consists of a bandgap voltage reference, a PTAT current generator and a constant current generator.

BANDWIDTH ADJUST

It consists of a variable PTAT current generator whose current is set by an external resistor. Bias current variation is inversely proportional to the external resistor value. By varying the bias current for the level shifter and output buffer we can adjust the channel bandwidth.

SHUTDOWN

Shutdown enables/disables internal blocks of the 34830 based on the state of the enable input (EN).

FUNCTIONAL DEVICE OPERATION

INTRODUCTION

The 34830 is a very high performance video buffer designed for high-definition (HD) video applications. The device features an innovative adjustable bandwidth circuitry that allows the user to set the bandwidth of the device through an external resistor connected to R_{FREQ}. This feature allows the 34830 to fit in a variety of video applications giving it the flexibility to reduce power consumption when full bandwidth is not required. In this way the 34830 can support all video bandwidths, from standard definition (SD) to high definition (HD), including the 1080i as well as 1080p formats.

The 34830 also features an internal input clamp that works with all sync formats and types of video signals. The clamp can work in three different modes and allows both AC- and DC-coupled input signals.

The 34830 is optimized to drive a single standard video load while maintaining exceptional performance characteristics. Two video loads can also be supported by the device with a minimum tradeoff in performance specifications. The 34830 supports both AC- and DC-coupled outputs.

The 34830 can be disabled with an ultra-low current consumption of 0.12μA, by driving the EN input to ground. The 34830 operates using a single supply from 3V to 5.5V, and is designed to work in the extended temperature range from -40°C to 85°C. The device is offered in a small UDFN package ideal to fit into space-critical applications.

The signal path of the 34830 begins with the input clamp that DC-restores the input. The signal is then shifted up by a level shifter which brings it to the appropriate levels required for the output buffer. The level shifter also provides isolation between the very sensitive input clamp circuit and the input stage of the output buffer. The signal is then channeled to the output buffer which amplifies it with a gain of two and drives the output loads. Both the level shifter and output buffer blocks are biased through the bandwidth adjust circuitry which allows the user to set the bandwidth and quiescent power consumption according to the application at hand.

INPUT CLAMP

The function of the input clamp is to set the DC level of the signal at the input. The clamp can be operated in three modes.

Sync Tip Clamp

The clamp works in this mode for Y,CV, R, G, and B signals that are AC-coupled to the 34830. In this mode, the clamp senses the most negative level of the input signal and clamps it to ground. The clamp circuit does this by injecting current into the AC-coupling capacitor to make the voltage at the input rise. The current is disabled once the voltage has risen to the appropriate level. The clamp circuitry includes a small (2.0μA) pull-down current to guarantee operation of the clamp.

Key Clamp

The clamp works in this mode for C, P_b, P_r, U, and V signals that are AC-coupled to the 34830 while DC bias is set externally. In this configuration, ensure that the DC bias at the input is such that the most negative level of the signal never goes below 50mV, to avoid interference with the clamp. The DC bias at the input can be set through a resistive voltage divider after the AC-coupling capacitor (Figure 23). In order to maximize the input signal swing, it is recommended to set the input DC bias to 0.5V. This will also maximize the swing at the output of the 34830.

Transparent Clamp

The clamp works in this mode for all DC-biased signals. Ensure that the most negative level of the signal is above 50mV from ground. If this requirement is not met, the signal source and clamp both try to set the level at the input, resulting in signal distortion. The input clamp becomes transparent for signals above 50mV and the signal passes through unaffected.

BIAS CIRCUITRY

The bias circuit sets the operating bias for 34830's internal blocks. It includes a bandgap voltage reference, a PTAT current generator, as well as a constant current generator. These reference currents and voltages are then distributed to 34830's internal blocks to set their respective operating points.

BANDWIDTH ADJUST

The 34830 features a bandwidth adjust circuit that sets the bandwidth of the channel by adjusting quiescent supply current. It consists of a PTAT current generator whose current varies with the value of an external resistor (R_{FREQ}). This PTAT current is used to set the operating bias for the level shifter and output buffer blocks. Increasing the external resistor (R_{FREQ}) lowers the bias current, and hence reduces both supply current and bandwidth. Decreasing the value of R_{FREQ} increases both supply current and bandwidth. Select a value for R_{FREQ} in the range between 9kΩ and 108kΩ, to set the bandwidth between the upper and lower limits. Refer to Figure 5.

LEVEL-SHIFTER

After passing through the input clamp, which restores its DC level to a known value, the signal is level-shifted up by 250mV. The level-shifting operation is done for two reasons. The first is to isolate the input of the output buffer from the sensitive clamp circuitry to prevent distortion. In this sense,

the level-shifter acts simply as a buffer of gain one. The second reason, is to bring the input signal into the proper operating range of the output buffer. Shifting the signal up allows the output buffer to work in its sweet spot. This also prevents the output devices of the output buffer from going into saturation.

Since the level-shifter needs to pass the signal without affecting it, it really is a high-speed amplifier. The current that biases this block comes from the bandwidth adjust section, which allows for the power consumption to be decreased if lower bandwidths are required. Refer to Figure 6.

OUTPUT BUFFER

The output buffer is a high-speed (800MHz open-loop bandwidth), operational amplifier used in a non-inverting gain of two configuration through resistive feedback. The amplifier uses a class AB topology with a rail-to-rail output that incorporates saturation protection as well as current-limiting. In this way the 34830 is protected against excessive loads or short-circuit conditions to both supply and ground and will resume its normal operation as soon as the short-circuit or overload condition is removed.

The output buffer also uses PTAT current biasing that varies with R_{FREQ}. By increasing R_{FREQ}, the buffer bandwidth can be decreased, resulting in power consumption savings.

The output buffer has been optimized to drive a standard video load (150Ω) with up to 5pF of load capacitance, while meeting all of the specifications listed in the electrical characteristics table. The output buffer can also support two standard video loads with a slight relaxation in the specifications.

SHUTDOWN

The 34830 features an enable input (EN) that allows the device to be placed in a low-supply-current shutdown state when not required to pass a video signal. Driving EN high puts the 34830 in its active mode. Driving EN low puts the 34830 in shutdown. In shutdown, the device has a supply current of 120nA and its output becomes high impedance. The shutdown feature makes the 34830 ideal for portable applications where power consumption is critical.

SETTING KEY CLAMP BIAS

For C, P_b, P_r, U, and V signals, use a resistor divider to set the DC bias (V_{CLAMP}) at the input of the 34830, as shown in Figure 23. In this configuration.

$$V_{CLAMP} = \frac{R_{C1} \times V_{CC}}{R_{C1} + R_{C2}}$$

Ensure that V_{CLAMP} is set to a value such that the most negative value of the signal at the input to the 34830 is above 50mV. This prevents the internal clamp from turning on. To maximize signal swing, set V_{CLAMP} = 0.5V. The general procedure for selecting the resistor values for R_{C1} and R_{C2}, is to first select a value for V_{CLAMP} and R_{C1}, and then solve for R_{C2} using the formula:

$$R_{C2} = \frac{R_{C1} \times (V_{CC} - V_{CLAMP})}{V_{CLAMP}}$$

The values selected for R_{C1} should not be too small, The bias current that flows through the resistor divider network comes directly from V_{CC}, and hence adds to power consumption. A typical value for R_{C1} is 10kΩ.

The general relationship between input and output voltage of the channel is given by the formula:

$$V_{OUT} = 2 \times (V_{IN} + 250mV) \pm 100mV$$

Where the 250mV term is the offset provided by the internal level shifter. The 100mV term that is added to the equation represents the worst case errors and offsets that can be expected from the signal path, due to process and temperature variations. The DC bias at the output is given by the same formula substituting V_{CLAMP} for V_{IN}. Thus the DC bias at the output for V_{CLAMP} = 0.5V is around 1.5V.

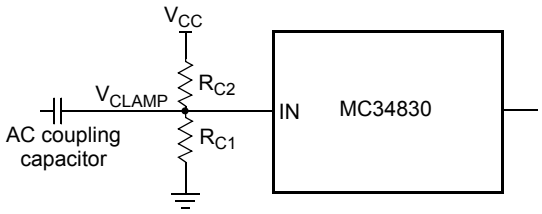


Figure 23. Key Clamp DC Bias Configuration

SETTING BANDWIDTH

The bandwidth of the 34830 is set through an external resistor connected from input R_{FREQ} to ground. Increasing the value of the resistor causes the quiescent current of the device to decrease, which in turn decreases its bandwidth. Decreasing the value of R_{FERQ} has the opposite effect, mainly to increase quiescent supply current and thus bandwidth. Select the value of R_{FREQ} in the range between 9kΩ and 108kΩ. Refer to Figure 5 for a relationship between the value of R_{FREQ} and the corresponding bandwidth of the 34830. To ensure that the channel bandwidth is greater than the one needed for the application, after taking into account process and temperature variation, multiply the value of RFREQ obtained from the graph by 0.6. Use this number as the value of the external resistor.

It is recommended to place a small capacitor (100pF) in parallel with the external resistor at R_{FREQ}. This capacitor helps to filter any noise or signal that couples into the R_{FREQ} input, which may disturb the bias conditions of the device.

INPUT CONSIDERATIONS

As explained in the Input Clamp section, the 34830 features an internal clamp that allows the device to work with both AC as well as DC-coupled input signals. To AC-couple the input signal, use a 0.1μF capacitor following the video signal source. If the signal being AC-coupled has sync, then the 34830's clamp circuit ensures that the sync tip is detected and positioned near ground (Sync Tip Clamp). If the signal that is being AC-coupled does not have sync (Key Clamp), care must be taken to ensure that its most negative portions are not confused as being sync tips and clamped, resulting in signal distortion. In order to prevent this from happening, the user must set the DC bias at the input correctly. See the SETTING KEY CLAMP BIAS section.

When the input to the 34830 goes above 50mV, the clamp circuit becomes transparent and does not have any effect on the signal being passed. This allows the 34830 to work with DC-coupled signals. To DC-couple the input signal, simply connect the video source directly to the input of the 34830.

OUTPUT CONISDERATIONS

The relationship between input and output for the 34830 follows the equation:

$$V_{OUT} = 2 \times (V_{IN} + 250mV) \pm 100mV$$

Where the 250mV term is the offset provided by the internal level shifter. The 100mV term that is added to the equation represents the worst case errors and offsets that can be expected from the signal path, due to process and temperature variations.

The 34830 has been optimized to drive a single standard video load. A standard video load typically consists of a 75Ω back-termination resistor, followed by a matched video cable and a 75Ω load resistor. The 34830 can drive up to 5pF of load capacitance in parallel with the video cable and load resistor. Two video loads can be supported by the 34830 with a minimum tradeoff in performance parameters.

The output of the 34830 can be both AC or DC-coupled. When the output is AC-coupled the AC-coupling capacitor forms a high-pass filter with the load resistor. Ensure that the value of the AC-coupling capacitor is such that the lowest frequencies of the video signal are passed without attenuation from this filter. A typical value for the output AC-coupling capacitor is 220μF.

Place the output termination resistor as close to the output as possible to minimize parasitic inductance and capacitance effects that tend to deteriorate signal quality.

TYPICAL APPLICATIONS

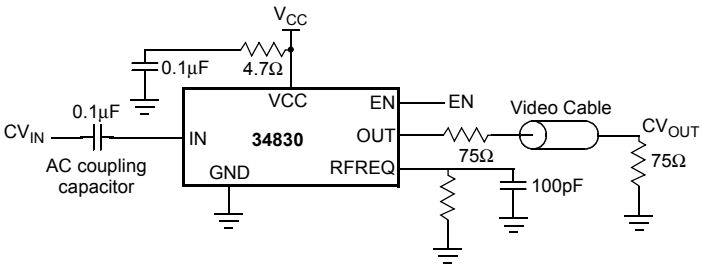


Figure 24. Composite Video Signal

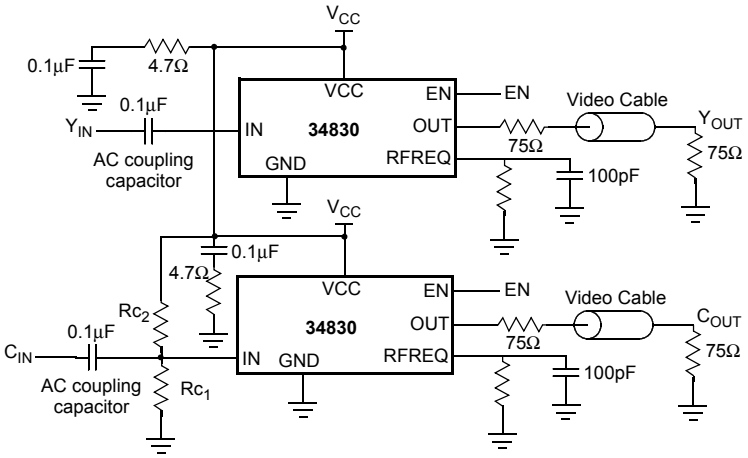


Figure 25. S-Video Application

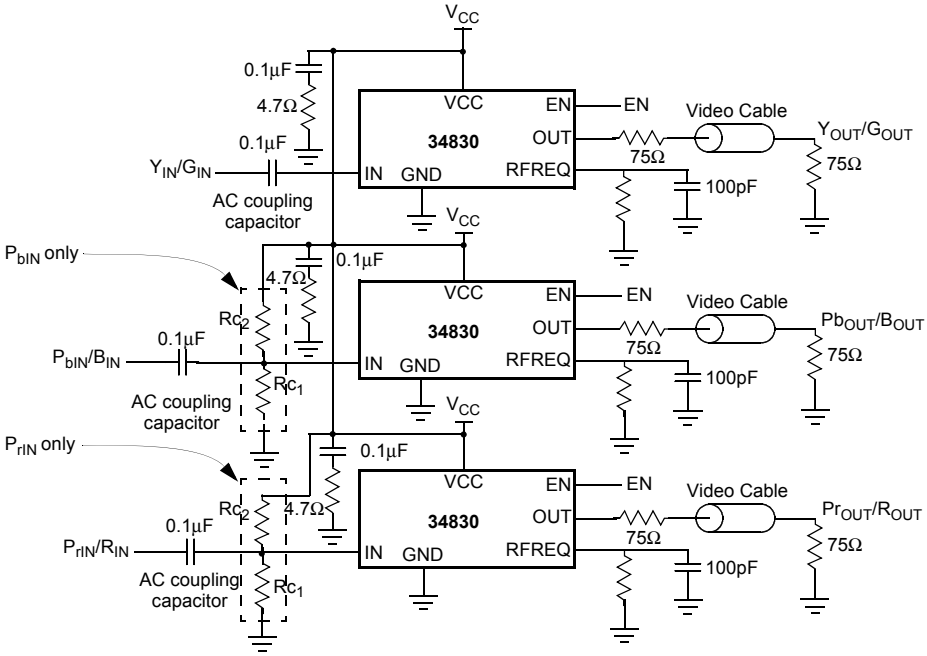


Figure 26. Component Video Application

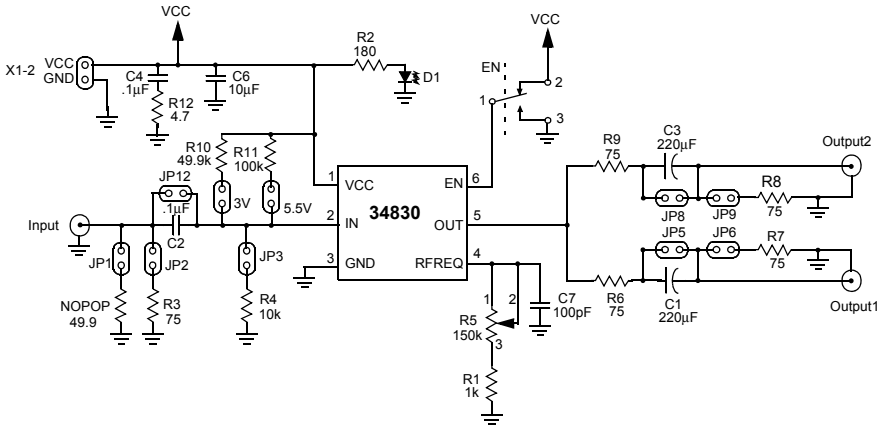


Figure 27. 34830 Evaluation Board Schematic

BILL OF MATERIAL

Table 5. 34830 Bill of Material

Item	Qty	Part Description	Value/Rating	Part Number/Manufacturer	Install
C1, C3	2	Capacitor	220µF, 10V	UVZ1A221MED, Nichicon, radial, electrolytic	Y
C2	1	Capacitor	.1µF, 25V	0603, ceramic, 03CER	Y
C4	1	Capacitor	.1µF, 6.3V	0204, ceramic, Murata, LLL153C80J104ME01B	Y
C6	1	Capacitor	10µF, 25V	1206, ceramic	
C7	1	Capacitor	100pF, 50V	0603, metal film chip	Y
X1-2	2			FIDICUAL_40	N
JP1-3, JP5-6, JP8-9, JP12, 3.0V, 5.5V	10	1x2 Male header strip		HDR1X2, .1 Pitch straight for .062 BD.	Y
D1	1	LED		HSMx-c670 HP 0805	N
U1	1	MC34830		MC34830	Y
R1	1	Resistor	1.0kΩ, 1/10W, 1%	0603, metal flip chip	Y
R2	1	Resistor	180Ω, 1/10W, 1%	0603, metal flip chip	N
R3, R6 - R9	5	Resistor	75Ω, 1/10W, 1%	0603, metal flip chip, Speer Electronics	Y
R4	1	Resistor	10kΩ, 1/10W, 1%	0603, metal flip chip	Y
R5	1	Potentiometer	150kΩ	Bourns 3299Y-1-154L, trrimpot, 25 turn	Y
R10	1	Resistor	49.9kΩ, 1/10W, 1%	Speer Electronics, 0603, metal flip chip	Y
R11	1	Resistor	100kΩ, 1/10W, 1%	0603, metal flip chip	Y
R12	1	Resistor	4.7Ω, 1/0W, 1%	0603, metal flip chip	Y
NOPOP	1	Resistor	49.9Ω, 1/10W, 1%	0603, metal flip chip, TTI CRCW060349R9FT	N
Input, Output 1-2	3	SMA Jack	SMA-PCB_EDGE_E	Johnson, 142-0711-826, Edge Mount	Y

Table 5. 34830 Bill of Material

Item	Qty	Part Description	Value/Rating	Part Number/Manufacturer	Install
EN	1	E-Switch	Switch SPDT	SPDT, EG1218	Y
VCC	1	2POL254 Phoenix Connector	Termblock2_MKD	MKDSN1.5/2, 2 pin Terminal block 2 Digakey, 5.0mm, 90 deg wire to pin, Stock number - 277-1236-ND	Y

Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

PCB LAYOUT CONSIDERATIONS

The 34830 is a high-speed amplifier, and as such requires careful attention to be paid to the way in which boards are laid out, in order to guarantee best performance. All high-speed layout techniques should be followed including the following points.

1. Minimize all trace inductances by reducing trace lengths. This is especially critical for the supply and ground lines as well as for the output line. Boards with multiple layers should have enough vias from the ground plane to the chip ground connection to further reduce inductance.
2. Make sure that a solid ground plane is available and run all traces above it.
3. Avoid traces with 90 degree bends.
4. Use a 0.1μF bypass capacitor in series with a 4.7Ω resistor as close to the V_{CC} and GND pins of the 34830 as possible. Include a 10μF bypass capacitor at the location on the board where V_{CC} and GND are connected to the external world.
5. Try to refer all ground connections to the same point as in a star ground configuration. Usually this point is the middle point of the ground plane.

THERMAL CONSIDERATIONS

Make sure that the thermal dissipation ratings for the 34830 package are not violated in the application at hand. The 34830 comes in a package with an exposed pad (EP). The primary function of the EP is to serve as an effective way to dissipate heat away from the inside of the package. Take full advantage of this feature and connect the EP to a surface or plane that can act as a heat sink. The EP is electrically connected to ground. Make sure that the heat sink is also connected to the same potential. If multiple heat generating components are used in the application, distribute these evenly throughout the board, so as not to create hot spots with large temperature gradients that could violate power and heat dissipation ratings.

POWER DISSIPATION

Care must be taken not to exceed the maximum die junction temperature of the 34830. The die junction temperature can be calculated through the formula:

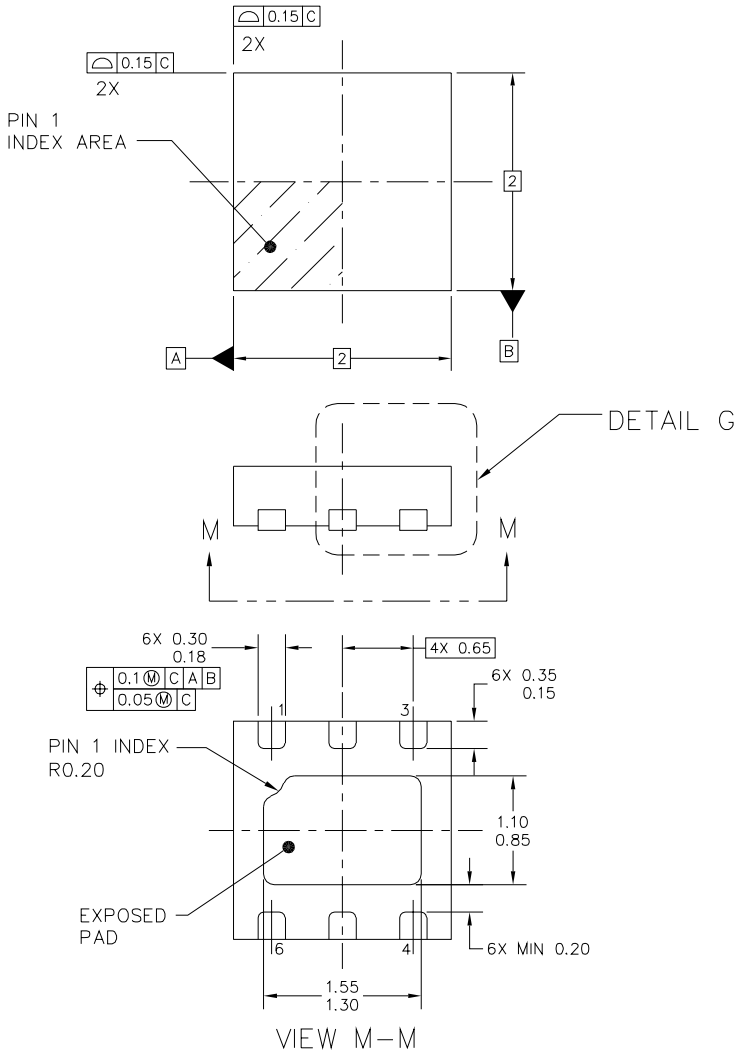
$$T_J = T_A + P_{DISS} \times \theta_{JA}$$

Where P_{DISS} is the average power dissipation of the device which can be calculated as $P_{DISS} = V_{CC}*(I_{CC} + V_{OUT(RMS)}^2/R_{LOAD})$.

PACKAGING

PACKAGE DIMENSIONS

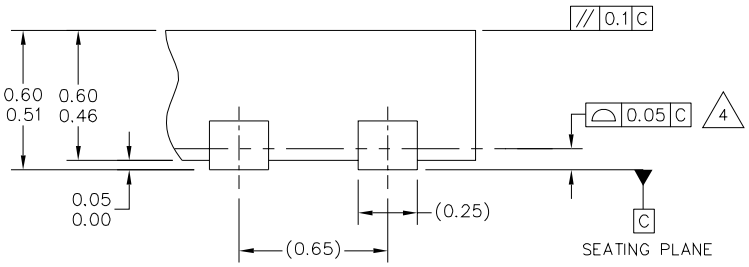
For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	9/2008	• Initial Release

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