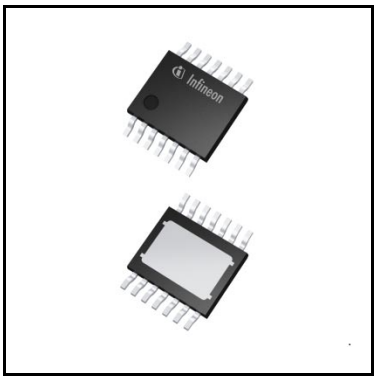
TLD2142-1EP

LITIX™ Basic+



Features

- Single channel device with integrated and protected output stage (current source), optimized to drive LEDs as additional low cost current source
- High output current (up to 240 mA)
- Very low current consumption in sleep mode
- Very low output leakage when channel is “off”
- Low current consumption during fault
- Output currents’ control via external low power resistor
- Additional output current demand supported by LITIX™ Companion direct drive without additional components
- Intelligent fault management: up to 16 and more devices can share a common error network with only one external resistor
- Reverse polarity protection allows reduction of external components and improves system performance at low battery/input voltages
- Overload protection
- Wide temperature range: -40°C < T_J < 150°C
- Output current control via external low power resistor
- Green product (RoHS compliant)

Potential applications

- Cost effective “stop”/ “tail” function implementation with shared and separated LEDs per function
- Turn indicators
- Position, fog, rear lights and side markers
- Animated light functions like wiping indicators and “welcome/goodbye” functions
- Day Running Light
- Interior lighting functions like ambient lighting (including RGB color control), illumination and dash board lighting
- LED indicators for industrial applications and instrumentation

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101.

Description

The LITIX™ Basic+ TLD2142-1EP is a single channel high-side driver IC with integrated output stage. It is designed to control LEDs with a current up to 240 mA. In typical automotive applications the device is capable of driving 3 red LEDs with a current up to 180 mA and even above, if not limited by the overall system thermal properties. Practically, the output current is controlled by an external resistor or reference source, independently from load and supply voltage changes.

Table 1 Product summary

Parameter	Symbol	Values
Operating voltage	$V_{S(nom)}$	5.5 V … 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUT(max)}$	40 V
Nominal output (load) current	$I_{OUT(nom)}$	180 mA (nominal) when using the automotive supply voltage range 8 V - 18 V. Currents up to $I_{OUT(max)}$ are possible with low thermal resistance R_{thJA}
Maximum output (load) current	$I_{OUT(max)}$	240 mA depending on R_{thJA}
Current accuracy at R_{SET} = 10 kΩ	K_{LT}	900±4.33%
Current consumption in sleep mode	$I_{S(sleep, typ)}$	0.1 µA
Maximum current consumption during fault	$I_{S(fault, ERRN)}$	850 µA or less when fault is detected from another device (disabled via ERRN)

Type	Package	Marking
TLD2142-1EP	PG-TSDSO-14	TLD2142

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1 Block diagram

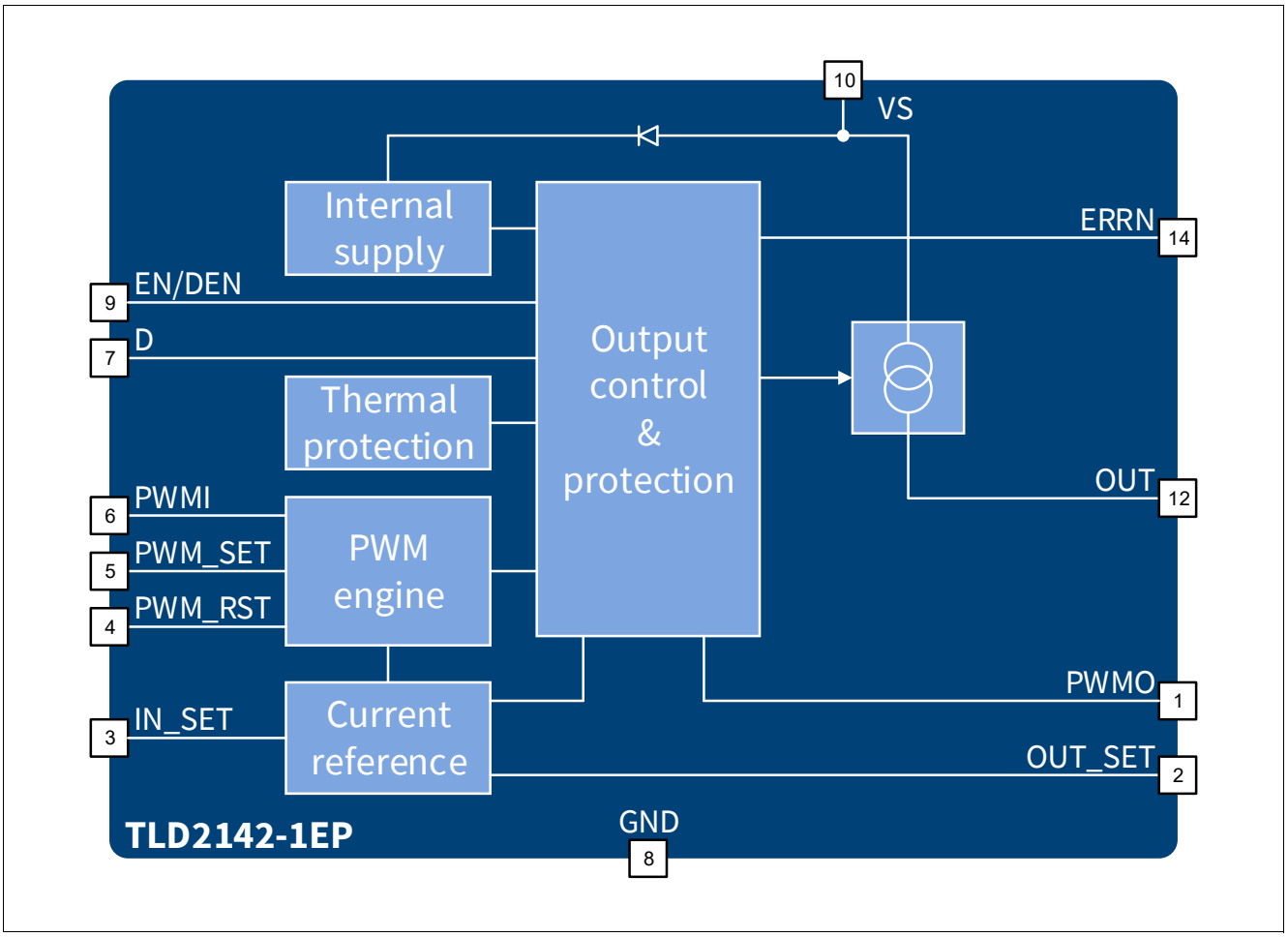


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

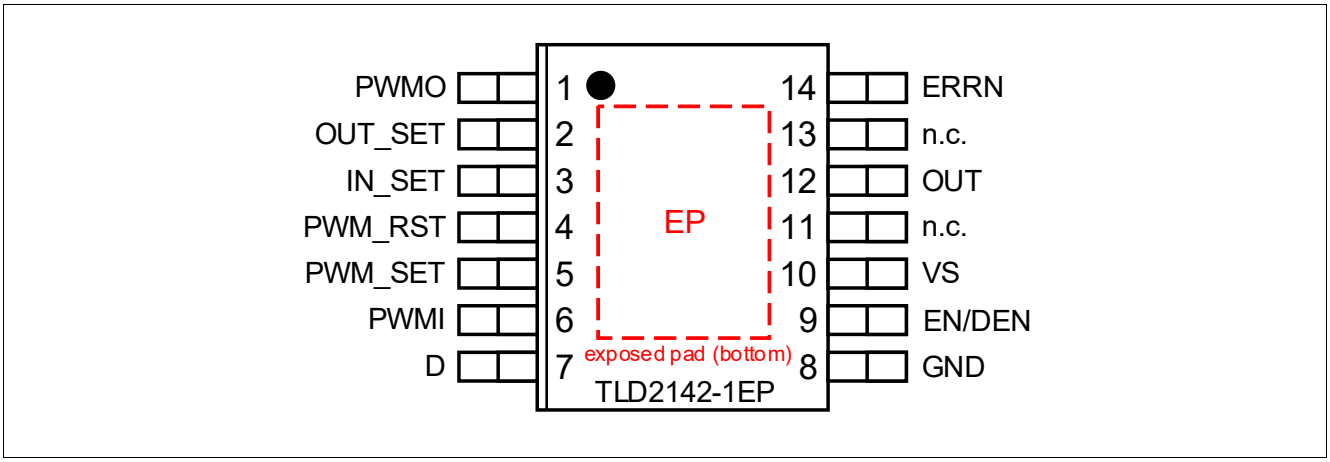


Figure 2 Pin configuration

2.2 Pin definitions and functions

Pin	Symbol	Function
10	VS	**Supply voltage;** Connected to battery or supply control switch, with EMC filter
8	GND	**Ground;** Signal ground
3	IN_SET	**Control input for OUT channel;** Connect to a low power resistor to adjust OUT output current. Alternatively, a different current reference (i.e. the OUT_SET of another LITIX™ Basic+ LED Driver) may be connected
2	OUT_SET	**Control output for additional current source;** If an additional channel or output current with same input control is needed, connect this pin to the IN_SET pin of the additional LED driver. If not used, leave the pin open
6	PWMI	**PWM input;** Connect to an external PWM controller or a ceramic capacitor (when internal PWM engine is intended to be used). If not used, connect to GND
1	PWMO	**PWM output;** Buffered PWMI logic state. Used to drive additional devices with same timing as PWMI. If not used, leave the pin open
4	PWM_RST	**PWM duty cycle reset input;** Connect to a low power resistor to adjust PWM frequency and duty cycle. If the internal PWM engine is not used (direct PWMI drive) it should be left open
5	PWM_SET	**PWM duty cycle set input;** Connect to a low power resistor to adjust PWM frequency and duty cycle. If the internal PWM engine is not used (direct PWMI drive) it should be left open
7	D	**Disable/delay error input;** Connect to a capacitor, leave open or connect to GND, depending on the required diagnosis management (see **Chapter 6** for further details)

Pin configuration

Pin	Symbol	Function
14	ERRN	**ERROR flag I/O;** Open drain, active low. Connect to a pull-up resistor
9	EN/DEN	**Output enable and diagnosis control input;** Connect to a control input (i.e. to VS via a resistor divider or a Zener diode) to enable OUT control and diagnosis capability
12	OUT	**Channel output;** Connect to the target load
11, 13	n.c.	**Not connected;** Leave these pins open
Exposed Pad	EP	**Exposed Pad;** Connected to GND-pin in application

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_J = -40°C to +150°C; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
Supply voltage	V_S	-18	–	40	V	–	P_4.1.1
EN/DEN voltage	$V_{EN/DEN}$	-18	–	40	V	–	P_4.1.3
EN/DEN voltage related to V_S: $V_{EN/DEN}$ - V_S	$V_{EN/DEN(VS)}$	-40	–	18	V	–	P_4.1.4
EN/DEN voltage related to V_{OUT}: $V_{EN/DEN}$ - V_{OUT}	$V_{EN/DEN(VOUT)}$	-18	–	40	V	–	P_4.1.5
Output voltage	V_{OUT}	-1	–	40	V	–	P_4.1.10
Output voltage related to V_S: V_S - V_{OUT}	$V_{OUT(VS)}$	-18	–	40	V	–	P_4.1.11
IN_SET voltage	V_{IN_SET}	-0.3	–	6	V	–	P_4.1.12
PWMI voltage	V_{PWMI}	-0.3	–	6	V	–	P_4.1.14
PWMO voltage	V_{PWMO}	-0.3	–	6	V	–	P_4.1.15
PWM_RST voltage	V_{PWM_RST}	-0.3	–	6	V	–	P_4.1.16
PWM_SET voltage	V_{PWM_SET}	-0.3	–	6	V	–	P_4.1.17
ERRN voltage	V_{ERRN}	-0.3	–	40	V	–	P_4.1.18
D Voltage	V_D	-0.3	–	6	V	–	P_4.1.19
Current							
Output current	I_{OUT}	0	–	250	mA	–	P_4.1.23
PWMI current	I_{PWMI}	-0.5	–	0.5	mA	–	P_4.1.26
PWMO current	I_{PWMO}	-2	–	2	mA	–	P_4.1.27
PWM_RST current	I_{PWM_RST}	0	–	300	µA	–	P_4.1.28
PWM_SET current	I_{PWM_SET}	0	–	300	µA	–	P_4.1.29
IN_SET current	I_{IN_SET}	0	–	300	µA	–	P_4.1.30
D current	I_D	-0.5	–	0.5	mA	–	P_4.1.31
OUT_SET current	I_{OUT_SET}	0	–	0.5	mA	–	P_4.1.32
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.33
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.34

Table 2 Absolute maximum ratings[1)] (cont'd)

T_J = -40°C to +150°C; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD susceptibility							
ESD susceptibility all pins to GND	V_{ESD}	-2	–	2	kV	HBM[2)]	P_4.1.36
ESD susceptibility all pins to GND	V_{ESD}	-500	–	500	V	CDM[3)]	P_4.1.37
ESD susceptibility Pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750	–	750	V	CDM[3)]	P_4.1.38

1) Not subject to production test, specified by design
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage range for normal operation	$V_{S(nom)}$	5.5	–	18	V	–	P_4.2.1
Extended supply voltage for functional range	$V_{S(ext)}$	$V_{SUV(ON)}$	–	40	V	–	P_4.2.2
Junction temperature	T_J	-40	–	150	°C	–	P_4.2.4

Note: Within the Normal Operation range, the IC operates as described in the circuit description. Within the Extended Operation range, parameters deviations are possible. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	10	K/W	1)2)	P_4.3.1
Junction to Ambient 1s0p board	R_{thJA1}	– –	61 56	– –	K/W	1)3) T_A = 85°C T_A = 135°C	P_4.3.3
Junction to Ambient 2s2p board	R_{thJA2}	– –	45 43	– –	K/W	1)4) T_A = 85°C T_A = 135°C	P_4.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and exposed pad are fixed to ambient temperature). T_A = 85°C. Total power dissipation = 1.5 W

3) Specified R_{thJA} value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 70 µm Cu, 300 mm^2 cooling area. Total power dissipation 1.5 W distributed statically and homogenously over all power stages

4) Specified R_{thJA} value is according to Jedec JESD51-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogenously over all power stages

4 Internal supply

This chapter describes the internal supply in its main parameters and functionality.

4.1 Description

The internal supply principle is highlighted in the concept diagram of **Figure 3**.

If the voltage applied at the EN/DEN pin is below $V_{EN(th)}$ the device enters sleep mode. In this state all internal functions are switched off and the current consumption is reduced to $I_{S(sleep)}$.

As soon as the voltage applied at the supply pin V_S is above $V_{SUV(ON)}$ and the voltage applied at the EN/DEN pin is above $V_{EN(th)}$, after the power-on reset time t_{POR}, the device is ready to deliver output current from the output stage. The power on reset time t_{POR} has to be taken into account also in relevant application conditions, i. e. with PWM control from *VS* or EN/DEN lines.

Also if PWM control is done via the PWM engine, the conditions $V_S > V_{SUV(ON)}$ and $V_{EN} > V_{EN(th)}$ must be fulfilled for PWM engine (and, therefore, output) activation.

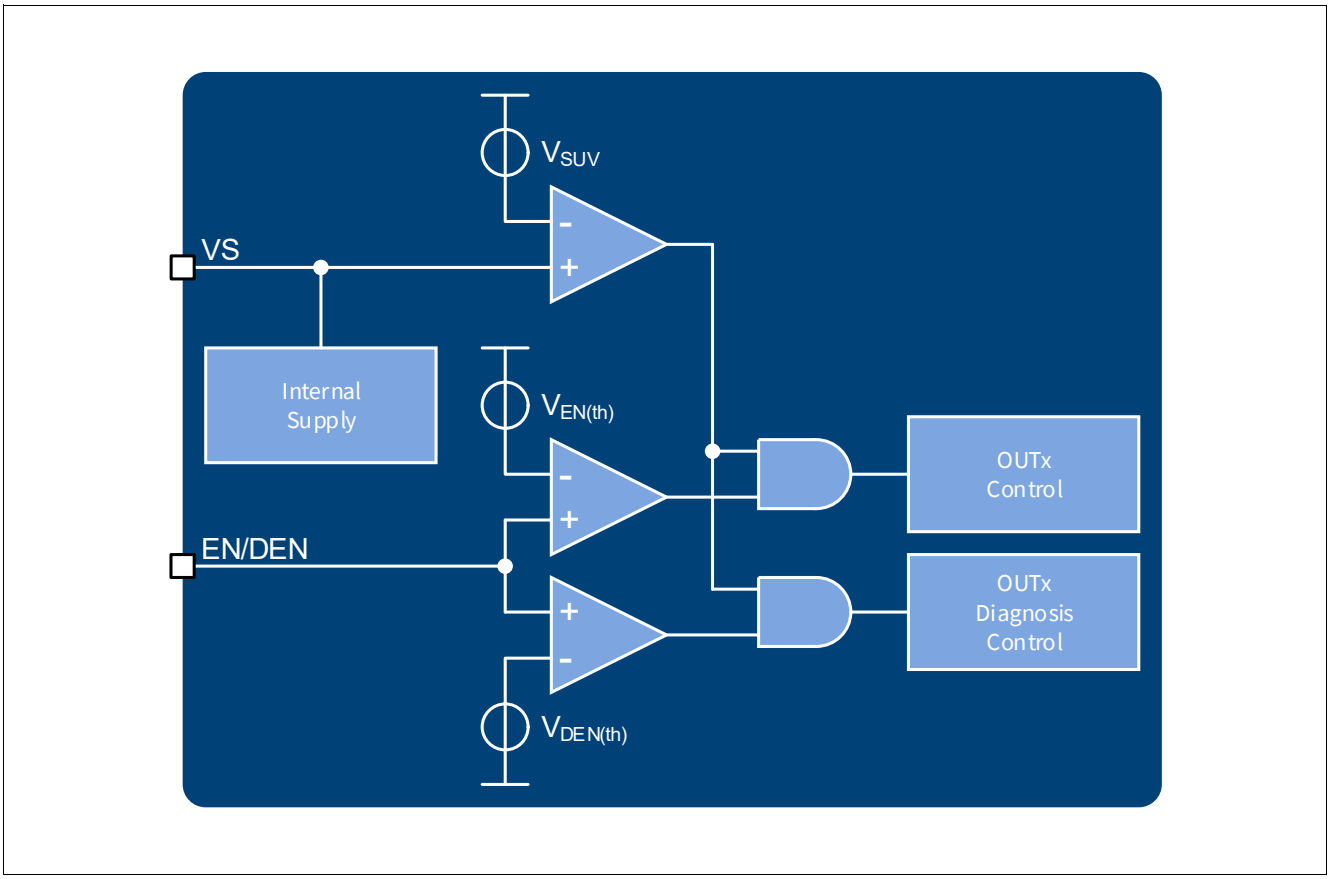


Figure 3 Internal supply

Furthermore, as soon as the voltage applied at the supply pin *VS* is above $V_{SUV(ON)}$ and the voltage applied to the EN/DEN pin V_{EN} is above $V_{DEN(th)}$, the device is ready to detect and report fault conditions via ERRN (error network pin) as described in **Chapter 6**.

To program output enable and diagnosis enable via EN/DEN pin there are several possibilities, like a resistor divider from VS to GND, a Zener diode from EN/DEN to VS and also a logic control pin (e.g. from a microcontroller output).

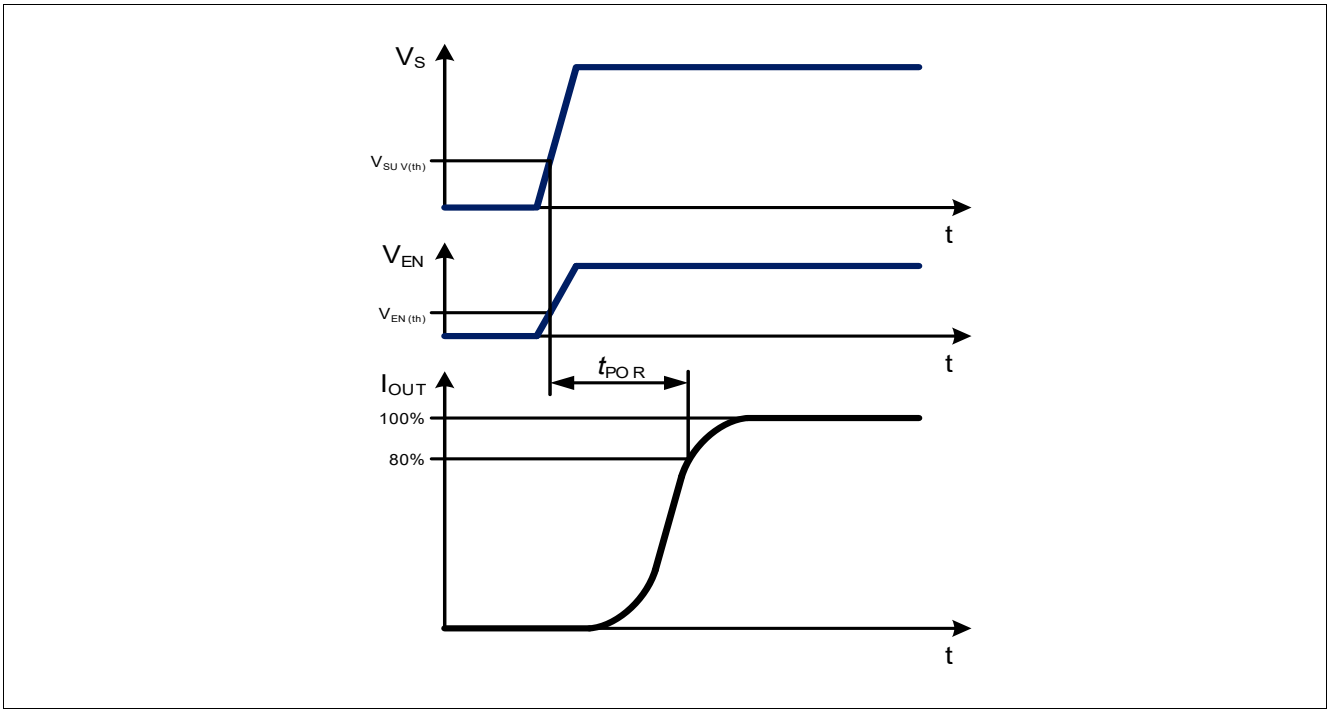


Figure 4 Power on reset timing diagram

4.2 Electrical characteristics internal supply and EN pin

Table 5 Electrical characteristics: Internal supply and EN pin

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption, sleep mode	$I_{S(sleep)}$	–	0.1	2	µA	[1] V_{EN} = 0 V T_J < 85°C V_S = 18 V V_{OUT} = 3.6 V	P_5.2.1
Current consumption, active mode (no fault)	$I_{S(active)}$	–	1.5	3	mA	V_{EN} = 5.5 V I_{IN_SET} = 0 µA T_J < 105°C V_S = 18 V V_{OUT} = 3.6 V I_{PWM_SET} = I_{PWM_RST} = 100 µA V_{PWMI} = 0 V	P_5.2.3
Current consumption during fault condition triggered from another device sharing ERRN bus	$I_{S(fault, ERRN)}$	–	–	850	µA	V_{EN} = 5.5 V T_J < 105°C V_S = 18 V V_{ERRN} = 0 V V_{OUT} = 3.6 V D open V_{PWMI} = 0 V	P_5.2.4
Current consumption during fault condition	$I_{S(fault, OUT)}$	–	–	1.25	mA	V_{EN} = 5.5 V T_J < 105°C V_S = 18 V V_{OUT} = 0 V V_{OUT} D open V_{PWMI} = 0 V	P_5.2.16
Supply thresholds							
Required supply voltage for output activation	$V_{SUV(ON)}$	–	–	5.5	V	V_{EN} = V_S V_{OUT} = 3 V R_{IN_SET} = 6.8 kΩ I_{OUT} > 50% $I_{OUT(nom)}$	P_5.2.5
Required supply voltage for output deactivation	$V_{SUV(OFF)}$	4.5	–	–	V	V_{EN} = V_S V_{OUT} = 3 V R_{IN_SET} = 6.8 kΩ I_{OUT} < 50% $I_{OUT(nom)}$	P_5.2.6
Supply voltage activation hysteresis: $V_{SUV(ON)}$ - $V_{SUV(OFF)}$	$V_{SUV(hys)}$	–	200	–	mV	[1] V_{EN} > $V_{EN(th)}$	P_5.2.8

Table 5 Electrical characteristics: Internal supply and EN pin (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
EN pin							
EN output enable threshold	$V_{EN(th)}$	1.4	1.65	1.8	V	V_S = 5.5 V V_{PS} = 2 V R_{IN_SET} = 6.8 kΩ I_{OUT} = 50% $I_{OUT(nom)}$	P_5.2.9
DEN diagnosis enable threshold	$V_{DEN(th)}$	2.4	2.5	2.8	V	V_S = 5.5 V	P_5.2.11
DEN diagnosis enable hysteresis	$V_{DEN(hys)}$	–	120	–	mV	1) R_{IN_SET} = 6.8 kΩ	P_5.2.12
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	60	µA	1) V_S > 8 V $V_{EN/DEN}$ = 2.8 V	P_5.2.17
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	110	µA	1) V_S > 8 V $V_{EN/DEN}$ = 5.5 V	P_5.2.14
EN/DEN pull-down current	$I_{EN/DEN(PD)}$	–	–	350	µA	1) V_S > 8 V $V_{EN/DEN}$ = V_S	P_5.2.15
Timing							
Power on reset delay time	t_{POR}	–	–	25	µs	1) V_S rising from 0 V to 13.5 V V_{OUT} = 3.6 V R_{IN_SET} = 6.8 kΩ I_{OUT} = 80% $I_{OUT(nom)}$	P_5.2.13

1) Not subjected to production test: specified by design

5 Power stage

The output stage is realized as high-side current source with an output current up to 240mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.
The maximum output current is limited by the power dissipation and used PCB cooling areas.
For an operating output current control loop, the supply and output voltage have to be considered according to the following parameters:

- Required supply voltage for current control $V_{S(CC)}$
- Voltage drop over through the output stage during current control $V_{PS(CC)}$
- Required output voltage for current control $V_{OUT(CC)}$

5.1 Protection

The device provides embedded protective functions, which are designed to prevent IC damage under fault conditions described in this datasheet. Fault conditions are considered as “outside” normal operating range. Protective functions are not designed for continuous nor for repetitive operations.

5.1.1 Thermal protection

A thermal protection circuitry is integrated in the device. It is realized by a temperature monitoring of the output stages.

As soon as the junction temperature exceeds the current reduction temperature threshold $T_{J(CRT)}$ the output current can be reduced by the device by reducing the IN_SET reference voltage $V_{IN_SET(ref)}$. This feature greatly helps to avoid LEDs flickering during static output overload conditions. Furthermore, it helps to protect the LEDs, which are mounted thermally close to the device, against overtemperature. If the device temperature still increases, the three output currents decrease close to 0 A. As soon as the device cools down the output currents rise again.

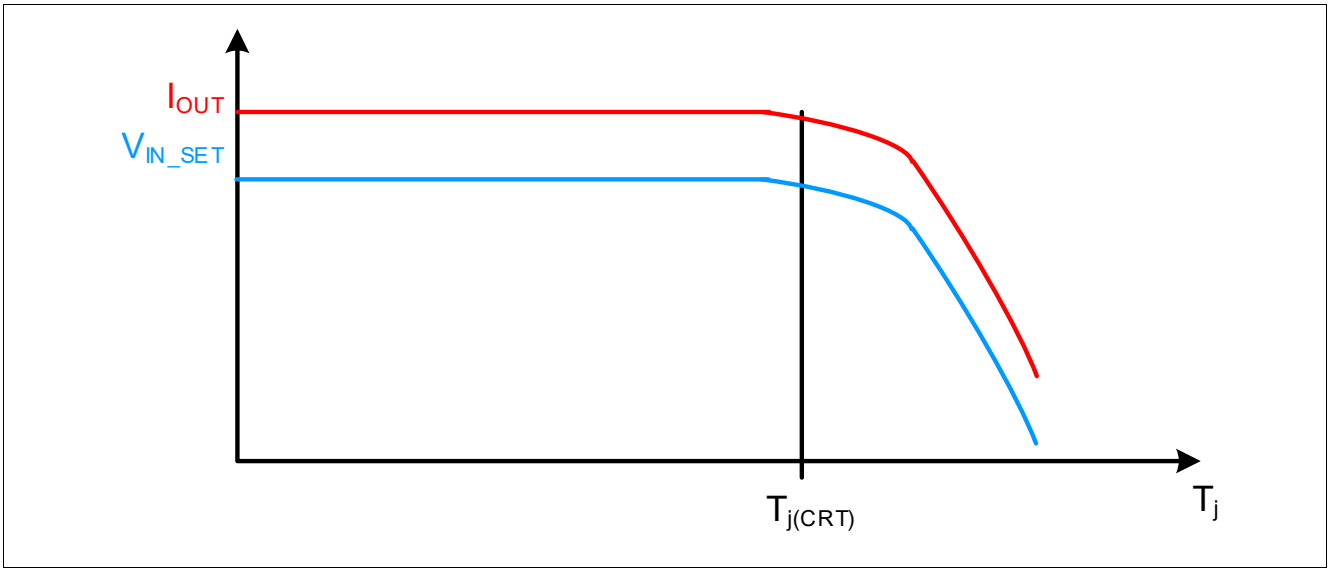


Figure 5 Output current reduction at high temperature (qualitative diagram)

Note: It is assumed that a configuration resistor R_{SET} is applied from IN_SET to GND, and not a current source, to make the protection effective.

5.1.2 Reverse battery protection

The device has an integrated reverse battery protection feature. This feature protects the driver IC itself and, potentially, also connected LEDs. The output reverse current is limited to $I_{OUT(REV)}$ by the reverse battery protection.

5.2 Output configuration via IN_SET, OUT_SET and PWMI pins

Outputs current can be defined via IN_SET and OUT_SET (to drive additional devices without further external components) pin.

5.2.1 IN_SET pin

The IN_SET pin is a multiple function pin for the output current definition and input control.

Output current definition and analog dimming control can be done defining accordingly the IN_SET current.

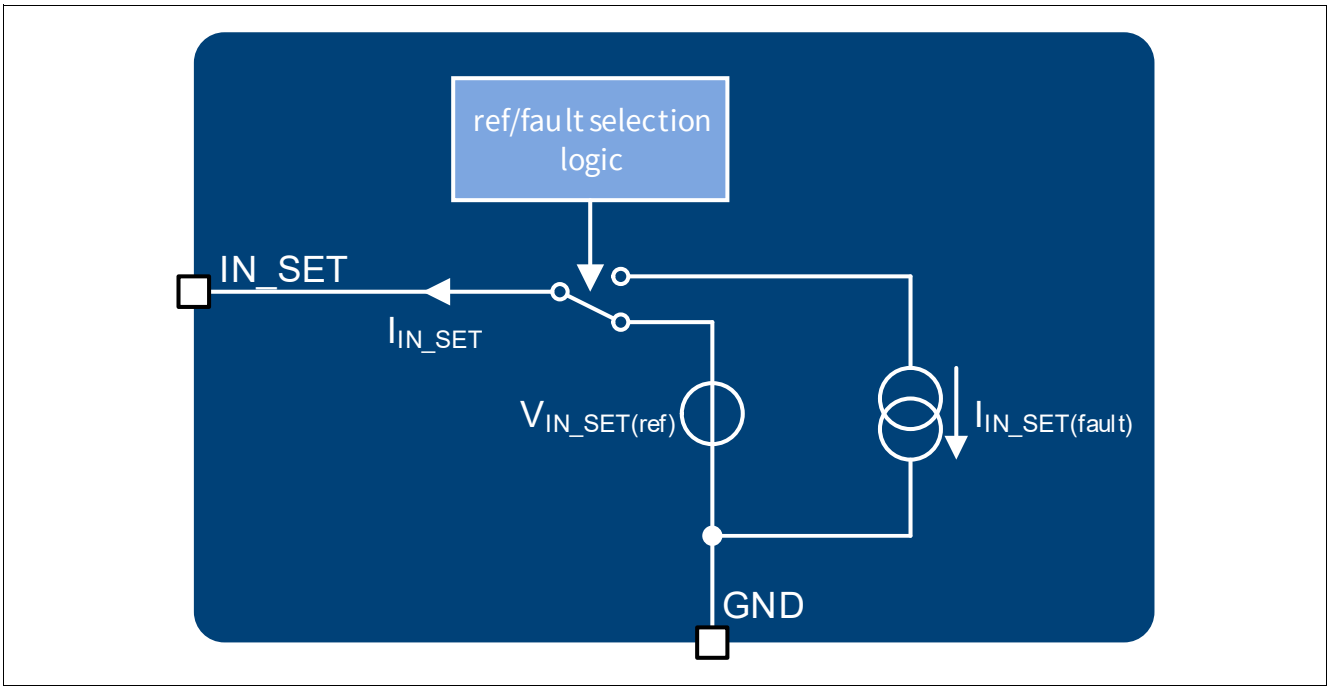


Figure 6 IN_SET pin block diagram

5.2.2 Output current adjustment via R_{SET}

The output current for the channel can be defined connecting a low power resistor (R_{SET}) between the IN_SET pin and GND. The dimensioning of the resistor can be done using the formula:

$$I_{OUT} = k \cdot I_{IN_SET} = k \cdot V_{IN_SET(ref)} / R_{SET} \quad (5.1)$$

The gain factor k (defined as the ratio I_{OUT}/I_{IN_SET}) is graphically described in **Figure 7**.

The current through the R_{SET} is defined by the resistor itself and the reference voltage $V_{IN_SET(ref)}$, which is applied to the IN_SET pin when the device is supplied and the channel enabled.

5.2.3 Output control via IN_SET

The IN_SET pin can be connected via R_{SET} to the open-drain output of a microcontroller or to an external NMOS transistor as described in **Figure 9**. This signal can be used to turn off the relative output stages of the IC.

A minimum IN_SET current of $I_{IN_SET(ACT)}$ is required to turn on the output stages. This feature is implemented to prevent glowing of LEDs caused by leakage currents on the IN_SET pin, see again **Figure 7** for details.

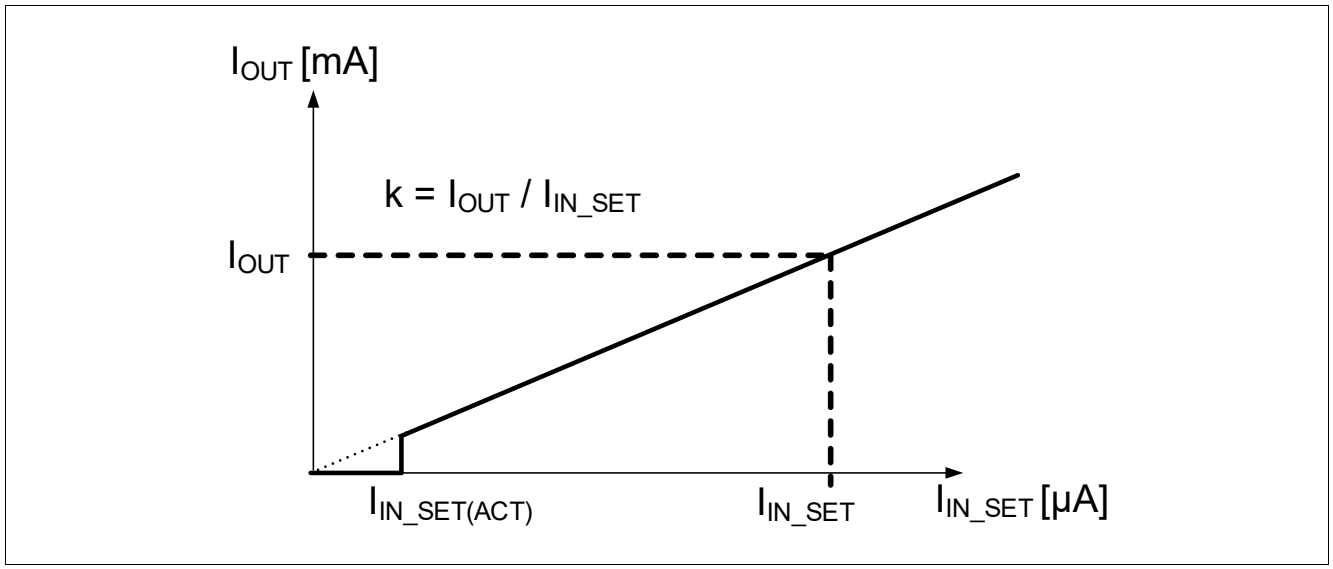


Figure 7 I_{OUT} **vs** I_{IN_SET}

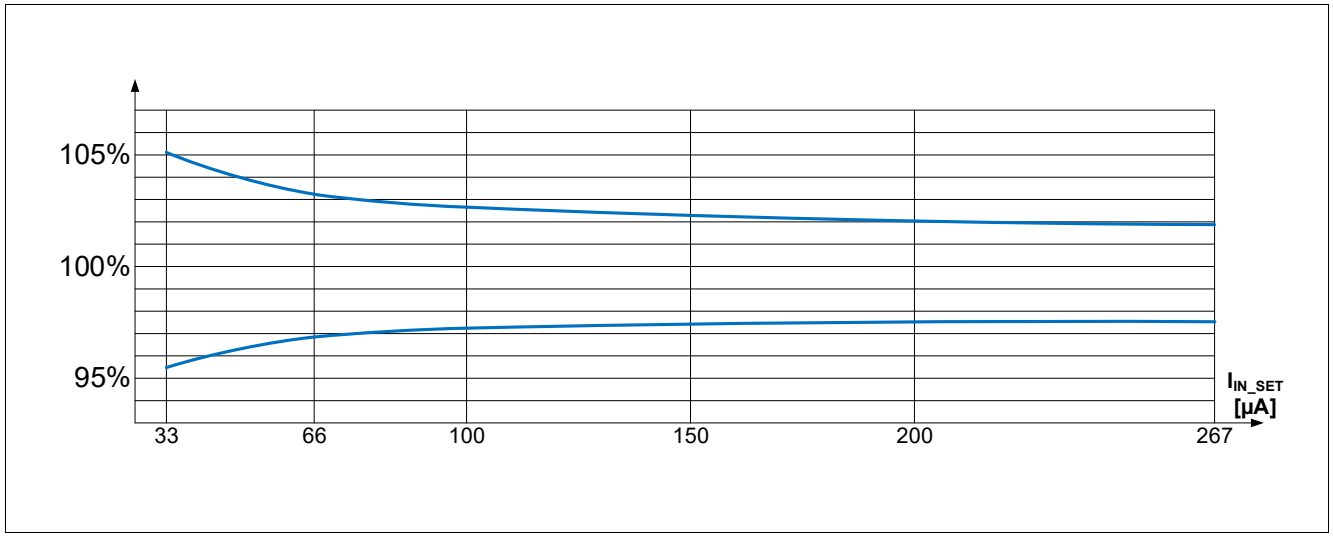


Figure 8 **Typical output current accuracy** I_{OUT} **/** I_{IN_SET} **at** T_J **= 25°C**

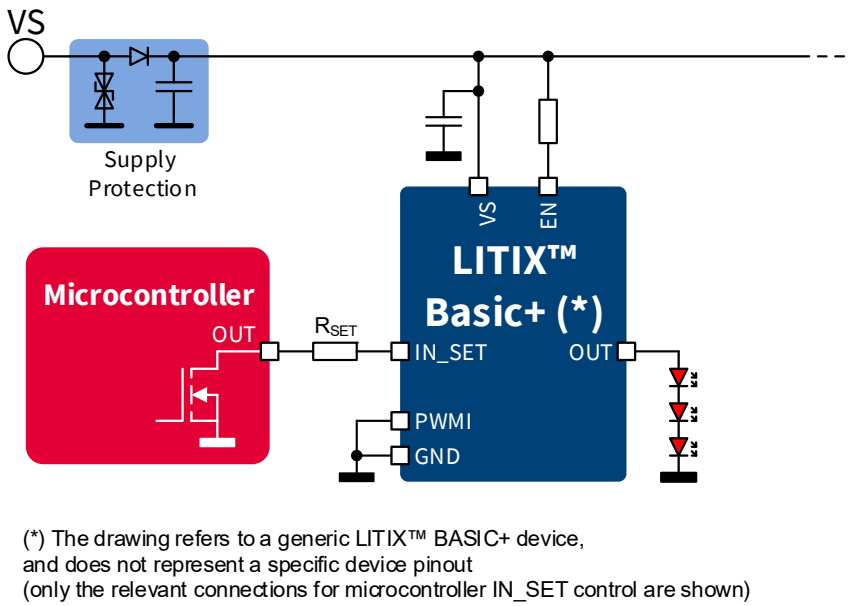


Figure 9 Output control via IN_SET pin and open-drain microcontroller out (simplified diagram)

5.2.4 IN_SET pin behavior during device fault management

If a fault condition arises on the channel controlled by the IN_SET pin, once the D-pin reaches the high level threshold $V_{D(th)}$, the current of the IN_SET pin is reduced to $I_{IN_SET(fault)}$, in order to minimise the current consumption of the whole device under fault condition (detailed description is in the load diagnosis section, **Chapter 6**).

5.2.5 OUT_SET pin

The OUT_SET pin, mirroring the IN_SET current defined by the external resistor R_{SET}, can be used to define the IN_SET current of an additional companion device.

If minimum IN_SET activation current $I_{IN_SET(act)}$ is not reached or if the D-pin reaches the high level threshold $V_{D(th)}$ the OUT_SET current is reduced to $I_{OUT_SET(OFF)}$. This allows to drive other devices via OUT_SET, even when digital dimming is required, without external components (see application drawing example in **Chapter 8**).

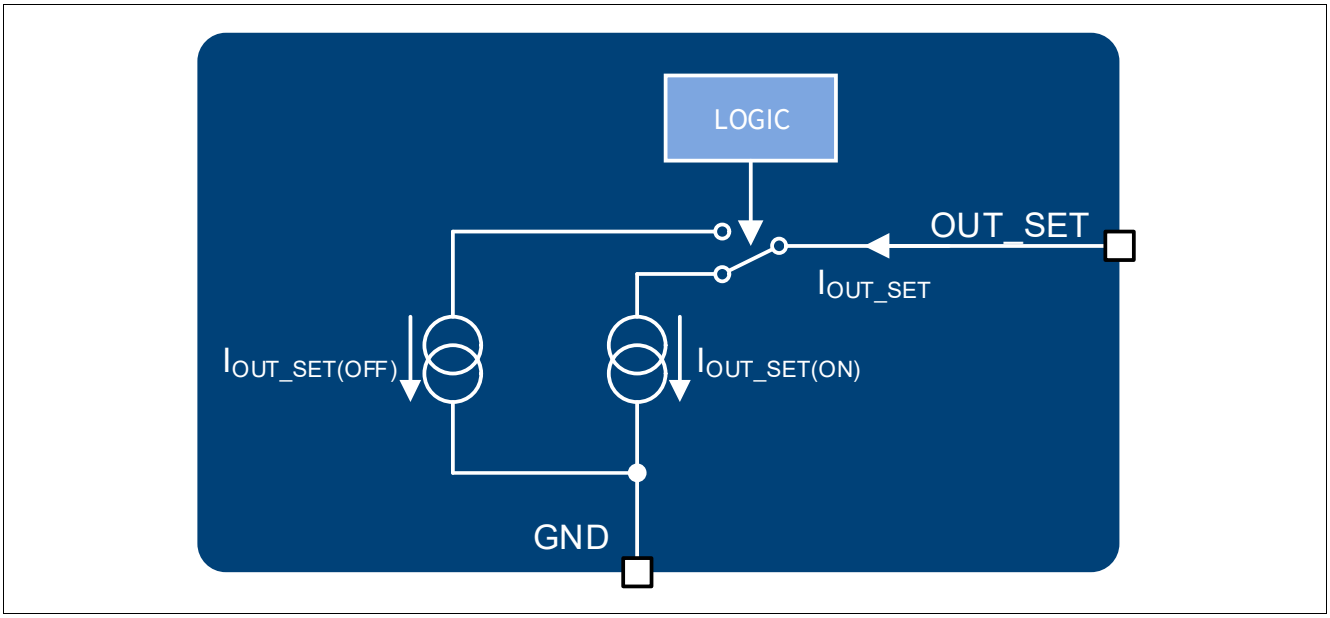


Figure 10 OUT_SET pin block diagram

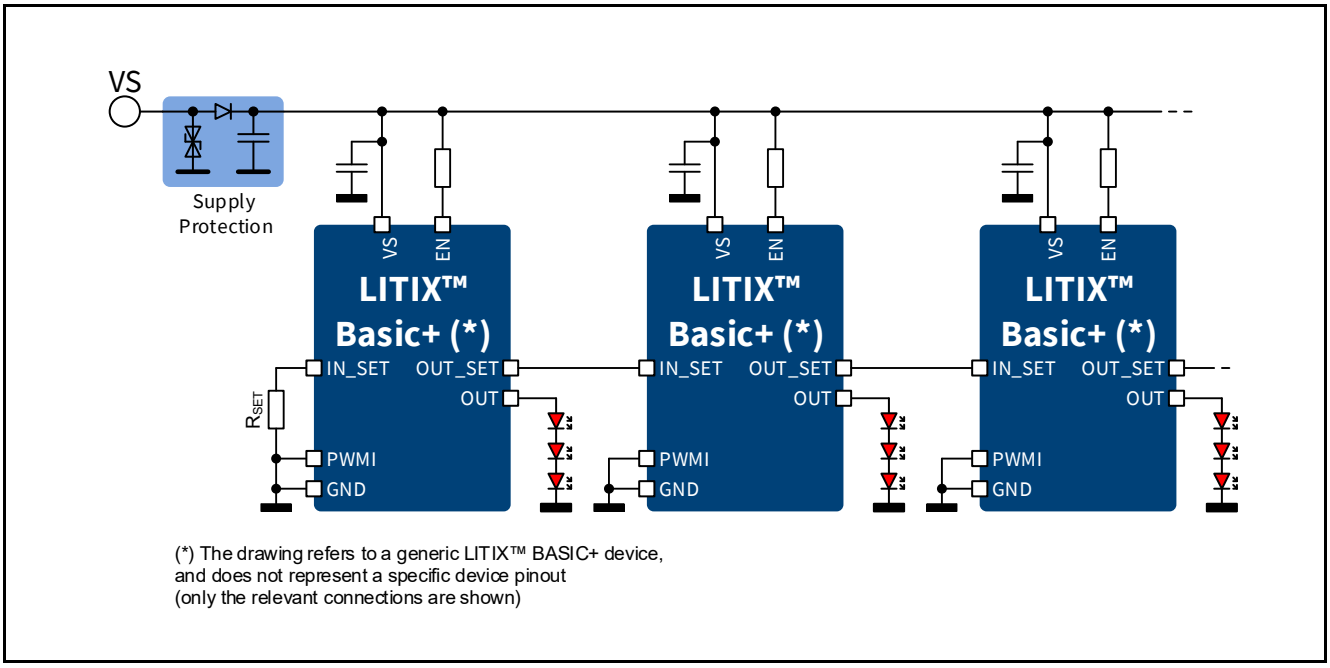


Figure 11 IN_SET to OUT_SET serial connection example

5.2.6 Direct control of PWMI

PWMI input can be controlled by the PWMO output of another device of LITIX™ Basic+ family or, alternatively, a push-pull output stage of a microcontroller: the host device decides the digital dimming characteristics by applying the proper control cycle in order to set the “on”/“off” timing, according to the chosen dimming function.

5.2.7 Timing diagrams

In the following diagrams (**Figure 12**, **Figure 14**) the influences of different driving inputs on output activation delays are shown.

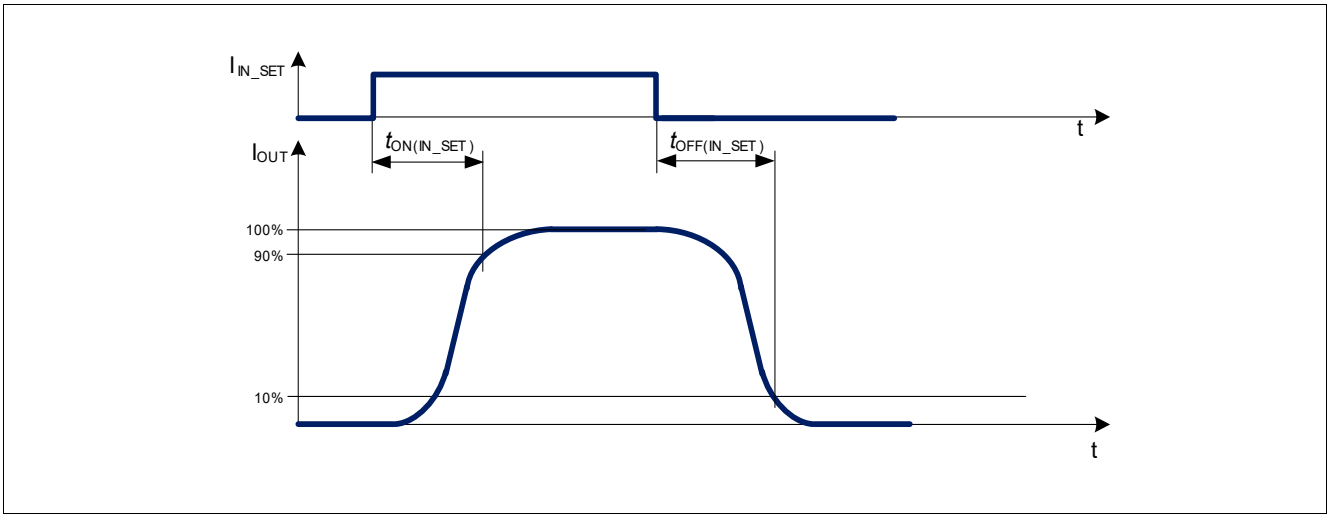


Figure 12 IN_SET turn on and turn off delay timing diagram

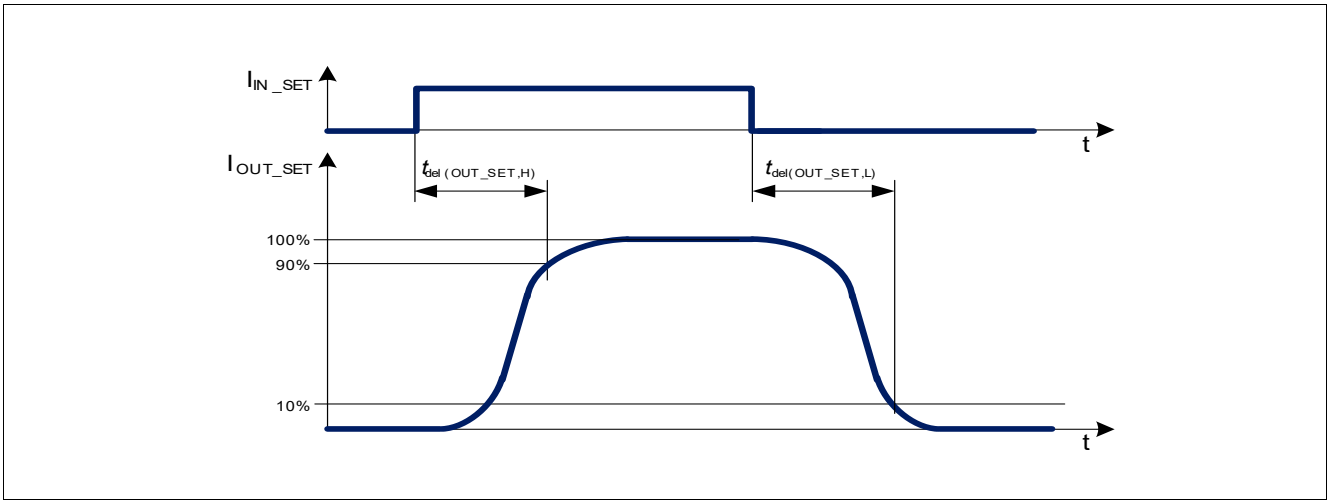


Figure 13 IN_SET to OUT_SET activation and deactivation delay timing diagram

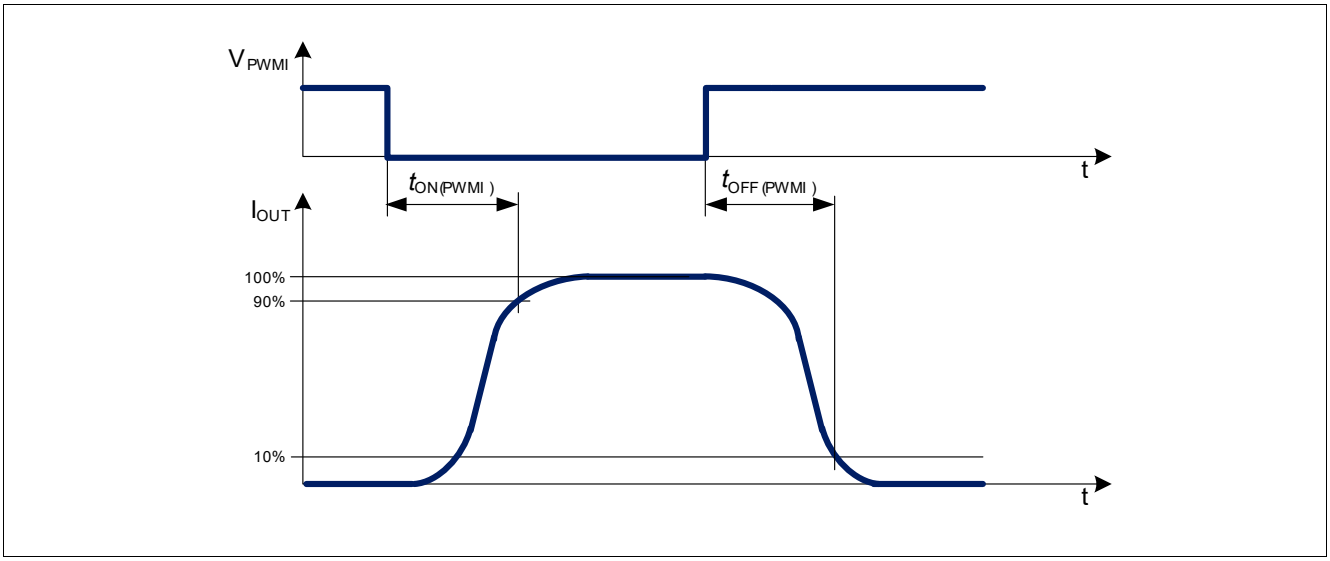


Figure 14 PWMI turn on and turn off timing diagram

5.3 Electrical characteristics power stage

Table 6 Electrical characteristics: Power stage

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current	$I_{OUT(leak)}$	–	–	9	µA	1) V_{EN} = 5.5 V I_{IN_SET} = 0 µA V_{OUT} = 2.5 V T_J = 85°C	P_6.5.51
Output leakage current	$I_{OUT(leak)}$	–	–	21	µA	1) V_{EN} = 5.5 V I_{IN_SET} = 0 µA V_{OUT} = 2.5 V T_J = 150°C	P_6.5.60
Reverse output current	$I_{OUT(rev)}$	–	–	3	µA	1) V_{EN} = V_s V_S = -18 V Output load: LED with break down voltage < - 0.6 V	P_6.5.2
Output current accuracy							
Output current accuracy	K_{LT}	852	900	948	–	1) T_J = 25... 115°C V_S = 8... 18 V V_{PS} = 2 V I_{IN_SET} = 33 µA	P_6.5.53
Output current accuracy	K_{ALL}	843	900	957	–	1) T_J = -40... 115°C V_S = 8... 18 V V_{PS} = 2 V I_{IN_SET} = 33 µA	P_6.5.54
Output current accuracy	K_{LT}	861	900	939	–	1) T_J = 25... 115°C V_S = 8... 18 V V_{PS} = 2 V I_{IN_SET} = 66 µA	P_6.5.55
Output current accuracy	K_{ALL}	852	900	948	–	1) T_J = -40... 115°C V_S = 8... 18 V V_{PS} = 2 V I_{IN_SET} = 66 µA	P_6.5.56
Output current accuracy	K_{LT}	870	900	930	–	1) T_J = 25... 115°C V_S = 8... 18 V V_{PS} = 2 V I_{IN_SET} = 200 µA	P_6.5.57
Output current accuracy	K_{ALL}	861	900	939	–	1) T_J = -40... 115°C V_S = 8... 18 V V_{PS} = 2 V I_{IN_SET} = 200 µA	P_6.5.58

Table 6 Electrical characteristics: Power stage (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	1.0	–	–	V	2) V_S = 8... 18 V I_{OUT} > 90% of $K_{(typ)}$*I_{IN_SET}	P_6.5.36
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.65	–	–	V	2) V_S = 8... 18 V I_{IN_SET} = 133 µA I_{OUT} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = -40°C	P_6.5.37
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.75	–	–	V	2) V_S = 8... 18 V I_{IN_SET} = 133 µA I_{OUT} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = 25°C	P_6.5.38
Required voltage drop during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.85	–	–	V	2) V_S = 8... 18V I_{IN_SET} = 133 µA I_{OUT} > 90% of $K_{(typ)}$*I_{IN_SET} T_J = 150°C	P_6.5.39
Required supply voltage for current control	$V_{S(CC)}$	5.5	–	–	V	V_{EN} = 5.5 V V_{OUT} = 3 V R_{IN_SET} = 6.8 kΩ I_{OUT} > 90% of K*I_{IN_SET}	P_6.5.40
Required output voltage for current control	$V_{OUT(CC)}$	1.4	–	–	V	V_S = 8... 18 V I_{OUT} > 90% of K*I_{IN_SET}	P_6.5.41
Current reduction temperature threshold	$T_{J(CRT)}$	–	140	–	°C	1)	P_6.5.44
Output current during current reduction at high temperature	$I_{OUT(CRT)}$	85% of $I_{OUT(typ)}$	–	–	mA	1) T_J = 150°C	P_6.5.45

1) Not subjected to production test: specified by design

2) In these test conditions, the parameter $K_{(typ)}$ represents the typical value of output current accuracy.

5.4 Electrical characteristics IN_SET, OUT_SET and PWMI pins for output settings

Table 7 Electrical characteristics: IN_SET, OUT_SET and PWMI pins

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET reference voltage	$V_{IN_SET(ref)}$	1.195	1.22	1.245	V	[1] V_{EN} = 5.5 V T_J = 25°C	P_6.6.1
IN_SET reference voltage	$V_{IN_SET(ref)}$	1.184	1.22	1.256	V	[1] V_{EN} = 5.5 V T_J = -40... 115°C	P_6.6.17
IN_SET output activation current	$I_{IN_SET(ACT)}$	–	–	15	µA	V_{EN} = 5.5 V V_{PS} = 3 V I_{OUT} > 50% of $K_{(typ)}$*I_{IN_SET}	P_6.6.2
OUT_SET output current matching	$\Delta I_{OUT_SET(ON)}/I_{IN_SET}$	-4	–	4	%	V_S = 8 V to 18 V V_{OUT_SET} = 1.2V I_{IN_SET} = 267 µA	P_6.6.3
Timing							
IN_SET turn on time	$t_{ON(IN_SET)}$	–	–	20	µs	[1][2] V_S = 13.5 V V_{PS} = 4 V I_{IN_SET} rising from 0 to 180 µA I_{OUT} = 90% of K*I_{IN_SET}	P_6.6.8
IN_SET turn off time	$t_{OFF(IN_SET)}$	–	–	10	µs	[1][2] V_S = 13.5 V V_{PS} = 4 V I_{IN_SET} falling from 180 to 0 µA I_{OUT} = 10% of K*I_{IN_SET}	P_6.6.9
OUT_SET activation time	$t_{del(OUT_SET,H)}$	–	–	5	µs	[1][3] V_S = 13.5 V I_{IN_SET} rising from 0 to 180 µA I_{OUT_SET} = 90% of I_{IN_SET}	P_6.6.10
OUT_SET deactivation time	$t_{del(OUT_SET,L)}$	–	–	5	µs	[1][3] V_S = 13.5 V I_{IN_SET} falling from 180 to 0 µA I_{OUT_SET} = 10% of I_{IN_SET}	P_6.6.11

Table 7 Electrical characteristics: IN_SET, OUT_SET and PWMI pins (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI turn on time	$t_{ON(PWMI)}$	–	–	15	µs	[1)4)] V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} falling from 5 V to 0 V I_{OUT} = 90% of $K^*I_{IN_SET}$ T_J = -40... 115°C	P_6.6.12
PWMI turn off time	$t_{OFF(PWMI)}$	–	–	10	µs	[1)4)] V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} = 0 rising from 0 V to 5 V I_{OUT} = 10% of $K^*I_{IN_SET}$ T_J = -40... 115°C	P_6.6.13

1) Not subjected to production test: specified by design
2) Refer to **Figure 12**
3) Refer to **Figure 13**
4) Refer to **Figure 14**

6 Load diagnosis

6.1 Error management via ERRN and D-pins

Several diagnosis features are integrated in the TLD2142-1EP:

- Open load detection (OL).
- Short circuit OUT-GND (SC).

6.1.1 ERRN pin

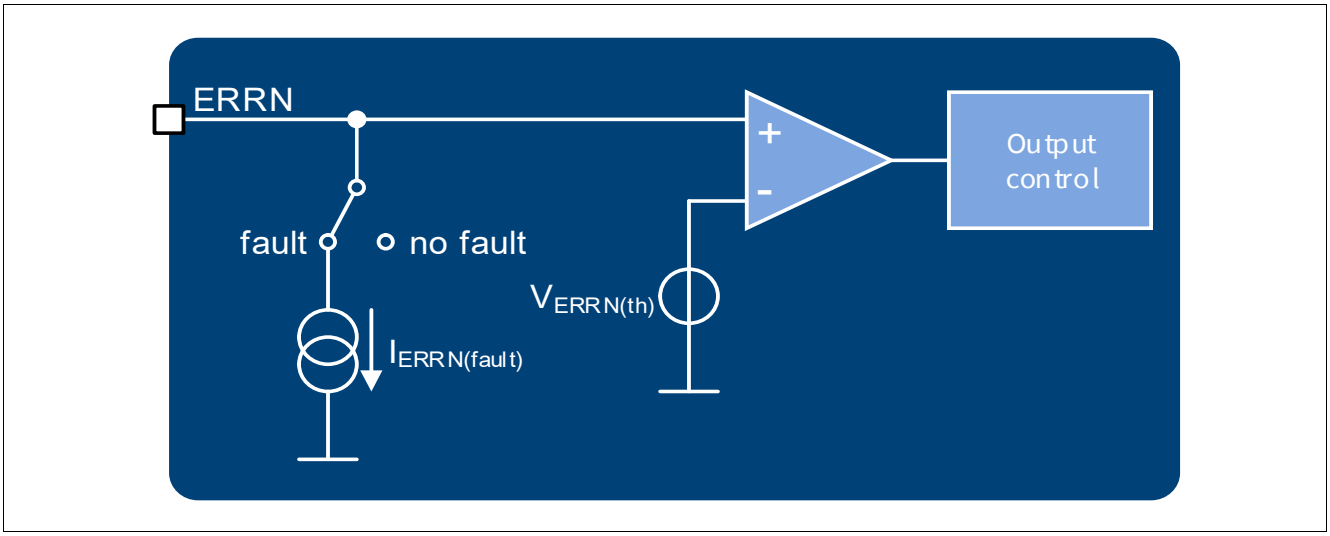


Figure 15 ERRN pin (block diagram)

The device is able to report a detected failure in its driven load and react to a fault detected by another LED driver in the system if a shared error network is implemented (i. e. driving LED chains of the same light function). This is possible with the usage of an external pull-up resistor, allowing multiple devices to share the open drain diagnosis output pin ERRN. All devices sharing the common error network are capable to detect the fault from any of the channels driven by the LITIX™ Basic+ LED drivers and, if desired, to switch multiple loads off.

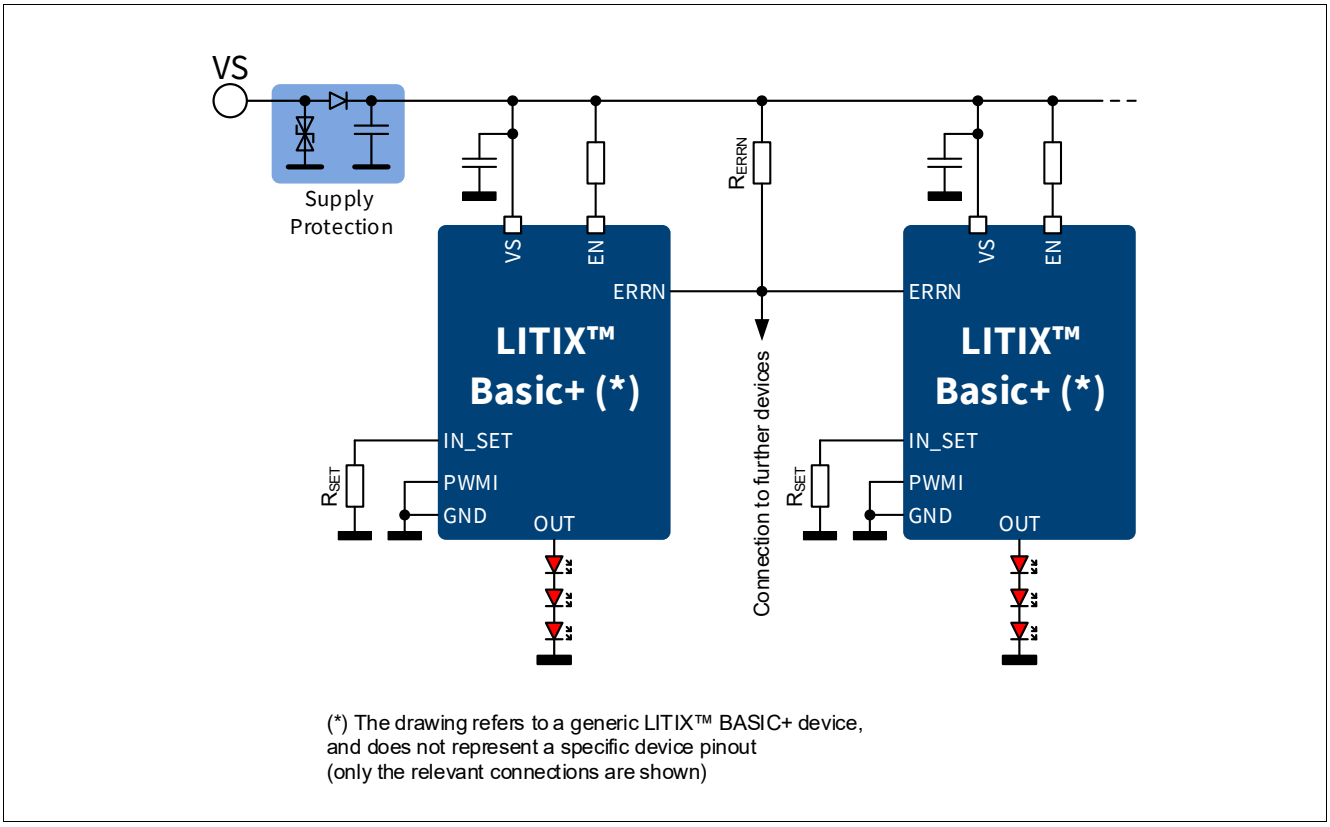


Figure 16 Shared error network principle between LITIX™ Basic+ family devices

When the channel is detected to be under fault conditions (for, at least, a filter time t_{fault}), the open-drain ERRN pin sinks a pull-down current $I_{ERRN(fault)}$ toward GND. Therefore an active low state can be detected at ERRN pin when $V_{ERRN} < V_{ERRN(fault)}$ and if this condition is reached, provided the proper setup of the delay pin D, the channel is switched off. Similarly, when the fault is removed, ERRN pin is put back in high impedance state, and the channels reactivation procedure can be completed once D-pin voltage is below the value $V_{D(th)}$, as illustrated in the timing diagrams in this chapter.

6.1.2 D-pin

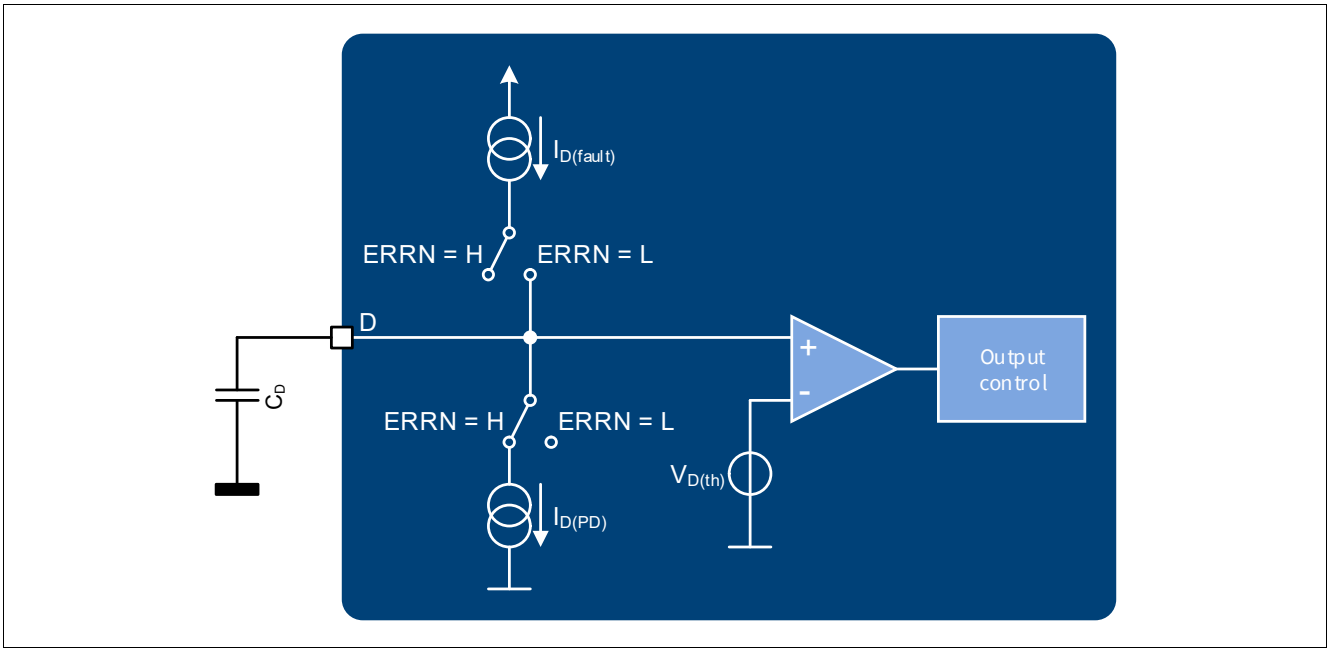


Figure 17 D-pin (block diagram).

The D-pin is designed for 2 main purposes:

- To react to error conditions in LED arrays according to the implemented fault management policy, in systems where multiple LED chains are used for a given light function.
- To extend the channel deactivation delay time of a value t_D, adding a small signal capacitor from the D-pin to GND. In this way, an unstable or noisy fault condition may be prevented from switching off all the channels of a given light function (i.e. driven by several driver ICs sharing the same error network).

The functionality of the D-pin is shown in the **Figure 17** simplified block diagram:

If one LED within one chain fails in open load condition or the device output is shorted to GND, the respective LED chain is off. Different automotive applications require a complete deactivation of a light function, if the desired brightness of the function (LED array) can not be achieved due to an internal error condition.

In normal operative status (no fault) a pull-down current $I_{D(PD)}$ is sunk from the D-pin to GND. If there is a fault condition (for, at least, a filter time t_{fault}) in one of the LED channels driven by the IC or in any of the devices sharing the same ERRN error network line, a pull-up current $I_{D(fault)}$ is instead sourced from the D-pin. As a consequence, if a capacitive or open load is applied at this pin, its voltage starts rising.

When $V_{D(th)}$ is reached at D-pin, all the channels driven by the device are switched off and if other devices share the same ERRN and D-pins nodes, all the devices turn their outputs off.

Alternatively, if the D-pin is tied to GND, only the channel that has been detected with a fault is safely deactivated.

The capacitor value used at the D-pin, C_D, sets the delay times $t_{D(set/reset)}$ according to the following equations:

$$t_{D(set)} = \frac{C_D \cdot V_{D(th)}}{I_{D(fault)}} \quad (6.1)$$

$$t_{D(reset)} = \frac{C_D \cdot (V_{D(CL)} - V_{D(th)})}{I_{D(PD)}} \quad (6.2)$$

6.2 Open Load (OL) and short OUT to GND (SC)

The behavior of the device during overload conditions that lead to an excess of internal heating up to overtemperature condition, is already described in **Chapter 5**.

Open load (OL) and OUT shorted to GND (SC) diagnosis features are also integrated in the TLD2142-1EP.

An open load condition is detected if the voltage drop over the output stage V_{PS} is below the threshold $V_{PS(OL)}$ at least for a filter time t_{fault}.

A short to GND condition is detected if the voltage of the output stages V_{OUT} is below the threshold $V_{OUT(SC)}$ at least for a filter time t_{fault}.

6.2.1 Fault management (D-pin open or connected with a capacitor to GND)

With D-pin open or connected with a capacitor to GND configuration, it is possible to switch off all the channels which share a common error network, without the need of an auxiliary microcontroller. For more details refer also to the timing diagram of **Figure 18**, **Figure 19**.

If there is an OL or SC condition on the output, a pull-up current $I_{OUT(fault)}$ then flows out from the channel, replacing the configured output current (but limited by the actual load impedance, e.g. reduced to zero with an ideal open load). Under these conditions, the ERRN pin starts sinking a current $I_{ERRN(fault)}$ toward GND and (with proper dimensioning of the external pull-up resistor) reaches a voltage level below $V_{ERRN(fault)}$.

After $t_{D(set)}$, the voltage $V_{D(th)}$ is reached at D-pin, the PWMO pin is pulled down and the IN_SET goes in a weak pull-down state with a current consumption $I_{IN_SET(fault)}$ after an additional latency time $t_{IN_SET(del)}$. The ERRN low voltage can also be used as input signal for a microcontroller to perform the desired diagnosis policy.

The OL and SC error conditions are not latched: as soon as the fault condition is no longer present (at least for a filter time t_{fault}) ERRN goes back to high impedance. When its voltage is above $V_{ERRN(fault)}$, the D-pin voltage starts decreasing and after $t_{D(reset)}$ goes below ($V_{D(th)}$ - $V_{D(th,hys)}$). Then the IN_SET voltage up to $V_{IN_SET(ref)}$, again after a time $t_{IN_SET(del)}$: at this point, the output stage are activated again. The total time between the fault removal and the IN_SET reactivation $t_{ERR(reset)}$ is extended by an additional latency which depends on the external ERRN pin pull-up and filter circuitry.

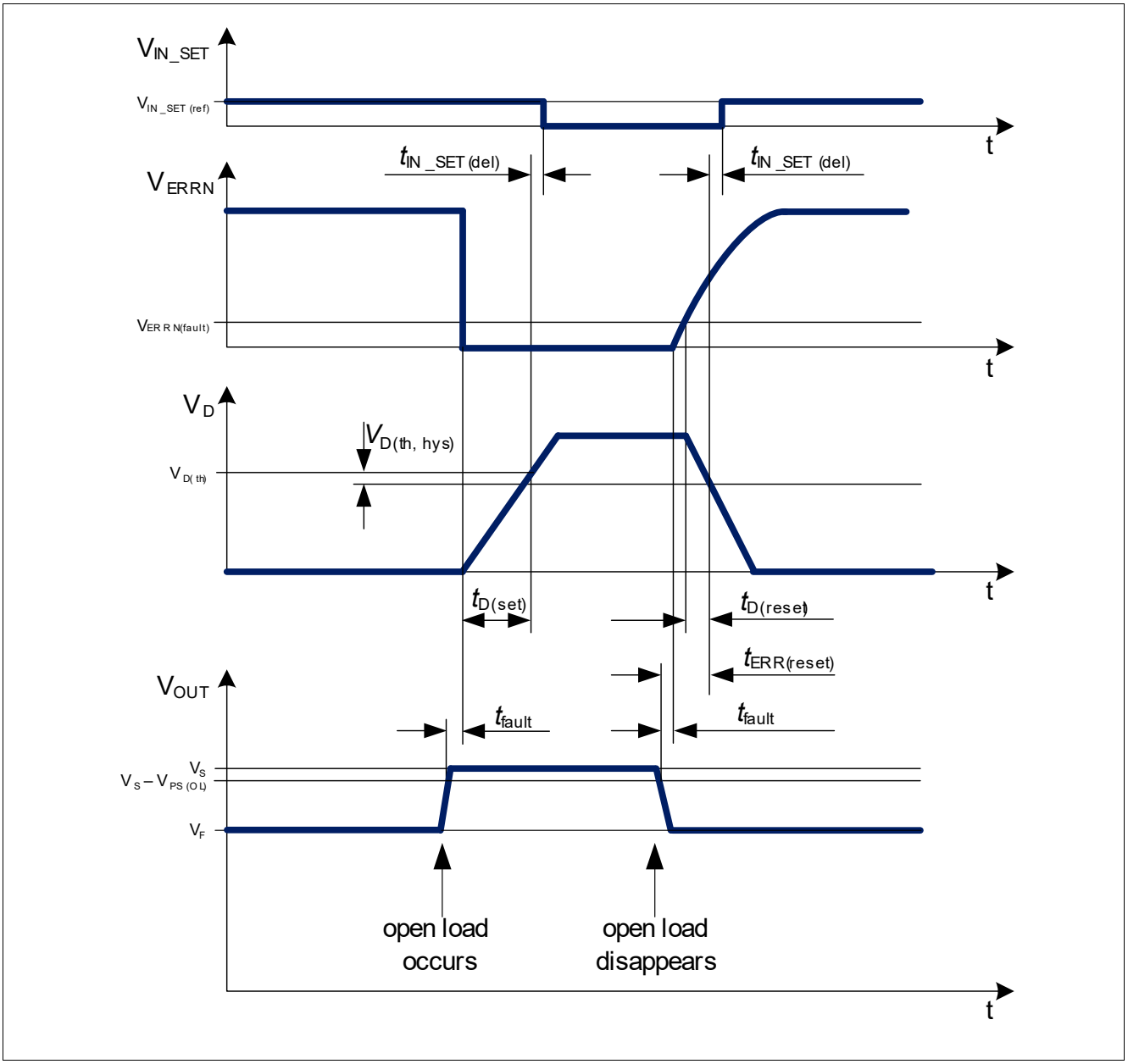


Figure 18 Open load condition timing diagram example (D-pin unconnected or connected to external capacitor to GND, V_F represents the typical forward voltage of the output load)

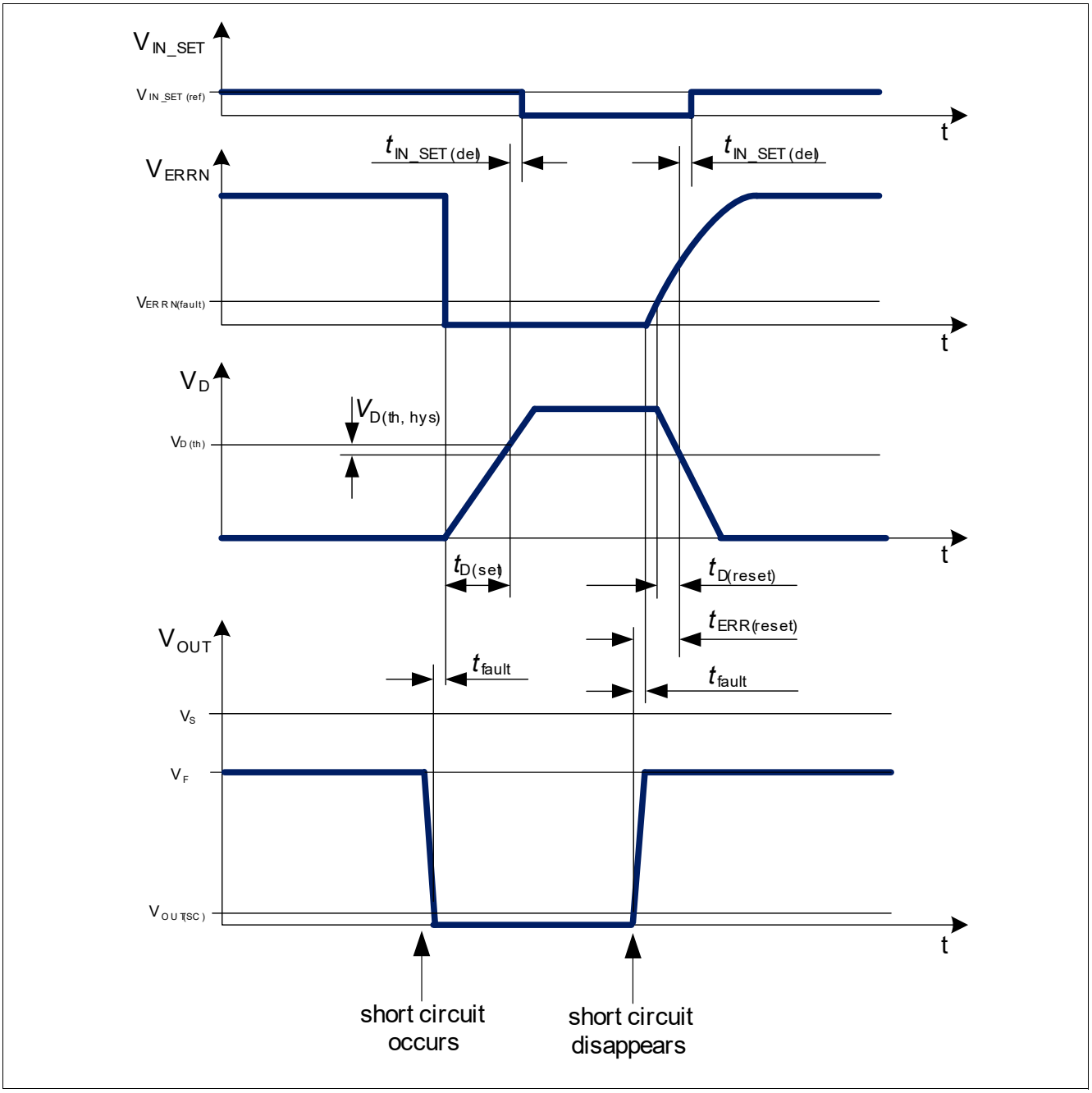


Figure 19 Short circuit to GND condition timing diagram example (D-pin not connected or connected to external capacitor to GND, V_{Fxyz} represents the forward voltage of the output loads)

6.2.2 Fault management (D-pin connected to GND)

With D-pin connected to GND configuration, it is possible to deactivate only the channel under fault conditions, still sharing ERRN pin in a common error network with other devices of LITIX™ Basic+ family.

If there is fault condition on the output, a pull-up current $I_{OUT(fault)}$ flows out from the channel, replacing the configured output current (but limited by the actual load impedance, e.g. reduced to zero with an ideal open load). Under fault conditions the ERRN pin starts sinking a current $I_{ERRN(fault)}$ to ground and the voltage level on this pin will drop below $V_{ERRN(fault)}$ if the external pull-up resistor is properly dimensioned. The ERRN low voltage can also be used as input signal for a µC to perform the desired diagnosis policy.

Load diagnosis

The fault status is not latched: as soon as the fault condition is no longer present (at least for a filter time t_{fault}), ERRN goes back to high impedance and, once its voltage is above $V_{ERRN(fault)}$, finally the output stages are activated again.

Examples of open load or short to GND diagnosis with D-pin open or connected to GND are shown in the timing diagrams of **Figure 20** and **Figure 21**.

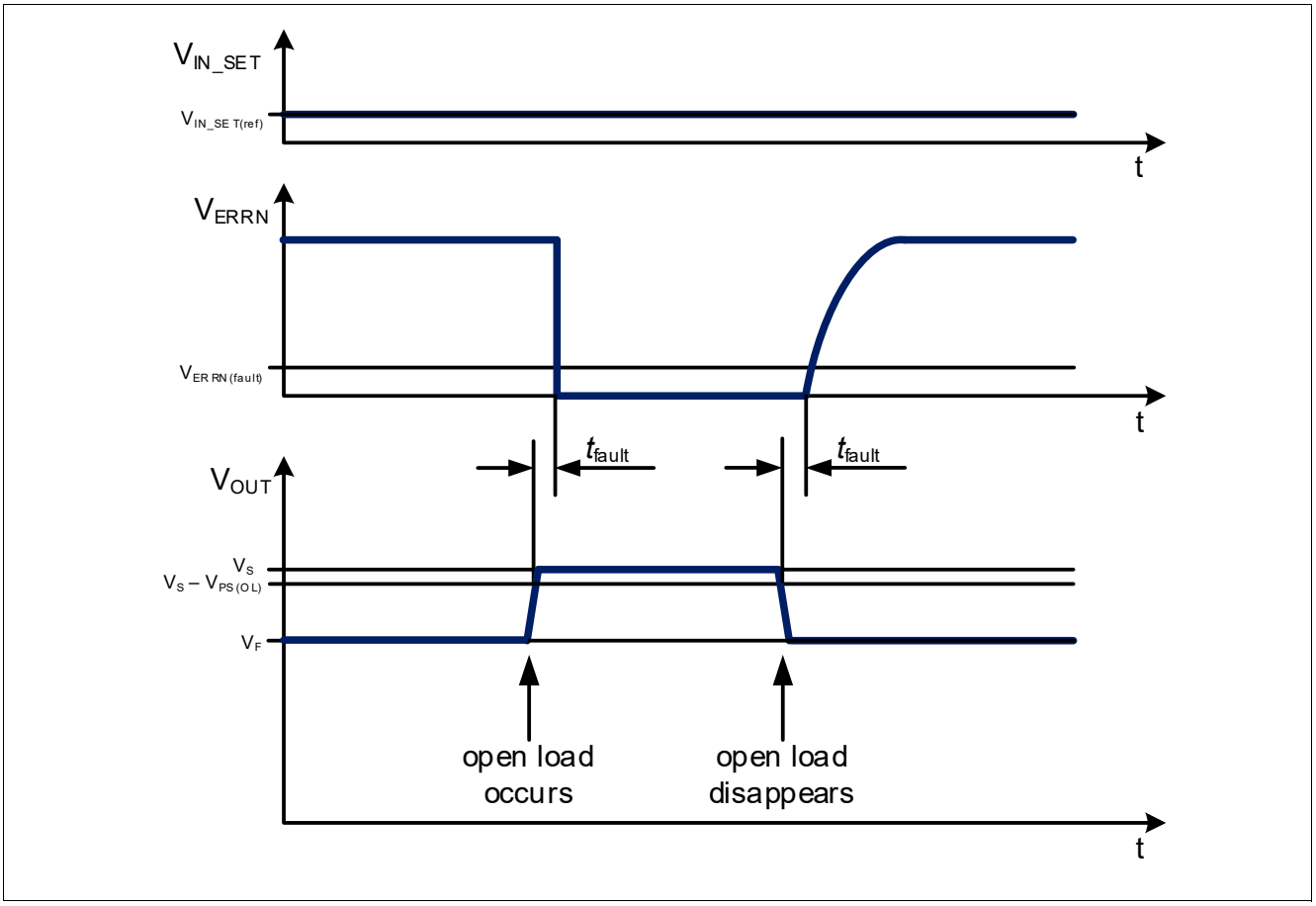


Figure 20 Open load condition timing diagram example (D-pin connected to GND, V_F represents the forward voltage of the output load)

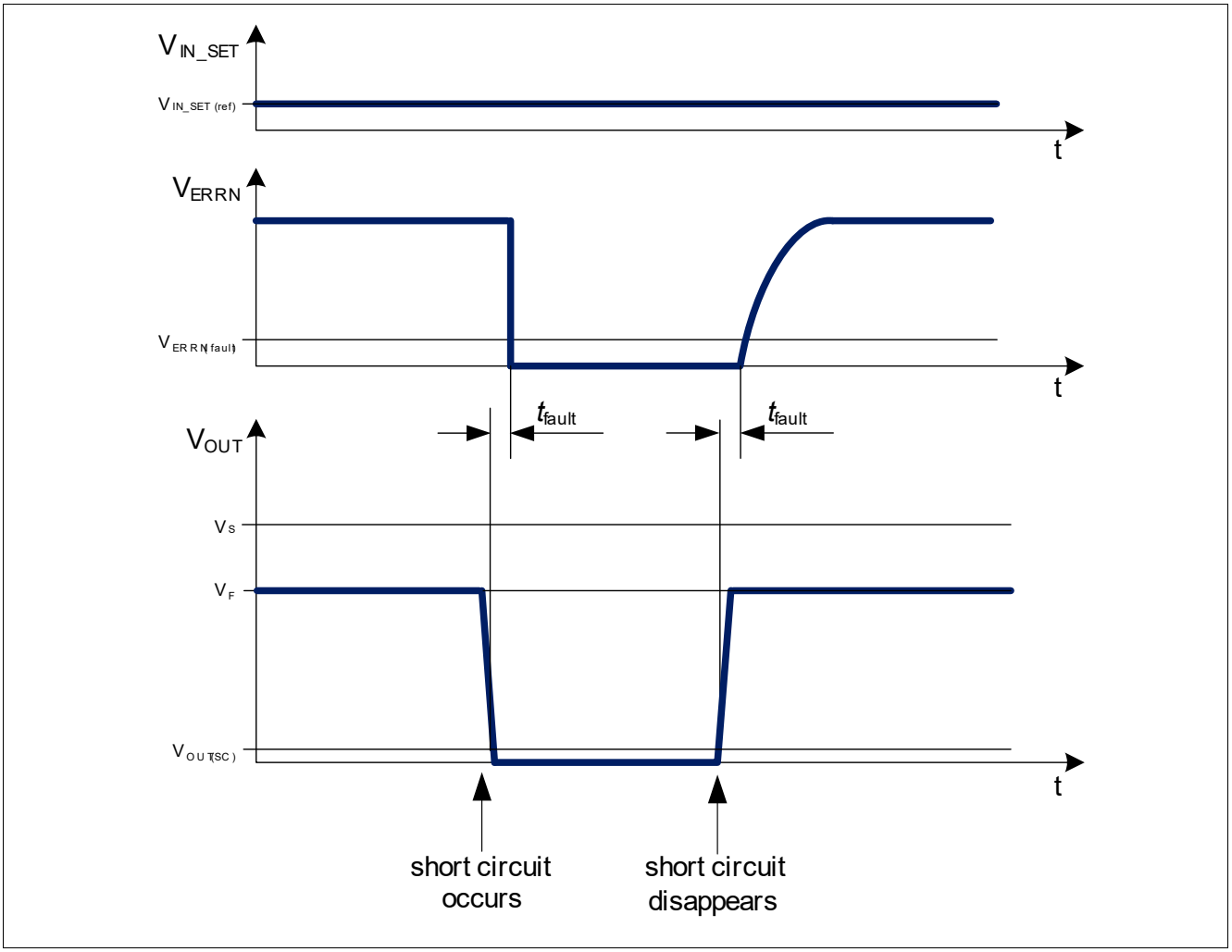


Figure 21 Short circuit condition timing diagram example (D-pin connected to GND, V_F represents the forward voltage of the output load)

6.3 Electrical characteristics: Load diagnosis and Overload management

Table 8 Electrical Characteristics: Fault management

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IN_SET fault current	$I_{IN_SET(fault)}$	–	–	10	µA	[1] V_S > 8 V V_{OUT} = 3.6 V V_{ERRN} = 0 V V_{IN_SET} = 1 V D open V_{EN} > $V_{DEN(th,max)}$	P_7.5.1
ERRN fault current	$I_{ERRN(fault)}$	2	–	–	mA	[1] V_S > 8 V V_{ERRN} = 0.8 V Fault condition V_{EN} > $V_{DEN(th,max)}$	P_7.5.2

Table 8 Electrical Characteristics: Fault management (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ERRN input threshold	$V_{ERRN(th)}$	0.8	–	2.0	V	[1] V_S > 8 V	P_7.5.3
OL detection threshold	$V_{PS(OL)}$	0.2	–	0.4	V	V_S > 8 V V_{EN} > $V_{DEN(th, max)}$	P_7.5.5
SC detection threshold	$V_{OUT(SC)}$	0.8	–	1.35	V	V_S > 8 V V_{EN} > $V_{DEN(th, max)}$	P_7.5.6
Fault detection current	$I_{OUT(fault)}$	50	–	180	µA	V_S > 8 V V_{OUT} = 0 V V_{EN} > $V_{DEN(th, max)}$	P_7.5.7
D-pin							
Threshold voltage for function de-activation	$V_{D(th)}$	1.4	1.7	2	V	V_S > 8 V V_{EN}= 5.5 V	P_7.5.8
Threshold hysteresis	$V_{D(hys)}$	–	100	–	mV	[1] V_S > 8 V V_{EN} = 5.5 V V_{OUT} = $V_{OUT(OL)}$	P_7.5.9
Fault pull-up current	$I_{D(fault)}$	20	35	50	µA	V_S > 8 V V_{OUT} = $V_{OUT(OL)}$ V_D = 2 V	P_7.5.10
Pull-down current	$I_{D(PD)}$	40	60	95	µA	V_S > 8 V V_{EN} = 5.5 V V_D = 1.4 V V_{ERRN} = 2 V V_{PS} = 3 V No fault conditions	P_7.5.11
Internal clamp voltage	$V_{D(CL)}$	4	–	6	V	V_S > 8 V V_{OUT} = $V_{OUT(OL)}$ D-pin open	P_7.5.12
Timing							
Fault to ERRN activation delay	t_{fault}	40	–	150	µs	[1] V_S > 8 V V_{OUT} rising from 5 V to V_S V_{EN} > $V_{DEN(th, max)}$	P_7.5.19
Fault appearance/removal to IN_SET deactivation/activation delay	$t_{IN_SET(del)}$	–	–	10	µs	[1] V_S > 8 V OUT open D rising from 0 V to 5 V V_{EN} > $V_{DEN(th, max)}$	P_7.5.20

1) Not subjected to production test: specified by design.

7 PWM control (Digital dimming)

Digital dimming via PWM control is commonly practiced to adjust luminous intensity, preventing color shift of the LED light source.

7.1 PWM unit

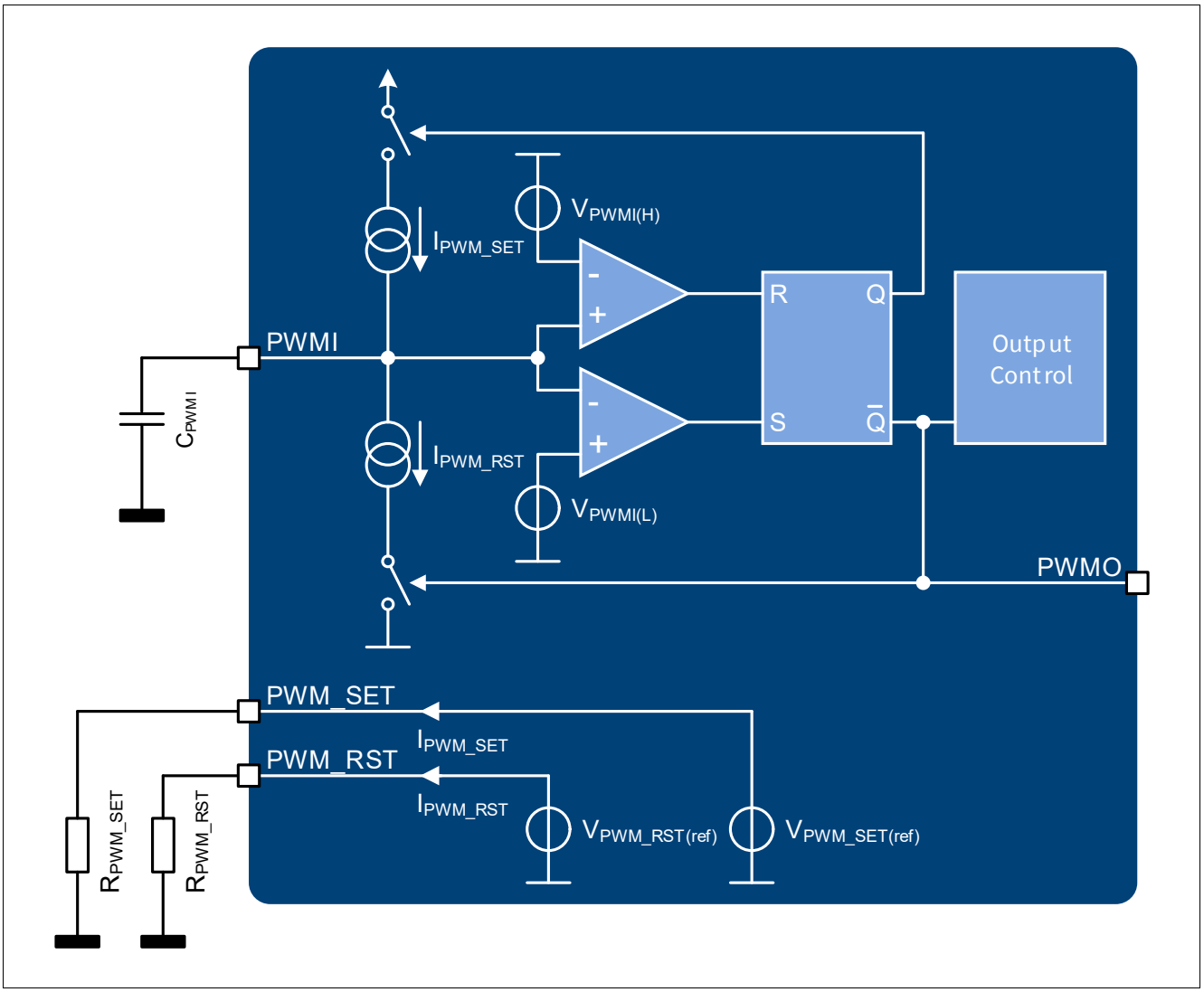


Figure 22 PWM unit concept diagram (including PWMO drive and typical external circuitry)

The PWM unit can be configured connecting a resistor on each of PWM_SET and PWM_RST configuration pins and a capacitor to the PWMI pin. This setup (provided that $V_{EN} > V_{EN(th)}$ and $V_S > V_{SUV(ON)}$) enables the internal Pulse Width Modulation (PWM) generator to drive the PWMO pin with a digital signal, which represents the desired PWM frequency and Duty Cycle (DC).

With reference to the block diagram of **Figure 22** the current flowing through PWM_SET and PWR_RST reference pins (I_{PWM_SET} and I_{PWM_RST}) are replicated to charge or discharge the capacitor C_{PWMI}

The following figure shows the charging and discharging phases defined by the chosen external components, according to **Figure 23** and the internal PWM unit.

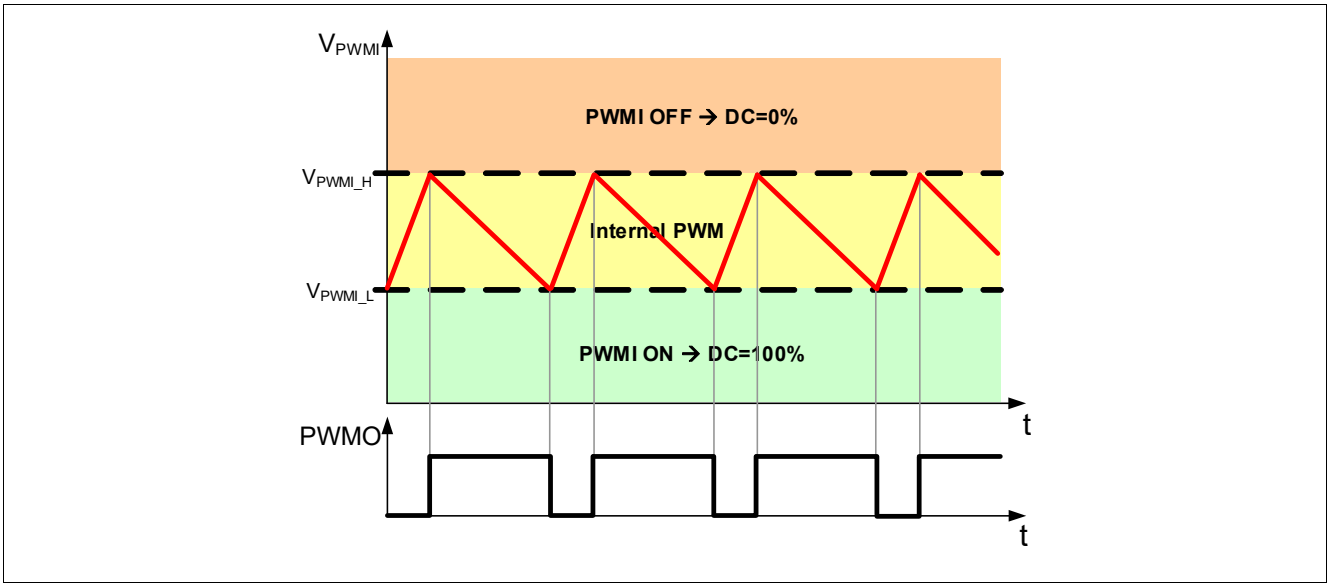


Figure 23 PWMI operating voltages and timing diagram example

The PWM typical characteristics can be adjusted using the formulas below.

$$t_{PWM(ON)} = \frac{C_{PWMI}}{I_{PWM_SET}}\left(V_{PWMI(H)} - V_{PWMI(L)}\right) = \frac{R_{PWM_SET} C_{PWMI}}{V_{REF_SET}}\left(V_{PWMI(H)} - V_{PWMI(L)}\right) \quad (7.1)$$

$$t_{PWM(OFF)} = \frac{C_{PWMI}}{I_{PWM_RST}}\left(V_{PWMI(H)} - V_{PWMI(L)}\right) = \frac{R_{PWM_RST} C_{PWMI}}{V_{REF_RST}}\left(V_{PWMI(H)} - V_{PWMI(L)}\right) \quad (7.2)$$

$$f_{PWMI} = \frac{1}{t_{PWMI(ON)} + t_{PWMI(OFF)}} = \frac{V_{REF_SET/RST}}{V_{PWMI(H)} - V_{PWMI(L)}} \cdot \frac{1}{\left(R_{PWM_SET} + R_{PWM_RST}\right) C_{PWMI}} \quad (7.3)$$

$V_{REF_SET/RST}$ is equal to 1.22 V. See P_8.4.12 and P_8.4.13.

$$DC_{PWMI} = \frac{t_{PWMI(ON)}}{t_{PWMI(ON)} + t_{PWMI(OFF)}} = \frac{R_{PWM_SET}}{R_{PWM_SET} + R_{PWM_RST}} \quad (7.4)$$

From these equations, the proper value C_{PWMI}, R_{PWM_SET} and R_{PWM_RST} can be calculated, according to the electrical characteristics defined in **Table 9**.

7.2 Direct control of PWMI

The PWM engine also drives the internal channel and, via the PWMO output pin, the PWM control can be used to synchronize other devices of the LITIX™ Basic+ family.

PWMI input can be also controlled by the PWMO output of another device of LITIX™ Basic+ family or, alternatively, a push-pull output stage of a microcontroller: the host device decides the digital dimming characteristics by applying the proper control cycle in order to set the “on”/”off” timing, according to the chosen dimming function.

7.3 Timing diagrams

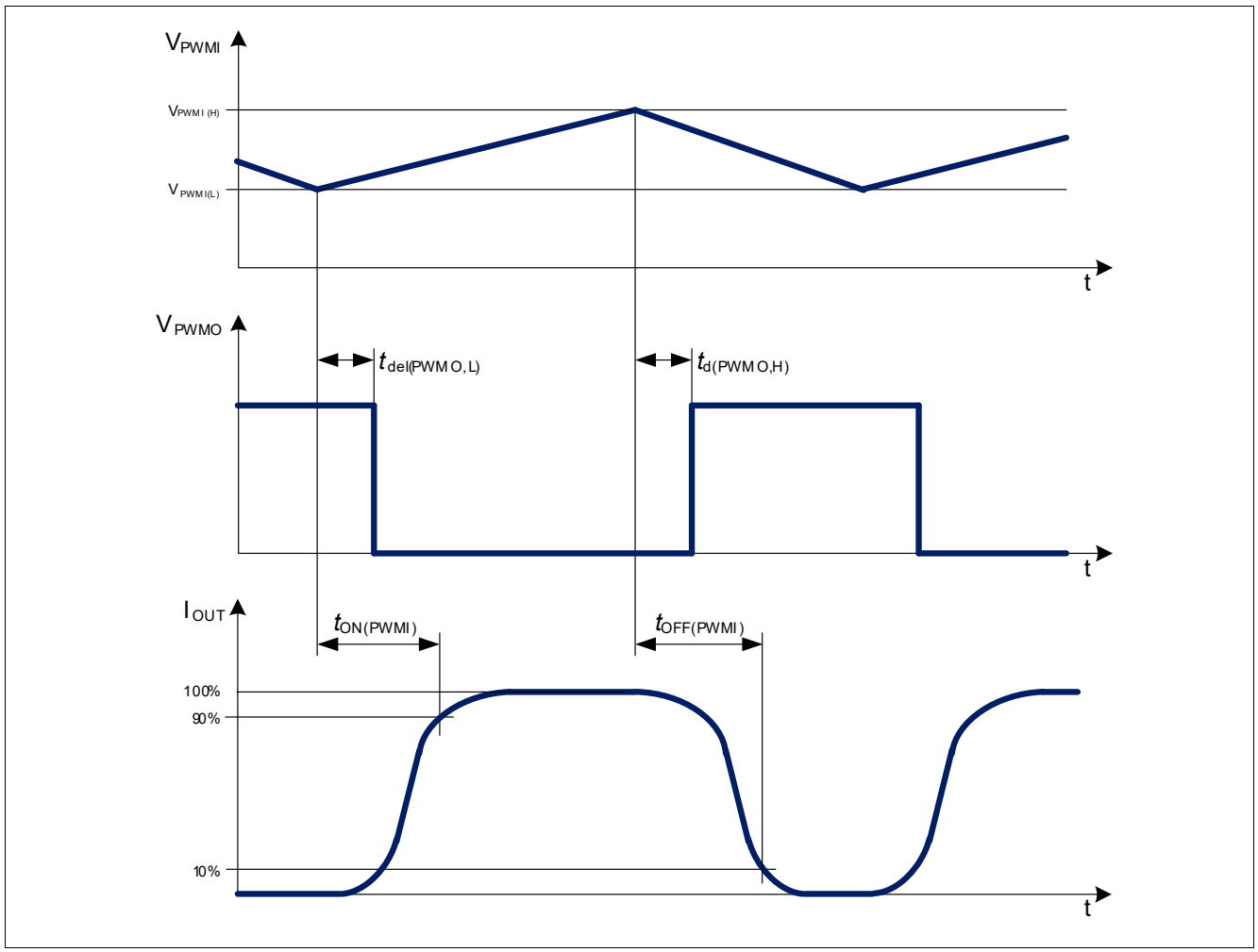


Figure 24 PWM engine timing overview

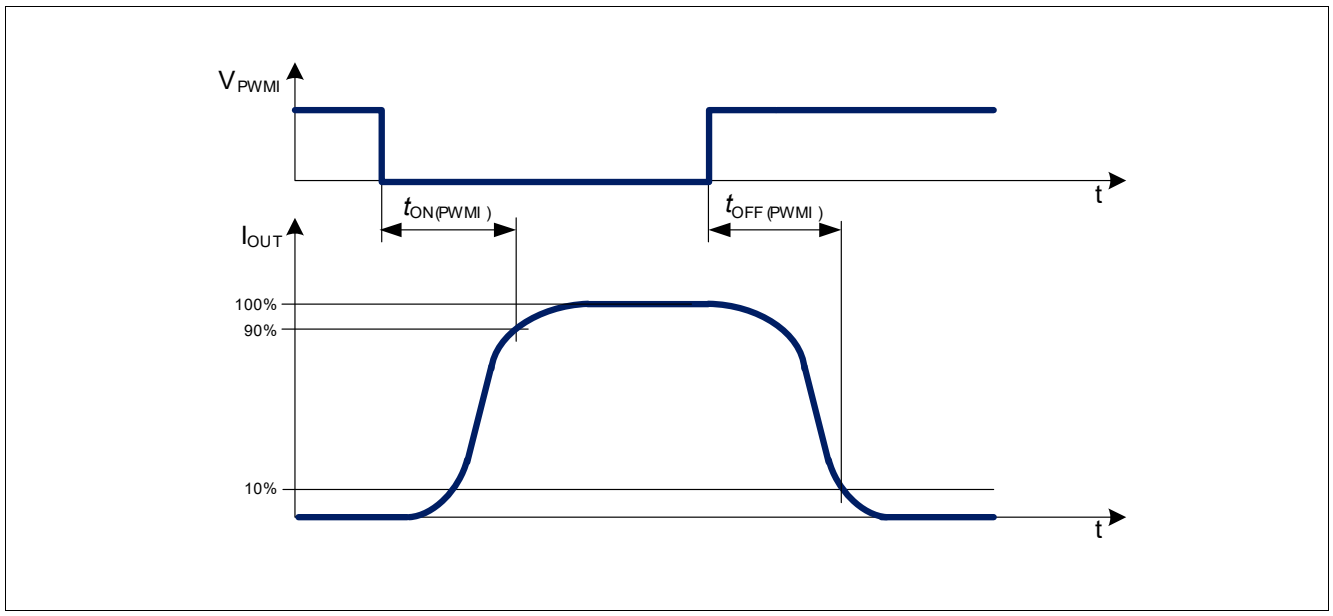


Figure 25 Output activation delay timing diagram

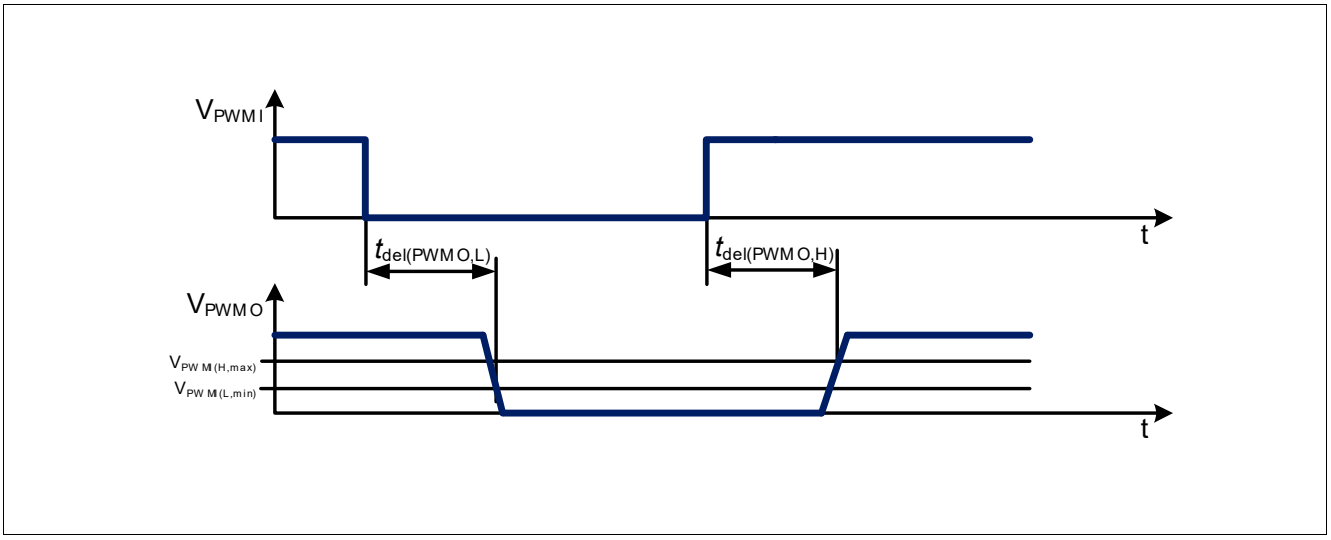


Figure 26 PWMO delay timing diagram

7.4 Electrical characteristics PWM engine

Table 9 Electrical characteristics: PWM engine

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWMI low threshold	$V_{PWMI(L)}$	1.5	1.7	2	V	V_S = 8 V to 18 V V_{EN} = 5.5 V	P_8.4.1
PWMI high threshold	$V_{PWMI(H)}$	2.5	2.7	3	V	V_S = 8 V to 18 V V_{EN} = 5.5 V	P_8.4.2
PWMI switching threshold difference $V_{PWMI(H)}$ - $V_{PWMI(L)}$	ΔV_{PWMI}	0.85	1.0	1.15	V	1) V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PS} = 3 V	P_8.4.3
PWMO Duty Cycle	DC_{PWMO}	9.5	10	10.5	%	1)2) V_S = 8 V to 18 V I_{PWM_SET} = 270 µA I_{PWM_RST} = 30 µA C_{PWMI} = 110 nF C_{PWMO} = 50 pF	P_8.4.9
PWMO Duty Cycle	DC_{PWMO}	47	50	53	%	1)2) V_S = 8 V to 18 V I_{PWM_SET} = 55 µA I_{PWM_RST} = 55 µA C_{PWMI} = 110 nF C_{PWMO} = 50 pF	P_8.4.8
PWMO Duty Cycle	DC_{PWMO}	78	80	82	%	1)2) V_S = 8 V to 18 V I_{PWM_SET} = 35 µA I_{PWM_RST} = 140 µA C_{PWMI} = 110 nF C_{PWMO} = 50 pF	P_8.4.11

Table 9 Electrical characteristics: PWM engine (cont'd)

T_J = -40°C to +150°C; V_S =5.5 V to 18 V; R_{IN_SET} = 10 kΩ; all voltages with respect to GND, positive current flowing into input and I/O pins, positive current flowing out from output pins (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
PWM_SET reference voltage	$V_{PWM_SET(ref)}$	1.184	1.22	1.256	–	1) V_{EN} = 5.5 V V_{PS} = 3 V T_J = -40... 115°C	P_8.4.12
PWM_RST reference voltage	$V_{PWM_RST(ref)}$	1.184	1.22	1.256	V	1) V_{EN} = 5.5 V V_{PS} = 3 V T_J = -40... 115°C	P_8.4.13
PWM reference voltages mismatch $V_{PWM_SET(ref)}$-$V_{PWM_RST(ref)}$	$V_{PWM_REF(ref)}$	-12	–	12	mV	1) V_S = 12.8 V V_{EN} = 5.5 V T_J = 25 °C	P_8.4.23
PWMO OFF pull-up current	$I_{PWMO(OFF)}$	0.75	–	1.6	mA	V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} = 3 V V_{PWMO} = 3 V No fault conditions	P_8.4.14
PWMO ON pull-down current	$I_{PWMO(ON)}$	-1.6	–	-0.75	mA	V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} = 1.5 V V_{PWMO} = 1.5 V No fault conditions	P_8.4.15
PWMO ON pull-down current	$I_{PWMO(ON)}$	-1.6	–	-0.4	mA	1) V_S = 8 V to 18 V V_{EN} = 5.5 V V_{PWMI} = 1.5 V V_{PWMO} = 1 V No fault conditions	P_8.4.25
Timing							
PWMO activation delay time	$t_{del(PWMO,L)}$	–	–	1	µs	1)3) V_S = 8 V to 18 V V_{EN} = 5.5 V C_{PWMO} = 50 pF V_{PWMI} falling from 5 V to 0 V V_{PWMO} = 1.5 V T_J = -40... 115°C	P_8.4.16
PWMO deactivation delay time	$t_{del(PWMO,H)}$	–	–	1	µs	1)3) V_S = 8 V to 18 V V_{EN} = 5.5 V C_{PWMO} = 50 pF V_{PWMI} rising from 0 V to 5 V V_{PWMO} = 3 V T_J = -40... 115°C	P_8.4.17
PWMO delay time matching $t_{del(PWMO,H)}$ - $t_{del(PWMO,L)}$	$\Delta t_{del(PWMO)}$	-200	–	200	ns	1)3) V_S = 12.8 V T_J = 25°C	P_8.4.21

PWM control (Digital dimming)

1) Not subjected to production test. specified by design
2) Measured at PWMO output waveform (V_{PWMO} crossing 3 V when rising from $V_{PWMO(L)}$, 2 V when falling from $V_{PWMO(H)}$)
3) Refer to **Figure 26**.

8 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

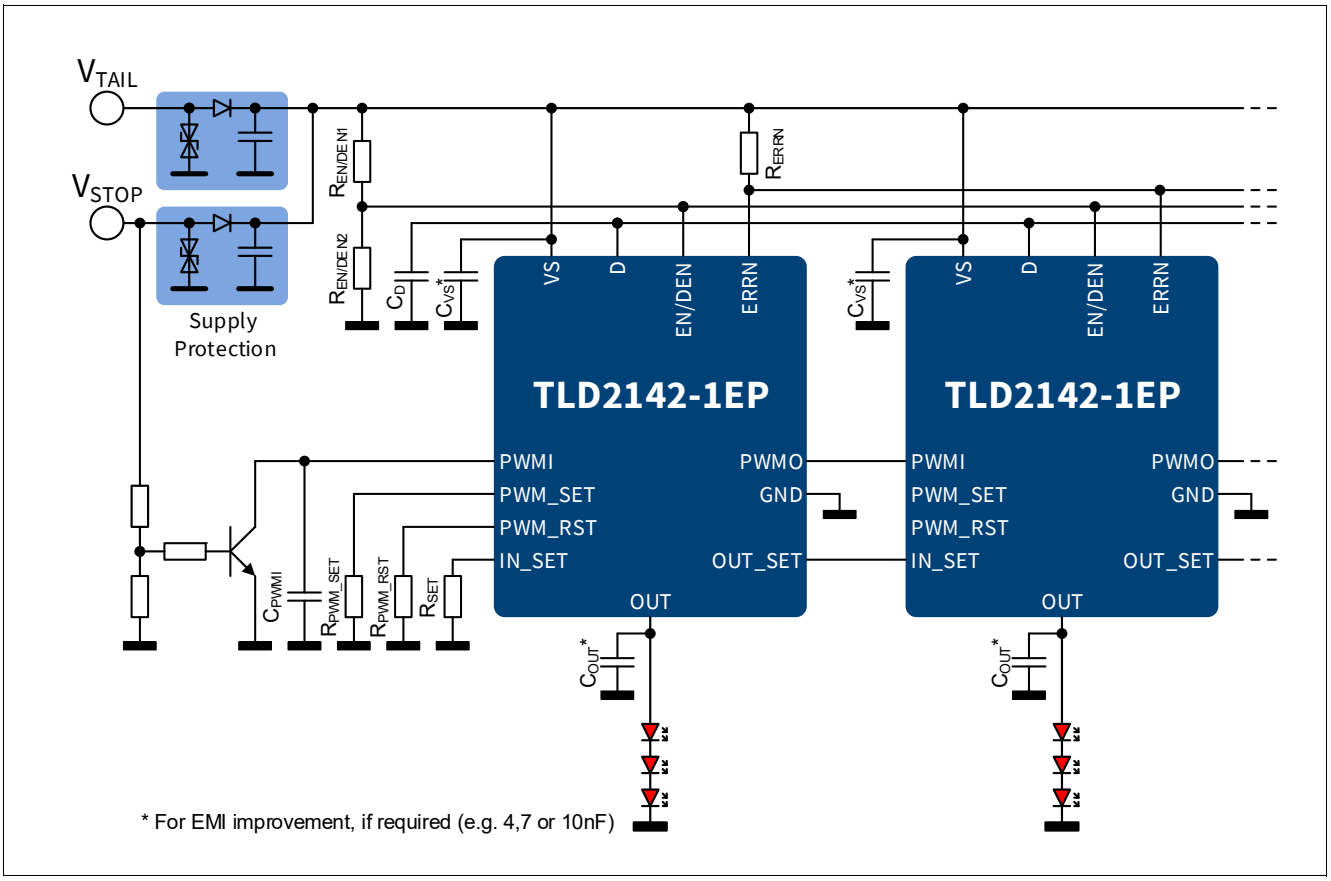


Figure 27 Application diagram example

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

9 Package outline

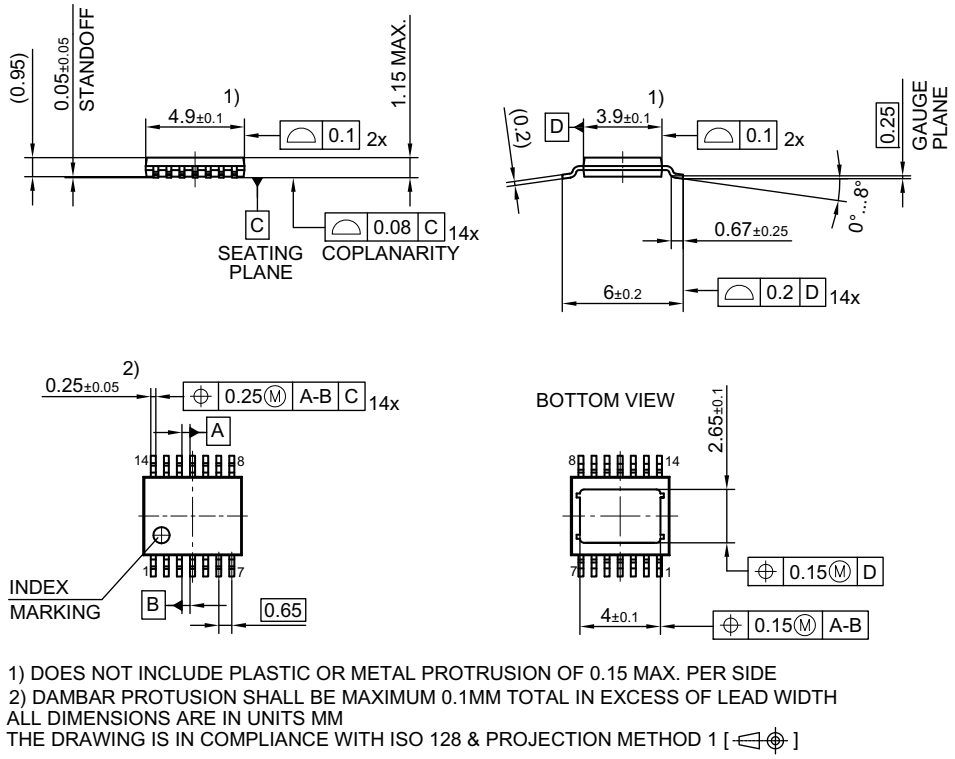


Figure 28 PG-TSDSO-14

Green product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

10 Revision History

Revision	Date	Changes
1.10	2019-09-26	Corrected copper dimensions in footnote[4] in **Table 4**
1.10	2019-09-26	Updated **Equation (6.1)** and **Equation (6.2)**
1.10	2019-09-26	Specified typical value for $V_{D(th)}$. See P_7.5.8
1.10	2019-09-26	Added explanation for $V_{REF_SET/RST}$ **Equation (7.3)**
1.00	2018-10-09	Initial datasheet created

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