16-CHANNEL LED DRIVER WITH DOT CORRECTION AND GRAYSCALE PWM CONTROL

Check for Samples: TLC5940-EP

FEATURES

- 16 Channels
- 12-Bit (4096 Steps) Grayscale PWM Control
- Dot Correction
  - 6 Bit (64 Steps)
  - Storable in Integrated EEPROM
- Drive Capability (Constant-Current Sink) of 0 mA to 72 mA (–40°C to 125°C)
  - 0 mA to 60 mA (V_{CC} < 3.6 V, –40°C to 85°C)
  - 0 mA to 120 mA (V_{CC} > 3.6 V, –40°C to 85°C)
- LED Power Supply Voltage up to 17 V
- V_{CC} = 3 V to 5.5 V
- Serial Data Interface
- Controlled In-Rush Current
- 30-MHz Data Transfer Rate
- CMOS Level I/O
- Error Information
  - LOD: LED Open Detection
  - TEF: Thermal Error Flag

APPLICATIONS

- Monocolor, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Backlighting
- General, High-Current LED Drive

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Q-Temp (–40°C/125°C)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

DESCRIPTION

The TLC5940 is a 16-channel, constant-current sink LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step, constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. The dot correction data is stored in an integrated EEPROM. Both grayscale control and dot correction are accessible via a serial interface. A single external resistor sets the maximum current value of all 16 channels.

The TLC5940 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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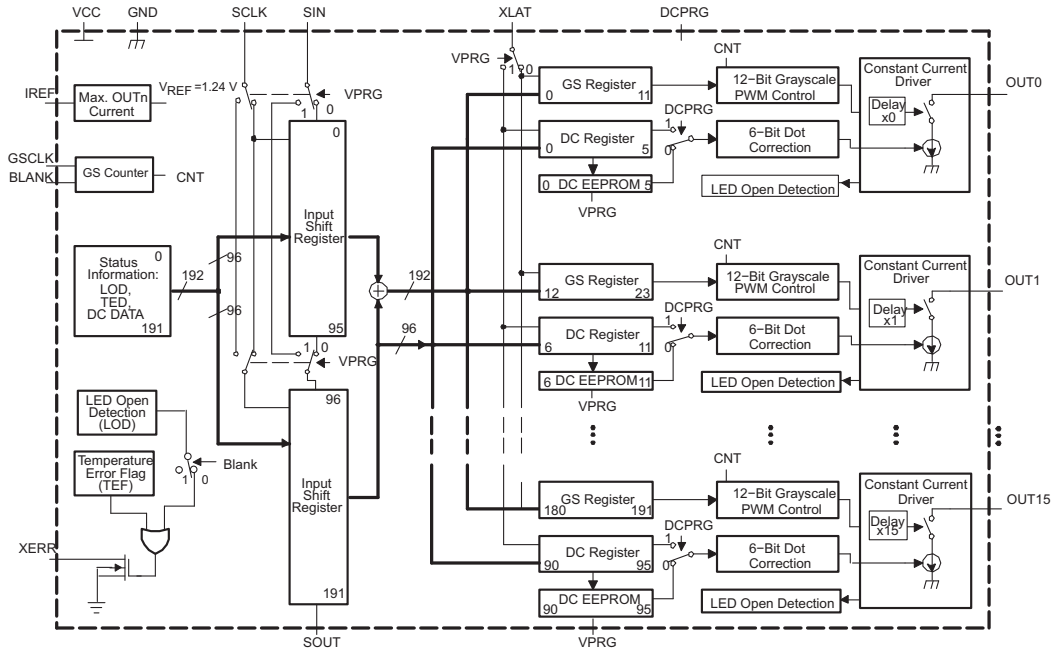

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PACKAGE(1)	PART NUMBER
–40°C to 125°C	28-pin HTSSOP PowerPAD™	TLC5940QPWPREP
	32-pin 5mm x 5mm QFN	TLC5940QRHBREP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

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THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		RHB	PWP	UNIT
		32 PINS	28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	33.9	35.4	°C/W
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(3)	30	24.94	°C/W
$\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance(4)	3.9	5.37	°C/W
θ_{JB}	Junction-to-board thermal resistance(5)	9.3	15.02	°C/W
Ψ_{JT}	Junction-to-top characterization parameter(6)	0.619	1.297	°C/W
Ψ_{JB}	Junction-to-board characterization parameter(7)	9.3	10.96	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction to case (bottom) thermal resistance is obtained by simulations of this device as configured per MilStd 883 method 1012.1.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

ABSOLUTE MAXIMUM RATINGS.

over operating free-air temperature range (unless otherwise noted)(1) (2)

			UNIT
V_I	Input voltage range(3)	VCC	–0.3V to 6V
I_O	Output current (dc)		130mA
V_I	Input voltage range	$V_{(BLANK)}$, $V_{(DCPRG)}$, $V_{(SCLK)}$, $V_{(XLAT)}$, $V_{(SIN)}$, $V_{(GSCLK)}$, $V_{(IREF)}$	–0.3V to V_{CC} +0.3V
V_O	Output voltage range	$V_{(SOUT)}$, $V_{(XERR)}$	–0.3V to V_{CC} +0.3V
		$V_{(OUT0)}$ to $V_{(OUT15)}$	–0.3V to 18V
	EEPROM program range	$V_{(VPRG)}$	–0.3V to 24V
	EEPROM write cycles		25
	ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2kV
		CBM (JEDEC JESD22-C101, Charged Device Model)	500V
T_{stg}	Storage temperature range		–55°C to 150°C
T_A	Operating ambient temperature range		–40°C to 125°C
	Package thermal impedance		See Thermal Characteristics table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See www.ti.com/ep_quality for additional information on enhanced plastic packaging.
(3) All voltage values are with respect to network ground terminal.

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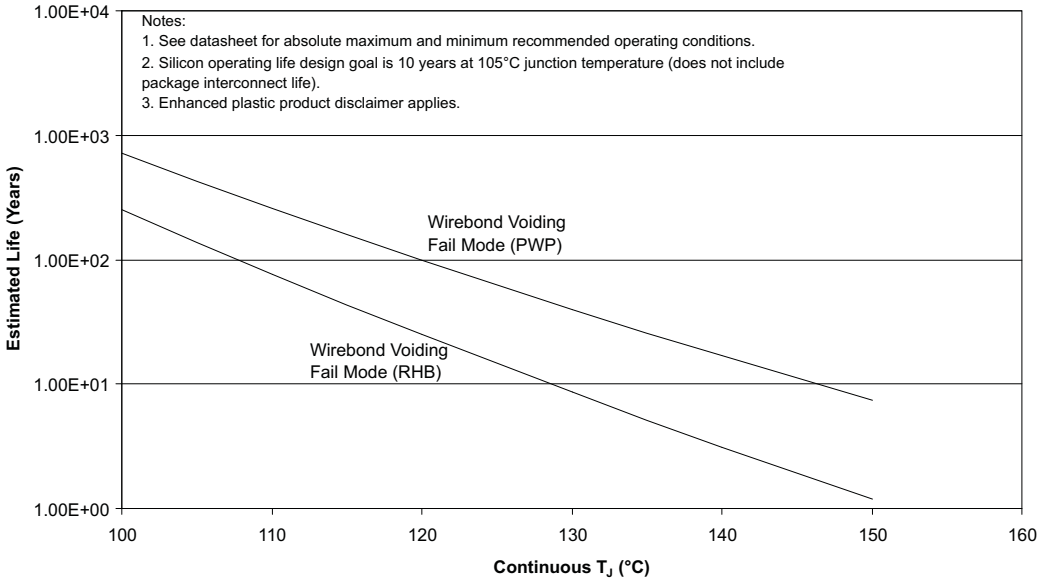

Figure 1. TLC5940-EP Mold Compound Operating Life

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RECOMMENDED OPERATING CONDITIONS

				MIN	NOM	MAX	UNIT
DC CHARACTERISTICS							
V_{CC}	Supply Voltage			3		5.5	V
V_O	Voltage applied to output (OUT0–OUT15)					17	V
V_{IH}	High-level input voltage			0.8 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage			GND		0.2 V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 5V at SOUT				–1	mA
I_{OL}	Low-level output current	V_{CC} = 5V at SOUT				1	mA
I_{OLC}	Constant output current	OUT0 to OUT15	–40°C to 125°C			72	mA
			–40°C to 85°C, V_{CC} < 3.6 V			60	
			–40°C to 85°C, V_{CC} > 3.6 V			120	
$V_{(VPRG)}$	EEPROM program voltage			20	22	23	V
T_A	Operating free-air temperature range			-40		125	°C
AC CHARACTERISTICS V_{CC} = 3 V to 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)							
$f_{(SCLK)}$	Data shift clock frequency	SCLK				30	MHz
$f_{(GSCLK)}$	Grayscale clock frequency	GSCLK				30	MHz
t_{wh0}/t_{wl0}	SCLK pulse duration	SCLK = H/L (see Figure 12)		16			ns
t_{wh1}/t_{wl1}	GSCLK pulse duration	GSCLK = H/L (see Figure 12)		16			ns
t_{wh2}	XLAT pulse duration	XLAT = H (see Figure 12)		20			ns
t_{wh3}	BLANK pulse duration	BLANK = H (see Figure 12)		20			ns
t_{su0}	Setup time	SIN to SCLK ↑(1) (see Figure 12)		5			ns
t_{su1}		SCLK ↓ to XLAT ↑ (see Figure 12)		10			ns
t_{su2}		VPRG ↑ ↓ to SCLK ↑ (see Figure 12)		10			ns
t_{su3}		VPRG ↑ ↓XLAT ↑ (see Figure 12)		10			ns
t_{su4}		BLANK ↓ to GSCLK ↑ (see Figure 12)		10			ns
t_{su5}		XLAT ↑ to GSCLK ↑ (see Figure 12)		30			ns
t_{su6}		VPRG ↑ to DCPRG ↑ (see Figure 17)		1			ms
t_{h0}	Hold Time	SCLK ↑ to SIN (see Figure 12)		3			ns
t_{h1}		XLAT ↓ to SCLK ↑ (see Figure 12)		10			ns
t_{h2}		SCLK ↑ to VPRG ↑ ↓ (see Figure 12)		10			ns
t_{h3}		XLAT ↓ to VPRG ↑ ↓ (see Figure 12)		10			ns
t_{h4}		GSCLK ↑ to BLANK ↑ (see Figure 12)		10			ns
t_{h5}		DCPRG ↓ to VPRG ↓ (see Figure 12)		1			ms
t_{prog}		Programming time for EEPROM (see Figure 17)		20			ms

(1) ↑ and ↓ indicates a rising edge, and a falling edge respectively.

DISSIPATION RATINGS

PACKAGE	POWER RATING T_A < 25°C	DERATING FACTOR ABOVE T_A = 25°C	POWER RATING T_A = 70°C	POWER RATING T_A = 85°C	POWER RATING T_A = 125°C
28-pin HTSSOP with PowerPAD™ soldered(1)	3958mW	31.67mW/°C	2533mW	2058mW	791mW
28-pin HTSSOP with PowerPAD™ unsoldered	2026mW	16.21mW/°C	1296mW	1053mW	405mW
32-pin QFN(1)	3482mW	27.86mW/°C	2228mW	1811mW	696mW

(1) The PowerPAD is soldered to the PCB with a 2 oz. (56,7 grams) copper trace. See SLMA002 for further information.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1mA, SOUT	V_{CC} –0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND; BLANK, DCPRG, GSCLK, SCLK, SIN, XLAT	–1		1	µA
		V_I = GND; VPRG	–2		2	
		V_I = V_{CC}; VPRG			50	
		V_I = 21V; VPRG; DCPRG = V_{CC}		4	10	mA
I_{CC}	Supply current	No data transfer, all output OFF, V_O = 1V, $R_{(IREF)}$ = 10kΩ		0.9	6	mA
		No data transfer, all output OFF, V_O = 1V, $R_{(IREF)}$ = 1.3kΩ		5.2	12	
		Data transfer 30MHz, all output ON, V_O = 1V, $R_{(IREF)}$ = 1.3kΩ		16		
		Data transfer 30MHz, all output ON, V_O = 1V, $R_{(IREF)}$ = 640Ω		30		
$I_{O(LC)}$	Constant sink current (see Figure 3)	All output ON, V_O = 1V, $R_{(IREF)}$ = 640Ω, 25°C	54	61	69	mA
		All output ON, V_O = 1V, $R_{(IREF)}$ = 640Ω, Full temperature	42	61	72	
I_{lkg}	Leakage output current	All output OFF, V_O = 15V, $R_{(IREF)}$ = 640Ω, OUT0 to OUT15			±1	µA
$\Delta I_{O(LC0)}$	Constant sink current error (see Figure 3)	All output ON, V_O = 1V, $R_{(IREF)}$ = 640Ω, OUT0 to OUT15, 25°C			±4	%
		All output ON, V_O = 1V, $R_{(IREF)}$ = 640Ω, OUT0 to OUT15(1), Full temperature			±12	
		All output ON, V_O = 1V, $R_{(IREF)}$ = 1300Ω, OUT0 to OUT15, 25°C			±4	
		All output ON, V_O = 1V, $R_{(IREF)}$ = 1300Ω, OUT0 to OUT15(1), Full temperature			±8	
$\Delta I_{O(LC1)}$	Constant sink current error (see Figure 3)	Device to device, Averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 1920Ω (20mA)(2)		–2 +0.4		%
$\Delta I_{O(LC2)}$	Constant sink current error (see Figure 3)	Device to device, Averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 480Ω (80mA)(2)		–2.7 +2		%
$\Delta I_{O(LC3)}$	Line regulation (see Figure 3)	All output ON, V_O = 1V, $R_{(IREF)}$ = 640Ω OUT0 to OUT15(3), 25°C			±4	%/V
		All output ON, V_O = 1V, $R_{(IREF)}$ = 640Ω OUT0 to OUT15(3), Full temperature			±11	
		All output ON, V_O = 1V, $R_{(IREF)}$ = 1300Ω , OUT0 to OUT15(3), 25°C			±4	
		All output ON, V_O = 1V, $R_{(IREF)}$ = 1300Ω , OUT0 to OUT15(3), Full temperature			±4	
$\Delta I_{O(LC4)}$	Load regulation (see Figure 3)	All output ON, V_O = 1V to 3V, $R_{(IREF)}$ = 640Ω, OUT0 to OUT15(4), 25°C			±6	%/V
		All output ON, V_O = 1V to 3V, $R_{(IREF)}$ = 640Ω, OUT0 to OUT15(4), Full temperature			±20	
		All output ON, V_O = 1V to 3V, $R_{(IREF)}$ = 1300Ω, OUT0 to OUT15(4), 25°C			±6	
		All output ON, V_O = 1V to 3V, $R_{(IREF)}$ = 1300Ω, OUT0 to OUT15(4), Full temperature			±6	

(1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by Equation 1 in Table 1.
(2) The deviation of average of OUT1-15 constant current from the ideal constant-current value. It is calculated by Equation 2 in Table 1. The ideal current is calculated by Equation 3 in Table 1.
(3) The line regulation is calculated by Equation 4 in Table 1.
(4) The load regulation is calculated by Equation 5 in Table 1.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(5)	150		170	°C
$V_{(LED)}$	LED open detection threshold			0.3	0.4	V
$V_{(IREF)}$	Reference voltage output	$R_{(IREF)}$ = 640Ω	1.20	1.24	1.28	V

(5) Not tested. Specified by design

Table 1. Test Parameter Equations

$\Delta(\%) = \frac{I_{OUTn} - I_{OUTavg_0-15}}{I_{OUTavg_0-15}} \times 100$	**(1)**
$\Delta(\%) = \frac{I_{OUTavg} - I_{OUT(IDEAL)}}{I_{OUT(IDEAL)}} \times 100$	**(2)**
$I_{OUT(IDEAL)} = 31.5 \times \left(\frac{1.24V}{R_{IREF}}\right)$	**(3)**
$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{CC} = 5.5V) - (I_{OUTn} \text{ at } V_{CC} = 3.0V)}{(I_{OUTn} \text{ at } V_{CC} = 3.0V)} \times \frac{100}{2.5}$	(4)
$\Delta(\%/V) = \frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0V) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1.0V)} \times \frac{100}{2.0}$	(5)

SWITCHING CHARACTERISTICS

V_{CC} = 3V to 5.5V, T_A = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT			16	ns
t_{r1}		OUTn, V_{CC} = 5V, T_A = 60°C, DCn = 3Fh		10	30	
t_{f0}	Fall time	SOUT			16	ns
t_{f1}		OUTn, V_{CC} = 5V, T_A = 60°C, DCn = 3Fh		10	30	
t_{pd0}	Propagation delay time	SCLK to SOUT (see Figure 12)			30	ns
t_{pd1}		BLANK to OUT0			60	ns
t_{pd2}		OUTn to XERR (see Figure 12)			1000	ns
t_{pd3}		GSCLK to OUT0 (see Figure 12)			60	ns
t_{pd4}		XLAT to I_{OUT} (dot correction) (see Figure 12)			60	ns
t_{pd5}		DCPRG to OUT0 (see Figure 12)			30	ns
t_d	Output delay time	OUTn to OUT(n+1) (see Figure 12)		20	30	ns
t_{on-err}	Output on-time error	t_{outon}– T_{gsclk} (see Figure 12), GSn = 01h, GSCLK = 11 MHz	10	–50	–90	ns

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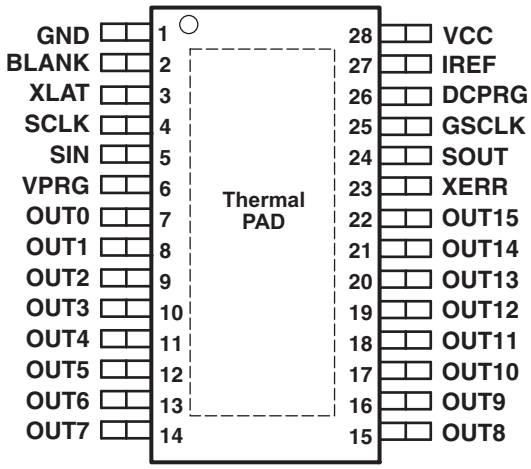
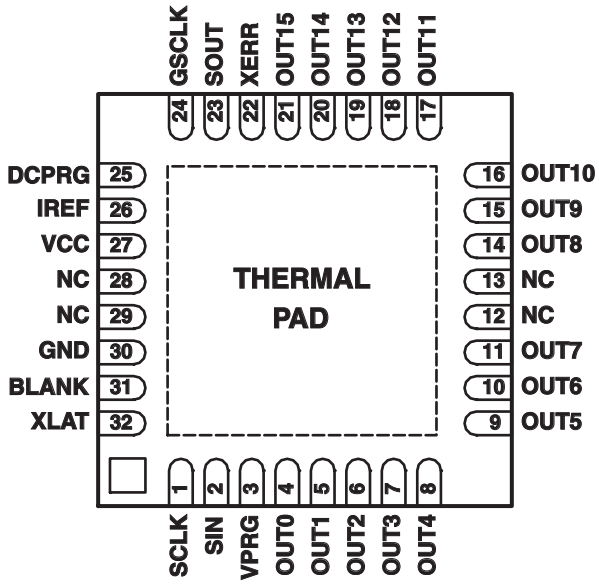
DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)



RHB PACKAGE
(TOP VIEW)



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TERMINAL FUNCTION

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PWP	RHB		
BLANK	2	31	I	Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control.
DCPRG	26	25	I	Switch DC data input. When DCPRG = L, DC is connected to EEPROM. When DCPRG = H, DC is connected to the DC register. DCPRG also controls EEPROM writing, when VPRG = $V_{(PRG)}$. EEPROM data = 3Fh (default)
GND	1	30	G	Ground
GSCLK	25	24	I	Reference clock for grayscale PWM control
IREF	27	26	I	Reference current terminal
NC	–	12, 13, 28, 29		No connection
OUT0	7	4	O	Constant current output
OUT1	8	5	O	Constant current output
OUT2	9	6	O	Constant current output
OUT3	10	7	O	Constant current output
OUT4	11	8	O	Constant current output
OUT5	12	9	O	Constant current output
OUT6	13	10	O	Constant current output
OUT7	14	11	O	Constant current output
OUT8	15	14	O	Constant current output
OUT9	16	15	O	Constant current output
OUT10	17	16	O	Constant current output
OUT11	18	17	O	Constant current output
OUT12	19	18	O	Constant current output
OUT13	20	19	O	Constant current output
OUT14	21	20	O	Constant current output
OUT15	22	21	O	Constant current output
SCLK	4	1	I	Serial data shift clock
SIN	5	2	I	Serial data input
SOUT	24	23	O	Serial data output
VCC	28	27	I	Power supply voltage
VPRG	6	3	I	Multifunction input pin. When VPRG = GND, the device is in GS mode. When VPRG = V_{CC}, the device is in DC mode. When VPRG = $V_{(VPRG)}$, DC register data can programmed into DC EEPROM with DCPRG=HIGH. EEPROM data = 3Fh (default)
XERR	23	22	O	Error output. XERR is an open-drain terminal. XERR goes L when LOD or TEF is detected.
XLAT	3	32	I	Level triggered latch signal. When XLAT = high, the TLC5940 writes data from the input shift register to either GS register (VPRG = low) or DC register (VPRG = high). When XLAT = low, the data in GS or DC register is held constant.

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PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

Resistor values are equivalent resistances, and they are not tested.

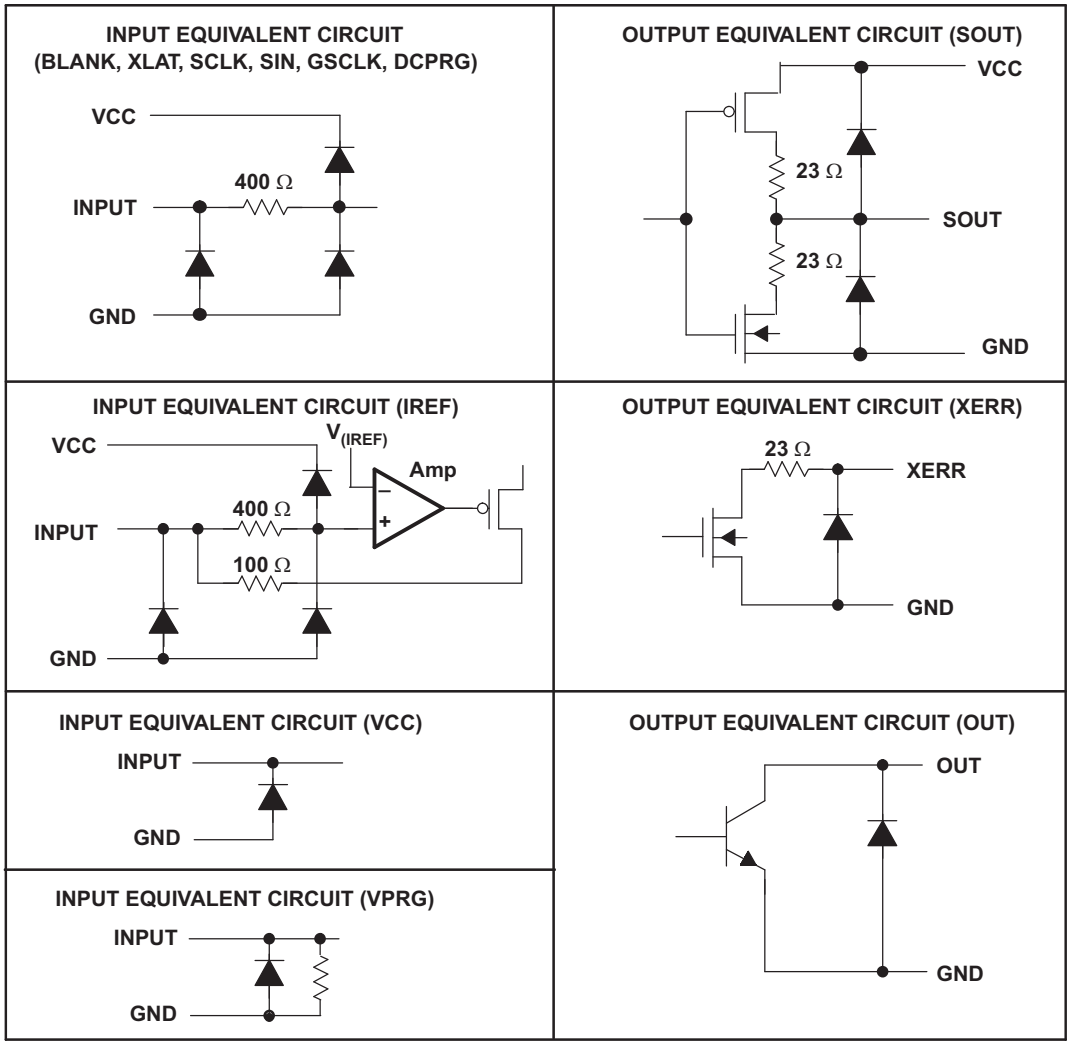

Figure 2. Input and Output Equivalent Circuits

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PARAMETER MEASUREMENT INFORMATION (continued)

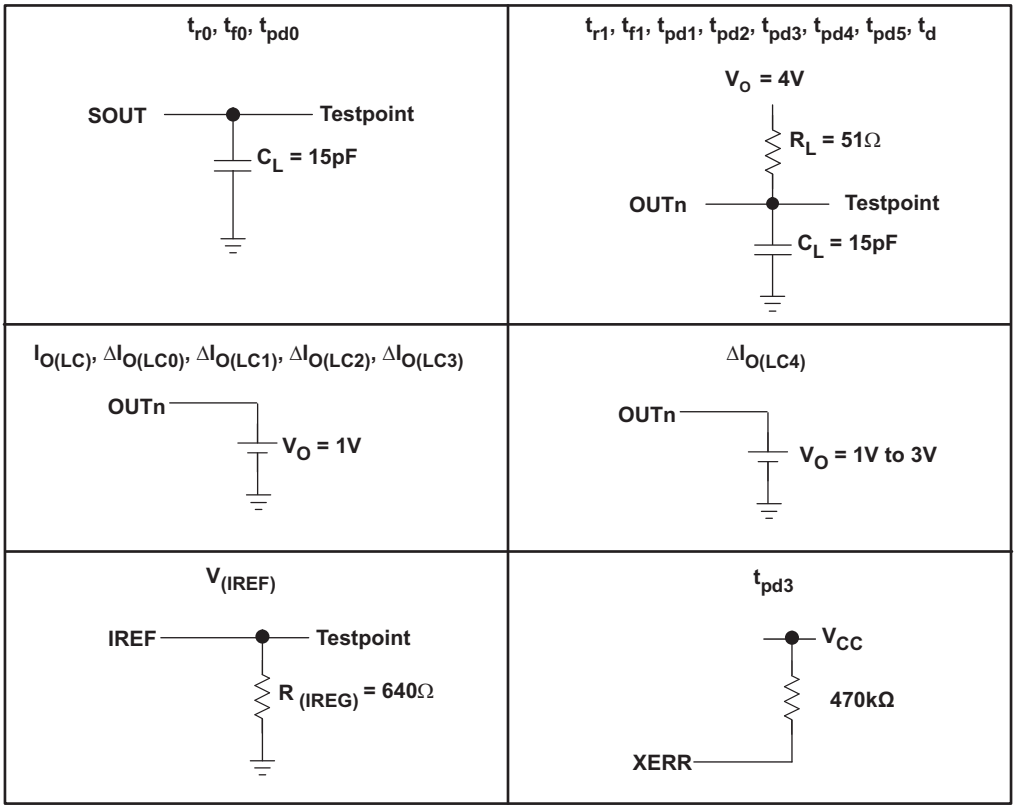

Figure 3. Parameter Measurement Circuits

TYPICAL CHARACTERISTICS

REFERENCE RESISTOR vs OUTPUT CURRENT

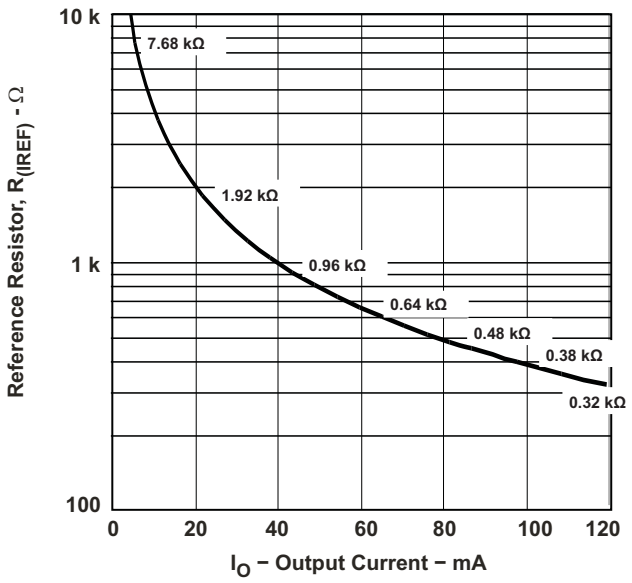

Figure 4.

POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

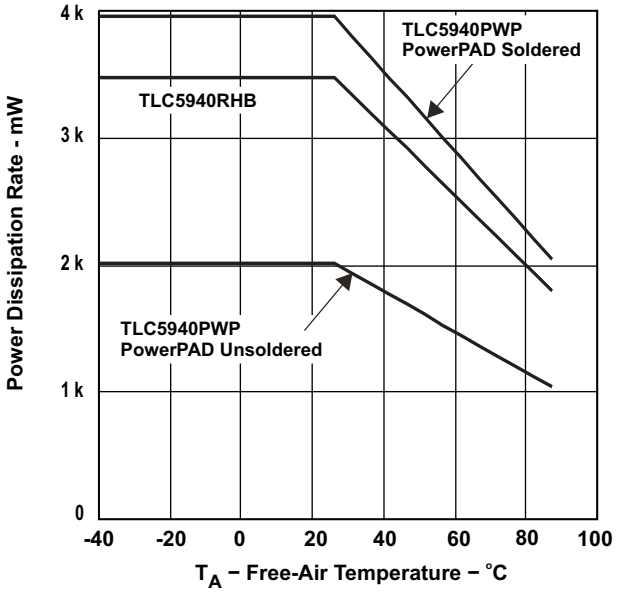

Figure 5.

OUTPUT CURRENT vs OUTPUT VOLTAGE

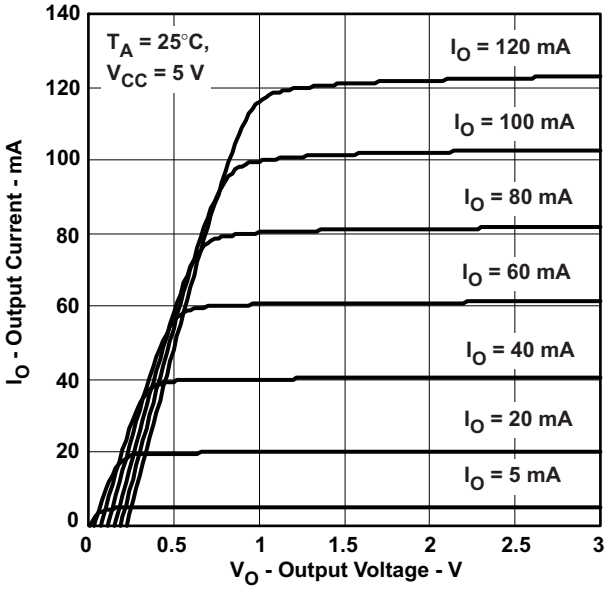

Figure 6.

OUTPUT CURRENT vs OUTPUT VOLTAGE

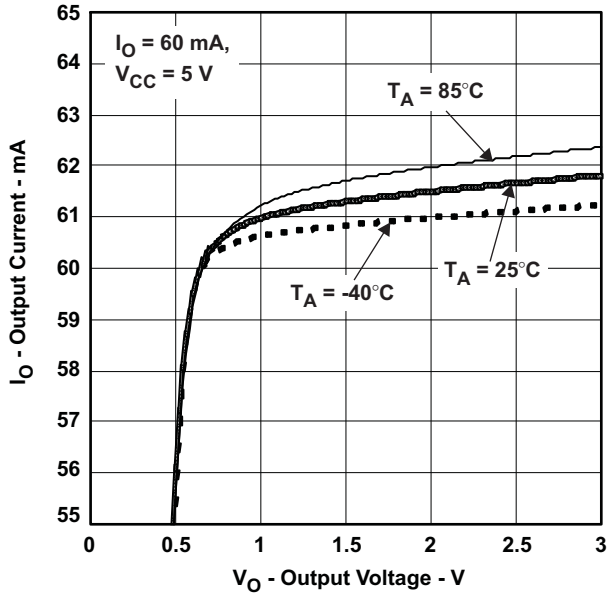

Figure 7.

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TYPICAL CHARACTERISTICS (continued)

CONSTANT OUTPUT CURRENT, ΔI_{OLC} vs AMBIENT TEMPERATURE

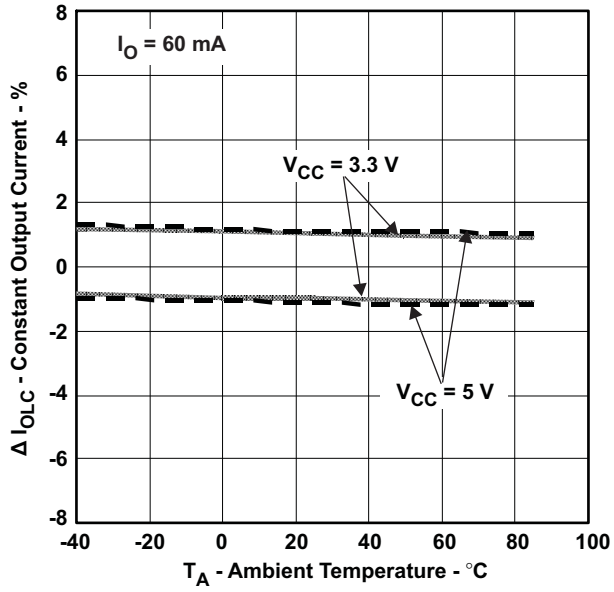

Figure 8.

CONSTANT OUTPUT CURRENT, ΔI_{OLC} vs OUTPUT CURRENT

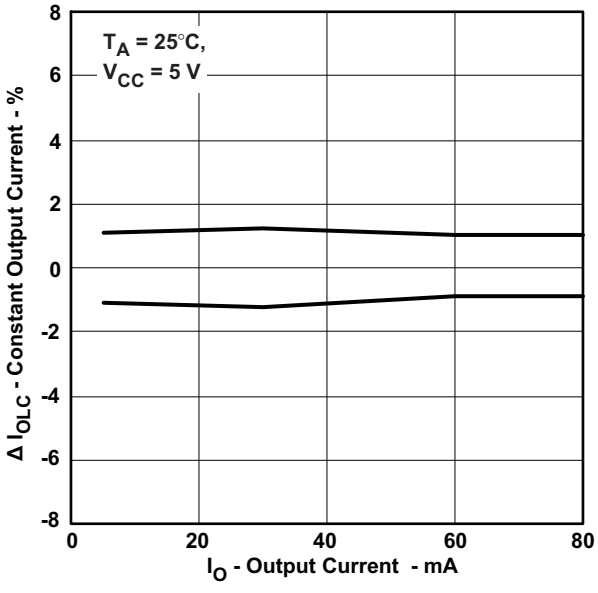

Figure 9.

OUTPUT CURRENT vs DOT CORRECTION LINEARITY (ABS VALUE)

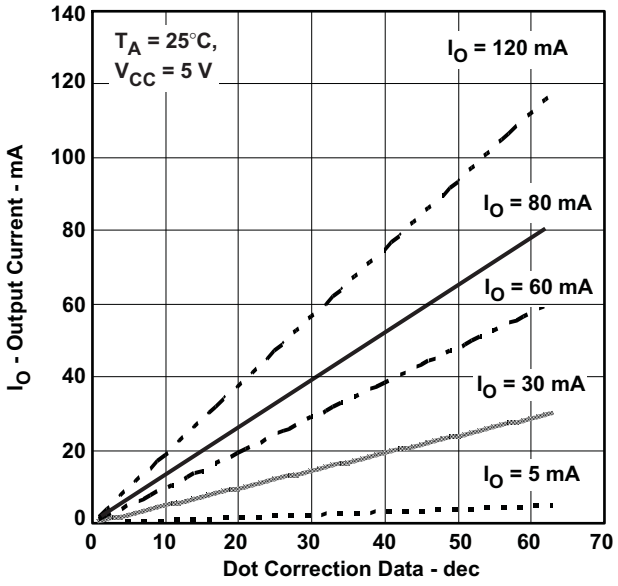

Figure 10.

OUTPUT CURRENT vs DOT CORRECTION LINEARITY (ABS VALUE)

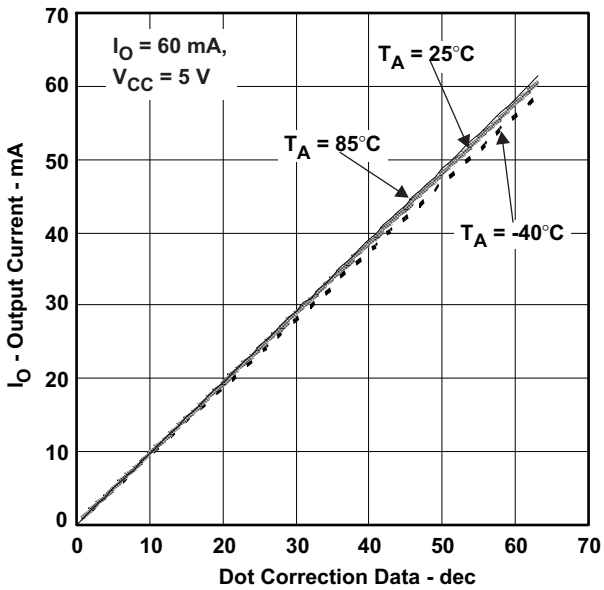

Figure 11.

PRINCIPLES OF OPERATION

SERIAL INTERFACE

The TLC5940 has a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only 3 pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data is clocked in, a high-level pulse of XLAT signal latches the serial data to the internal registers. The internal registers are level-triggered latches of XLAT signal. All data are clocked in with the MSB first. The length of serial data is 96 bit or 192 bit, depending on the programming mode. Grayscale data and dot correction data can be entered during a grayscale cycle. Although new grayscale data can be clocked in during a grayscale cycle, the XLAT signal should only latch the grayscale data at the end of the grayscale cycle. Latching in new grayscale data immediately overwrites the existing grayscale data. Figure 12 shows the timing chart. More than two TLC5940s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. An example of cascading two TLC5940s is shown in Figure 13 and the timing chart is shown in Figure 14. The SOUT pin can also be connected to the controller to receive status information from TLC5940 as shown in Figure 23.

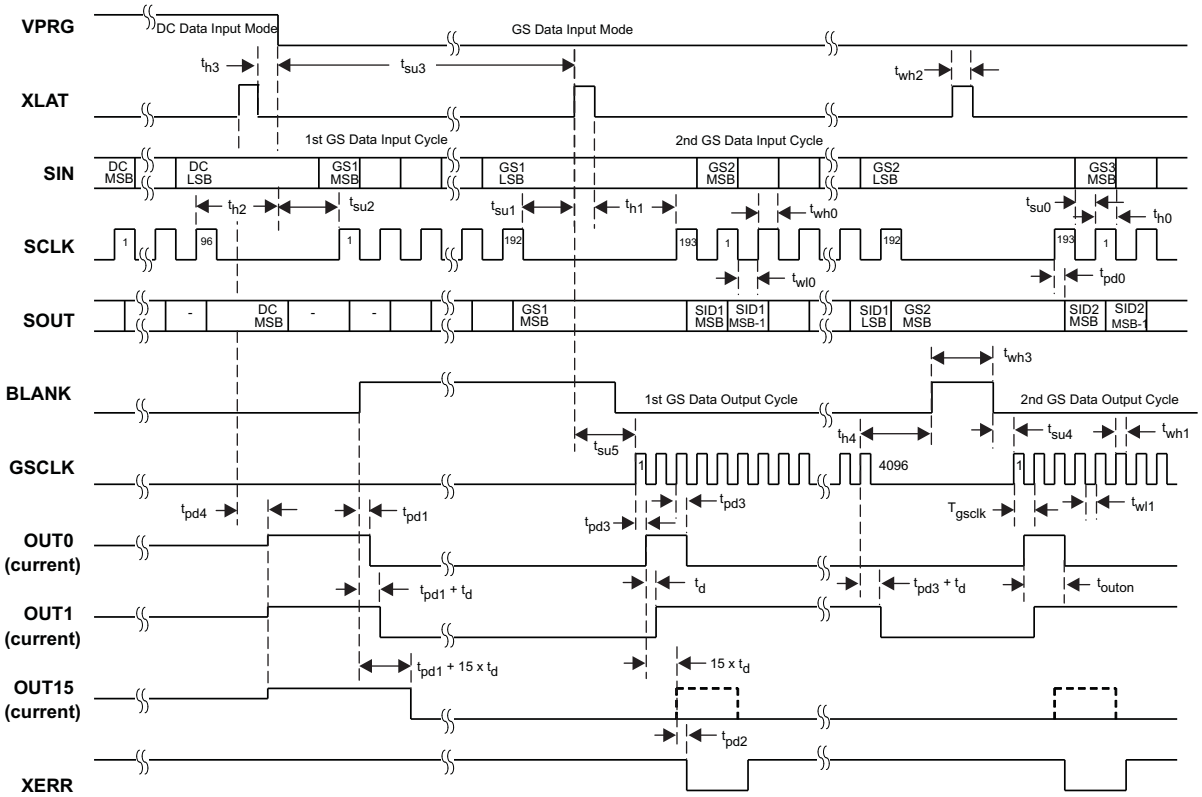

Figure 12. Serial Data Input Timing Chart

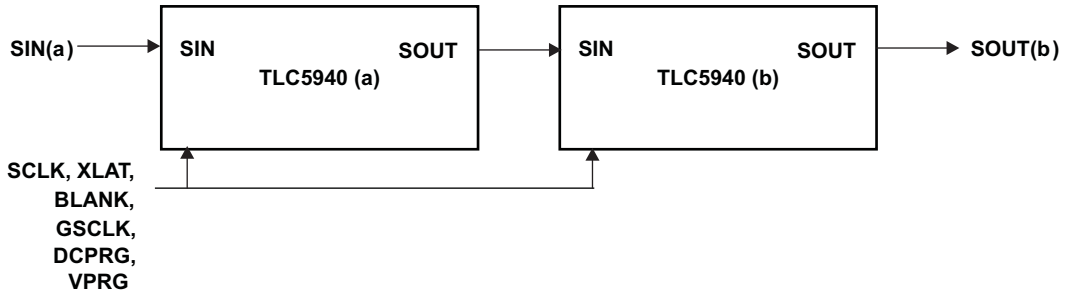

Figure 13. Cascading Two TLC5940 Devices

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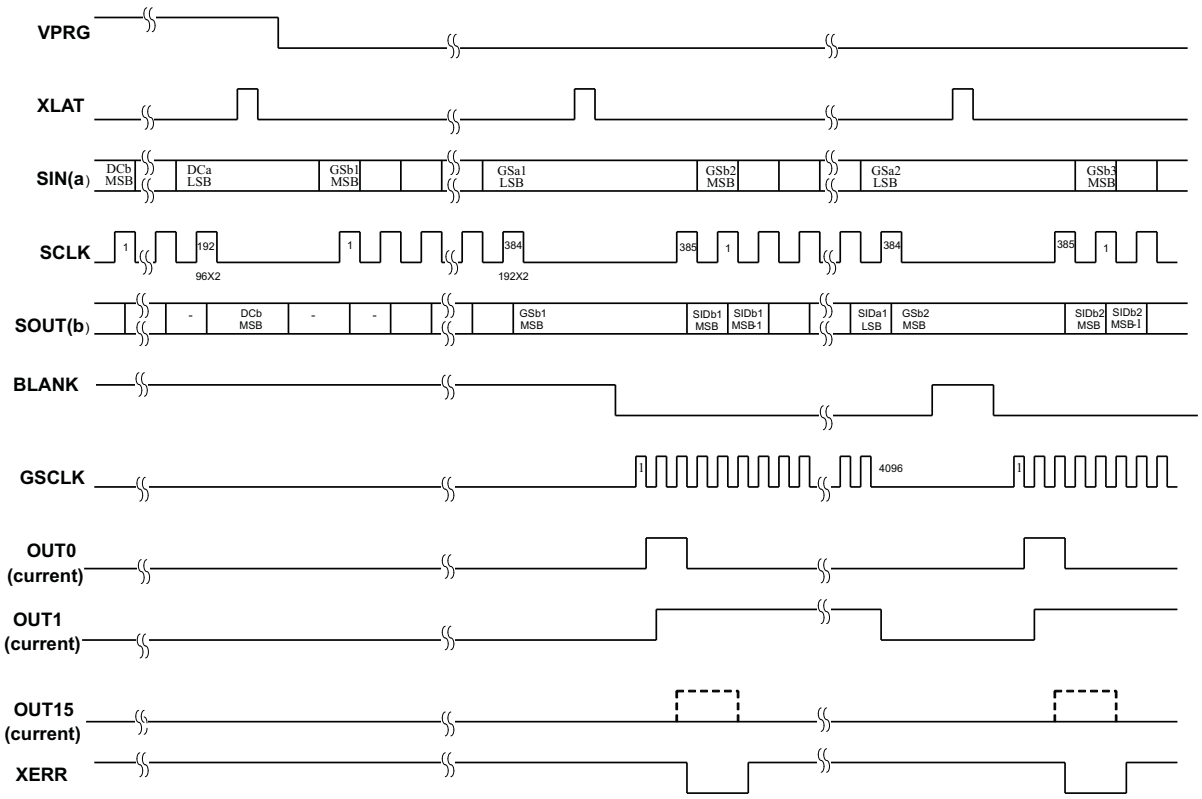

Figure 14. Timing Chart for Two Cascaded TLC5940 Devices

ERROR INFORMATION OUTPUT

The open-drain output XERR is used to report both of the TLC5940 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to V_{CC} through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Since XERR is an open-drain output, multiple ICs can be OR'ed together and pulled up to V_{CC} with a single pullup resistor. This reduces the number of signals needed to report a system error (see Figure 23).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

Table 2. XERR Truth Table

ERROR CONDITION		ERROR INFORMATION		SIGNALS	
TEMPERATURE	OUTn VOLTAGE	TEF	LOD	BLANK	XERR
$T_J < T_{(TEF)}$	Don't Care	L	X	H	H
$T_J > T_{(TEF)}$	Don't Care	H	X		L
$T_J < T_{(TEF)}$	OUTn > $V_{(LED)}$	L	L	L	H
	OUTn < $V_{(LED)}$	L	H		L
$T_J > T_{(TEF)}$	OUTn > $V_{(LED)}$	H	L		L
	OUTn < $V_{(LED)}$	H	H		L

TEF: THERMAL ERROR FLAG

The TLC5940 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160°C typical), TEF becomes H and XERR pin goes to low level. When the junction temperature becomes lower than the threshold temperature, TEF becomes L and XERR pin becomes high impedance. TEF status can also be read out from the TLC5940 status register.

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LOD: LED OPEN DETECTION

The TLC5940 has an LED-open detector that detects broken or disconnected LEDs. The LED open detector pulls the XERR pin to GND when an open LED is detected. XERR and the corresponding error bit in the Status Information Data is only active under the following open-LED conditions.

1. OUTn is on and the time tpd2 (1 μs typical) has passed.
2. The voltage of OUTn is < 0.3V (typical)

The LOD status of each output can be also read out from the SOUT pin. See STATUS INFORMATION OUTPUT section for details. The LOD error bits are latched into the Status Information Data when XLAT returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

DELAY BETWEEN OUTPUTS

The TLC5940 has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see the functional block diagram). The fixed-delay time is 20ns (typical), OUT0 has no delay, OUT1 has 20ns delay, and OUT2 has 40ns delay, etc. The maximum delay is 300ns from OUT0 to OUT15. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

OUTPUT ENABLE

All OUTn channels of the TLC5940 can be switched off with one signal. When BLANK is set high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set low, all OUTn channels work under normal conditions. If BLANK goes low and then back high again in less than 300ns, all outputs programmed to turn on still turn on for either the programmed number of grayscale clocks, or the length of time that the BLANK signal was low, which ever is lower. For example, if all outputs are programmed to turn on for 1ms, but the BLANK signal is only low for 200ns, all outputs still turn on for 200ns, even though some outputs are turning on after the BLANK signal has already gone high.

Table 3. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

SETTING MAXIMUM CHANNEL CURRENT

The maximum output current per channel is programmed by a single resistor, $R_{(IREF)}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 31.5. The maximum output current per channel can be calculated by Equation 6:

$$I_{max} = \frac{V_{(IREF)}}{R_{(IREF)}} \times 31.5 \quad (6)$$

where:

$V_{(IREF)}$ = 1.24 V

$R_{(IREF)}$ = User-selected external resistor.

I_{max} must be set between 5 mA and 120 mA. The output current may be unstable if I_{max} is set lower than 5 mA. Output currents lower than 5 mA can be achieved by setting Imax to 5 mA or higher and then using dot correction.

Figure 4 shows the maximum output current I_O versus $R_{(IREF)}$. $R_{(IREF)}$ is the value of the resistor between IREF terminal to GND, and I_O is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 31.5 times the current flowing out of the IREF pin.

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POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rating of the device package to ensure correct operation. Equation 7 calculates the power dissipation of device:

$$P_D = \left(V_{CC} \times I_{CC}\right) + \left(V_{OUT} \times I_{MAX} \times \frac{DC_n}{63} \times d_{PWM} \times N\right) \quad (7)$$

where:

V_{CC}: device supply voltage
I_{CC}: device supply current
V_{OUT}: TLC5940 OUTn voltage when driving LED current
I_{MAX}: LED current adjusted by $R_{(IREF)}$ Resistor
DC_n: maximum dot correction value for OUTn
N: number of OUTn driving LED at the same time
d_{PWM}: duty cycle defined by BLANK pin or GS PWM value

OPERATING MODES

The TLC5940 has operating modes depending on the signals DCPRG and VPRG. Table 4 shows the available operating modes. The TPS5940 GS operating mode (see Figure 12) and shift register values are not defined after power up. One solution to solve this is to set dot correction data after TLS5940 power-up and switch back to GS PWM mode. The other solution is to overflow the input shift register with 193 bits of dummy data and latch it while TLS540 is in GS PWM mode. The values in the input shift register, DC register and GS register are unknown just after power on. The DC and GS register values should be properly stored through the serial interface before starting the operation.

Table 4. TLC5940 Operating Modes Truth Table

SIGNAL		INPUT SHIFT REGISTER	MODE	DC VALUE
DCPRG	VPRG			
L	GND	192 bit	Grayscale PWM Mode	EEPROM
H				DC Register
L	V_{CC}	96 bit	Dot Correction Data Input Mode	EEPROM
H				DC Register
L	$V_{(VPRG)}$	X	EEPROM Programming Mode	EEPROM
H				Write dc register value to EEPROM. (Default data: 3Fh)

SETTING DOT CORRECTION

The TLC5940 has the capability to fine adjust the output current of each channel OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current I_{max}. Dot correction for all channels must be entered at the same time. Equation 8 determines the output current for each output n:

$$I_{OUTn} = I_{max} \times \frac{DCn}{63} \quad (8)$$

where:

I_{max} = the maximum programmable output current for each output.
DCn = the programmed dot correction value for output n (DCn = 0 to 63).
n = 0 to 15

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Figure 15 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc. The DC 15.5 in Figure 15 stands for the 5th most significant bit for output 15.

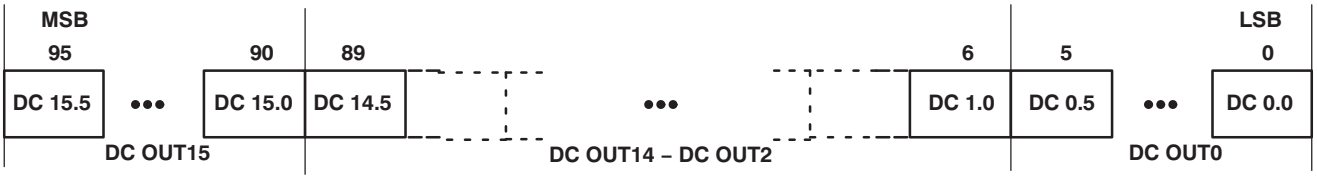

Figure 15. Dot Correction Data Packet Format

When VPRG is set to VCC, the TLC5940 enters the dot correction data input mode. The length of input shift register becomes 96 bits. After all serial data are shifted in, the TLC5940 writes the data in the input shift register to DC register when XLAT is high, and holds the data in the DC register when XLAT is low. The DC register is a level triggered latch of XLAT signal. Since XLAT is a level-triggered signal, SCLK and SIN must not be changed while XLAT is high. After XLAT goes low, data in the DC register is latched and does not change. BLANK signal does not need to be high to latch in new data. XLAT has setup time (tsu1) and hold time (th1) to SCLK as shown in Figure 16.

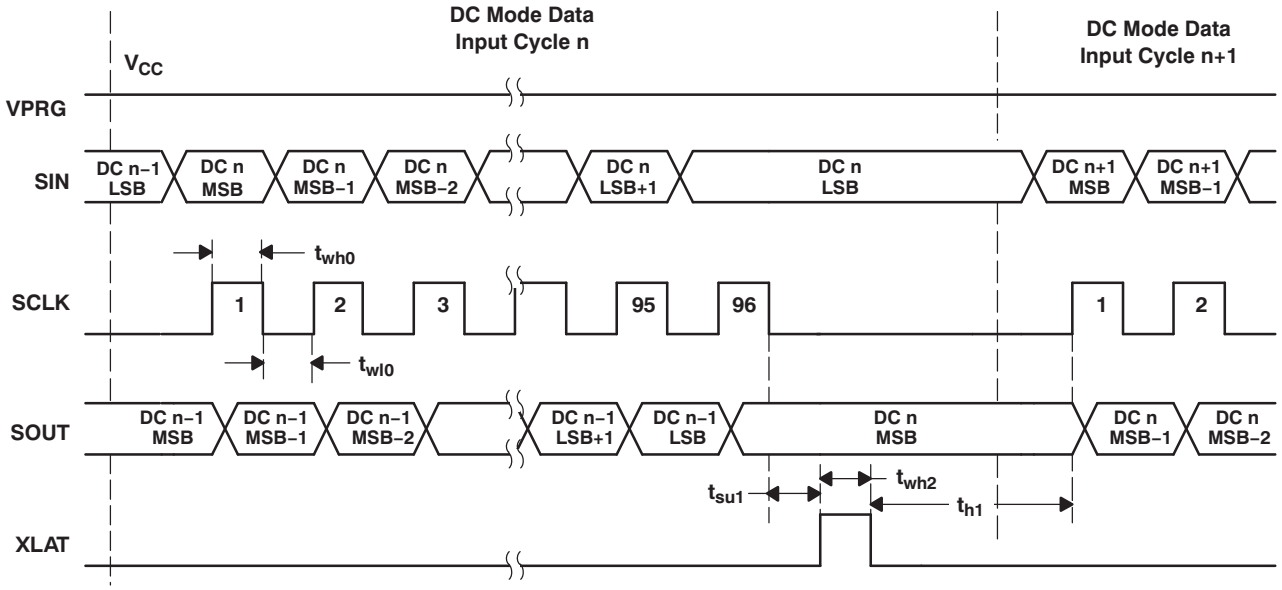

Figure 16. Dot Correction Data Input Timing Chart

The TLC5940 also has an EEPROM to store dot correction data. To store data from the dot correction register to EEPROM, DCPRG is set to high after applying V_{PRG} to the VPRG pin. Figure 17 shows the EEPROM programming timings. The EEPROM has a default value of all 1s.

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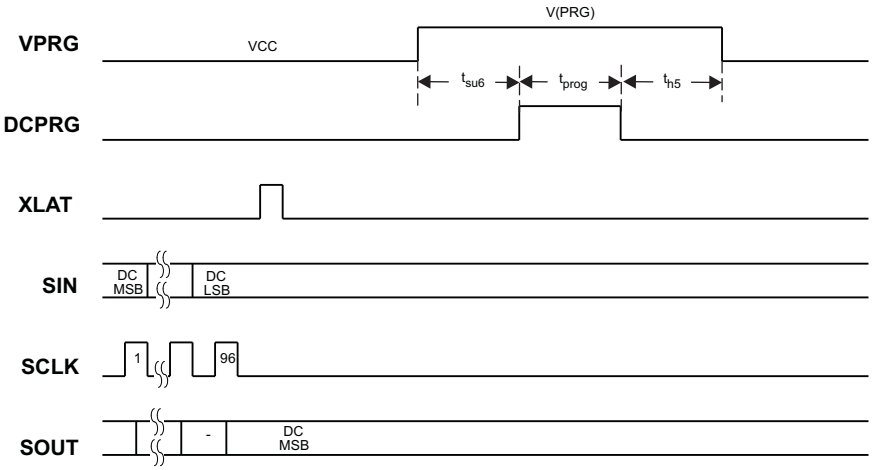

Figure 17. EEPROM Programming Timing Chart

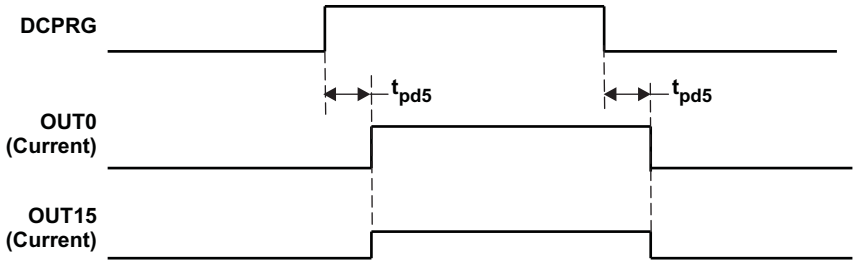

Figure 18. DCPRG and OUTn Timing Diagram

SETTING GRAYSCALE

The TLC5940 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, respective 0% to 100% brightness. Equation 9 determines the brightness level for each output n:

$$\text{Brightness in \%} = \frac{GSn}{4095} \times 100 \tag{9}$$

where:

GSn = the programmed grayscale value for output n (GSn = 0 to 4095)

n = 0 to 15

Grayscale data for all OUTn

Figure 19 shows the grayscale data packet format which consists of 12 bits x 16 channels, totaling 192 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc.

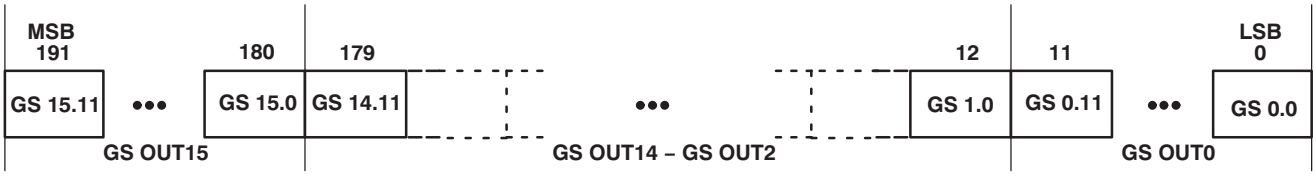

Figure 19. Grayscale Data Packet Format

When VPRG is set to GND, the TLC5940 enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the XLAT signal latches the data into

the grayscale register (see Figure 12). New grayscale data immediately becomes valid at the rising edge of the XLAT signal; therefore, new grayscale data should be latched at the end of a grayscale cycle when BLANK is high.The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after updated the grayscale register.

STATUS INFORMATION OUTPUT

The TLC5940 does have a status information register, which can be accessed in grayscale mode (VPRG=GND). After the XLAT signal latches the data into the GS register the input shift register data will be replaced with status information data (SID) of the device (see Figure 19). LOD, TEF, and dot correction EEPROM data (DCPRG=LOW) or dot correction register data (DCPRG=HIGH) can be read out at SOUT pin. The status information data packet is 192 bits wide. Bits 0-15 contain the LOD status of each channel. Bit 16 contains the TEF status. If DCPRG is low, bits 24-119 contain the data of the dot-correction EEPROM. If DCPRG is high, bits 24-119 contain the data of the dot-correction register.The remaining bits are reserved. The complete status information data packet is shown in Figure 20.

SOUT outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown Figure 21. The next SCLK pulse, which will be the clock for receiving the SMB of the next grayscale data, transmits MSB-1 of SID. If output voltage is < 0.3 V (typical) when the output sink current turns on, LOD status flage becomes active. The LOD status flag is an internal signal that pulls XERR pin down to low when the LOD status flag becomes active. The delay time, tpd2 (1 μs maximum), is from the time of turning on the output sink current to the time LOD status flage becomes valid. The timing for each channel's LOD status to become valid is shifted by the 30-ns (maximum) channel-to-channel turn-on time. After the first GSCLK goes high, OUT0 LOD status is valid; tpd3 + tpd2 = 60 ns + 1 μs. OUT1 LOD status is valid; tpd3 + td + tpd2 = 60 ns + 30 ns + 1 μs = 1.09 μs. OUT2 LOD status is valid; tpd3 + 2*td + tpd2 = 1.12 μs, and so on. It takes 1.51 μs maximum (tpd3 + 15*td + tpd2) from the first GSCLK rising edge until all LOD become valid; *tsuLOD* must be > 1.51 μs (see Figure 21) to ensure that all LOD data are valid.

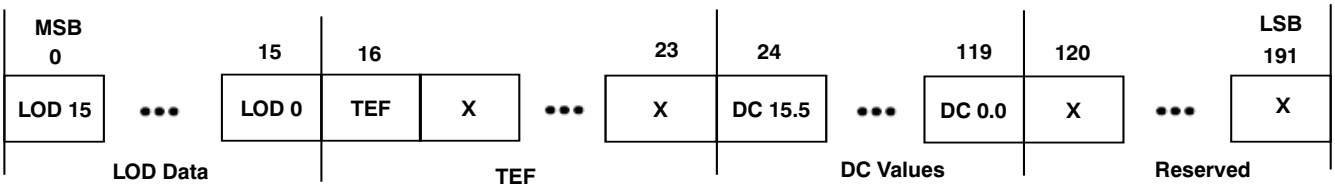

Figure 20. Status Information Data Packet Format

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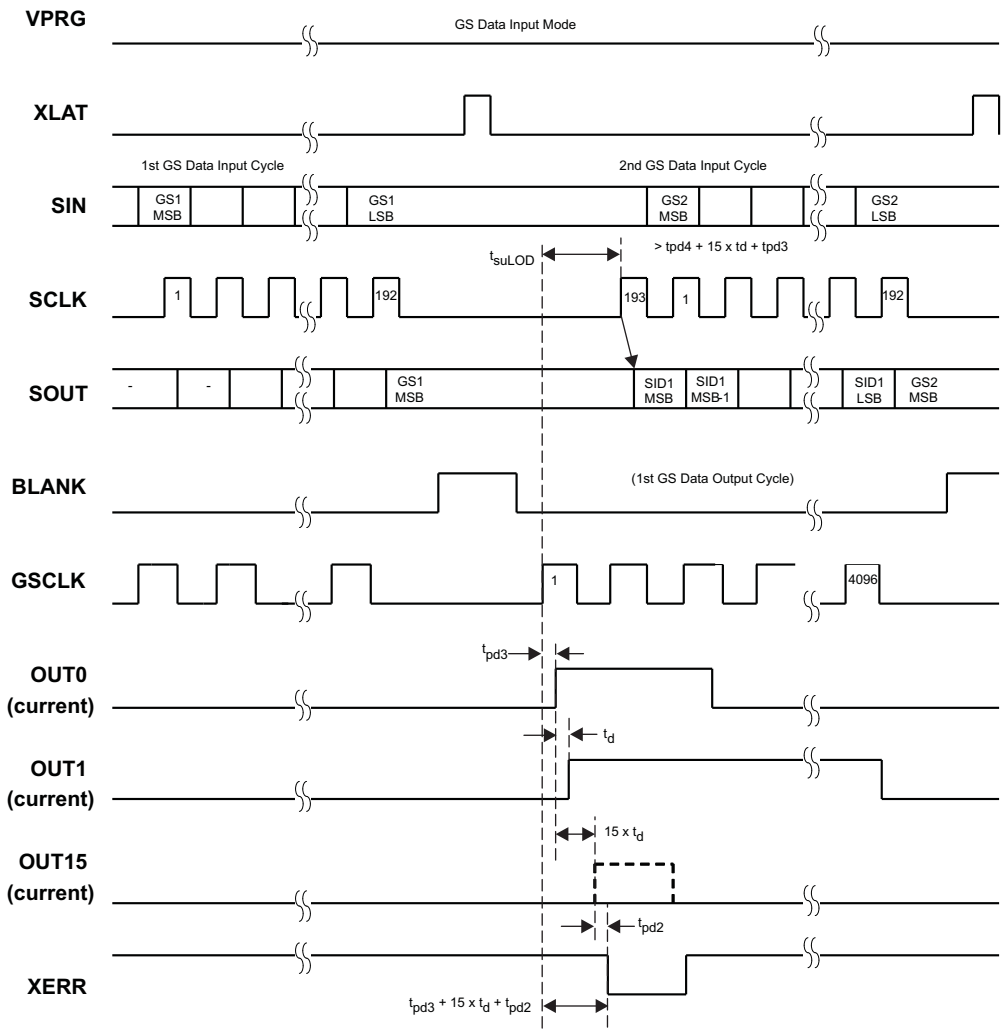

Figure 21. Readout Status Information Data (SID) Timing Chart

GRAYSCALE PWM OPERATION

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK goes low increases the grayscale counter by one and switches on all OUTn with grayscale value not zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC5940 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to the counter values are switched off. A BLANK=H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 22). When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling BLANK high before the counter reaches FFFh immediately resets the counter to zero.

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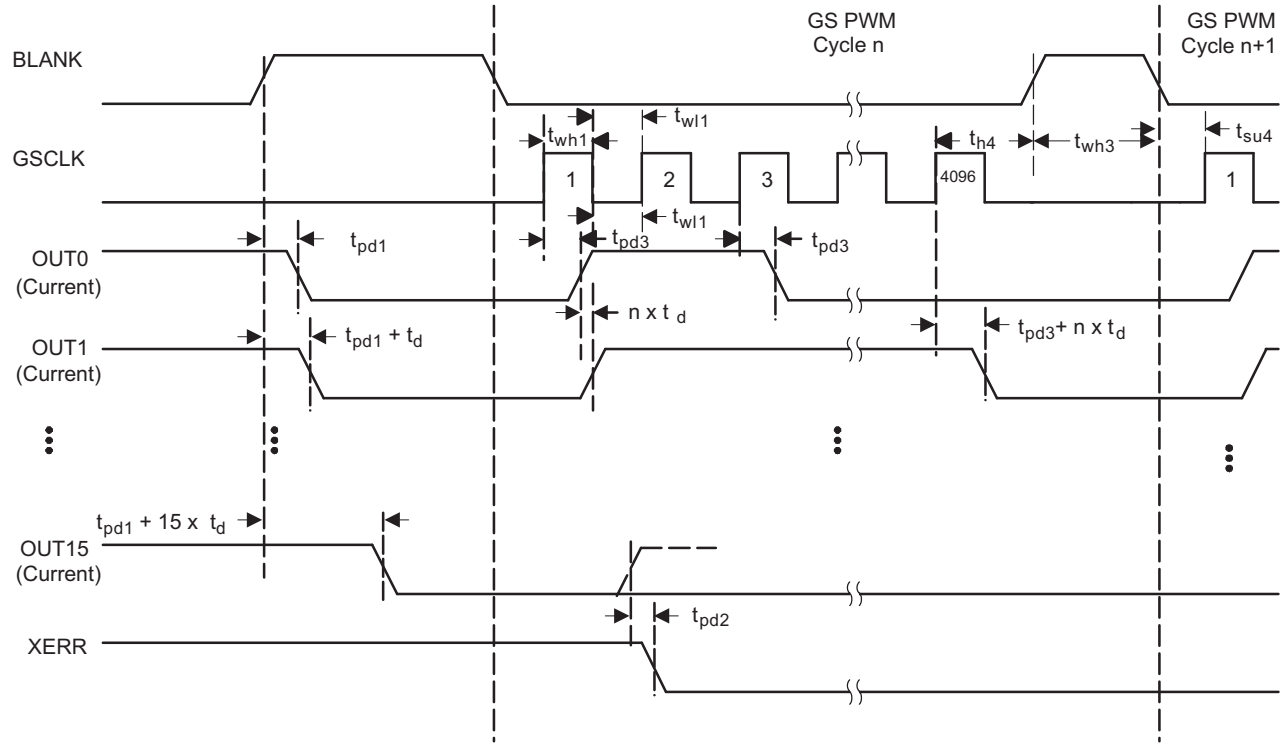

Figure 22. Grayscale PWM Cycle Timing Chart

SERIAL DATA TRANSFER RATE

Figure 23 shows a cascading connection of *n* TLC5940 devices connected to a controller, building a basic module of an LED display system. The maximum number of cascading TLC5940 devices depends on the application system and is in the range of 40 devices. Equation 10 calculates the minimum frequency needed:

$$f_{(GSCLK)} = 4096 \times f_{(update)}$$

$$f_{(SCLK)} = 193 \times f_{(update)} \times n \quad (10)$$

where:

$f_{(GSCLK)}$: minimum frequency needed for GSCLK
$f_{(SCLK)}$: minimum frequency needed for SCLK and SIN
$f_{(update)}$: update rate of whole cascading system
n: number cascaded of TLC5940 device

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APPLICATION EXAMPLE

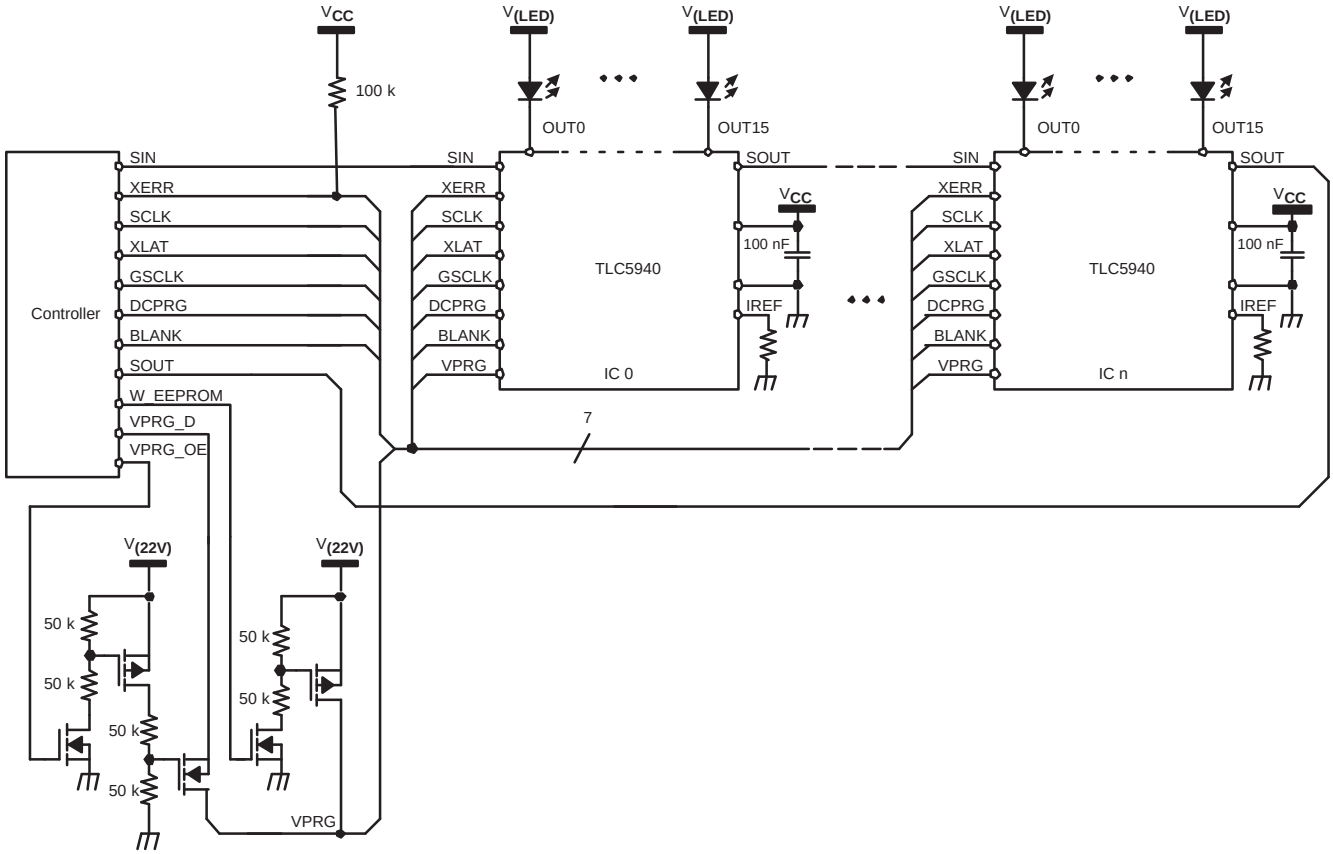

Figure 23. Cascading Devices

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC5940QPWPREP	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLC5940QRHBREP	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
V62/10610-01XE	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
V62/10610-01YE	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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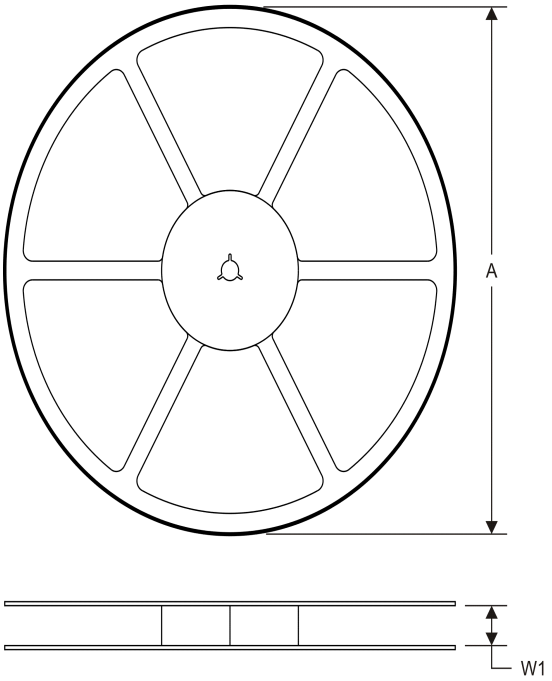
OTHER QUALIFIED VERSIONS OF TLC5940-EP :
- Catalog: TLC5940

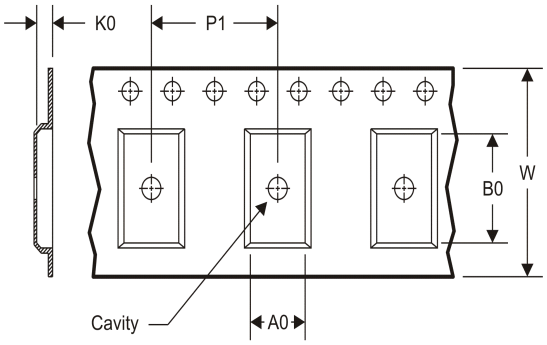
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



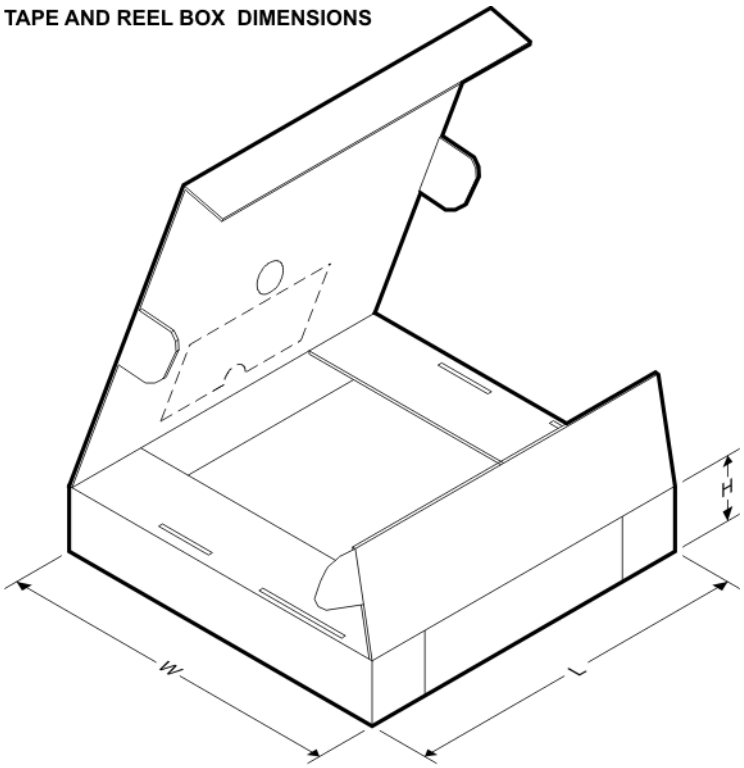
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5940QRHBREP	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

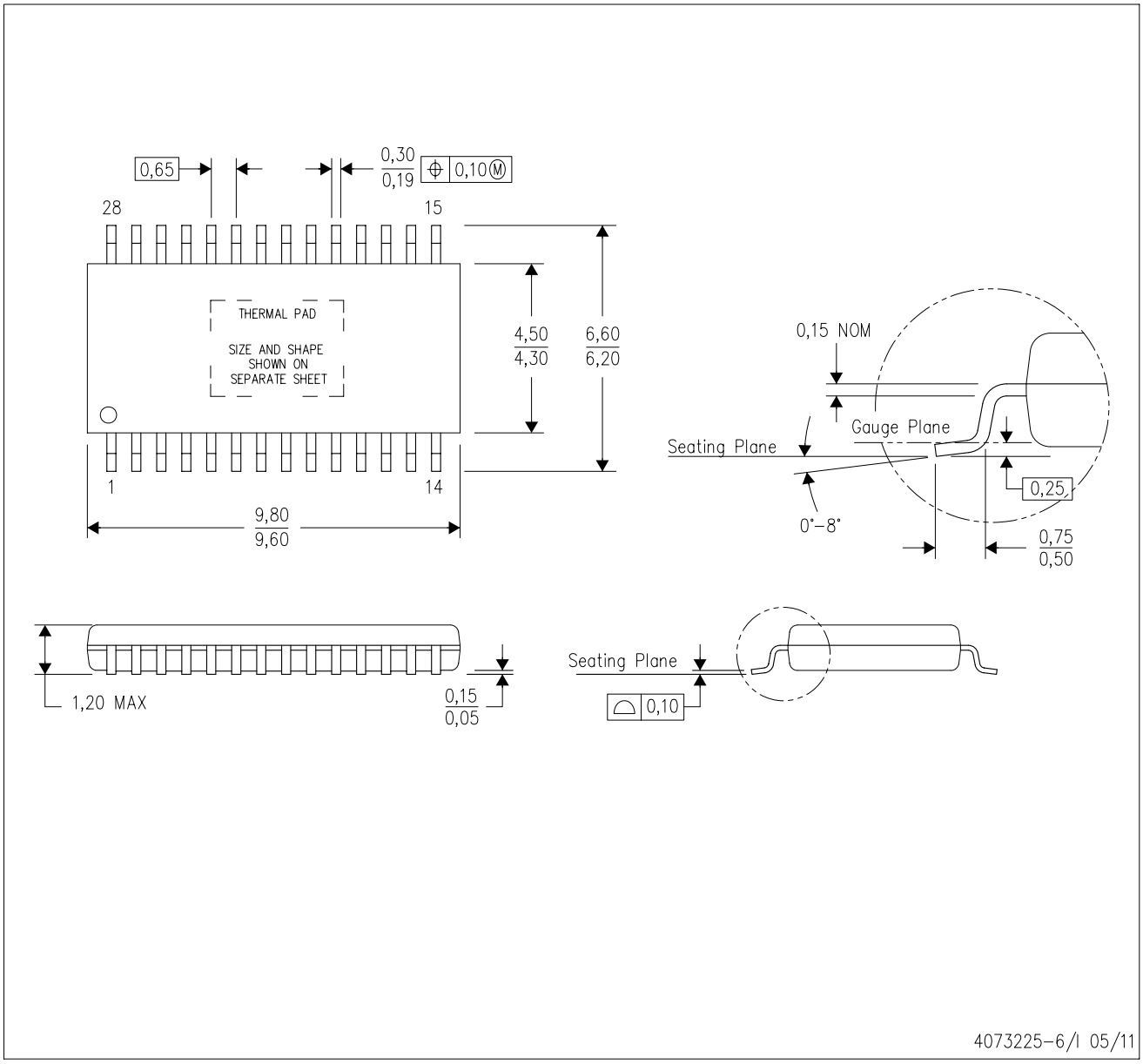
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5940QRHBREP	QFN	RHB	32	3000	367.0	367.0	35.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

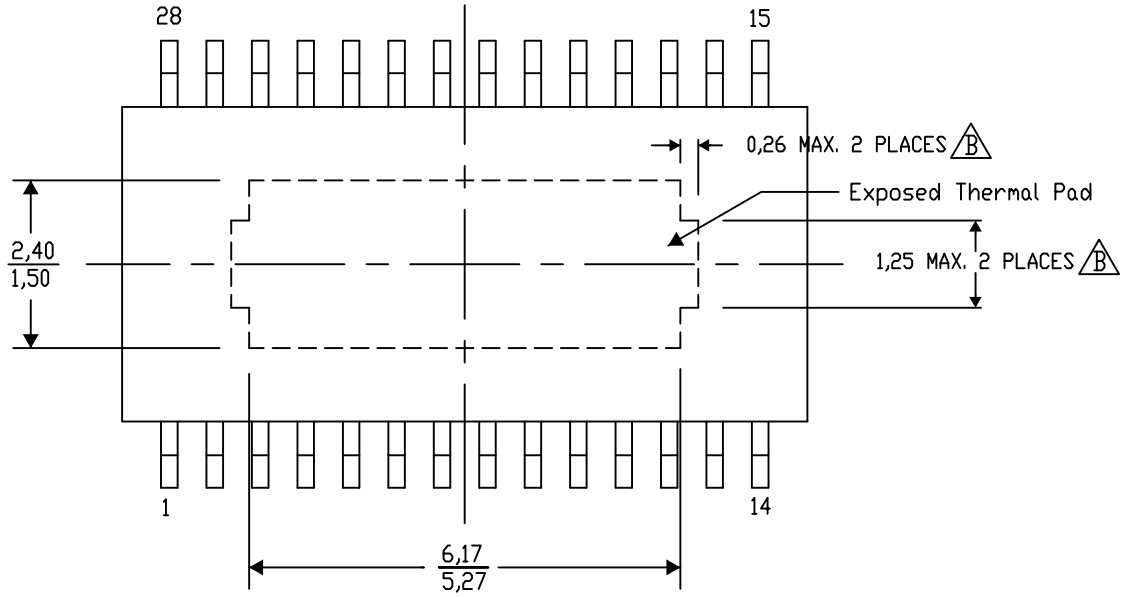
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

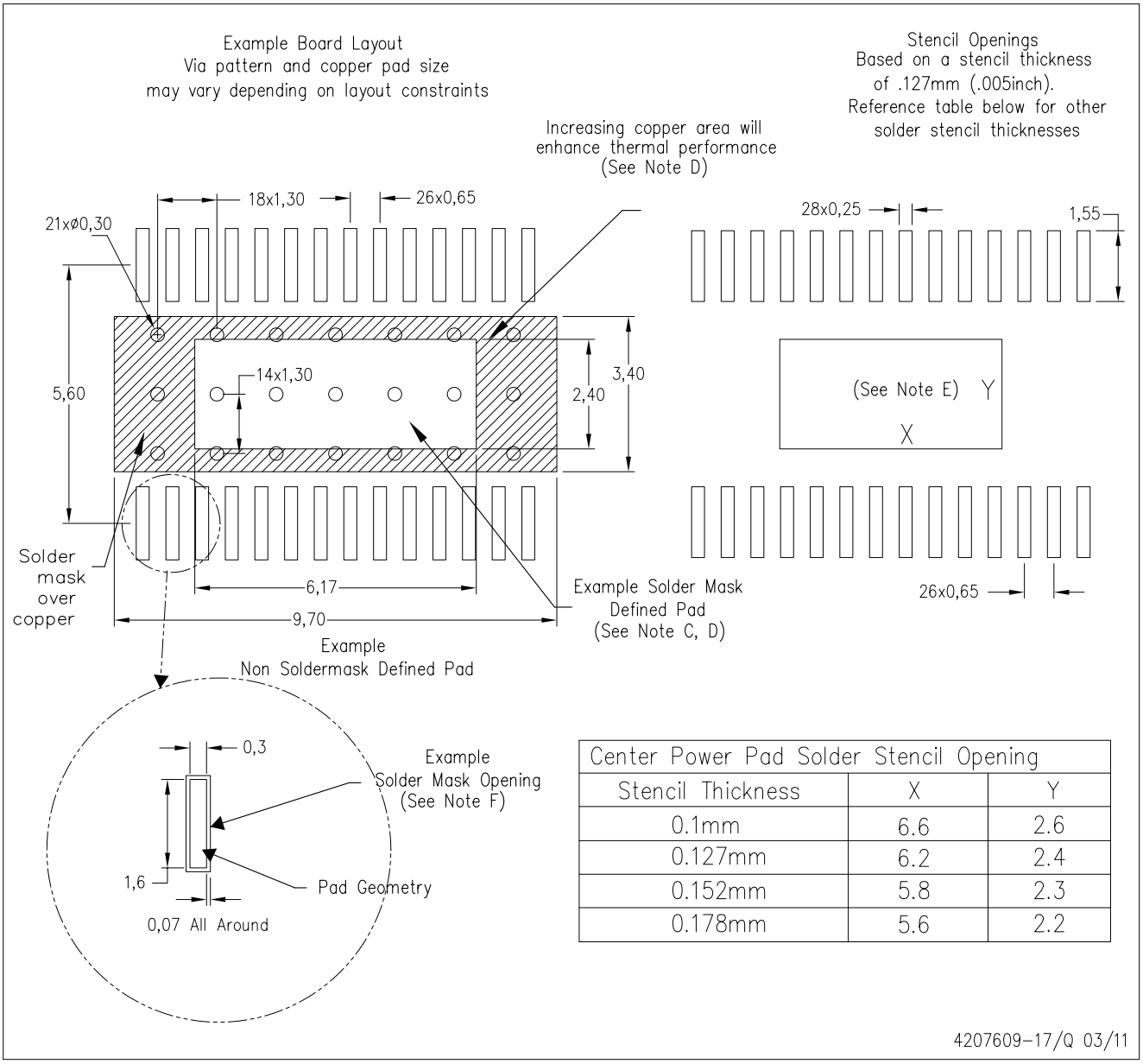
4206332–33/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE

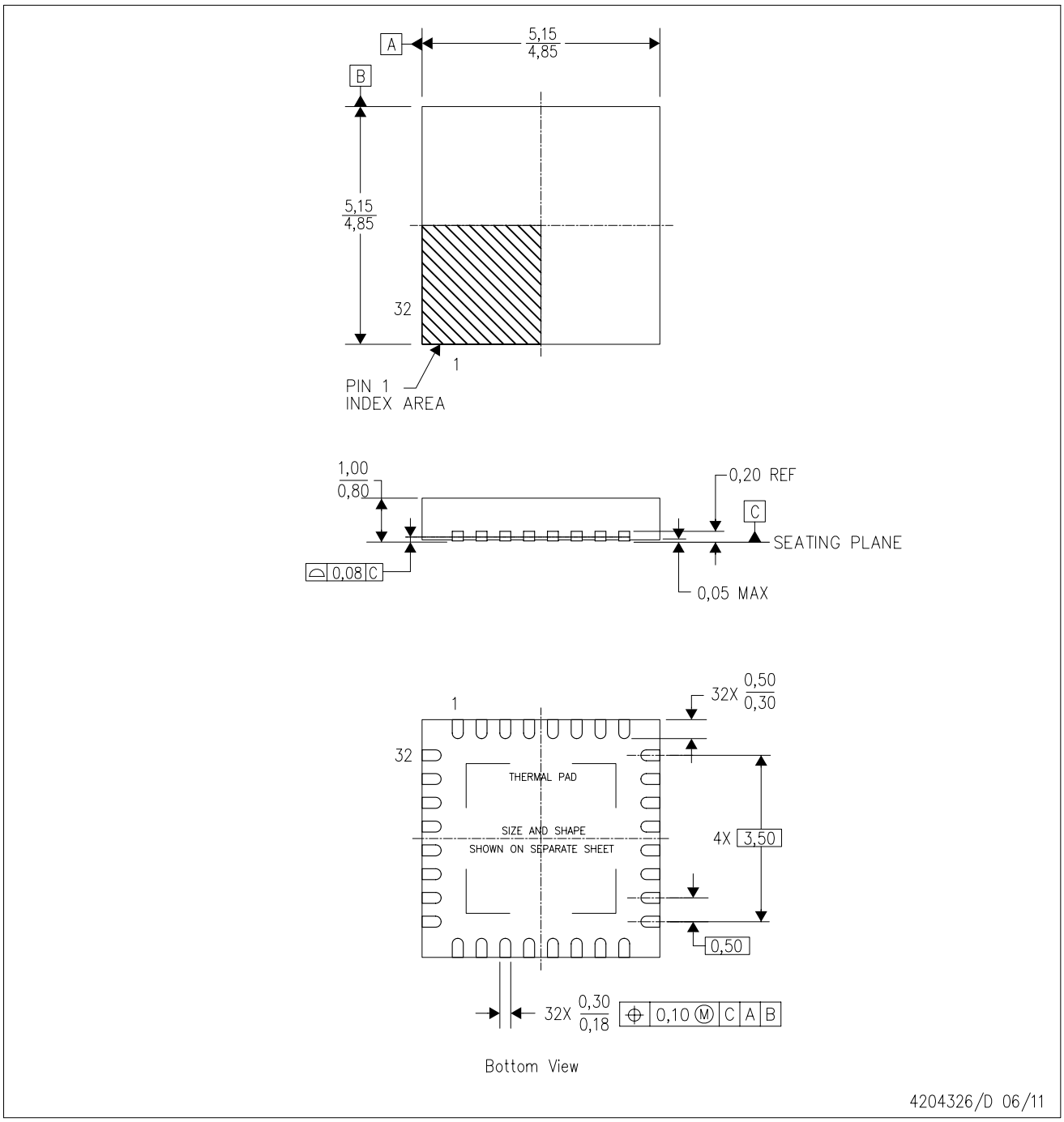


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.2	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

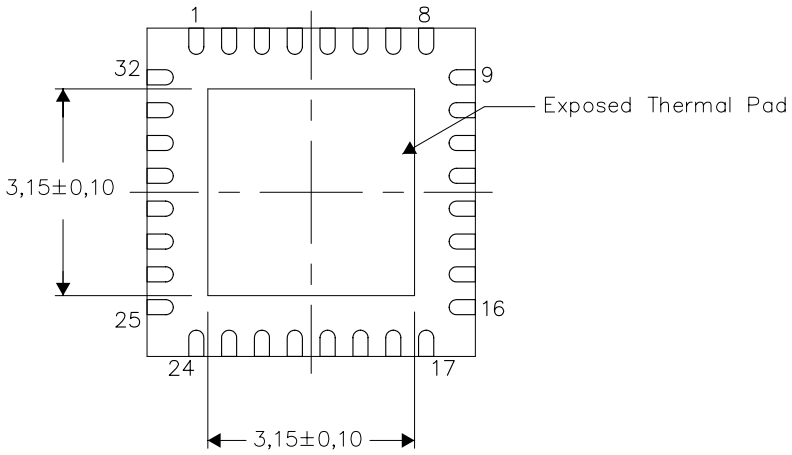
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



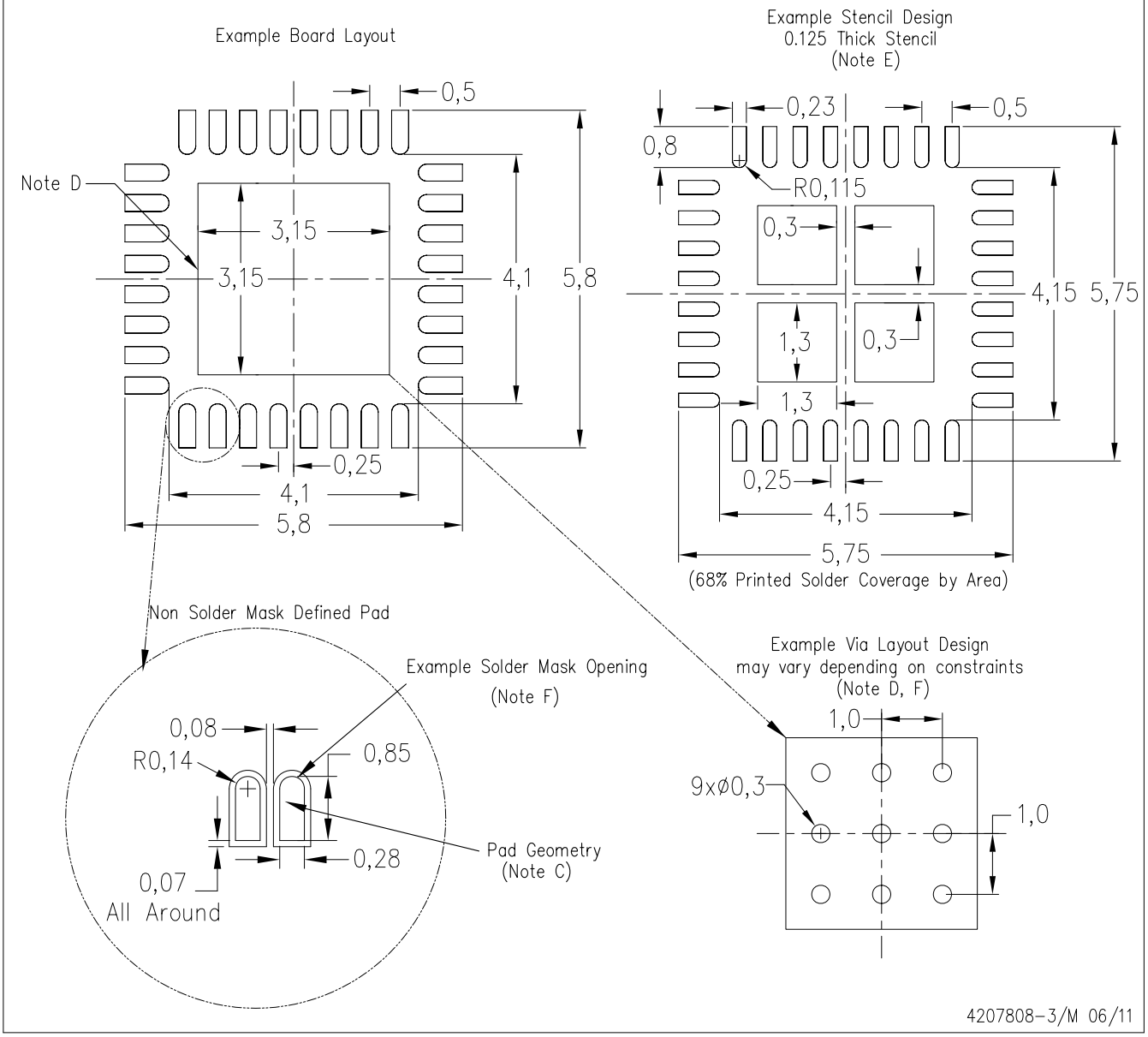
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/U 06/11

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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