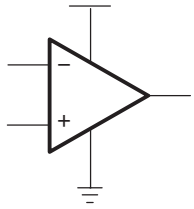
WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

Check for Samples: TLC080-Q1, TLC081-Q1, TLC082-Q1, TLC083-Q1, TLC084-Q1, TLC085-Q1

FEATURES

- Wide Bandwidth...10 MHz
- High Output Drive
  - I_{OH}...57 mA at V_{DD} –1.5 V
  - I_{OL}...55 mA at 0.5 V
- High Slew Rate
  - SR+...16 V/µs
  - SR−...19 V/µs
- Wide Supply Range...4.5 V to 16 V
- Supply Current...1.9 mA/Channel
- Ultralow-Power Shutdown Mode
  I_{DD}...125 µ/Channel
- Low Input Noise Voltage...8.5 nV$\sqrt{Hz}$
- Input Offset Voltage...60 µV
- Ultra-Small Packages
  8- or 10-Pin MSOP (TLC080/081/082/083) (1)

Operational Amplifier



(1) TLC080/081/083 in Product Preview

DESCRIPTION

The first members of TI's new BiMOS general-purpose operational amplifier family are the TLC08x. The BiMOS family concept is simple—provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher ac and dc performance. With performance rated from 4.5 V to 16 V across an automotive temperature range (–40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial, and instrumentation applications. Familiar features, such as offset nulling pins, and new features, such as MSOP PowerPAD™ packages and shutdown modes, enable higher levels of performance in a variety of applications.

Developed in TI's patented LBC3 BiCMOS process, the new BiMOS amplifiers combine a very high input impedance, low-noise CMOS front end with a high-drive bipolar output stage, thus providing the optimum performance features of both. AC performance improvements over the TL08x BiFET predecessors include a bandwidth of 10 MHz (an increase of 300%) and voltage noise of 8.5 nV/$\sqrt{Hz}$ (an improvement of 60%). DC improvements include an ensured V_{ICR} that includes ground, a factor of 4 reduction in input offset voltage down to 1.5 mV (maximum), and a power-supply rejection improvement of greater than 40 dB to 130 dB. Added to this list of impressive features is the ability to drive ±50-mA loads comfortably from an ultra-small-footprint MSOP PowerPAD package, which positions the TLC08x as the ideal high-performance general-purpose operational amplifier family.

Table 1. FAMILY PACKAGES

DEVICE	NO. OF CHANNELS	PACKAGE			SHUTDOWN	UNIVERSAL EVM BOARD
		MSOP	SOIC	TSSOP		
TLC080(1)	1	8	8	—	Yes	Refer to the *EVM Selection Guide* (literature number SLOU060)
TLC081(1)	1	8	8	—	—	
TLC082	2	8	8	—	—	
TLC083(1)	2	10	14	—	Yes	
TLC084	4	—	14	20	—	
TLC085(1)	4	—	16	20	Yes	

(1) Product Preview

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
PowerPAD is a trademark of Texas Instruments.
Parts, PSpice are trademarks of MicroSim Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006–2011, Texas Instruments Incorporated

Table 2. TLC080 and TLC081 AVAILABLE OPTIONS(1) (2)

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (D)(3)	SMALL OUTLINE (DGN)(3)
–40°C to 125°C	TLC080QDRQ1 TLC081QDRQ1	TLC080QDGNRQ1 TLC081QDGNRQ1

(1) Product Preview
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.
(3) This package is available taped and reeled.

Table 3. TLC082 and TLC083 AVAILABLE OPTIONS (1)

T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)(2)	MSOP (DGN)(2)	MSOP (DGQ)(2)
–40°C to 125°C	TLC082QDRQ1(3) TLC083QDRQ1(3)	TLC082QDGNRQ1	TLC083QDGQRQ1(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.
(2) This package is available taped and reeled.
(3) Product Preview

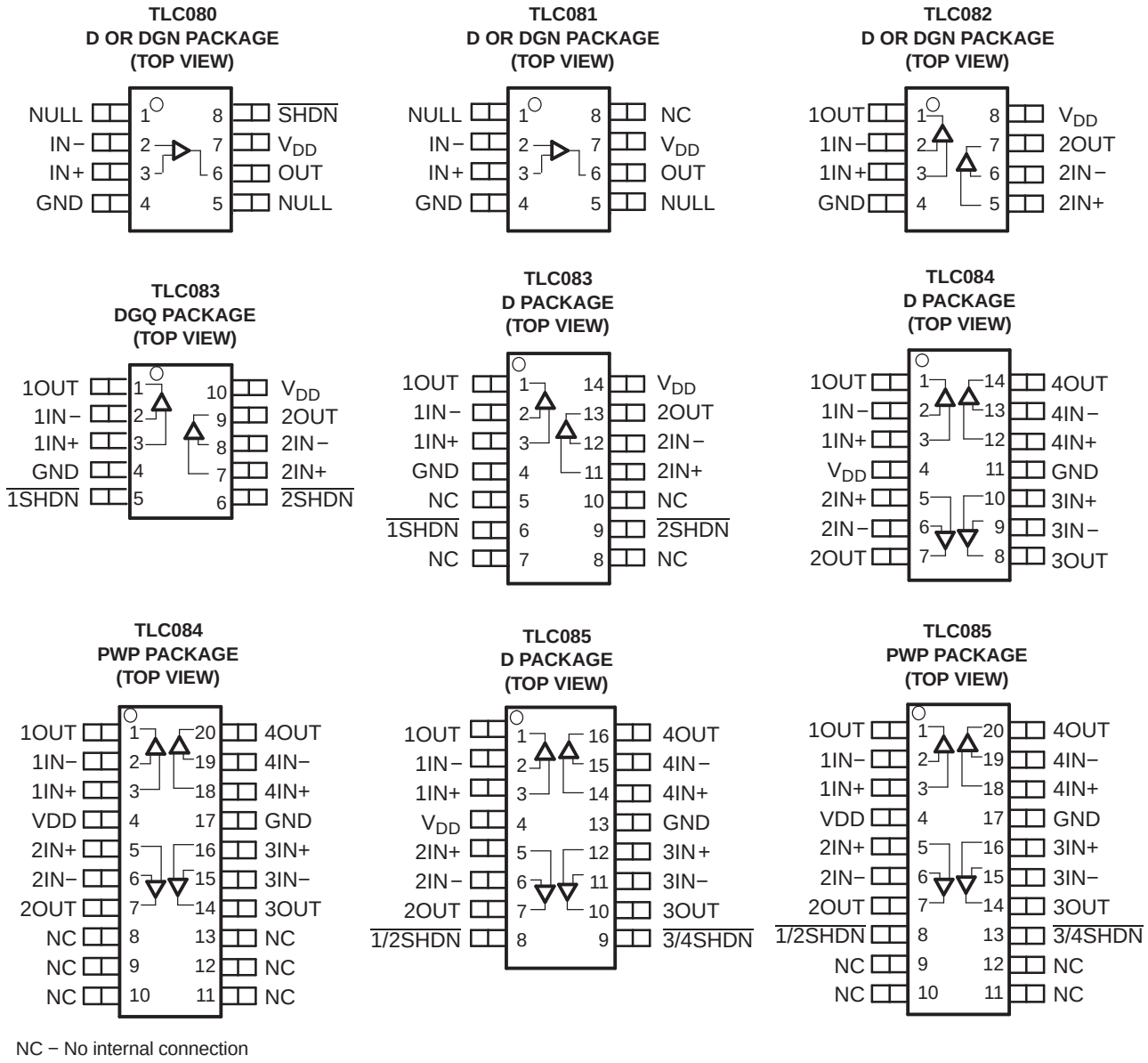
Table 4. TLC084 and TLC085 AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (D)(2)	TSSOP (PWP)(2)
–40°C to 125°C	TLC084QDRQ1(3) TLC085QDRQ1(3)	TLC084QPWPRQ1 TLC085QPWPRQ1(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.
(2) This package is available taped and reeled.
(3) Product Preview

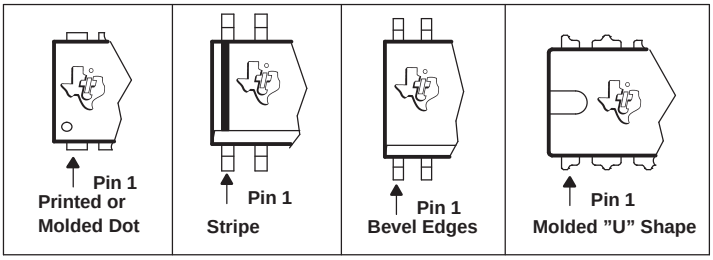
Copyright © 2006–2011, Texas Instruments Incorporated

Figure 1. TLC08x PACKAGE PINOUTS



NC − No internal connection

Figure 2. Typical Pin 1 Indicators



Copyright © 2006–2011, Texas Instruments Incorporated

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage(2)		17	V
V_{ID}	Differential input voltage		$\pm V_{DD}$	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_J	Operating junction temperature range	–40	125	°C
T_A	Operating ambient temperature range	–40	125	°C
$T_{J(max)}$	Maximum junction temperature		150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND .

Dissipation Ratings

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \le 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DGN (8)	4.7	52.7	2.37 W
DGQ (10)	4.7	52.3	2.39 W
PWP (20)	1.4	26.1	4.79 W

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage	Single supply	4.5	16	V
		Split supply	±2.25	±8	
V_{ICR}	Common-mode input voltage		GND	V_{DD} – 2	V
	Shutdown on/off voltage level(1)	V_{IH}	2		V
		V_{IL}		0.8	
T_J	Operating junction temperature		–40	125	°C

(1) Relative to the voltage on the GND terminal of the device

Copyright © 2006–2011, Texas Instruments Incorporated

Electrical Characteristics

V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		390	1900	μV
				Full range			3300	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω				1.2		μV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		1.9	50	pA
				Full range			700	
I_{IB}	Input bias current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		3	50	pA
				Full range			700	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω		25°C	0 to 3	0 to 3.5		V
				Full range	0 to 3	0 to 3.5		
V_{OH}	High-level output voltage	V_{IC} = 2.5 V	I_{OH} = –1 mA	25°C	4.1	4.3		V
				Full range	3.9			
			I_{OH} = –20 mA	25°C	3.7	4		
				Full range	3.5			
			I_{OH} = –35 mA	25°C	3.4	3.8		
				Full range	3.2			
			I_{OH} = –50 mA	25°C	3.2	3.6		
				Full range	3			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 1 mA	25°C		0.18	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.39	
				Full range			0.45	
			I_{OL} = 35 mA	25°C		0.43	0.55	
				Full range			0.7	
			I_{OL} = 50 mA	25°C		0.45	0.63	
				Full range			0.7	
I_{OS}	Short-circuit output current	Sourcing		25°C		100		mA
		Sinking				100		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail				55		
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ		25°C	100	120		dB
				Full range	100			
$r_{j(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		22.9		pF
Z_O	Closed-loop output impedance	f = 10 kHz, A_V = 10		25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3 V, R_S = 50 Ω		25°C	70	110		dB
				Full range	70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.5 V to 16 V, V_{IC} = V_{DD}/2, No load		25°C	80	100		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load		25°C		1.8	2.5	mA
				Full range			3.5	
$I_{DD(SHDN)}$	Supply current in shutdown mode (per channel) (TLC080, TLC083, TLC085)	$\overline{SHDN}$ ≤ 0.8 V		25°C		125	200	μA
				Full range			250	

(1) Full range is –40°C to 125°C.

Copyright © 2006–2011, Texas Instruments Incorporated

Operating Characteristics

V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J (1)	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 50 pF, R_L = 10 kΩ		25°C	10	16		V/μs
				Full range	9			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 50 pF, R_L = 10 kΩ		25°C	11	19		V/μs
				Full range	8.5			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		12		nV/√Hz
		f = 1 kHz				8.5		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002		%
			A_V = 10			0.012		
			A_V = 100			0.085		
$t_{(on)}$	Amplifier turn-on time(2)	R_L = 10 kΩ		25°C		0.15		μs
$t_{(off)}$	Amplifier turn-off time(2)	R_L = 10 kΩ		25°C		1.3		μs
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ		25°C		10		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.18		μs
			0.01%			0.39		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.18		
			0.01%			0.39		
φ_m	Phase margin	R_L = 10 kΩ	C_L = 50 pF	25°C		32		deg
			C_L = 0 pF			40		
	Gain margin	R_L = 10 kΩ	C_L = 50 pF	25°C		2.2		dB
			C_L = 0 pF			3.3		

(1) Full range is –40°C to 125°C.
(2) Disable time and enable time are defined as the interval between application of the logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.

Copyright © 2006–2011, Texas Instruments Incorporated

Electrical Characteristics

V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω		25°C		390	1900	μV
				Full range			3300	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω				1.2		μV/°C
I_{IO}	Input offset current	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω		25°C		1.5	50	pA
				Full range			700	
I_{IB}	Input bias current	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω		25°C		3	50	pA
				Full range			700	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω		25°C	0 to 10	0 to 10.5		V
				Full range	0 to 10	0 to 10.5		
V_{OH}	High-level output voltage	V_{IC} = 6 V	I_{OH} = –1 mA	25°C	11.1	11.2		V
				Full range	11			
			I_{OH} = –20 mA	25°C	10.8	11		
				Full range	10.7			
			I_{OH} = –35 mA	25°C	10.6	10.7		
				Full range	10.3			
			I_{OH} = –50 mA	25°C	10.3	10.5		
				Full range	10.1			
V_{OL}	Low-level output voltage	V_{IC} = 6 V	I_{OL} = 1 mA	25°C		0.17	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.45	
				Full range			0.55	
			I_{OL} = 35 mA	25°C		0.4	0.52	
				Full range			0.6	
			I_{OL} = 50 mA	25°C		0.45	0.6	
				Full range			0.7	
I_{OS}	Short-circuit output current	Sourcing		25°C		150		mA
		Sinking				150		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail				55		
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 8 V, R_L = 10 kΩ		25°C	110	130		dB
				Full range	110			
$r_{j(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		21.6		pF
Z_O	Closed-loop output impedance	f = 10 kHz, A_V = 10		25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 10 V, R_S = 50 Ω		25°C	80	110		dB
				Full range	80			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.5 V to 16 V, V_{IC} = V_{DD}/2, No load		25°C	80	100		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 7.5 V, No load		25°C		1.9	2.9	mA
				Full range			3.5	
$I_{DD(SHDN)}$	Supply current in shutdown mode (per channel) (TLC080, TLC083, TLC085)	$\overline{SHDN}$ ≤ 0.8 V		25°C		125	200	μA
				Full range			250	

(1) Full range is –40°C to 125°C.

Copyright © 2006–2011, Texas Instruments Incorporated

Operating Characteristics

V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J (1)	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 50 pF, R_L = 10 kΩ		25°C	10	16		V/μs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 50 pF, R_L = 10 kΩ		25°C	12.5	19		V/μs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz				8.5		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 8 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002		%
			A_V = 10			0.005		
			A_V = 100			0.022		
$t_{(on)}$	Amplifier turn-on time(2)	R_L = 10 kΩ		25°C		0.47		μs
$t_{(off)}$	Amplifier turn-off time(2)	R_L = 10 kΩ		25°C		2.5		μs
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ		25°C		10		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.17		μs
			0.01%			0.22		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.17		
			0.01%			0.29		
φ_m	Phase margin	R_L = 10 kΩ	C_L = 50 pF	25°C		37		deg
			C_L = 0 pF			42		
	Gain margin	R_L = 10 kΩ	C_L = 50 pF	25°C		3.1		dB
			C_L = 0 pF			4		

(1) Full range is –40°C to 125°C.
(2) Disable time and enable time are defined as the interval between application of the logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.

Copyright © 2006–2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

Table 5. Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IO}	Input offset current	vs Free-air temperature	3, 4
I_{IB}	Input bias current	vs Free-air temperature	3, 4
V_{OH}	High-level output voltage	vs High-level output current	5, 7
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8
Z_O	Output impedance	vs Frequency	9
I_{DD}	Supply current	vs Supply voltage	10
PSRR	Power supply rejection ratio	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
V_n	Equivalent input noise voltage	vs Frequency	13
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	14, 15
	Crosstalk	vs Frequency	16
	Differential voltage gain	vs Frequency	17, 18
	Phase	vs Frequency	17, 18
φ_m	Phase margin	vs Load capacitance	19, 20
	Gain margin	vs Load capacitance	21, 22
	Gain-bandwidth product	vs Supply voltage	23
SR	Slew rate	vs Supply voltage	24
		vs Free-air temperature	25, 26
THD+N	Total harmonic distortion plus noise	vs Frequency	27, 28
		vs Peak-to-peak output voltage	29, 30
	Large-signal follower pulse response		31, 32
	Small-signal follower pulse response		33
	Large-signal inverting pulse response		34, 35
	Small-signal inverting pulse response		36
	Shutdown forward isolation	vs Frequency	37, 38
	Shutdown reverse isolation	vs Frequency	39, 40
	Shutdown supply current	vs Supply voltage	41
		vs Free-air temperature	42
	Shutdown pulse		43, 44

Copyright © 2006–2011, Texas Instruments Incorporated

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

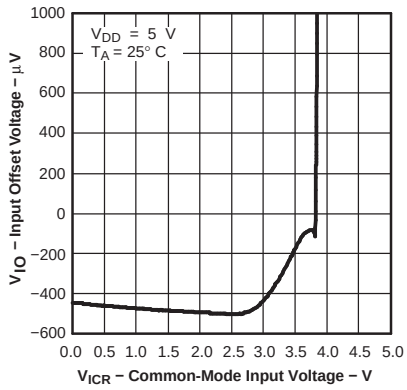


Figure 3.

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

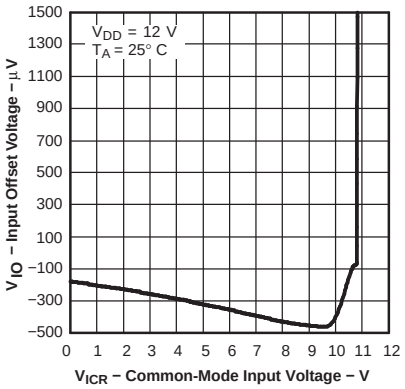


Figure 4.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

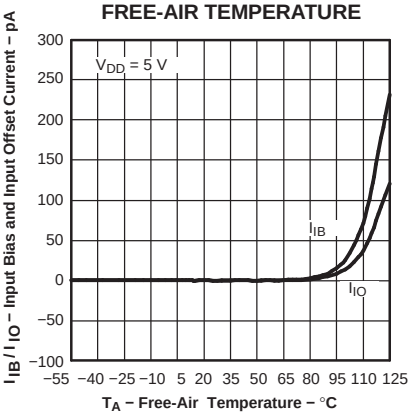


Figure 5.

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

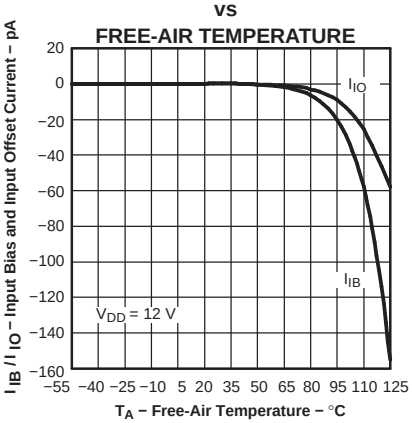


Figure 6.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

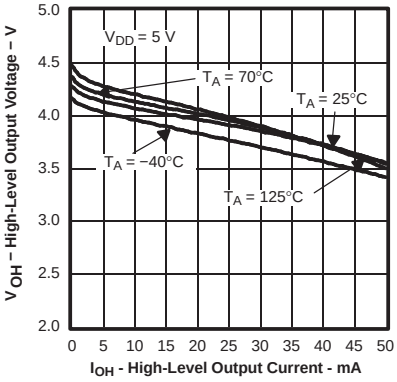


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

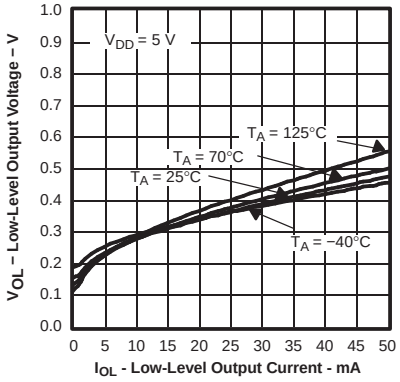


Figure 8.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

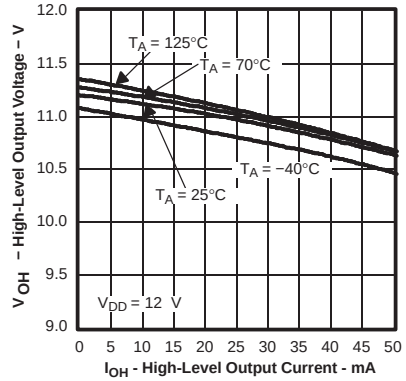


Figure 9.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

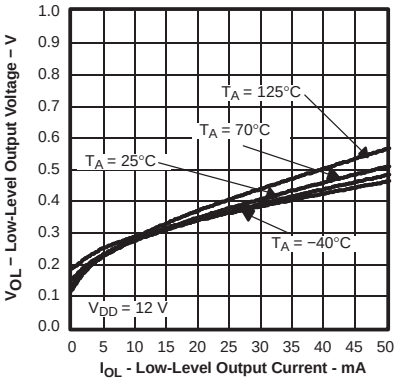


Figure 10.

OUTPUT IMPEDANCE vs FREQUENCY

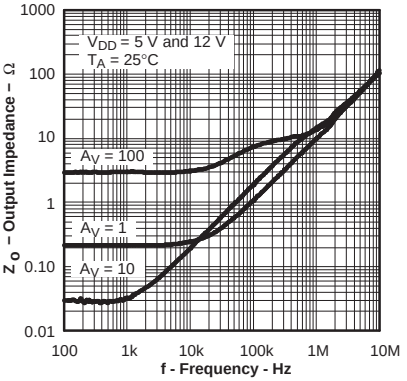


Figure 11.

Copyright © 2006–2011, Texas Instruments Incorporated

SUPPLY CURRENT vs SUPPLY VOLTAGE

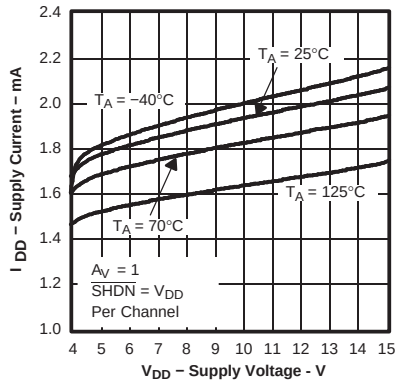


Figure 12.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

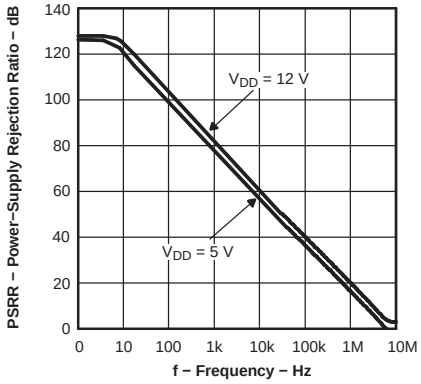


Figure 13.

COMMON-MODE REJECTION RATIO vs FREQUENCY

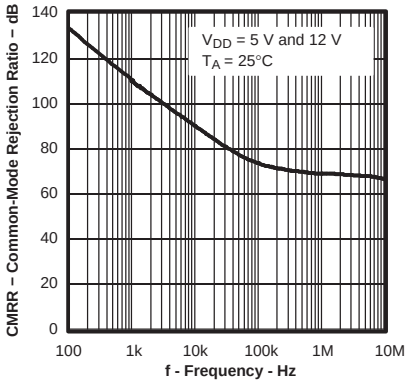


Figure 14.

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

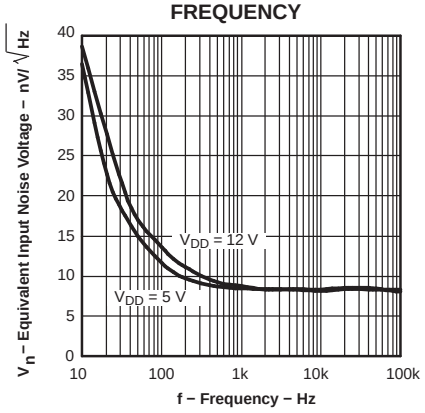


Figure 15.

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

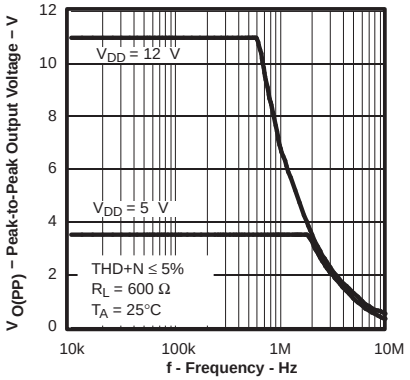


Figure 16.

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

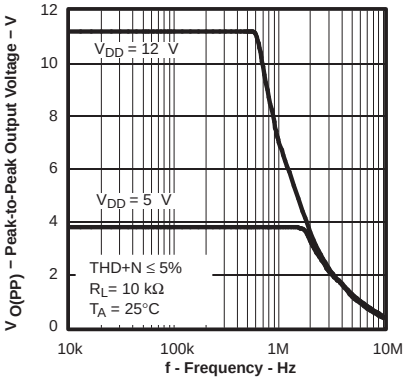


Figure 17.

CROSSTALK vs FREQUENCY

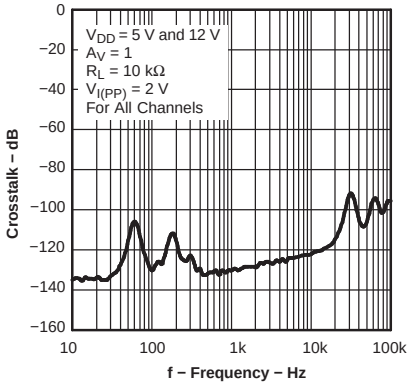


Figure 18.

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

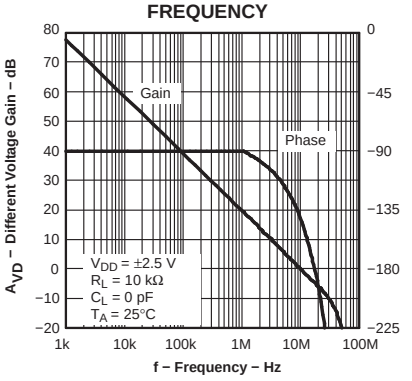


Figure 19.

DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY

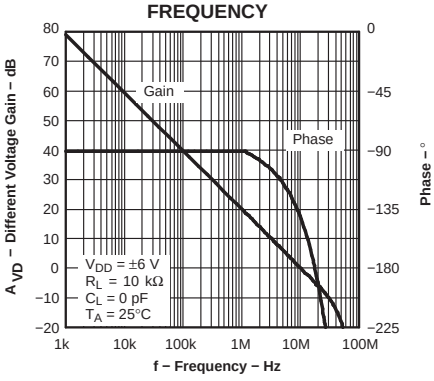


Figure 20.

Copyright © 2006–2011, Texas Instruments Incorporated

PHASE MARGIN vs LOAD CAPACITANCE

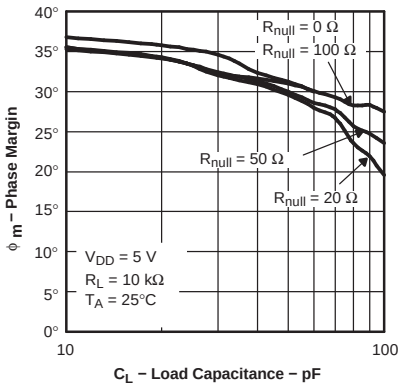


Figure 21.

PHASE MARGIN vs LOAD CAPACITANCE

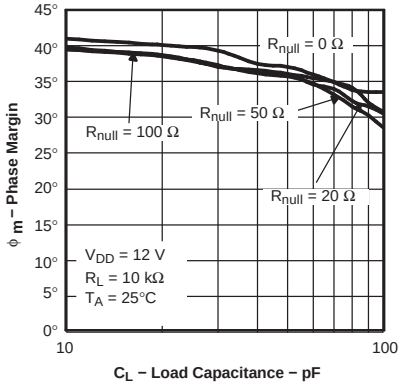


Figure 22.

GAIN MARGIN vs LOAD CAPACITANCE

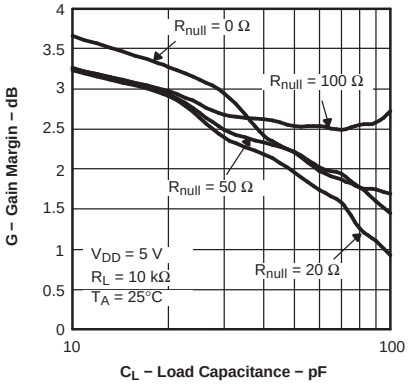


Figure 23.

GAIN MARGIN vs LOAD CAPACITANCE

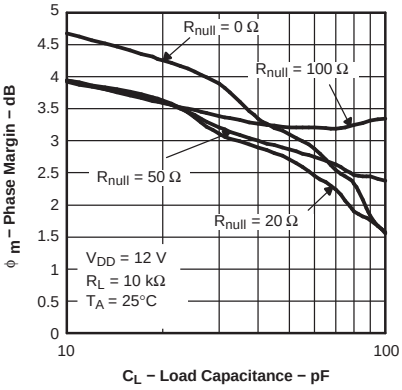


Figure 24.

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

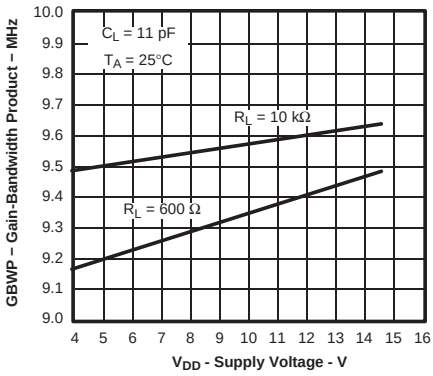


Figure 25.

SLEW RATE vs SUPPLY VOLTAGE

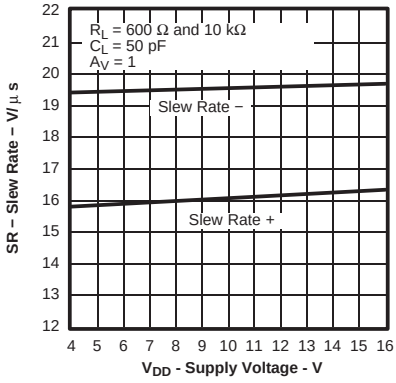


Figure 26.

SLEW RATE vs FREE-AIR TEMPERATURE

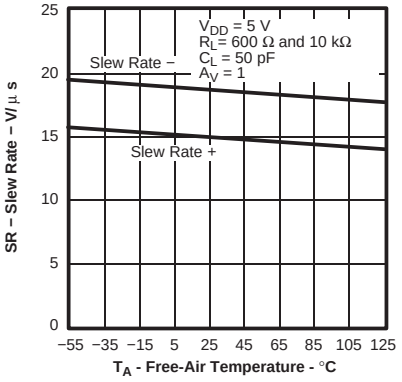


Figure 27.

SLEW RATE vs FREE-AIR TEMPERATURE

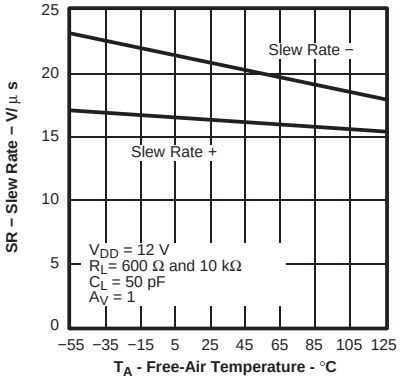


Figure 28.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

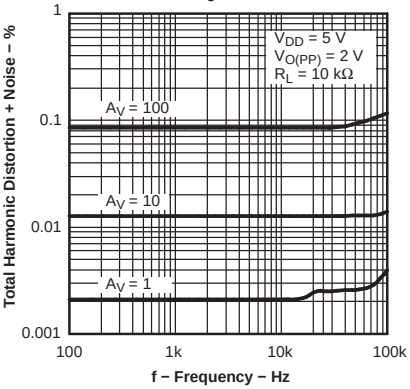


Figure 29.

Copyright © 2006–2011, Texas Instruments Incorporated

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

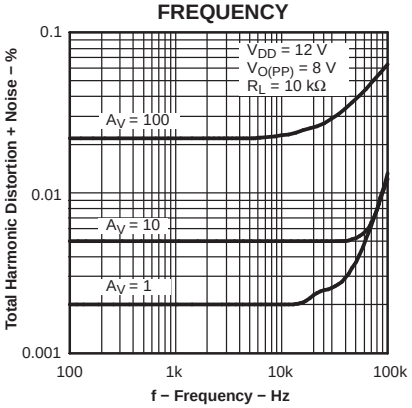


Figure 30.

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK OUTPUT VOLTAGE

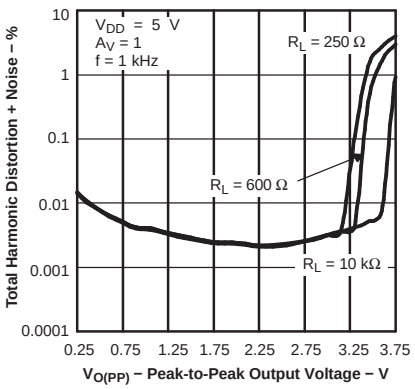


Figure 31.

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK OUTPUT VOLTAGE

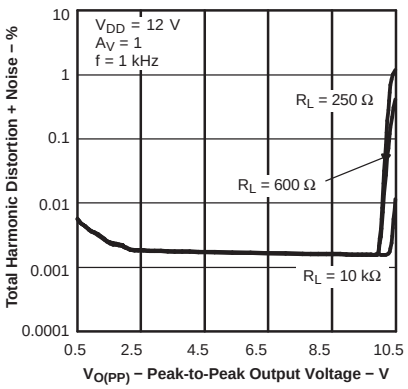


Figure 32.

LARGE-SIGNAL FOLLOWER PULSE RESPONSE

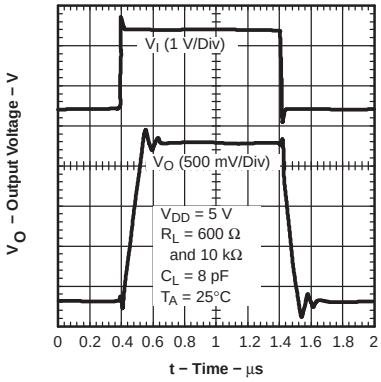


Figure 33.

LARGE-SIGNAL FOLLOWER PULSE RESPONSE

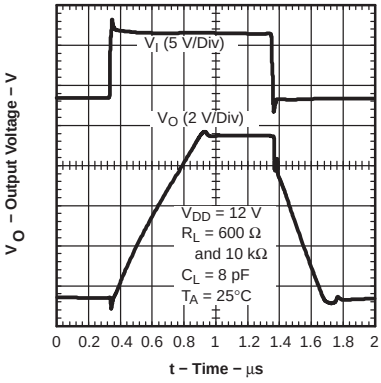


Figure 34.

SMALL-SIGNAL FOLLOWER PULSE RESPONSE

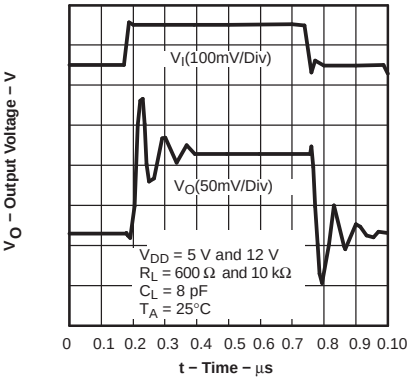


Figure 35.

LARGE-SIGNAL INVERTING PULSE RESPONSE

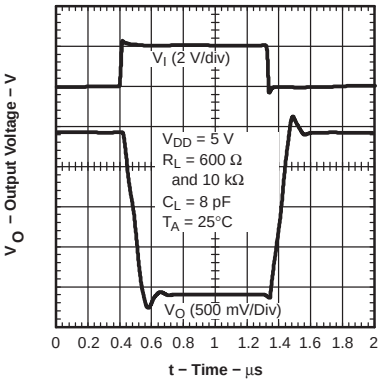


Figure 36.

LARGE-SIGNAL INVERTING PULSE RESPONSE

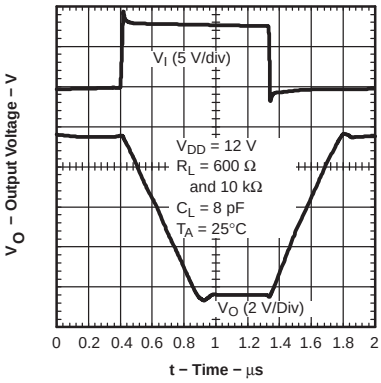


Figure 37.

SMALL-SIGNAL INVERTING PULSE RESPONSE

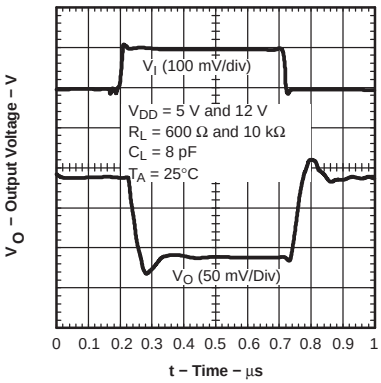


Figure 38.

Copyright © 2006–2011, Texas Instruments Incorporated

SHUTDOWN FORWARD ISOLATION vs FREQUENCY

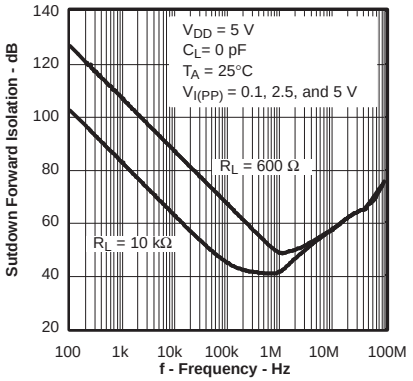


Figure 39.

SHUTDOWN FORWARD ISOLATION vs FREQUENCY

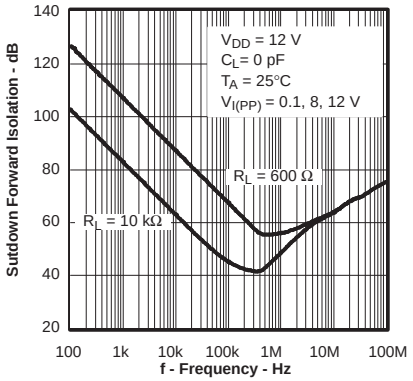


Figure 40.

SHUTDOWN REVERSE ISOLATION vs FREQUENCY

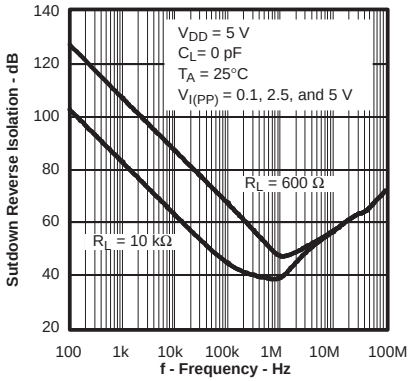


Figure 41.

SHUTDOWN REVERSE ISOLATION vs FREQUENCY

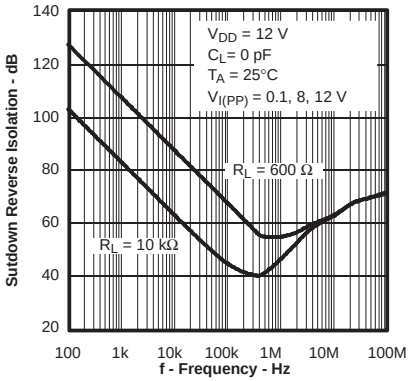


Figure 42.

SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

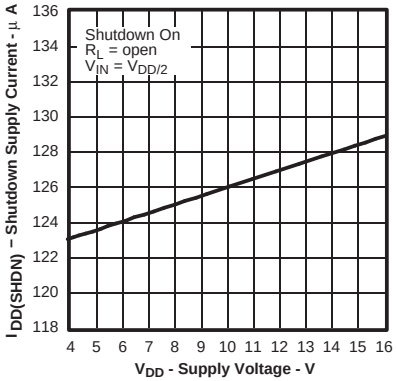


Figure 43.

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

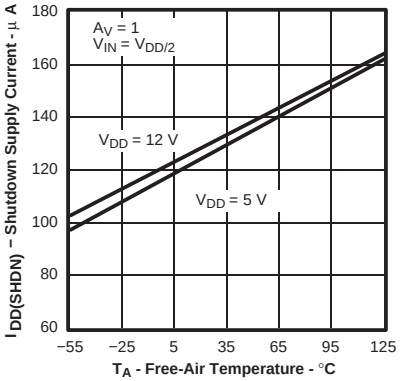


Figure 44.

SHUTDOWN PULSE

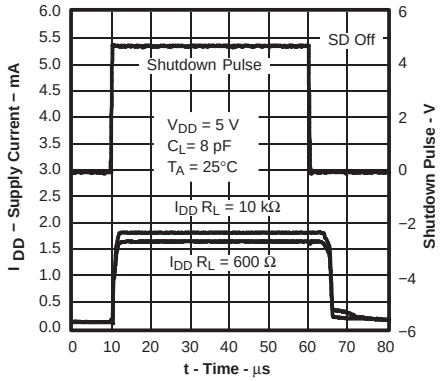


Figure 45.

SHUTDOWN PULSE

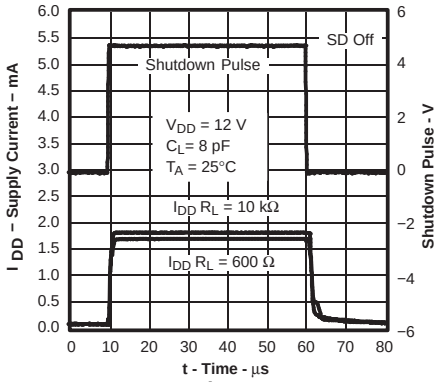


Figure 46.

Copyright © 2006–2011, Texas Instruments Incorporated

PARAMETER MEASUREMENT INFORMATION

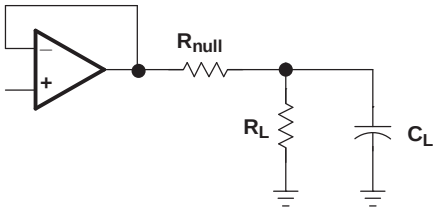


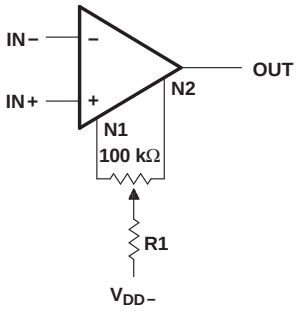
Figure 47.

Copyright © 2006–2011, Texas Instruments Incorporated

APPLICATION INFORMATION

Input Offset Voltage Null Circuit

The TLC080 and TLC081 have an input offset nulling function (see Figure 48).



A. R1 = 5.6 kΩ for offset voltage adjustment of ±10 mV
R1 = 20 kΩ for offset voltage adjustment of ±3 mV

Figure 48. Input Offset Voltage Null Circuit

Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications.

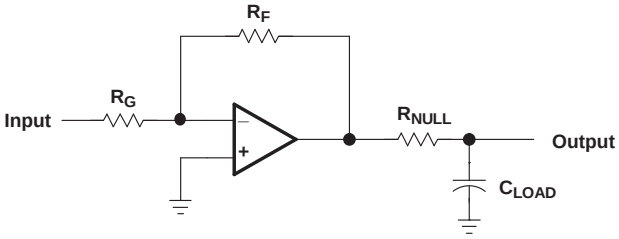
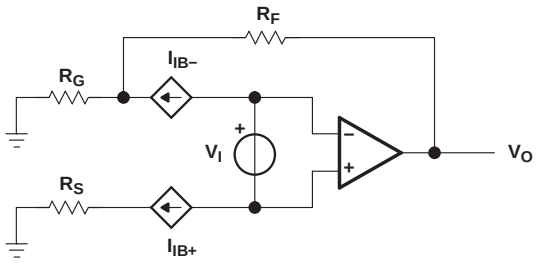


Figure 49. Driving a Capacitive Load

Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The schematic and formula in Figure 50 can be used to calculate the output offset voltage.



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 50. Output Offset Voltage Model

Copyright © 2006–2011, Texas Instruments Incorporated

High-Speed CMOS Input Amplifiers

The TLC08x is a family of high-speed low-noise CMOS input operational amplifiers that has an input capacitance on the order of 20 pF. Any resistor used in the feedback path adds a pole in the transfer function equivalent to the input capacitance multiplied by the combination of source resistance and feedback resistance. For example, a gain of –10, a source resistance of 1 kΩ, and a feedback resistance of 10 kΩ add an additional pole at approximately 8 MHz. This is more apparent with CMOS amplifiers than bipolar amplifiers due to their greater input capacitance.

This is of little consequence on slower CMOS amplifiers, as this pole normally occurs at frequencies above their unity-gain bandwidth. However, the TLC08x with its 10-MHz bandwidth means that this pole normally occurs at frequencies where there is on the order of 5-dB gain left and the phase shift adds considerably.

The effect of this pole is the strongest with large feedback resistances at small closed loop gains. As the feedback resistance is increased, the gain peaking increases at a lower frequency and the 180° phase shift crossover point also moves down in frequency, decreasing the phase margin.

For the TLC08x, the maximum feedback resistor recommended is 5 kΩ; larger resistances can be used but a capacitor in parallel with the feedback resistor is recommended to counter the effects of the input capacitance pole.

The TLC083 with a 1-V step response has an 80% overshoot with a natural frequency of 3.5 MHz when configured as a unity gain buffer and with a 10-kΩ feedback resistor. By adding a 10-pF capacitor in parallel with the feedback resistor, the overshoot is reduced to 40% and eliminates the natural frequency, resulting in a much faster settling time (see Figure 51). The 10-pF capacitor was chosen for convenience only.

Load capacitance had little effect on these measurements due to the excellent output drive capability of the TLC08x.

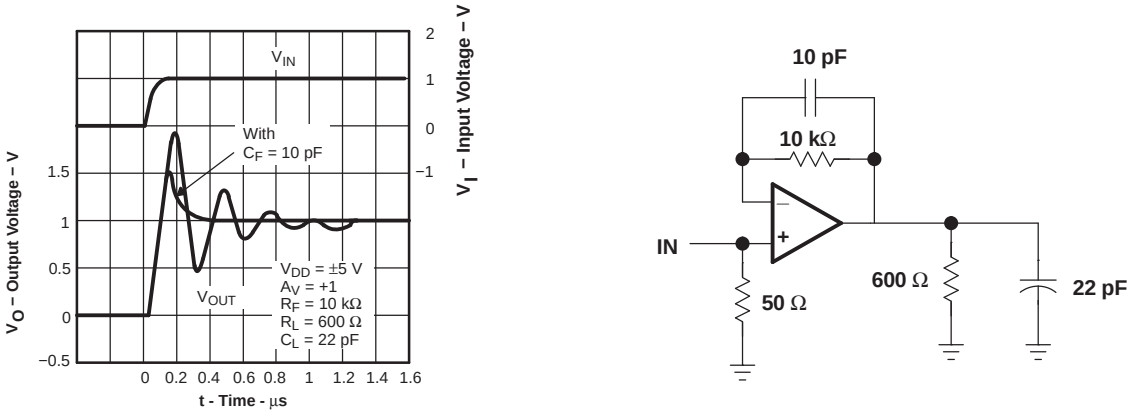


Figure 51. 1-V Step Response

Copyright © 2006–2011, Texas Instruments Incorporated

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 52).

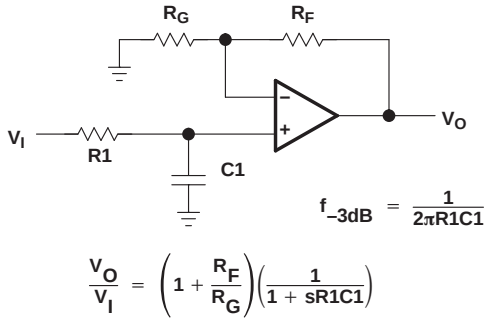


Figure 52. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

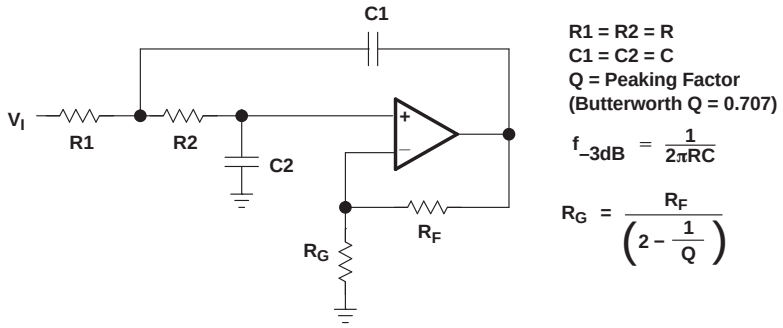


Figure 53. 2-Pole Low-Pass Sallen-Key Filter

Shutdown Function

Three members of the TLC08x family (TLC080/3/5) have a shutdown ($\overline{SHDN}$) terminal for conserving battery life in portable applications. When $\overline{SHDN}$ is tied low, the supply current is reduced to 125 μA/channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. To enable the amplifier, $\overline{SHDN}$ can either be left floating or pulled high. When $\overline{SHDN}$ is left floating, care should be taken to ensure that parasitic leakage current at $\overline{SHDN}$ does not inadvertently place the operational amplifier into shutdown. $\overline{SHDN}$ threshold is always referenced to the voltage on the GND terminal of the device. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), $\overline{SHDN}$ needs to be pulled to V_{DD-} (not system ground) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figure 45 and Figure 46. The amplifier is powered with a single 5-V supply and is configured as noninverting with a gain of 5. The amplifier turn-on and turn-off times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figure 39 through Figure 42 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is configured as a voltage follower (A_V = 1). The isolation performance is plotted across frequency using 0.1-V_{PP}, 2.5-V_{PP}, and 5-V_{PP} input signals at ±2.5-V supplies and 0.1-V_{PP}, 8-V_{PP}, and 12-V_{PP} input signals at ±6-V supplies.

Copyright © 2006–2011, Texas Instruments Incorporated

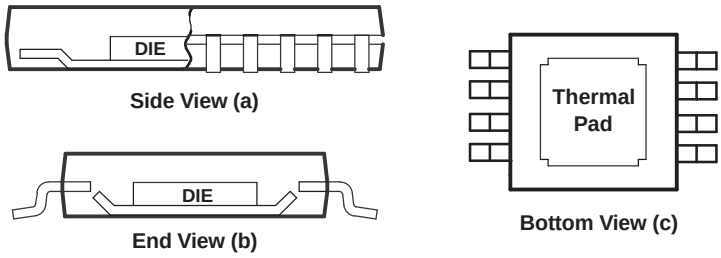
Circuit Layout Considerations

To achieve the levels of high performance of the TLC08x, follow proper printed circuit board (PCB) design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the PCB is the best implementation.
- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high-performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

General PowerPAD Design Considerations

The TLC08x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 54(a) and Figure 54(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 54(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 54. Views of Thermally-Enhanced DGN Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. **Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation.** This soldering provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

Although there are many ways to properly heatsink the PowerPAD package, the following steps list the recommended approach.

Copyright © 2006–2011, Texas Instruments Incorporated

The PowerPAD must be connected to the most negative supply voltage (GND pin potential) of the device.

1. Prepare the PCB with a top-side etch pattern (see the landing patterns at the end of this data sheet). There should be etch for the leads, as well as etch for the thermal pad.
2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLC08x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal plane that is at the same potential as the ground pin of the device.
5. When connecting these holes to this internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLC08x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal-pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal-pad area. This prevents solder from being pulled away from the thermal-pad area during the reflow process.
7. Apply solder paste to the exposed thermal-pad area and all of the IC terminals.
8. With these preparatory steps in place, the TLC08x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

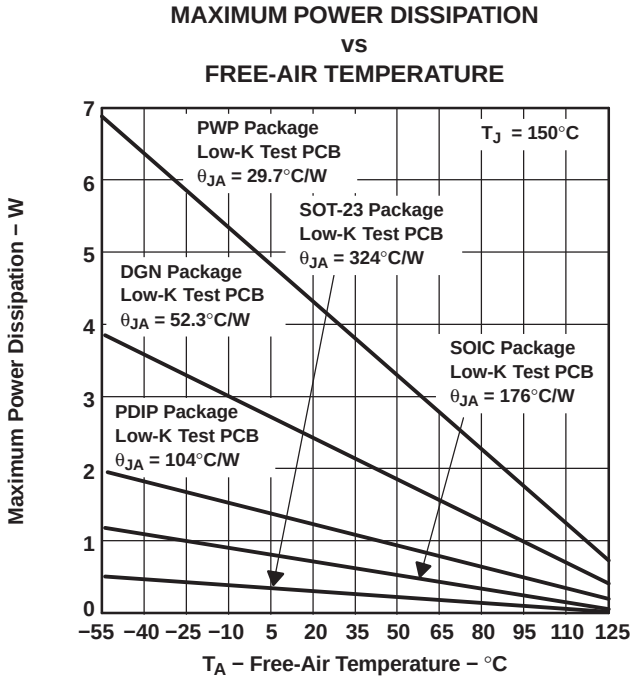
For a given θ_{JA}, the maximum power dissipation is shown in Figure 55 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (1)$$

Where:

P_D = Maximum power dissipation of TLC08x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

Copyright © 2006–2011, Texas Instruments Incorporated



A. Results are with no airflow and using JEDEC Standard Low-K test PCB.

Figure 55. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in *Typical Characteristics* are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

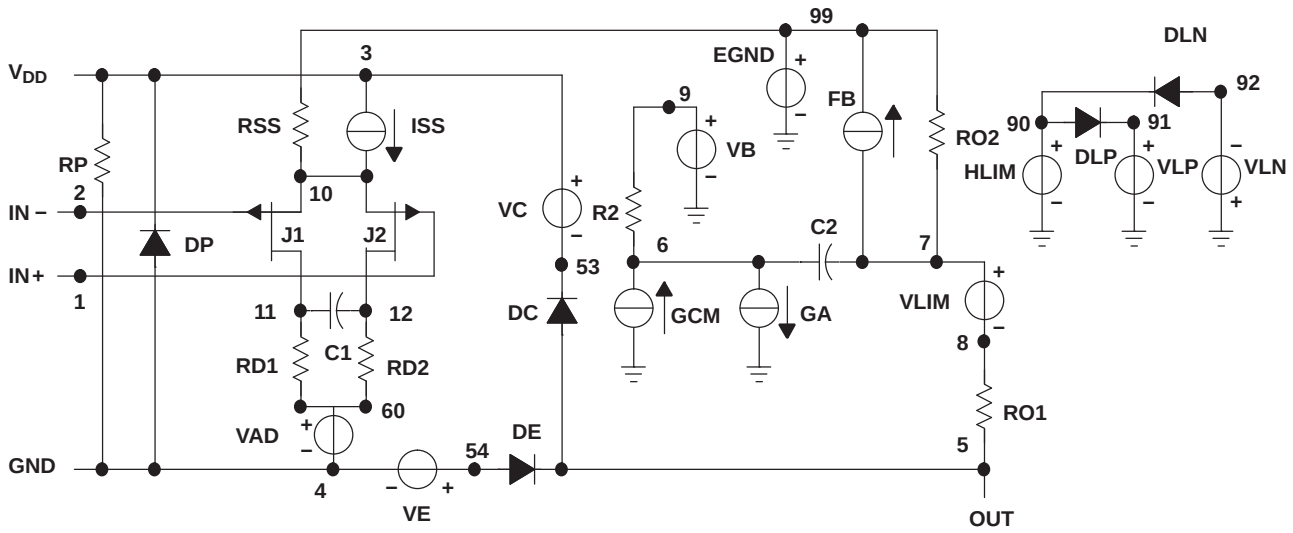
Macromodel Information

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel(1) and subcircuit in Figure 56 are generated using the TLC08x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

Copyright © 2006–2011, Texas Instruments Incorporated




```
*DEVICE=TLC08X_5V, OPAMP, PJF, INT

* TLC08X_5V − 5V operational amplifier "macromodel" subcir-
cuit
* created using Parts release 8.0 on 12/16/99 at 14:03
* Parts is a MicroSim product.
*
* connections:              | non-inverting input
*                           |  | inverting input
*                           |  |  | positive power supply
*                           |  |  |  | negative power supply
*                           |  |  |  |  | output
*                           |  |  |  |  |
.subckt TLC08X_5V  1 2 3 4 5
*
 c1     11  12  4.6015E−12
 c2     6   7   8.0000E−12
 css    10  99  986.29E−15
 dc     5   53  dy
 de     54  5   dy
 dlp    90  91  dx
 dln    92  90  dx
 dp     4   3   dx
 egnd   99  0   poly(2) (3,0) (4,0) 0 .5 .5
 fb     7   99  poly(5) vb vc ve vlp vln 0 13.984E6 −1E3 1E3
                14E6 −14E6
 ga     6   0   11  12 402.12E−6
 gcm    0   6   10  99 1.5735E−6
 ioff   0   6   dc  1.212E−6
 iss    3   10  dc  130.40E−6
 hlim   90  0   vlim 1K
 j1     11  2   10  jx1
 j2     12  1   10  jx2
 r2     6   9       100.00E3
 rd1    4   11      2.4868E3
 rd2    4   12      2.4868E3
 ro1    8   5   10
 ro2    7   99  10
 rp     3   4       2.8249E3
 rss    10  99      1.5337E6
 vb     9   0   dc  0
 vc     3   53  dc  1.5537
 ve     54  4   dc  .84373
 vlim   7   8   dc  0
 vlp    91  0   dc  117.60
 vln    0   92  dc  117.60
.model  dx  D(Is=800.00E−18)
.model  dy  D(Is=800.00E−18 Rs=1m Cjo=10p)
.model  jx1 PJF(Is=80.000E−15 Beta=1.2401E−3  Vto=−1)
.model  jx2 PJF(Is=80.000E−15 Beta=1.2401E−3  Vto=−1)
.ends
```

Figure 56. Boyle Macromodel and Subcircuit

Copyright © 2006–2011, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLC082QDGNRQ1	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TLC084QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC082-Q1, TLC084-Q1 :

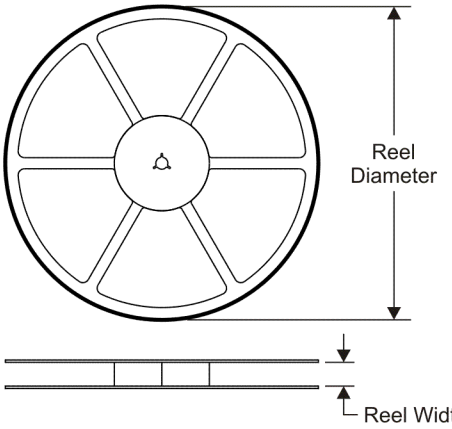
- Catalog: TLC082, TLC084

NOTE: Qualified Version Definitions:

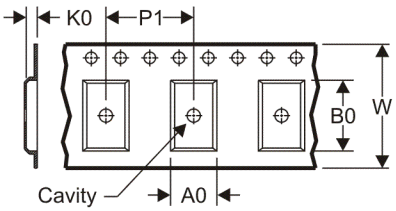
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

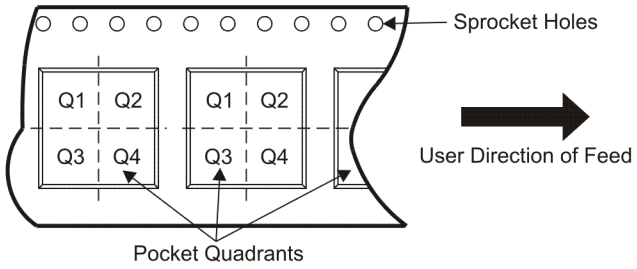


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

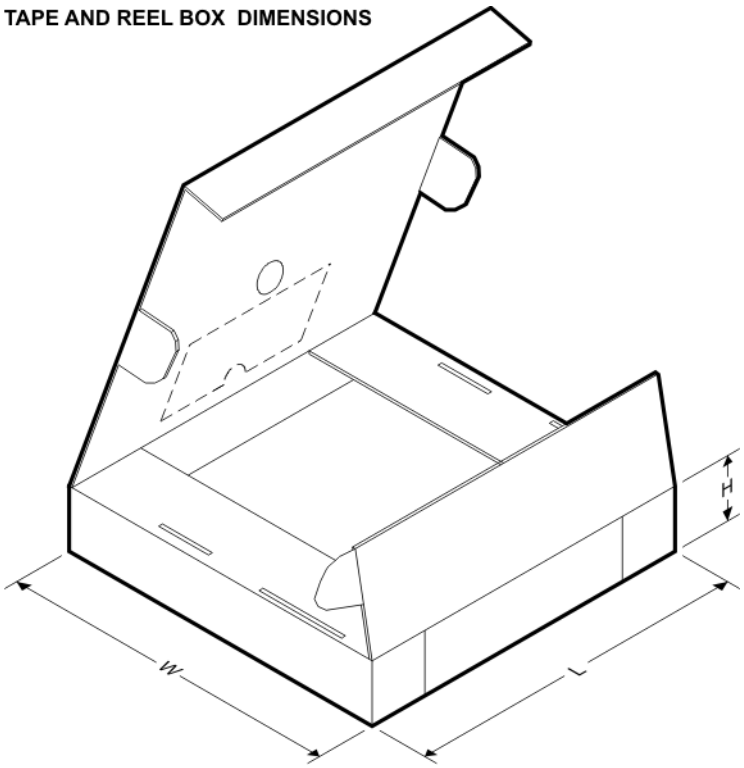
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC082QDGNRQ1	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

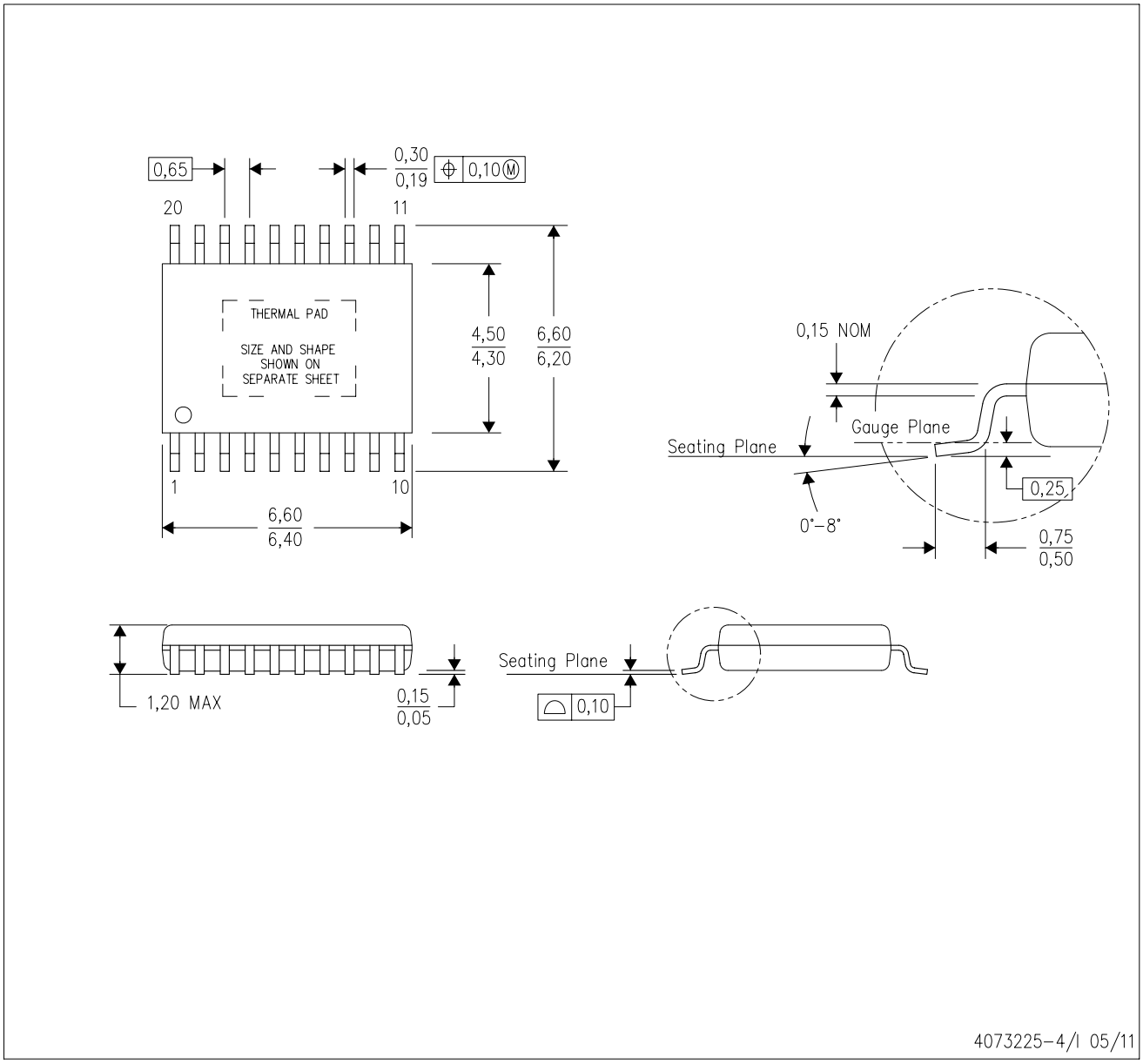
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC082QDGNRQ1	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

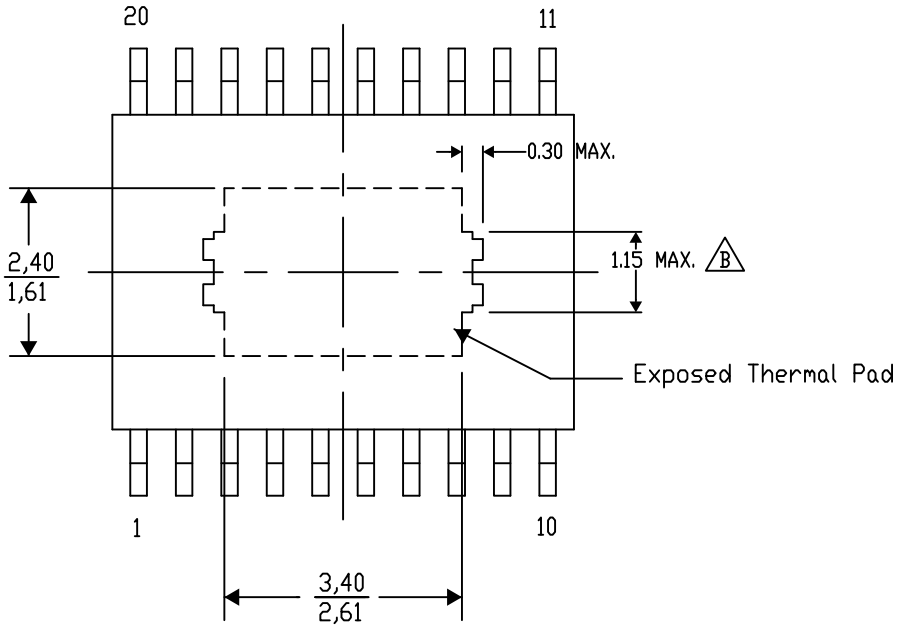
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

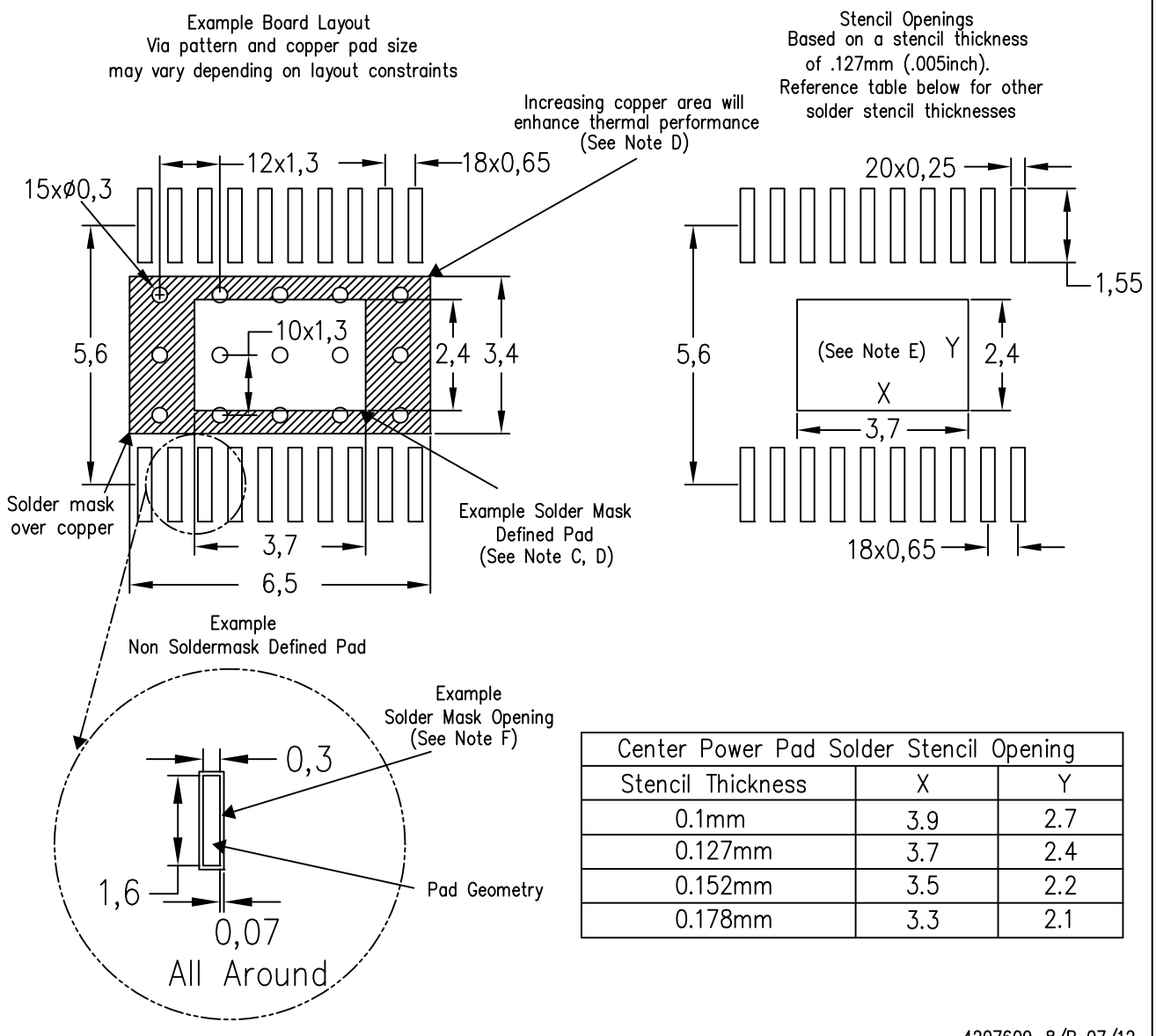
4206332–15/AC 07/12

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

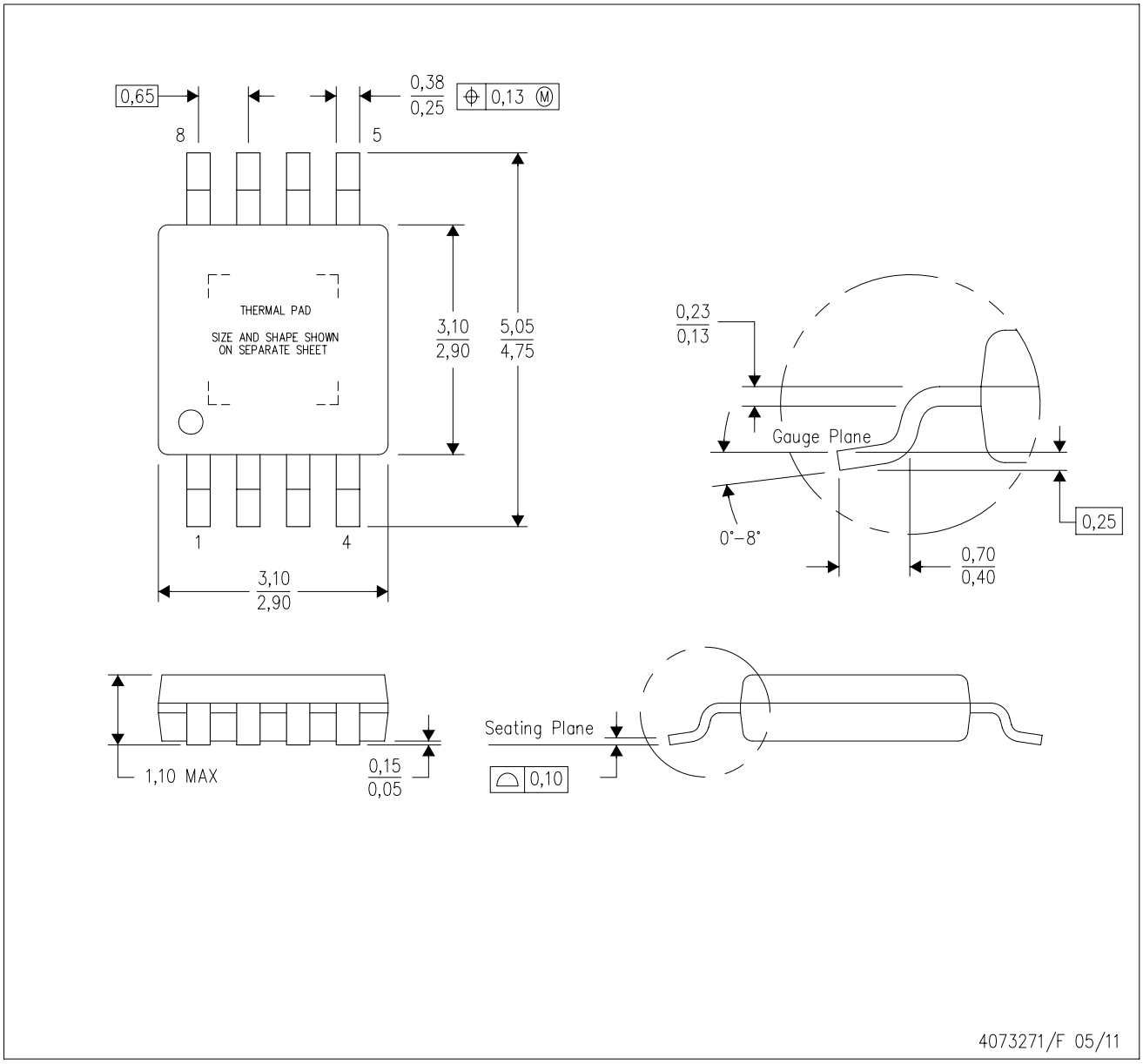


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/R 07/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated