

- Excellent Dynamic Range
- Wide Bandwidth
- Built-In Temperature Compensation
- Log Linearity (30-dB Sections) . . . 1 dB Typ
- Wide Input Voltage Range

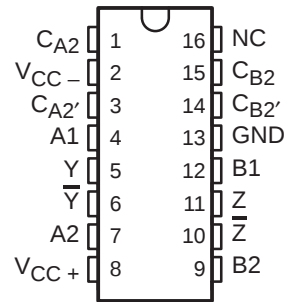
description

This amplifier circuit contains four 30-dB logarithmic stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dB input voltage range. Each half of the circuit contains two of these 30-dB stages summed together in one differential output that is proportional to the sum of the logarithms of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120-dB. In practice, this permits the input voltage range typically to be greater than 80-dB with log linearity of ± 0.5 -dB (see application data). Bandwidth is from dc to 40 MHz.

This circuit is useful in data compression and analog compensation. This logarithmic amplifier is used in log IF circuitry as well as video and log amplifiers.

The TL441 is characterized for operation over 0°C to 70°C.

N PACKAGE
(TOP VIEW)



NC — No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

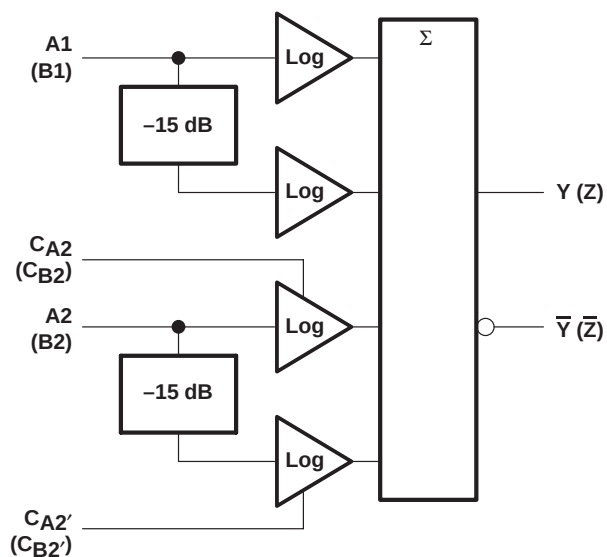
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TL441 LOGARITHMIC AMPLIFIER

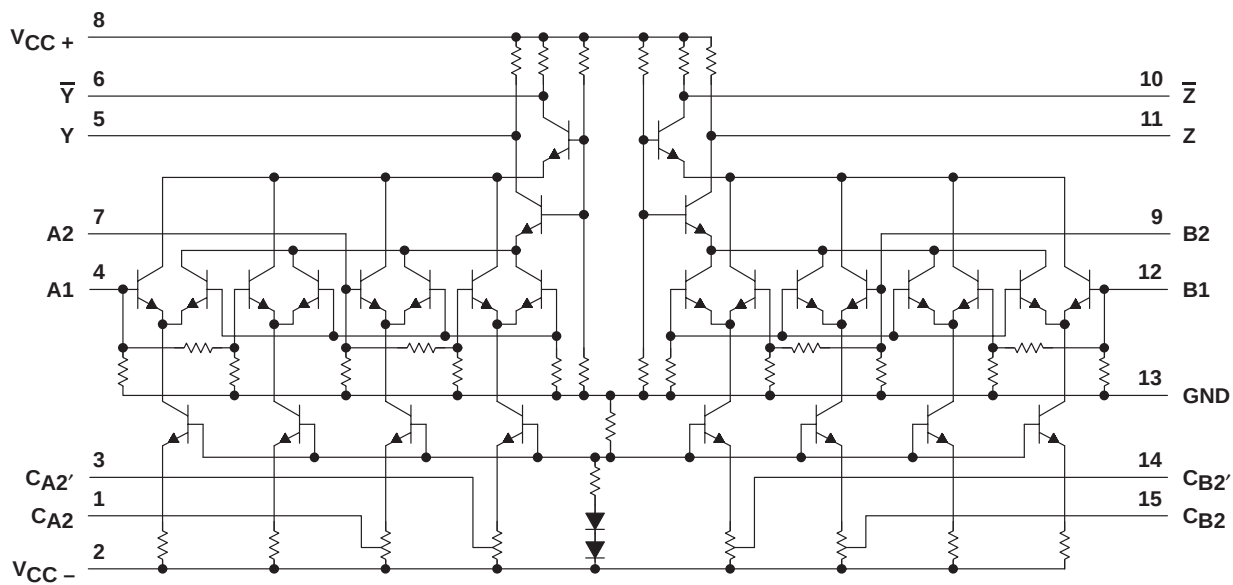
SLVS328 – OCTOBER 2000

functional logic diagram (one half)



$Y \propto \log A1 + \log A2$; $Z \propto \log B1 + \log B2$ where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.
CA2, CA2', CB2, and CB2' are detector compensation inputs.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltages (see Note 1): V_{CC+}	8 V
V_{CC-}	–8 V
Input voltage (see Note 1)	6 V
Output sink current (any one output)	30 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3)	67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages, except differential out voltages, are with respect to network ground terminal.
2. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	MAX	UNIT
Peak-to-peak input voltage for each 30-dB stage	0.01	1	V
Operating free-air temperature, T_A	0	70	°C

electrical characteristics, $V_{CC\pm} = \pm 6$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	MIN	TYP	MAX	UNIT
Differential output offset voltage	1		±40		mV
Quiescent output voltage	2	5.45	5.6	5.85	V
DC scale factor (differential output), each 3-dB stage, – 35 dBV to – 5 dBV	3	6	8	12	mV/dB
AC scale factor (differential output)			8		mV/dB
DC error at – 20 dBV (midpoint of – 35 dBV to – 5 dBV range)	3		1		dB
Input impedance			500		Ω
Output impedance			200		Ω
Rise time, 10% to 90% points, $C_L = 24$ pF	4		20	30	ns
Supply current from V_{CC+}	2	14.5	18.5	23	mA
Supply current from V_{CC-}	2	– 6	– 8.5	– 10.5	mA
Power dissipation	2	123	162	201	mW

PARAMETER MEASUREMENT INFORMATION

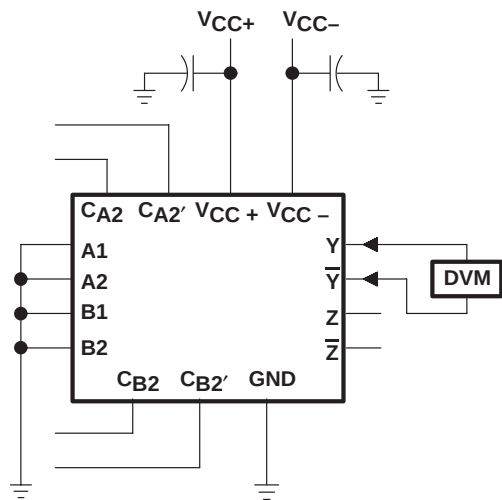


Figure 1

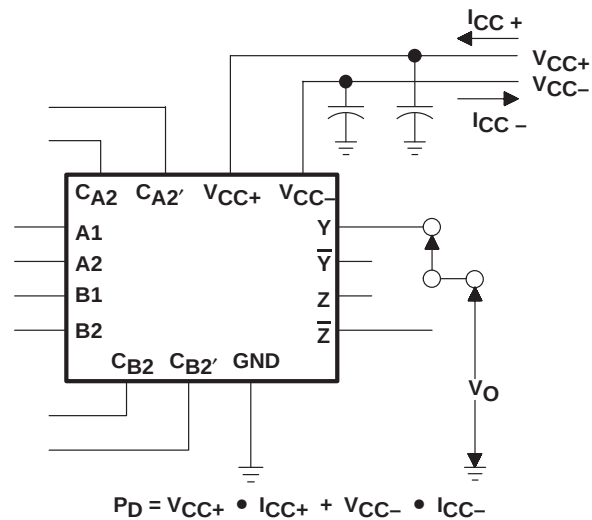


Figure 2

PARAMETER MEASUREMENT INFORMATION

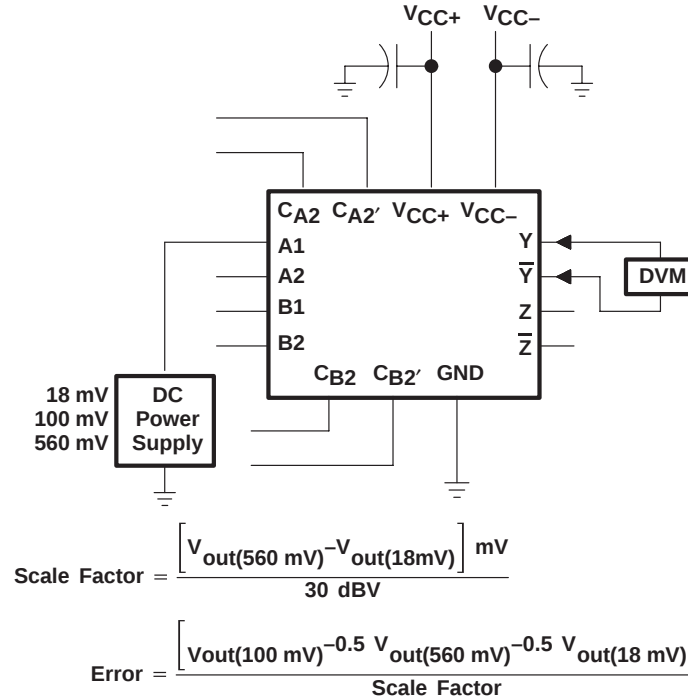
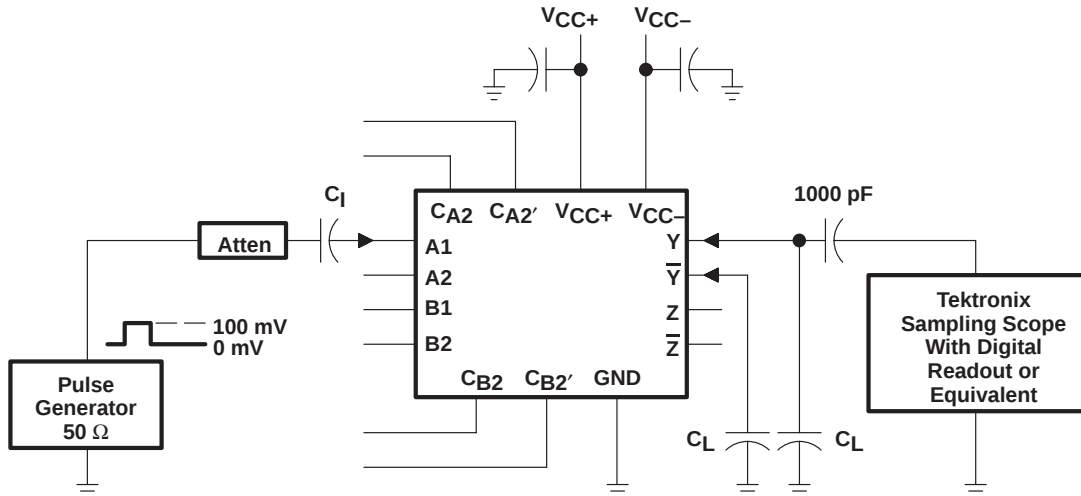


Figure 3



- NOTES:
- A. The input pulse has the following characteristics: $t_W = 200 \text{ ns}$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$, $\text{PRR} \leq 10 \text{ MHz}$.
 - B. Capacitor C_1 consists of three capacitors in parallel: $1 \mu\text{F}$, $0.1 \mu\text{F}$, and $0.01 \mu\text{F}$.
 - C. C_L includes probe and jig capacitance.

Figure 4

TYPICAL CHARACTERISTICS†

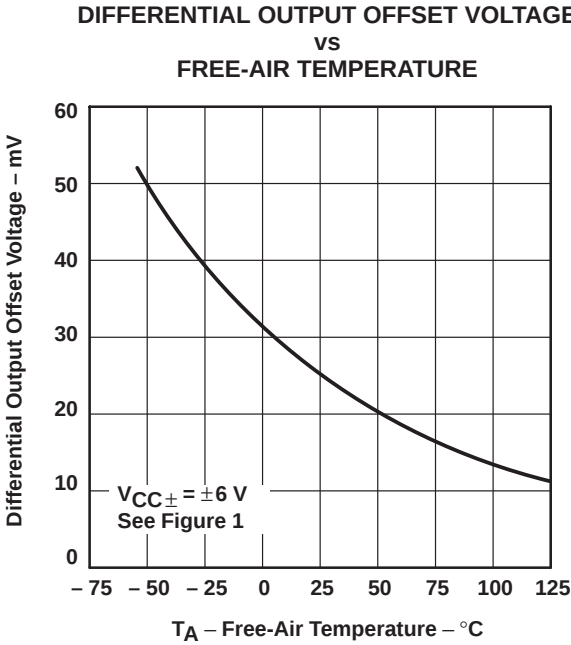


Figure 5

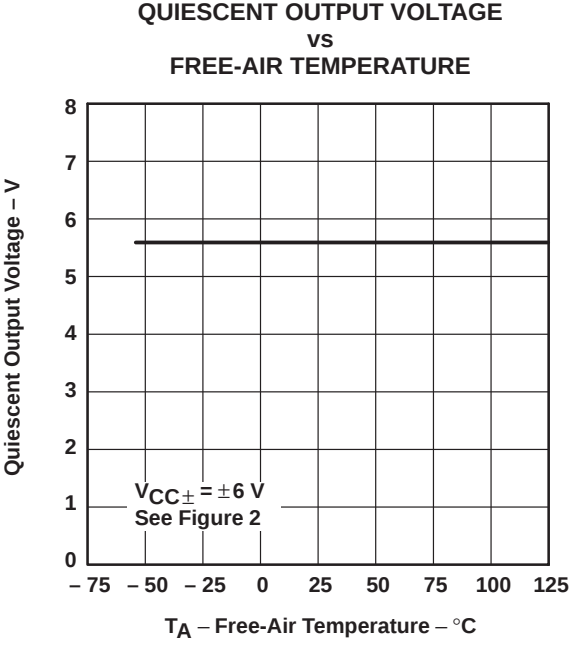


Figure 6

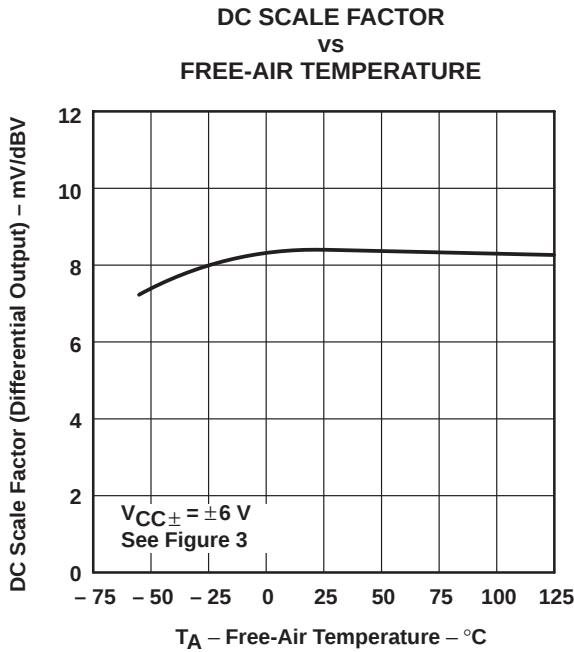


Figure 7

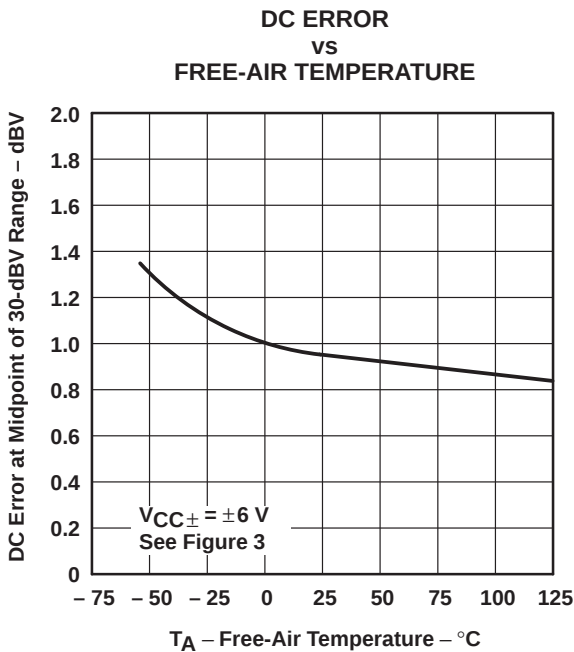


Figure 8

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

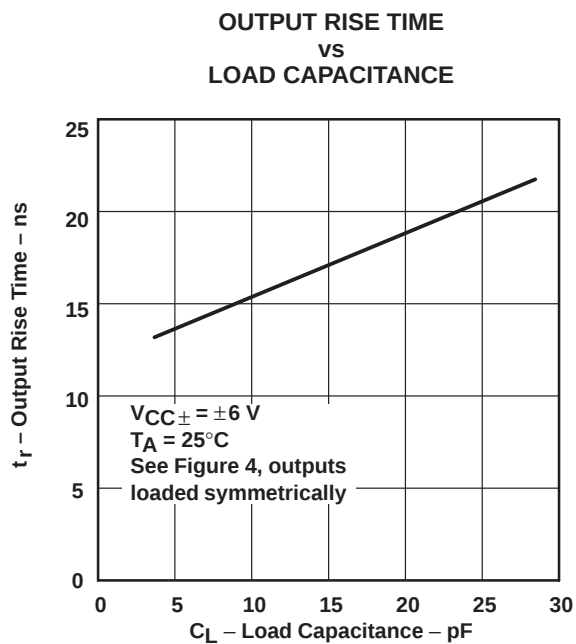


Figure 9

APPLICATION INFORMATION

Although designed for high-performance applications such as infrared detection, this device has a wide range of applications in data compression and analog computation.

basic logarithmic function

The basic logarithmic response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln [(I_C + I_{CES})/I_{CES}]$$

where:

- I_C = collector current
- I_{CES} = collector current at $V_{BE} = 0$
- $m = q/kT$ (in V^{-1})
- V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to common-mode noise.

functional block diagram

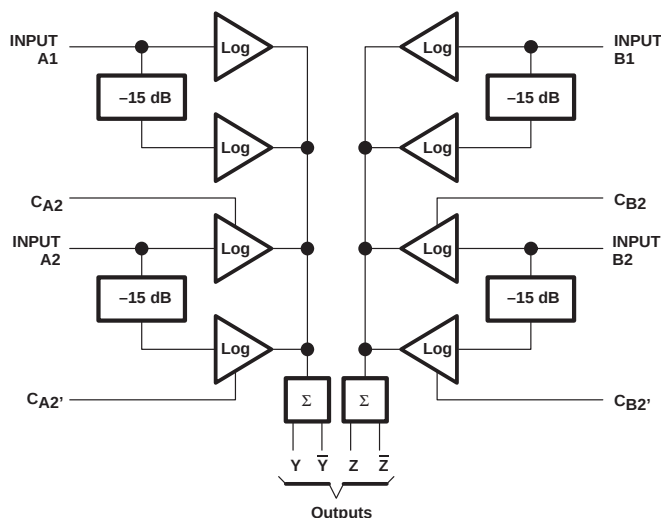


Figure 10

logarithmic sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dB log subsection, and each input feeds two pairs, for a range of 30-dB per stage.

Four compensation points are available to allow slight variations in the gain (slope) of the two individual 15-dB stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from their quiescent values, the gain of that particular 15-dB stage can be adjusted to match the other 15-dB stage in the pair. The compensation pins also can be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\bar{Y}$ (or Z and $\bar{Z}$), which are equal in amplitude, but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, and linear attenuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 V to 1 V. Input levels in excess of 1 V may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that can be applied. As the input drive reaches ± 3.5 V, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ± 3 V to ensure a clean output.

APPLICATION INFORMATION

output levels

Differential-output-voltage levels are low, generally less than 0.6 V. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin also can be adjusted by positioning the offset of the output buffer.

circuits

Figures 12 through 19 show typical circuits using this logarithmic amplifier. Operational amplifiers not otherwise designated are TLC271. For operation at higher frequencies, the TL592 is recommended instead of the TLC271.

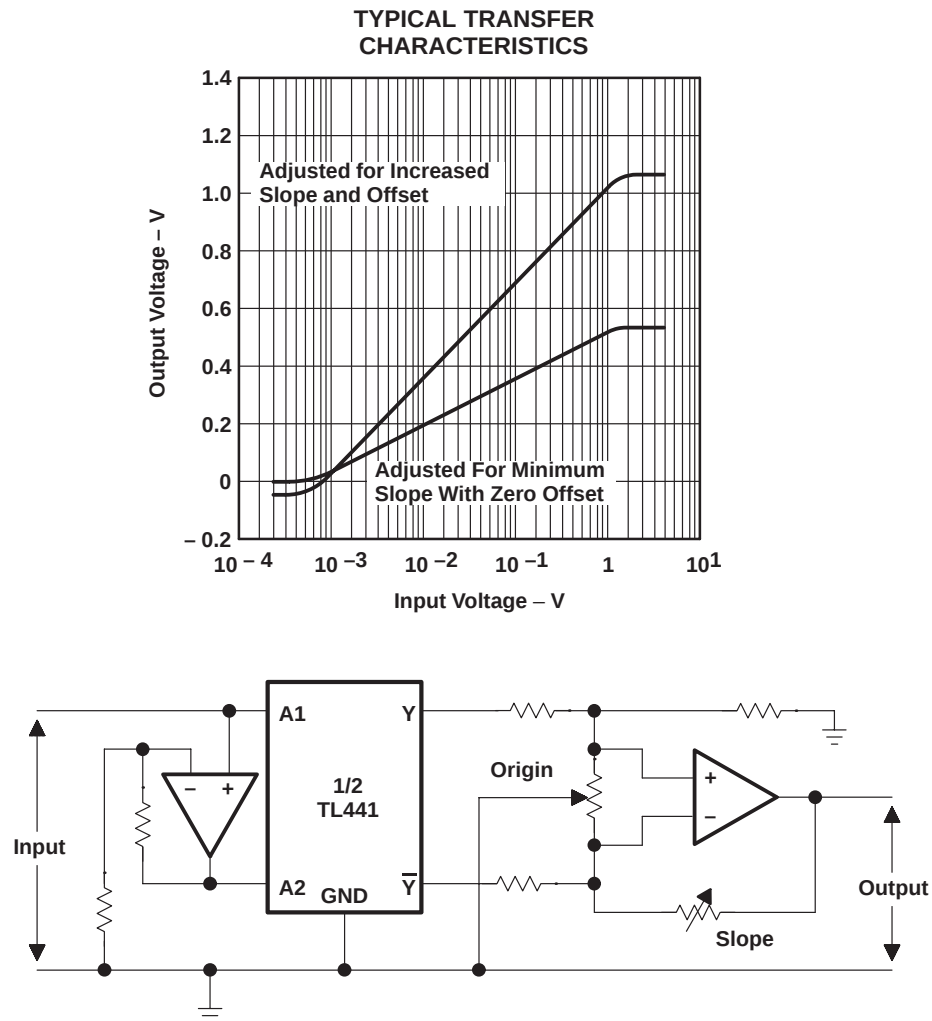


Figure 12. Output Slope and Origin Adjustment

APPLICATION INFORMATION

TRANSFER CHARACTERISTICS OF TWO TYPICAL INPUT STAGES

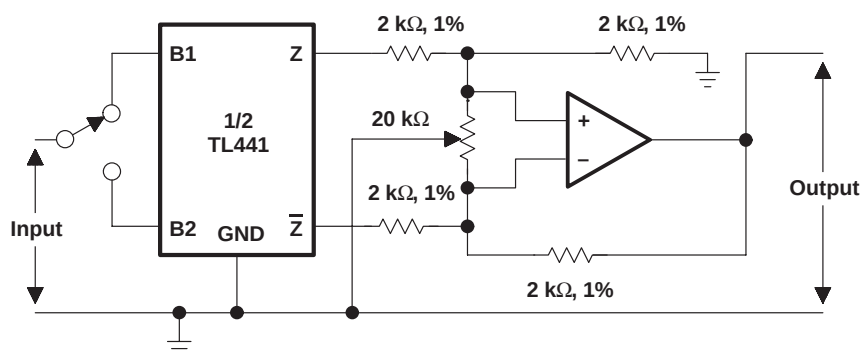
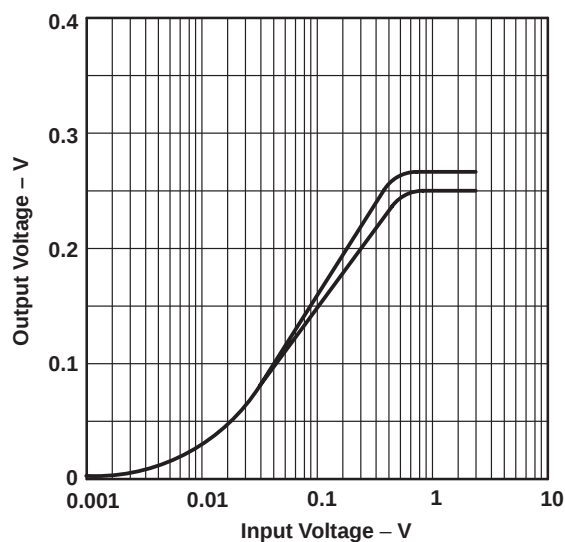


Figure 13. Utilization of Separate Stages

APPLICATION INFORMATION

TRANSFER CHARACTERISTICS WITH BOTH SIDES PARALLELED

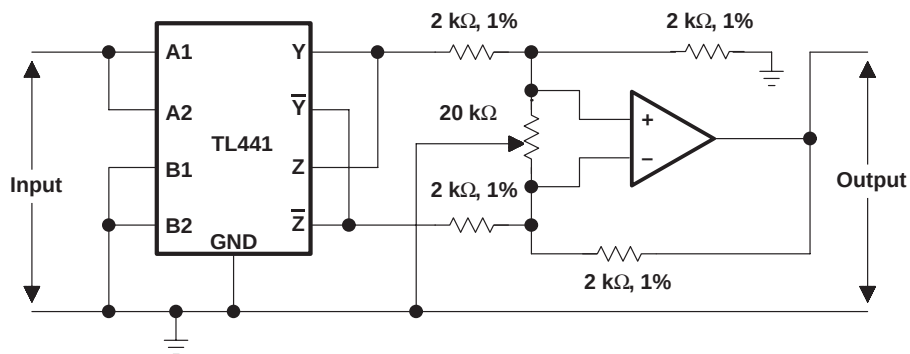
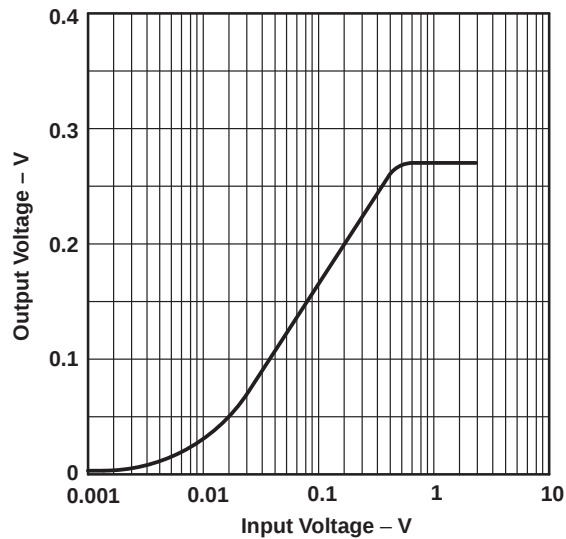
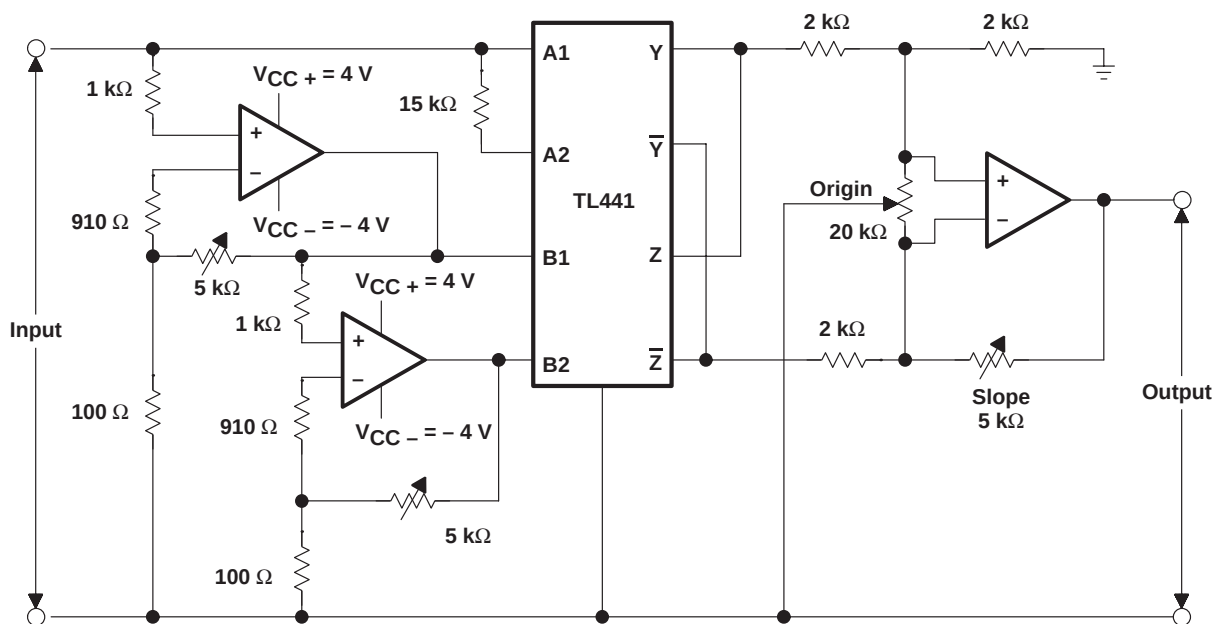
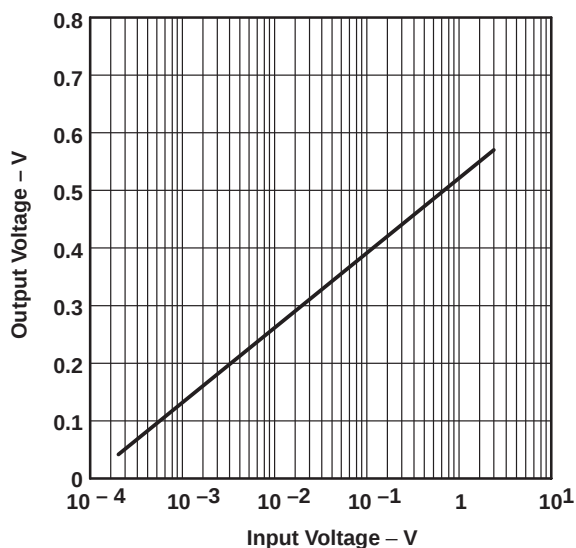


Figure 14. Utilization of Paralleled Inputs

APPLICATION INFORMATION

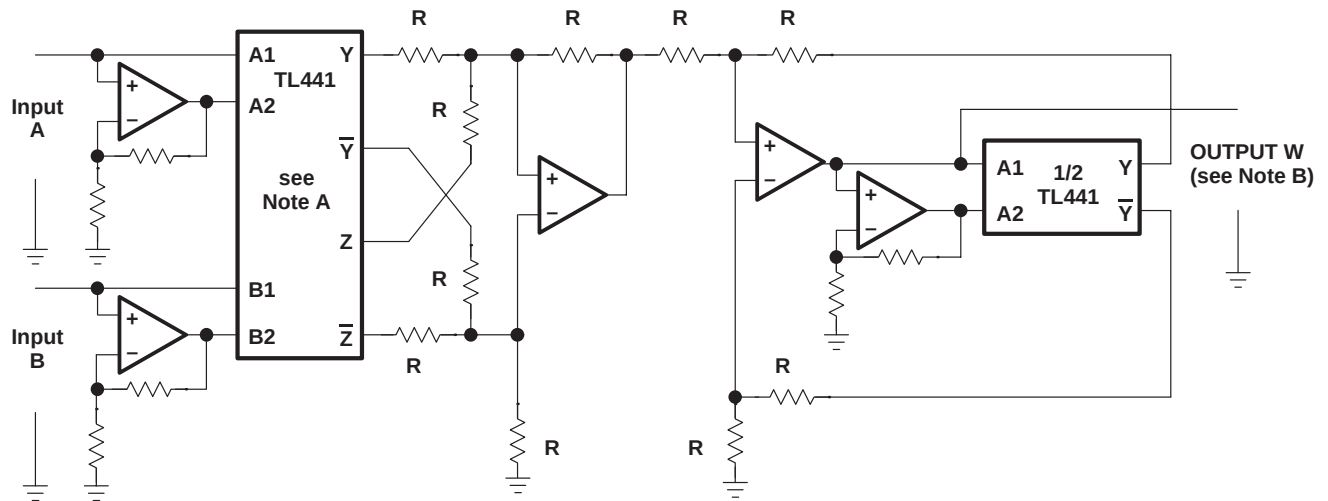
TRANSFER CHARACTERISTICS



- NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ± 4 V.
B. The gains of the input amplifiers are adjusted to achieve smooth transitions.

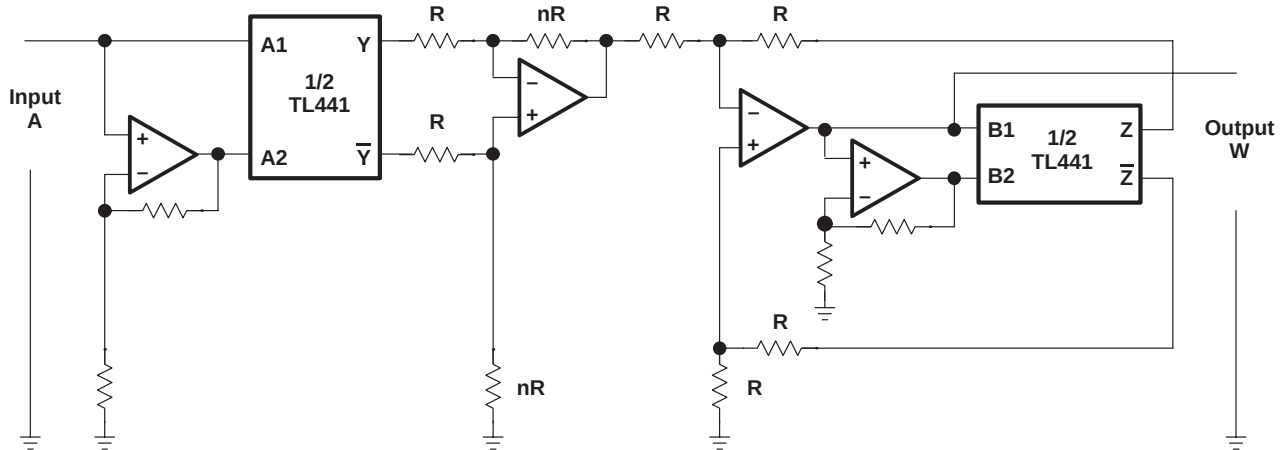
Figure 15. Logarithmic Amplifier With Input Voltage Range Greater Than 80 dB

APPLICATION INFORMATION



- NOTES: A. Connections shown are for multiplication. For division, Z and $\bar{Z}$ connections are reversed.
 B. Output W may need to be amplified to give actual product or quotient of A and B.
 C. R designates resistors of equal value, typically 2 k Ω to 10 k Ω .
- Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$
 Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A - \log_a B)}$

Figure 16. Multiplication or Division

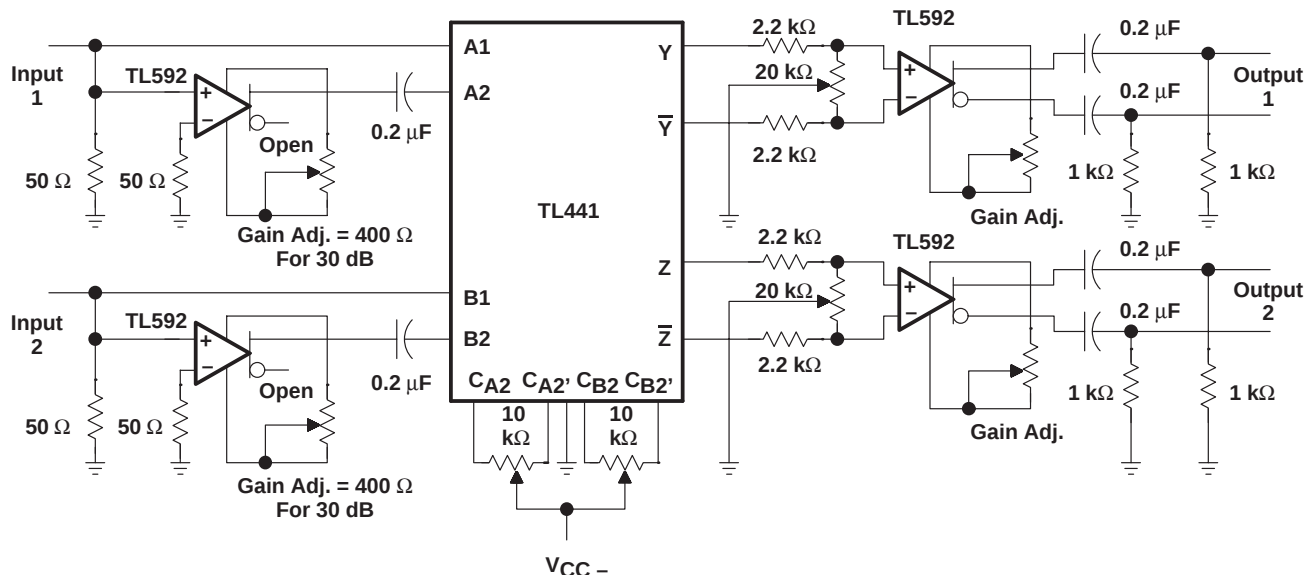


- NOTE: R designates resistors of equal value, typically 2 k Ω to 10 k Ω . The power to which the input variable is raised is fixed by setting nR.
 Output W may need to be amplified to give the correct value.
- Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

Figure 17. Raising a Variable to a Fixed Power

The circuit diagram shows a slope detector. It starts with an 'Input A' which is a ramp signal. This signal is connected to a network of resistors. One path goes through a $2\text{ k}\Omega$ resistor to the non-inverting input (+) of the first comparator. Another path goes through a $2\text{ k}\Omega$ resistor to the inverting input (-) of the first comparator. The inverting input (-) of the first comparator is also connected to a $20\text{ k}\Omega$ resistor that goes to ground. The output of the first comparator is labeled 'Slope'. This 'Slope' signal is connected to the input of a second comparator. The non-inverting input (+) of the second comparator is connected to ground through a resistor. The output of the second comparator is connected to the input of a TL441 monostable multivibrator. The TL441 is configured with its input pins A1 and A2 connected to the comparator output, its output pins Y and $\bar{Y}$ connected to the 'Output W', and its timing network (consisting of a capacitor and a resistor to ground) connected to its internal timing pins. The 'Output W' is a square wave pulse. The circuit is powered by a 20 V supply and ground.

Figure 18. Raising a Fixed Number to a Variable Power



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL441CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL441CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL441CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL441CNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL441CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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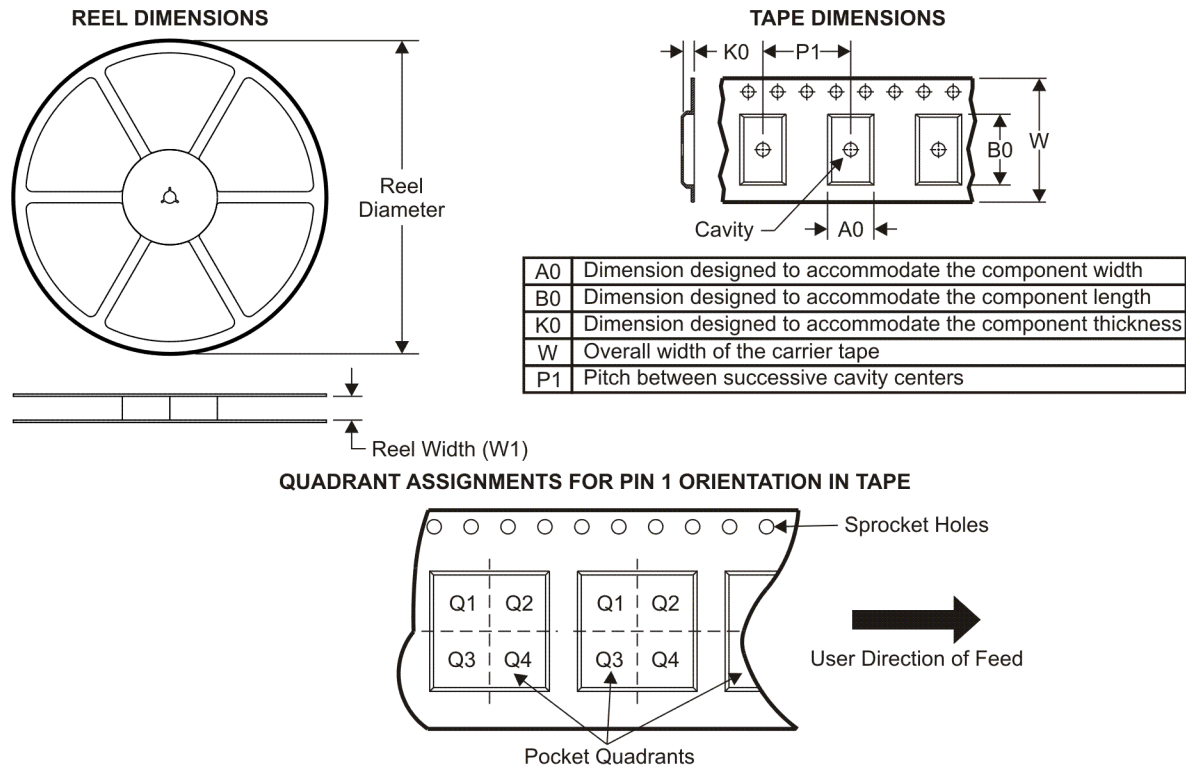
OTHER QUALIFIED VERSIONS OF TL441 :

- Enhanced Product: [TL441-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

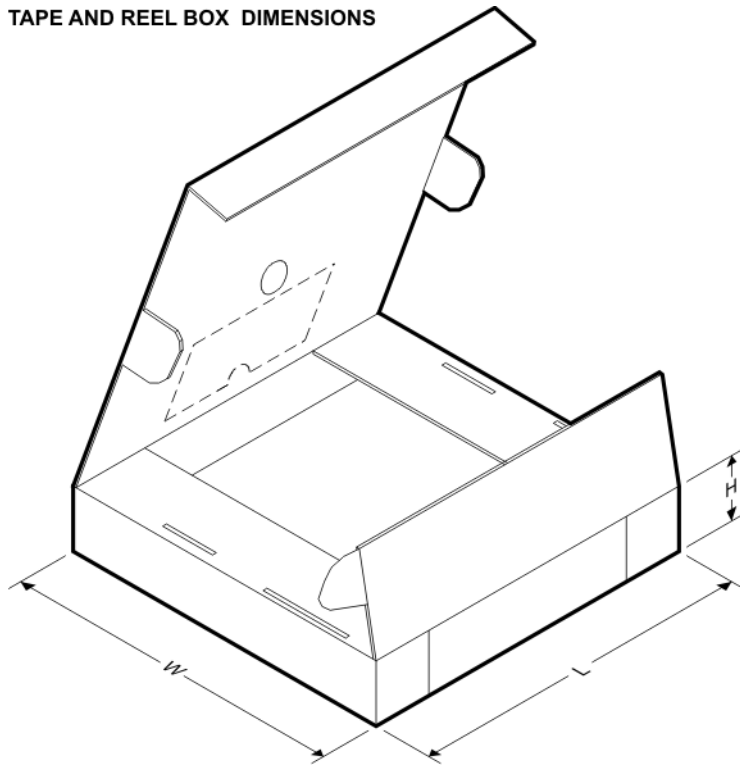
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL441CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

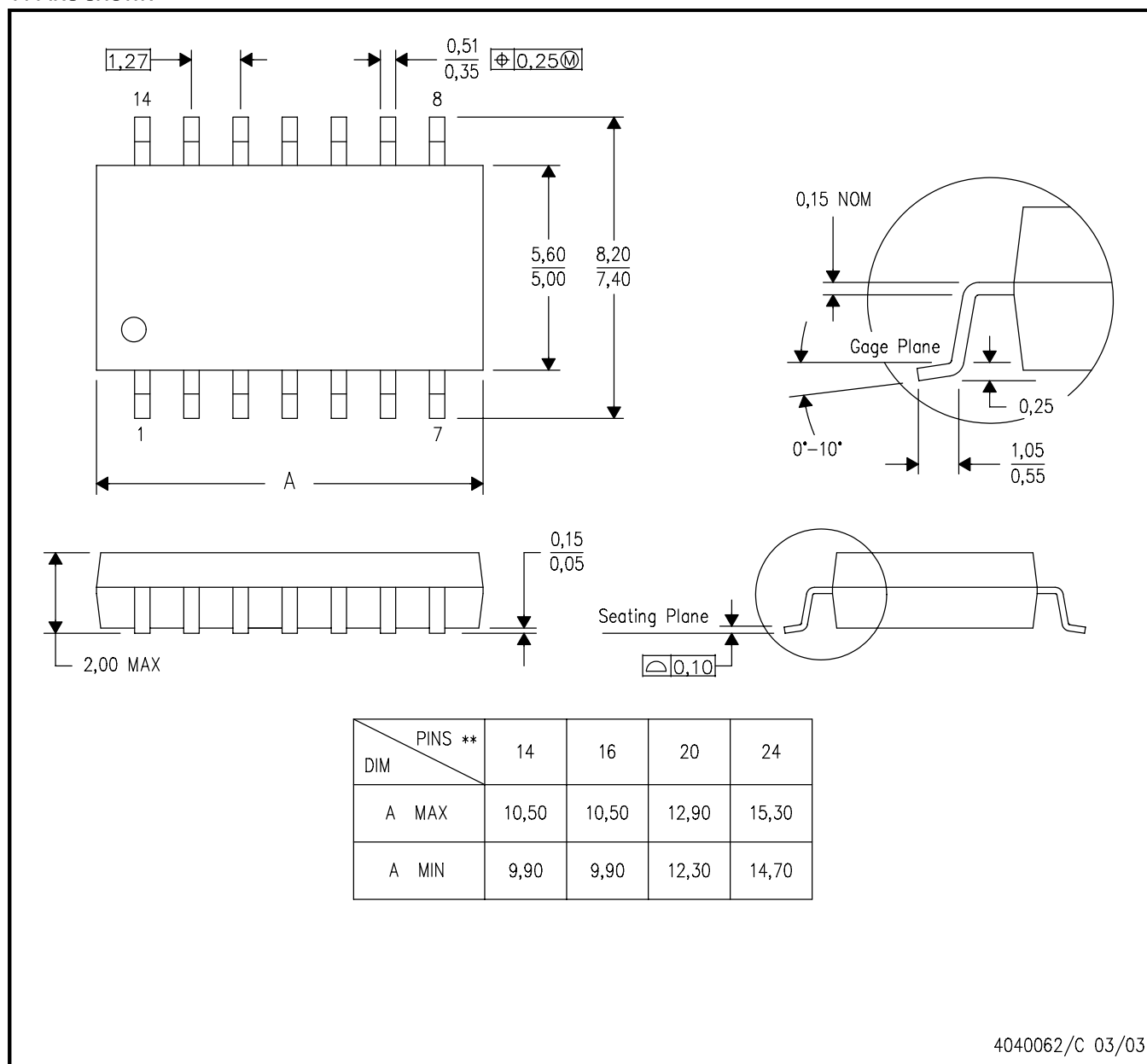
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL441CNSR	SO	NS	16	2000	346.0	346.0	33.0

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

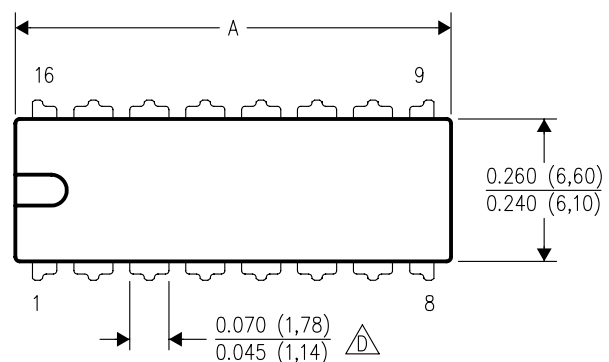


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

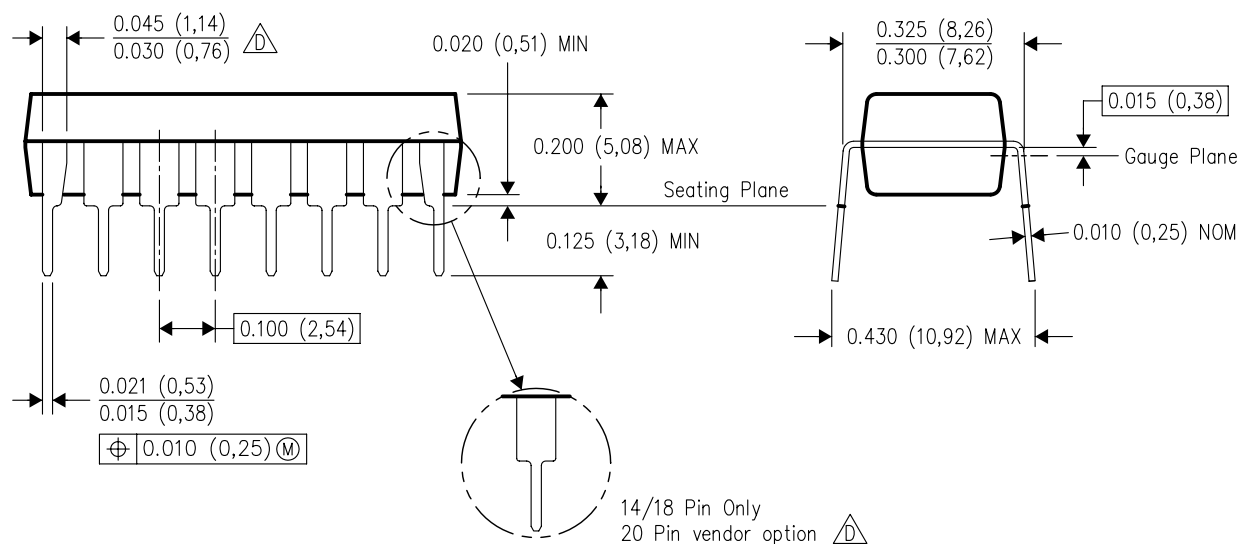
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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