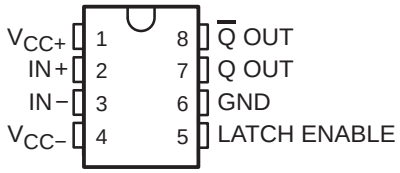
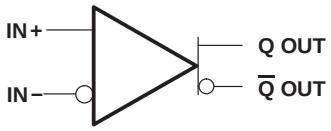
- **Ultra-Fast Operation . . . 10 ns (typ)**
- **Low Positive Supply Current 12.7 mA (Typ)**
- **Operates From a Single 5-V Supply or From a Split ±5-V Supply**
- **Complementary Outputs**
- **Input Common-Mode Voltage Includes Negative Rail**
- **Low Offset Voltage**
- **No Minimum Slew Rate Requirement**
- **Output Latch Capability**
- **Functional Replacement to the LT1116**

D AND PW PACKAGE
(TOP VIEW)



symbol (each comparator)



description

The TL3116 is an ultra-fast comparator designed to interface directly to TTL logic while operating from either a single 5-V power supply or dual ±5-V supplies. The input common-mode voltage extends to the negative rail for ground sensing applications. It features extremely tight offset voltage and high gain for precision applications. It has complementary outputs that can be latched using the LATCH ENABLE terminal. Figure 1 shows the positive supply current of the comparator. The TL3116 only requires 12.7 mA (typical) to achieve a propagation delay of 10 ns.

The TL3116 is a pin-for-pin functional replacement for the LT1116 comparator, offering high-speed operation but consuming much less power.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM‡ (Y)
	SMALL OUTLINE† (D)	TSSOP (PW)	
0°C to 70°C	TL3116CD	TL3116CPWLE	TL3116Y
−40°C to 85°C	TL3116ID	TL3116IPWLE	—

† The PW packages are available left-ended taped and reeled only.
‡ Chip forms are tested at T_A = 25°C only.

POSITIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

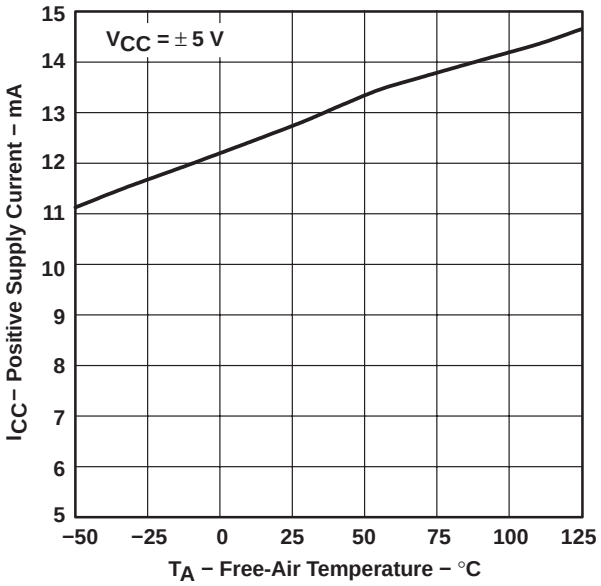


Figure 1

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

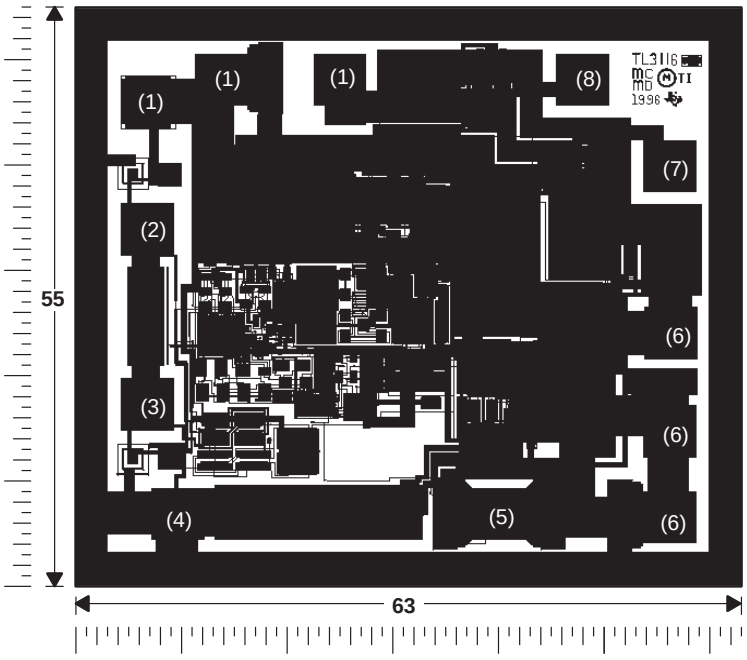
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

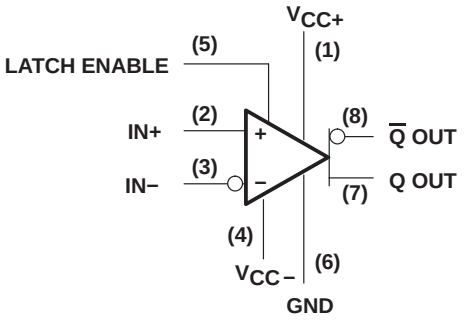
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TL3116Y chip information

This chip, when properly assembled, displays characteristics similar to the TL3116C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 1 AND 6 CAN BE CONNECTED TO MULTIPLE PADS.

COMPONENT COUNT	
Bipolars	53
MOSFETs	49
Resistors	46
Capacitors	14

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . − 7 V to 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . 7 V
Input voltage range, V_I . . . . . 7 V
Input voltage, V_I (LATCH ENABLE) . . . . . 7 V
Output current, I_O . . . . . ± 20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
PW	525 mW	4.2 mW/°C	336 mW

electrical characteristics at specified operating free-air temperature, V_{DD} = ±5 V, V_{LE} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL3116C			TL3116I			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	T_A = 25°C		0.5	3		0.5	3	mV
		T_A = full range			3.5			3.5	
α_{VIO}	Temperature coefficient of input offset voltage			−2.5			−2.8		µV/°C
I_{IO}	Input offset current	T_A = 25°C		0.1	0.2		0.1	0.2	µA
		T_A = full range			0.3			0.35	
I_{IB}	Input bias current	T_A = 25°C		0.7	1.1		0.7	1.1	µA
		T_A = full range			1.2			1.5	
V_{ICR}	Common-mode input voltage range	V_{DD} = ±5 V	−5		2.5	−5		2.5	V
		V_{DD} = 5 V	0		2.5	0		2.5	
CMRR	Common-mode rejection ratio	− 5 ≤ V_{IC} ≤ 2.5 V	75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio	Positive supply: 4.6 V ≤ +V_{DD} ≤ 5.4 V, T_A = 25°C	60	80		60	80		dB
		Negative supply: − 7 V ≤ −V_{DD} ≤ − 2 V, T_A = 25°C	80	100		80	100		
V_{OL}	Low-level output voltage	$I_{(sink)}$ = 4 mA, V+ ≤ 4.6 V, T_A = 25°C		400	600		400	600	mV
		$I_{(sink)}$ = 10 mA, V+ ≤ 4.6 V, T_A = 25°C		750			750		
V_{OH}	High-level output voltage	V+ ≤ 4.6 V, I_O = 1 mA, T_A = 25°C	3.6	3.9		3.6	3.9		V
		V+ ≤ 4.6 V, I_O = 10 mA, T_A = 25°C	3.4	3.8		3.4	3.8		
I_{CC}	Positive supply current	T_A = full range		12.7	14.7		12.7	15	mA
	Negative supply current		−2.6			−3			
V_{IL}	Low-level input voltage (LATCH ENABLE)				0.8			0.8	V
V_{IH}	High-level input voltage (LATCH ENABLE)		2			2			V
I_{IL}	Low-level input current (LATCH ENABLE)	V_{LE} = 0		0	1		0	1	µA
		V_{LE} = 2 V		24	39		24	45	µA

† Full range for the TL3116C is T_A = 0°C to 70°C. Full range for the TL3116I is T_A = −40°C to 85°C.
‡ All typical values are measures with T_A = 25°C.

switching characteristics, $V_{DD} = \pm 5$ V, $V_{LE} = 0$

PARAMETER		TEST CONDITIONS†		TL3116C			TL3116I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd1}	Propagation delay time‡	ΔV_I = 100 mV, V_{OD} = 5 mV	T_A = 25°C		9.9	12		9.9	12	ns
			T_A = full range		9.9	14		9.9	15	
		ΔV_I = 100 mV, V_{OD} = 20 mV	T_A = 25°C		8.2	10.3		8.2	10.3	
			T_A = full range		8.2	12.7		8.2	13.7	
$t_{sk(p)}$	Pulse skew ($\lvert t_{pd+} - t_{pd-} \rvert$)	ΔV_I = 100 mV, T_A = 25°C	V_{OD} = 5 mV,		0.5			0.5		ns
t_{su}	Setup time, LATCH ENABLE				3.4			3.4		ns

† Full range for the TL3116C is 0°C to 70°C. Full range for the TL3116I is −40°C to 85°C.

‡ t_{pd1} cannot be measured in automatic handling equipment with low values of overdrive. The TL3116 is 100% tested with a 1-V step and 500-mV overdrive at T_A = 25°C only. Correlation tests have shown that t_{pd1} limits given can be ensured with this test, if additional dc tests are performed to ensure that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{CC}	Positive supply current	vs Input voltage	2
		vs Frequency	3
		vs Free-air temperature	4
I_{CC}	Negative supply current	vs Free-air temperature	5
t_{pd}	Propagation delay time	vs Overdrive voltage	6
		vs Supply voltage	7
		vs Input impedance	8
		vs Load capacitance	9
		vs Free-air temperature	10
V_{IC}	Common-mode input voltage	vs Free-air temperature	11
V_{IT}	Input threshold voltage (LATCH ENABLE)	vs Free-air temperature	12
V_O	Output voltage	vs Output source current	13
		vs Output sink current	14
I_I	Input current (LATCH ENABLE)	vs Input voltage	15

TYPICAL CHARACTERISTICS

POSITIVE SUPPLY CURRENT vs INPUT VOLTAGE

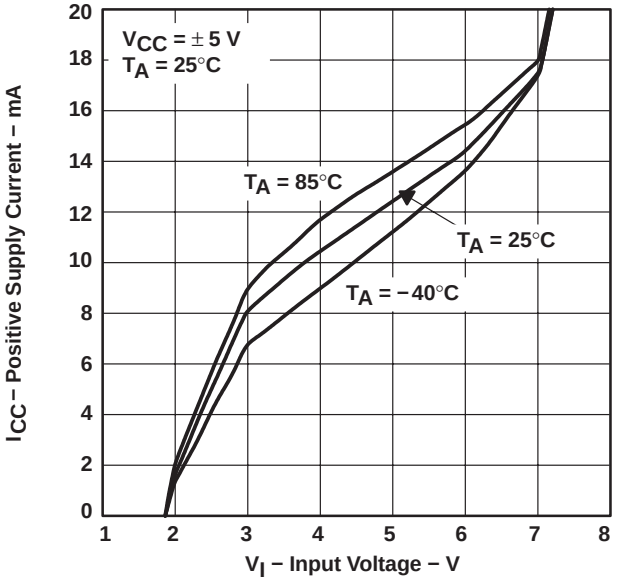


Figure 2

POSITIVE SUPPLY CURRENT vs FREQUENCY

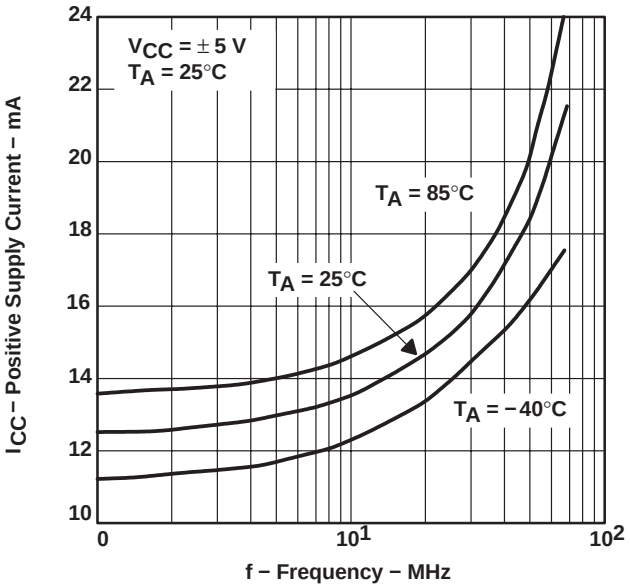


Figure 3

POSITIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

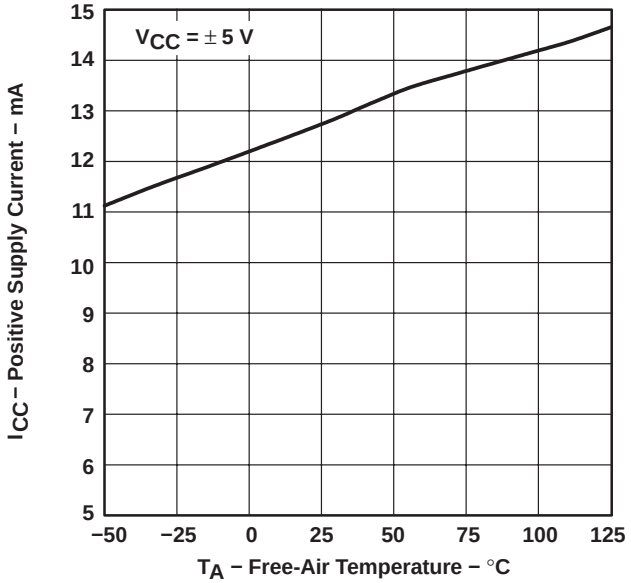


Figure 4

NEGATIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

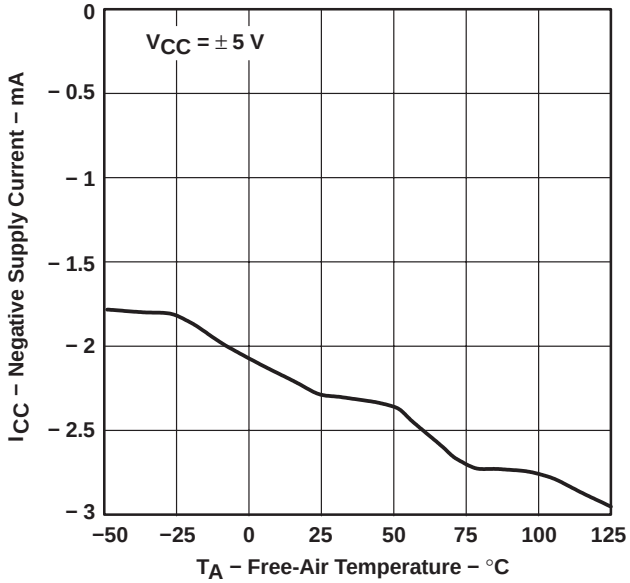


Figure 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs OVERDRIVE VOLTAGE

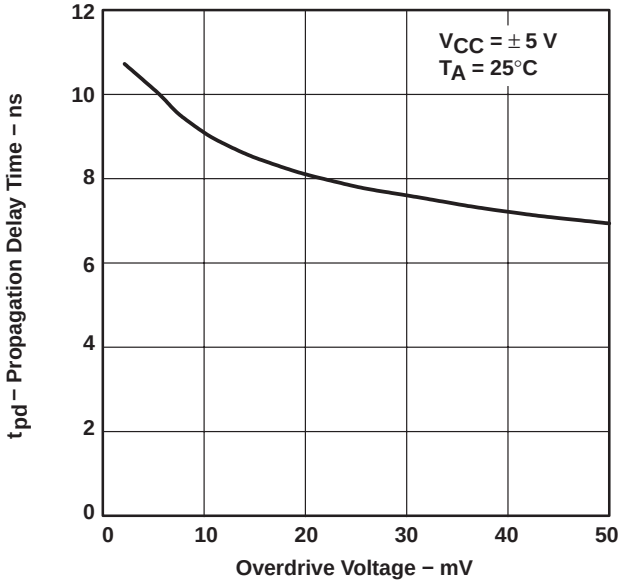


Figure 6

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

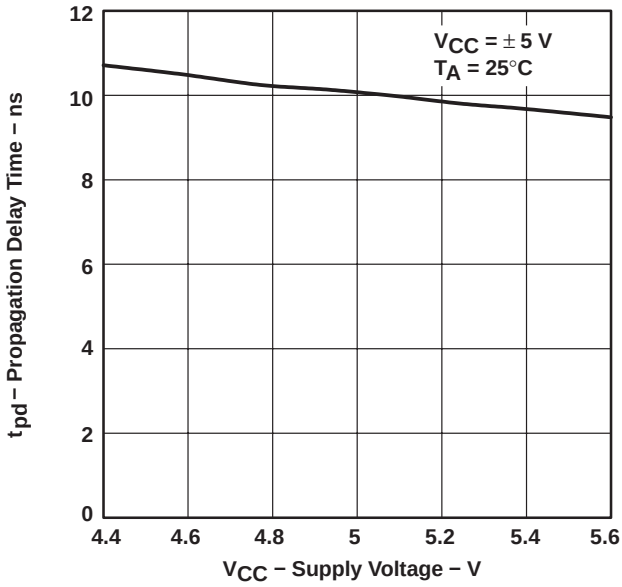


Figure 7

PROPAGATION DELAY TIME vs INPUT IMPEDANCE

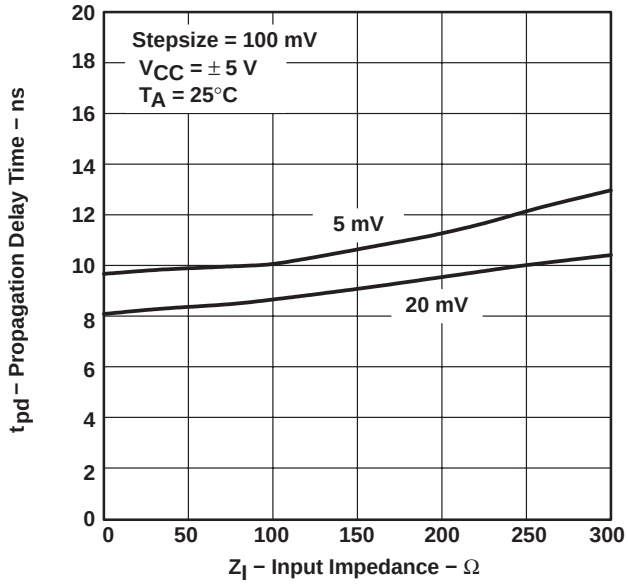


Figure 8

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

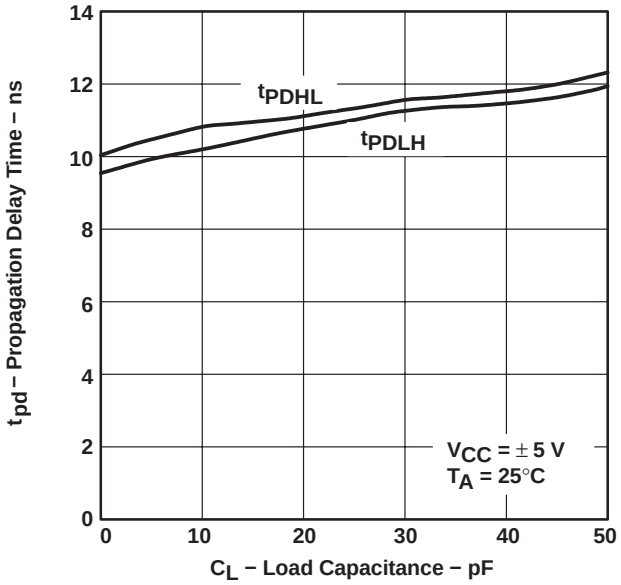


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

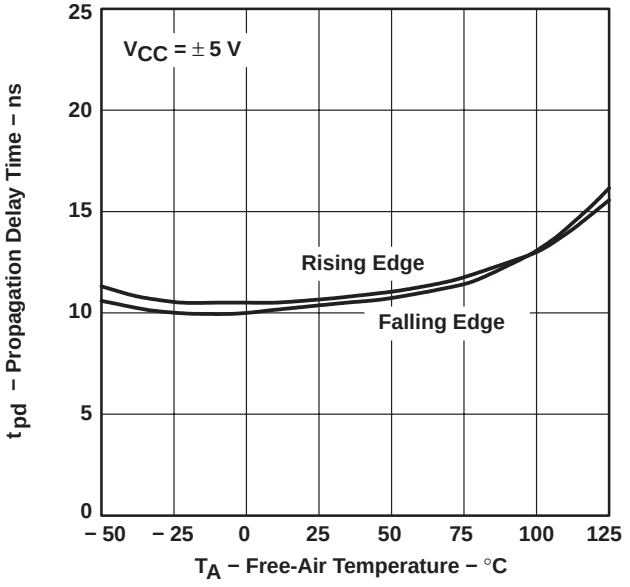


Figure 10

COMMON-MODE INPUT VOLTAGE vs FREE-AIR TEMPERATURE

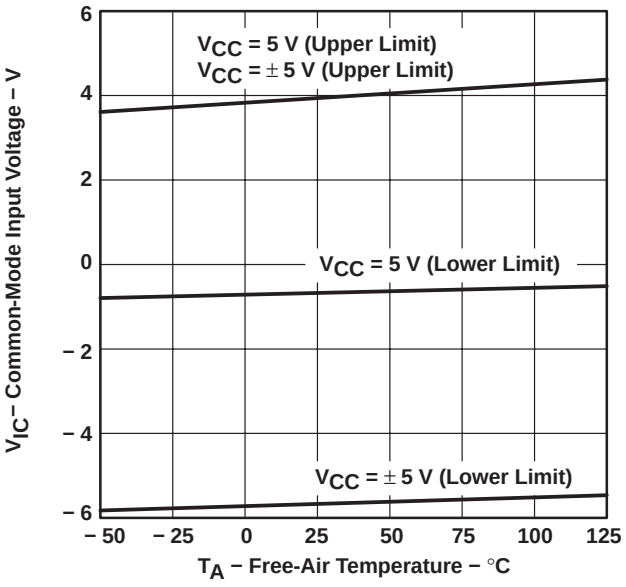


Figure 11

INPUT THRESHOLD VOLTAGE (LATCH ENABLE) vs FREE-AIR TEMPERATURE

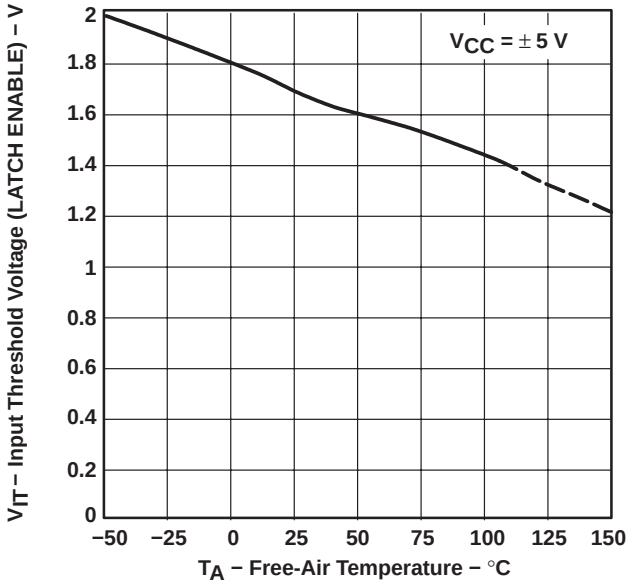


Figure 12

OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

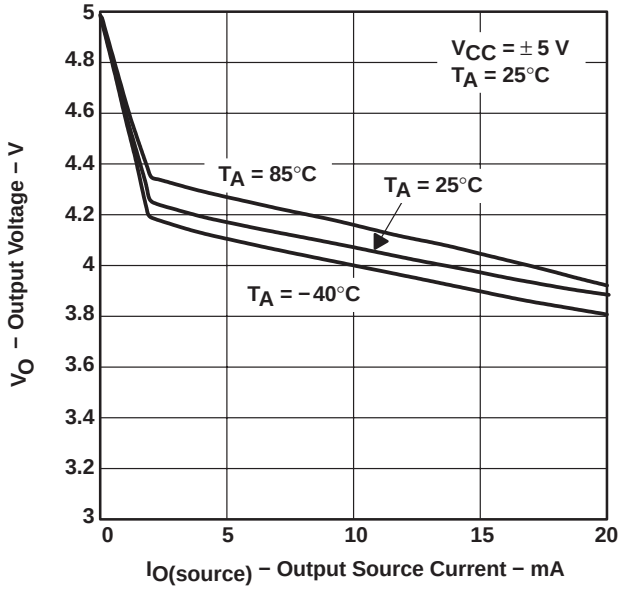


Figure 13

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

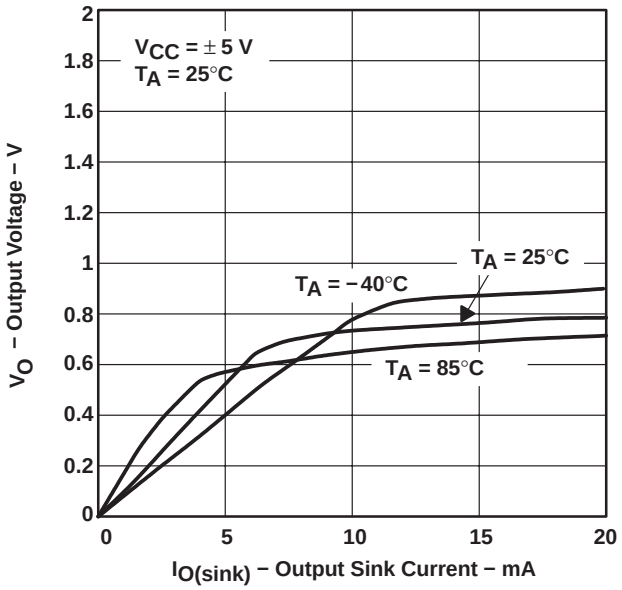


Figure 14

INPUT CURRENT (LATCH ENABLE) vs INPUT VOLTAGE

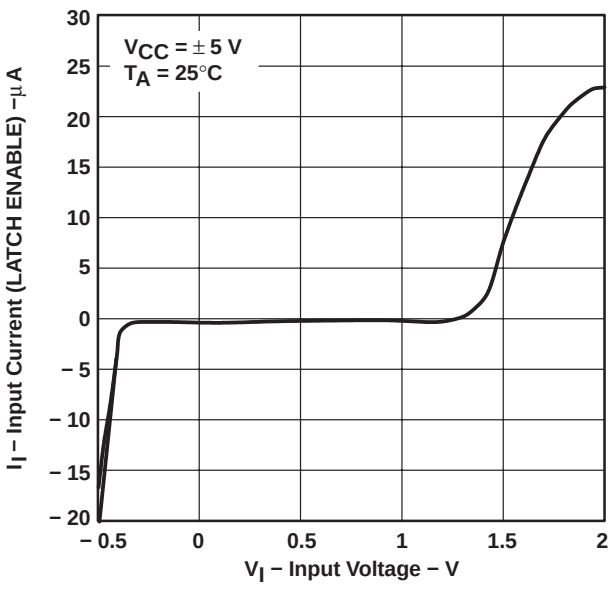
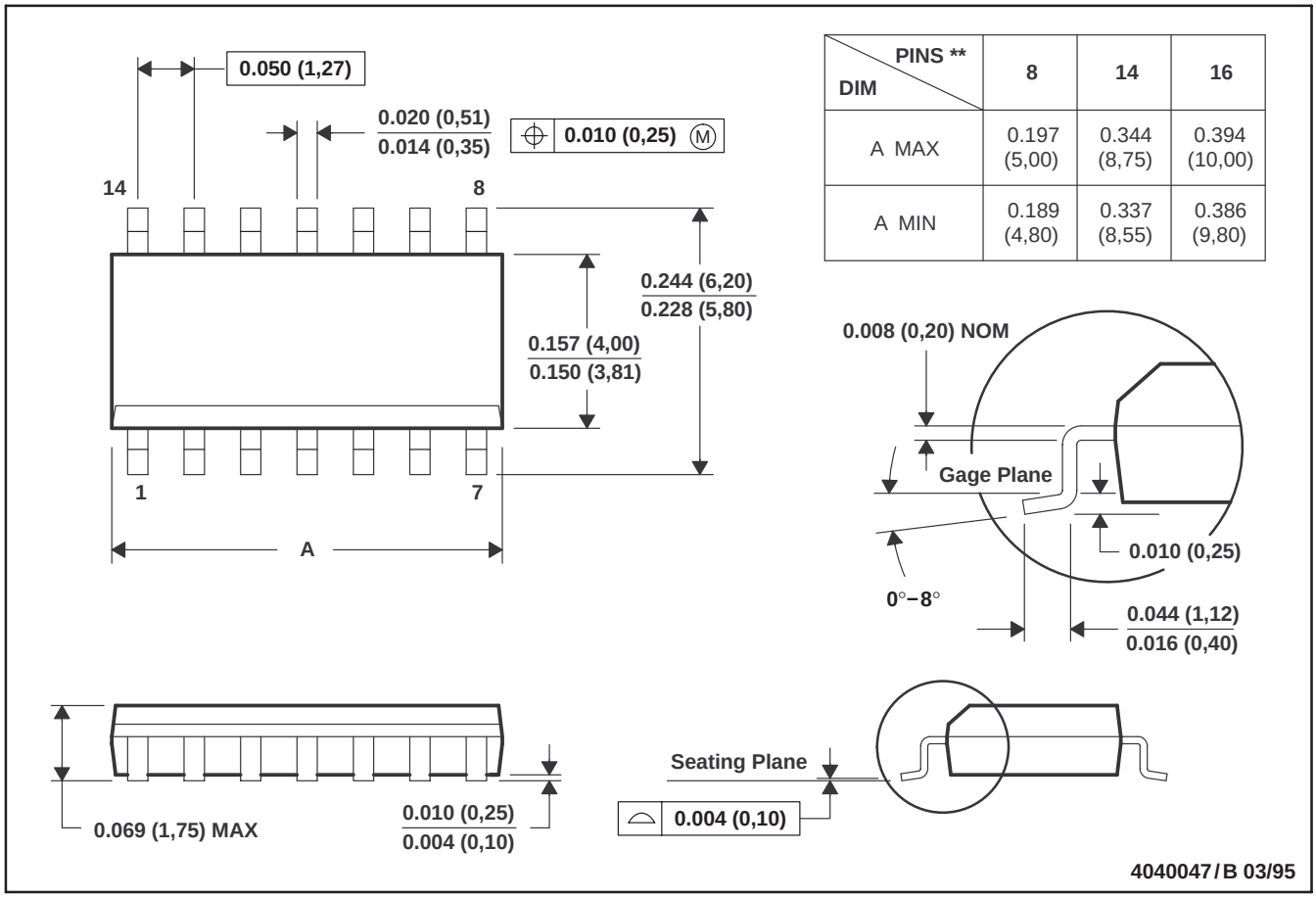


Figure 15

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



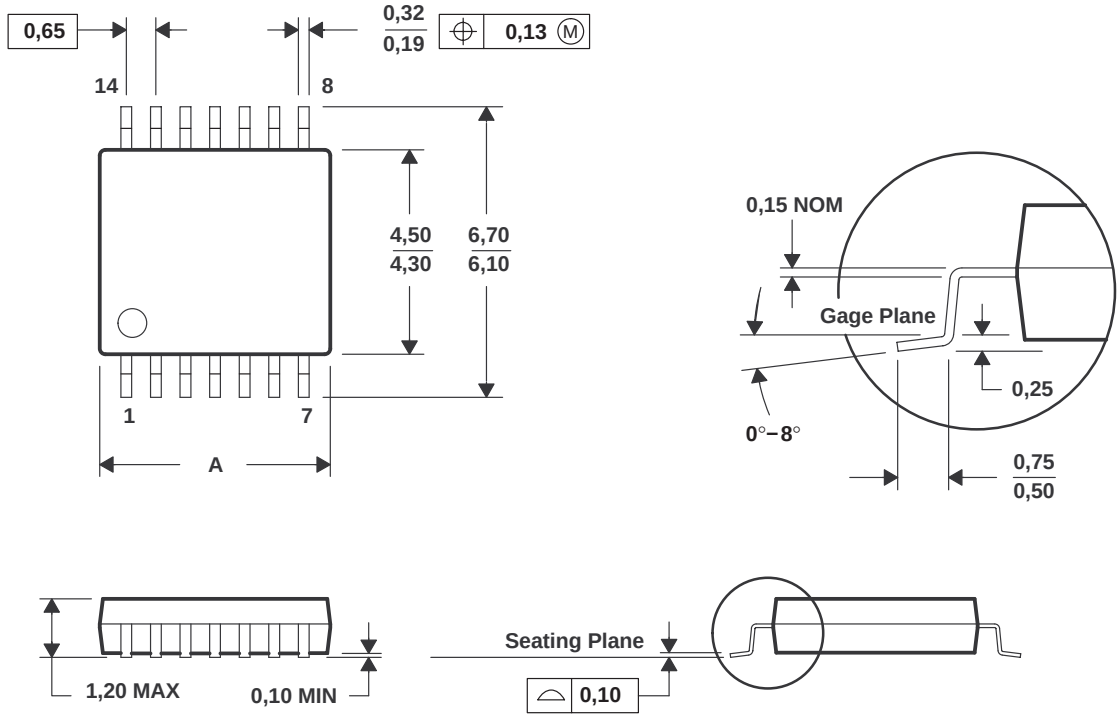
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL3116CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TL3116CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TL3116CPW	ACTIVE	TSSOP	PW	8	150	None	CU NIPDAU	Level-1-220C-UNLIM
TL3116CPWLE	OBSOLETE	TSSOP	PW	8		None	Call TI	Call TI
TL3116CPWR	ACTIVE	TSSOP	PW	8	2000	None	CU NIPDAU	Level-1-220C-UNLIM
TL3116ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TL3116IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TL3116IPW	ACTIVE	TSSOP	PW	8	150	None	CU NIPDAU	Level-1-220C-UNLIM
TL3116IPWLE	OBSOLETE	TSSOP	PW	8		None	Call TI	Call TI
TL3116IPWR	ACTIVE	TSSOP	PW	8	2000	None	CU NIPDAU	Level-1-220C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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