

TISP61089D, TISP61089SD, TISP61089AD, TISP61089ASD, TISP61089P, TISP61089AP

DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

TISP61089 Gated Protector Series

Overvoltage Protection for Negative Rail SLICs

Dual Voltage-Tracking Protectors
- **'61089 for Battery Voltages to ..... -75 V**
- **'61089A for Battery Voltages to ..... -100 V**
- **Low Gate Triggering Current ..... < 5 mA**
- **High Holding Current ..... > 150 mA**

Rated for GR-1089-CORE and K.44 Impulses

Impulse Wave Shape		I_{PPSM}
Voltage	Current	A
2/10	2/10	120
10/700	5/310	40
10/1000	10/1000	30

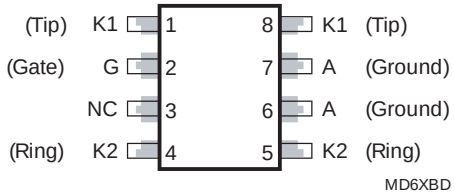
2/10 Overshoot Voltage Specified

Element	I_{PP} = 100 A, 2/10 V
Diode	8
SCR	12

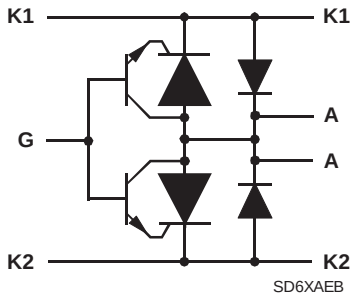
Package Options
- **Surface Mount 8-pin Small-Outline**
  - **Line Feed-Thru Connection (D)**
  - **Shunt Version Connection (SD)**
- **Through-Hole 8-pin DIP (P)**

..... UL Recognized Components

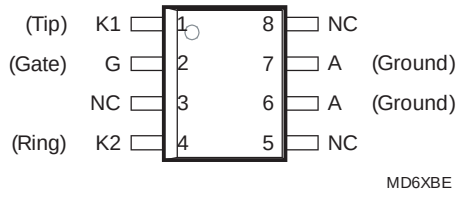
D Package, P Package Top Views and Device Symbol for Feed-Thru Pin-Out



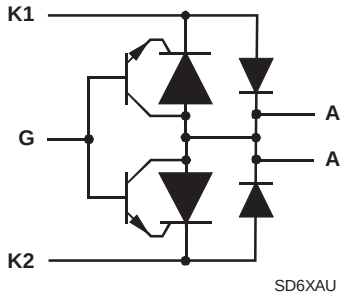
NC - No internal connection
Terminal typical application names shown in parenthesis



D Package Top View and Device Symbol for Shunt (SD) Pin-Out



NC - No internal connection
Terminal typical application names shown in parenthesis



How To Order

Device	Package	Carrier	Order as
TISP61089	D (Small-Outline)	R†	TISP61089DR
		Tube	TISP61089D
TISP61089S	D (Small-Outline)	R†	TISP61089SDR
		Tube	TISP61089SD
TISP61089	P (8-pin DIP)	Tube	TISP61089P
† Carrier R is Embossed Tape Reeled			

Device	Package	Carrier	Order as
TISP61089A	D (Small-Outline)	R†	TISP61089ADR
		Tube	TISP61089AD
TISP61089AS	D (Small-Outline)	R†	TISP61089ASDR
		Tube	TISP61089ASD
TISP61089A	P (8-pin DIP)	Tube	TISP61089AP
† Carrier R is Embossed Tape Reeled			

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Description

These ‘61089 parts are all dual forward-conducting buffered p-gate thyristor (SCR) overvoltage protectors. They are designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The ‘61089 limits voltages that exceed the SLIC supply rail voltage. The ‘61089 parameters are specified to allow equipment compliance with Telcordia (formally Bellcore) GR-1089-CORE and ITU-T recommendations K.20, K.21 and K.45.

The SLIC line driver section is typically powered from 0 V (ground) and a negative (battery) voltage. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. The protection voltage will then track the negative supply voltage and the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector SCR will switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of ‘61089 SCR avoids d.c. latchup.

The ‘61089 is intended to be used with a series resistance of at least 25 Ω and a suitable overcurrent function for Telcordia compliance. Power fault conditions require a series overcurrent element which either interrupts or reduces the circuit current before the ‘61089 current rating is exceeded. For equipment compliant to ITU-T recommendations K.20 or K.21 or K.45 only, the series resistor value is set by the coordination requirements. For coordination with a 400 V limit GDT, a minimum series resistor value of 10 Ω is recommended.

The ‘61089 buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction. The regular pin-out for surface mount and through-hole packages is a feed through configuration. Connection to the SLIC is made via the ‘61089, Ring through pins 4 - 5 and Tip through pins 1 - 8. A non-feed-through surface mount (D) package is available. This shunt (SD) version pin-out does not make duplicate connections to pin 5 and pin 8 which increases package creepage distance from ground of the other connections from about 0.7 mm to over 3 mm. High voltage ringing SLICs, with battery voltages below -100 V and down to -155 V, can be protected by the TISP61089B device. Details of this device are in the TISP61089B data sheet.

Absolute Maximum Ratings, -40 °C ≤ T_J ≤ 85 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, V_{GK} = 0	61089	V_{DRM}	-100	V
	‘61089A		-120	
Repetitive peak gate-cathode voltage, V_{KA} = 0	61089	V_{GKRM}	-85	V
	‘61089A		-120	
Non-repetitive peak on-state pulse current (see Notes 1 and 2)		I_{PPSM}		A
10/1000 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)			30	
5/320 µs (ITU-T K.20, K.21& K.45, K.44 open-circuit voltage wave shape 10/700 µs)			40	
1.2/50 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)			100	
2/10 µs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)			120	
Non-repetitive peak on-state current, V_{GG} = -75 V, 50 Hz to 60 Hz (see Notes 1 and 2)		I_{TSM}		A
0.1 s			11	
1 s			4.8	
5 s			2.7	
300 s			0.95	
900 s			0.93	
Non-repetitive peak gate current, 1/2 µs pulse, cathodes commoned (see Notes 1 and 2)		I_{GSM}	+40	A
Operating free-air temperature range		T_A	-40 to +85	°C
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-40 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions. Gate voltage ranges are -20 V to -75 V for the ‘61089 and -20 V to -100 V for the ‘61089A.

2. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above 85 °C, derate linearly to zero at 150 °C lead temperature.

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Recommended Operating Conditions

Component		Min	Typ	Max	Unit
C_G	Gate decoupling capacitor	100	220		nF
R_S	Series resistor for GR-1089-CORE first-level surge survival	25			Ω
	Series resistor for GR-1089-CORE first-level and second-level surge survival	40			Ω
	Series resistor for GR-1089-CORE intra-building port surge survival	8			Ω
	Series resistor for K.20, K.21 and K.45 coordination with a 400 V primary protector	10			Ω

Electrical Characteristics, T_J = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
$V_{(BO)}$	Breakover voltage	2/10 μs, I_{PP} = -56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			-57		V
		2/10 μs, I_{PP} = -100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			-60		
		1.2/50 μs, I_{PP} = -53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			-60		
		1.2/50 μs, I_{PP} = -96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			-64		
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	2/10 μs, I_{PP} = -56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			9		V
		2/10 μs, I_{PP} = -100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			12		
		1.2/50 μs, I_{PP} = -53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			12		
		1.2/50 μs, I_{PP} = -96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			16		
V_F	Forward voltage	I_F = 5 A, t_W = 200 μs				3	V
V_{FRM}	Peak forward recovery voltage	2/10 μs, I_{PP} = 56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			6		V
		2/10 μs, I_{PP} = 100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			8		
		1.2/50 μs, I_{PP} = 53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			8		
		1.2/50 μs, I_{PP} = 96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			12		
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -48 V		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GK} = V_{GKRM}$, V_{KA} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
I_{GT}	Gate trigger current	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -48 V				5	mA
V_{GT}	Gate-cathode trigger voltage	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -48 V				2.5	V
Q_{GS}	Gate switching charge	1.2/50 μs, I_{PP} = -53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			0.1		μC
C_{KA}	Cathode-anode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 3)	V_D = -3 V			100	pF
			V_D = -48 V			50	pF

NOTES: 3. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

Parameter		Test Conditions		Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	T_A = 25 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, P_{TOT} = 1.7 W	D Package			120	°C/W
			P package			100	

Parameter Measurement Information

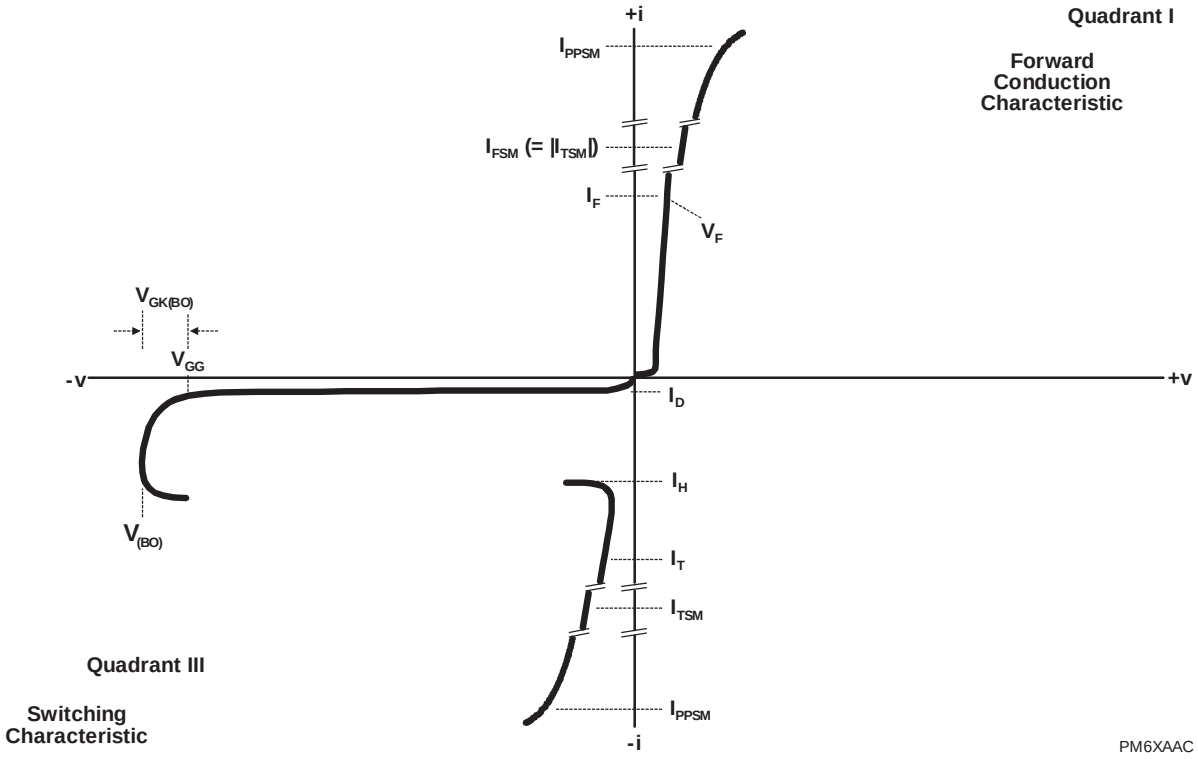


Figure 1. Voltage-Current Characteristic
Unless Otherwise Noted, All Voltages are Referenced to the Anode

Thermal Information

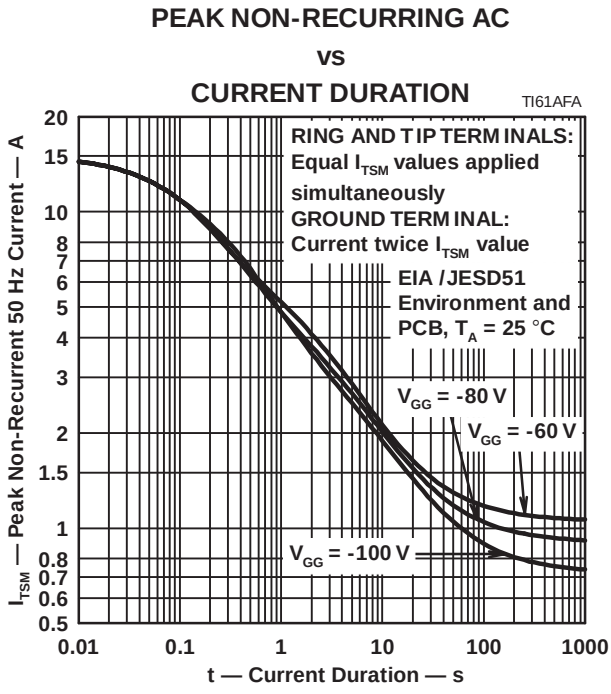


Figure 2. Non-repetitive Peak On-State Current against Duration
(Gate Voltage Ranges are -20 V to -75 V for the '61089 and -20 V to -100 V for the '61089A)

APPLICATIONS INFORMATION

Gated Protectors

This section covers three topics. First, it is explained why gated protectors are needed. Second, the voltage limiting action of the protector is described. Third, an example application circuit is described.

Purpose of Gated Protectors

Fixed voltage thyristor overvoltage protectors have been used since the early 1980s to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. As the SLIC was usually powered from a fixed voltage negative supply rail, the limiting voltage of the protector could also be a fixed value. The TISP1072F3 is a typical example of a fixed voltage SLIC protector.

SLICs have become more sophisticated. To minimize power consumption, some designs automatically adjust the supply voltage, V_{BAT}, to a value that is just sufficient to drive the required line current. For short lines the supply voltage would be set low, but for long lines, a higher supply voltage would be generated to drive sufficient line current. The optimum protection for this type of SLIC would be given by a protection voltage which tracks the SLIC supply voltage. This can be achieved by connecting the protection thyristor gate to the SLIC supply, Figure 3. This gated (programmable) protection arrangement minimizes the voltage stress on the SLIC, no matter what value of supply voltage.

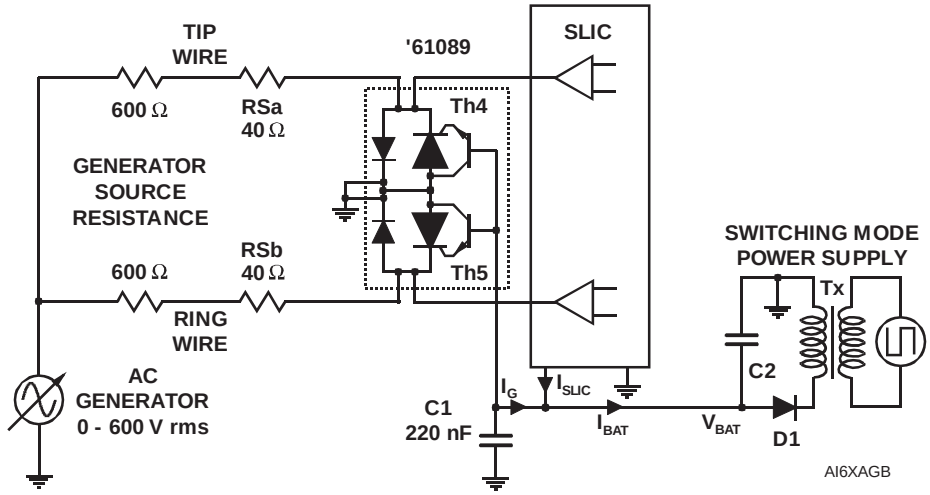


Figure 3. '61089 Buffered Gate Protector

Operation of Gated Protectors

Figures 4 and 5 show how the '61089 device limits negative and positive overvoltages. Positive overvoltages (Figure 5) are clipped by the antiparallel diodes in the '61089 protector and the resulting current is diverted to ground. Negative overvoltages (Figure 4) are initially clipped close to the SLIC negative supply rail value (V_{BAT}). If sufficient current is available from the overvoltage, then the protector (Th5) will crowbar into a low voltage on-state condition. As the overvoltage subsides the high holding current of the crowbar prevents d.c. latchup. The protection voltage will be the sum of the gate supply (V_{BAT}) and the peak gate-cathode voltage ($V_{GK(BO)}$). The protection voltage will be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 70 A/µs can cause inductive voltages of 0.7 V in 2.5 cm of printed wiring track. To minimize this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimized. Inductive voltages in the protector cathode wiring will also increase the protection voltage. These voltages can be minimized by routing the SLIC connection through the protector as shown in Figure 3.

Application Circuit

Figure 6 shows a typical '61089 part SLIC card protection circuit. The incoming line conductors, Ring (R) and Tip (T), connect to the relay matrix via the series overcurrent protection. Fusible resistors, fuses and positive temperature coefficient (PTC) thermistors can be used for overcurrent protection. Resistors will reduce the prospective current from the surge generator for both the '61089 device and the ring/test

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APPLICATIONS INFORMATION

Application Circuit (Continued)

protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration may be ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-conductor protection voltage is twice the conductor to ground value.

Relay contacts 3a and 3b connect the line conductors to the SLIC via the '61089 protector. The protector gate reference voltage comes from the SLIC negative supply (V_{BAT}). A 220 nF gate capacitor sources the high gate current pulses caused by fast rising impulses.

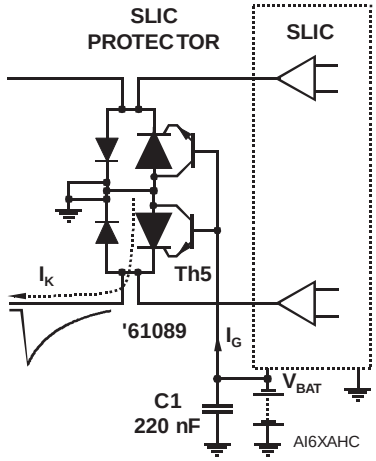


Figure 4. Negative Overvoltage Condition

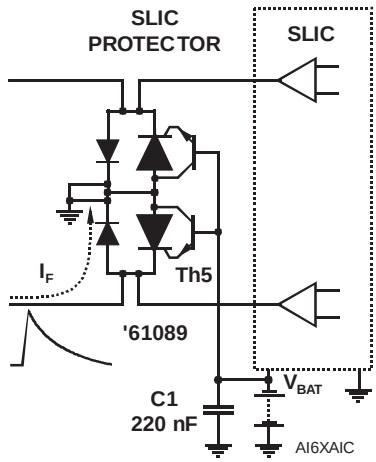


Figure 5. Positive Overvoltage Condition

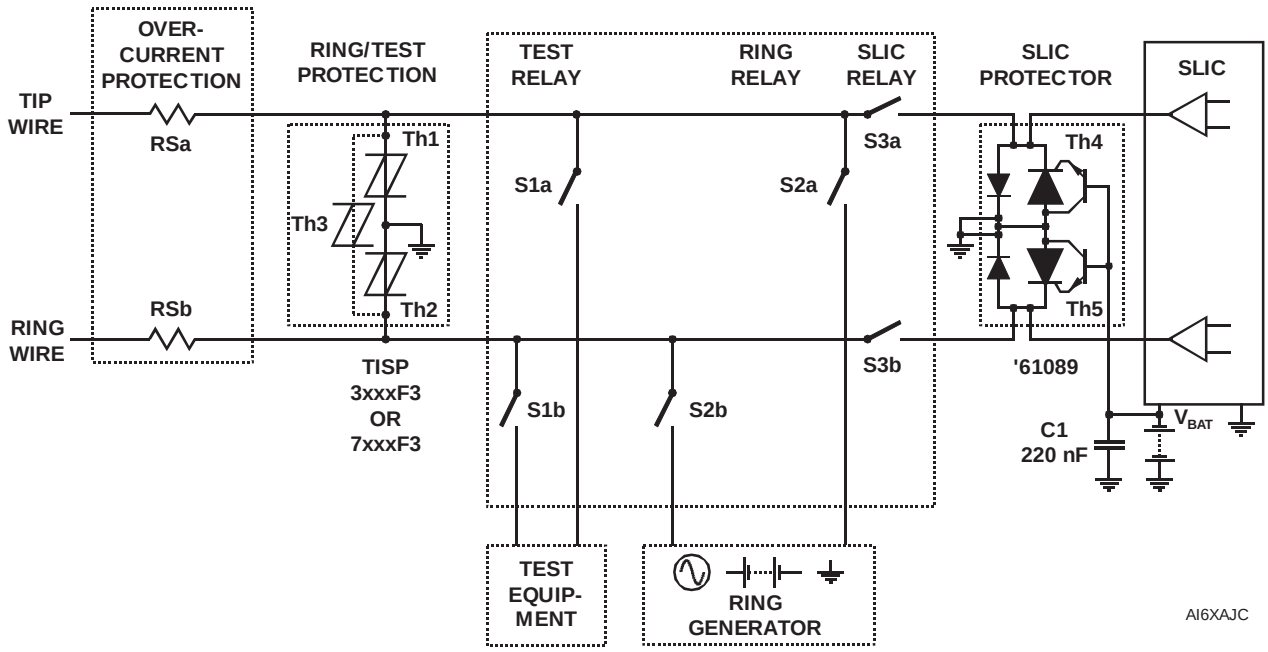


Figure 6. Typical Application Circuit

MECHANICAL DATA

Device Symbolization Code

Devices will be coded as below.

Device	Symbolization Code
TISP61089D	P61089
TISP61089SD	61089S
TISP61089AD	61089A
TISP61089ASD	1089AS
TISP61089P	TISP61089
TISP61089AP	61089A

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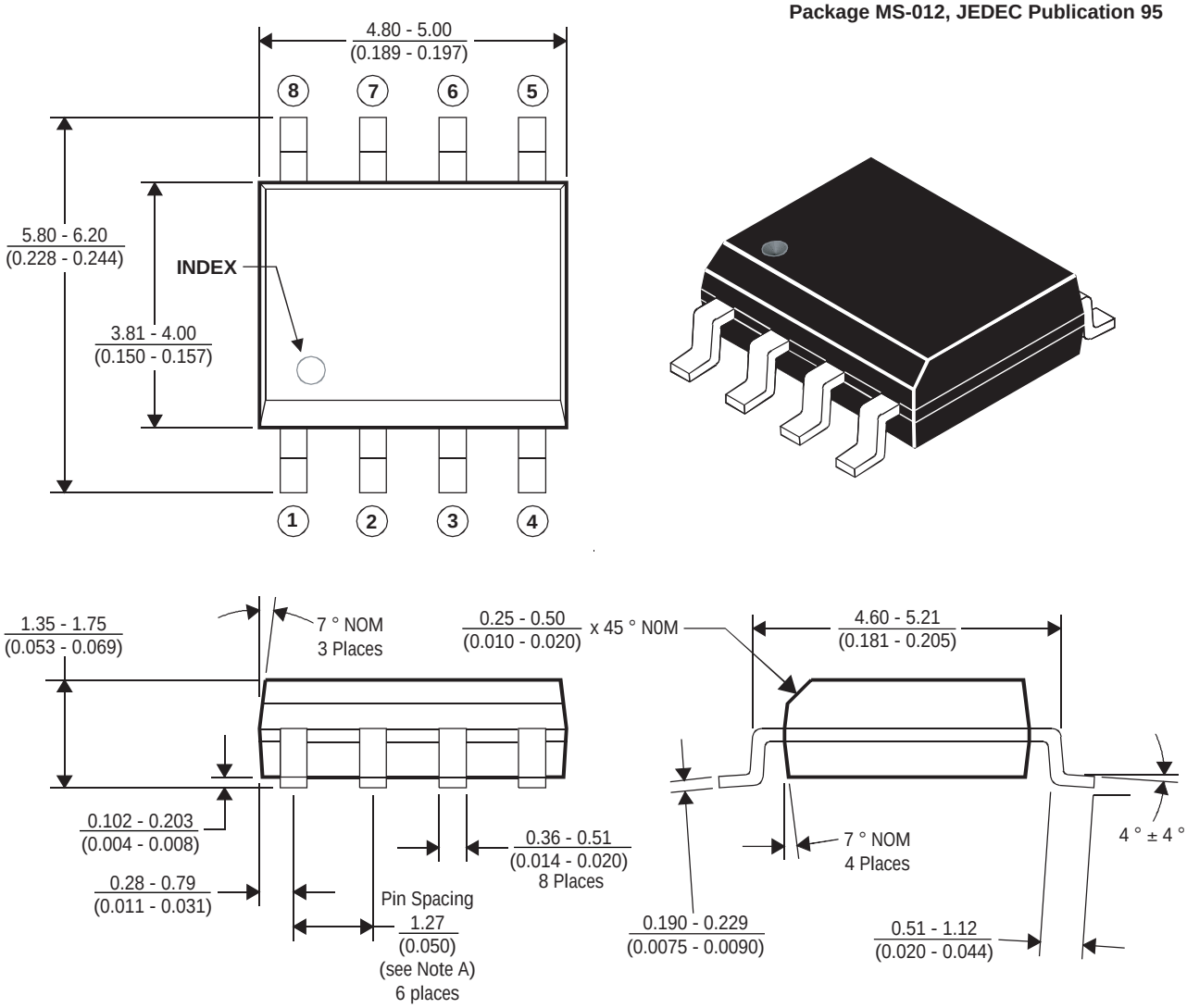
MECHANICAL DATA

D008 Plastic Small-outline Package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008

8-pin Small Outline Microelectronic Standard Package MS-012, JEDEC Publication 95



DIMENSIONS ARE: MILLIMETERS / (INCHES)

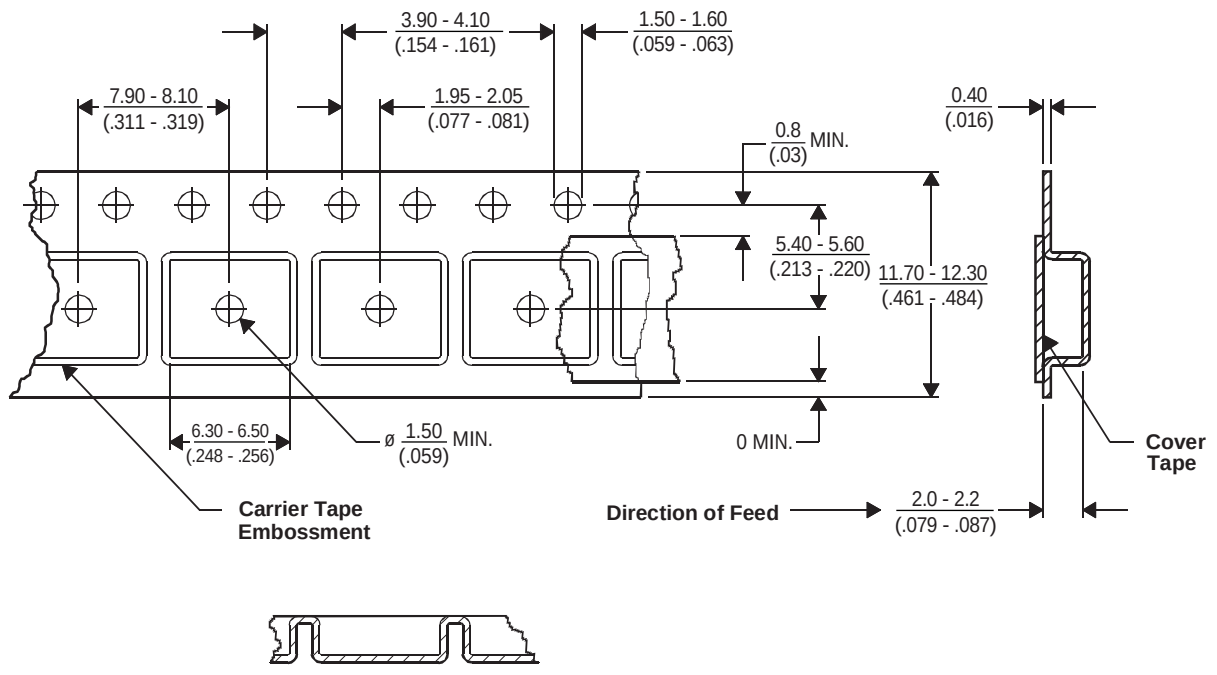
MDXXAAE

NOTES: A. Leads are within 0.25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0.15 (0.006).
D. Lead tips to be planar within ±0.051 (0.002).

MECHANICAL DATA

D008 Tape DImensions

D008 Package (8-pin Small Outline) Single-Sprocket Tape



DIMENSIONS ARE: MILLIMETERS / (INCHES)

NOTES: A. Taped devices are supplied on a reel of the following dimensions:-

MDXXATC

Reel diameter: 330 +0.0/-4.0 (12.99 +0.0/-.157)

Reel hub diameter: 100 ± 2.0 (3.937 ± .079)

Reel axial hole: 13.0 ± 0.2 (.512 ± .008)

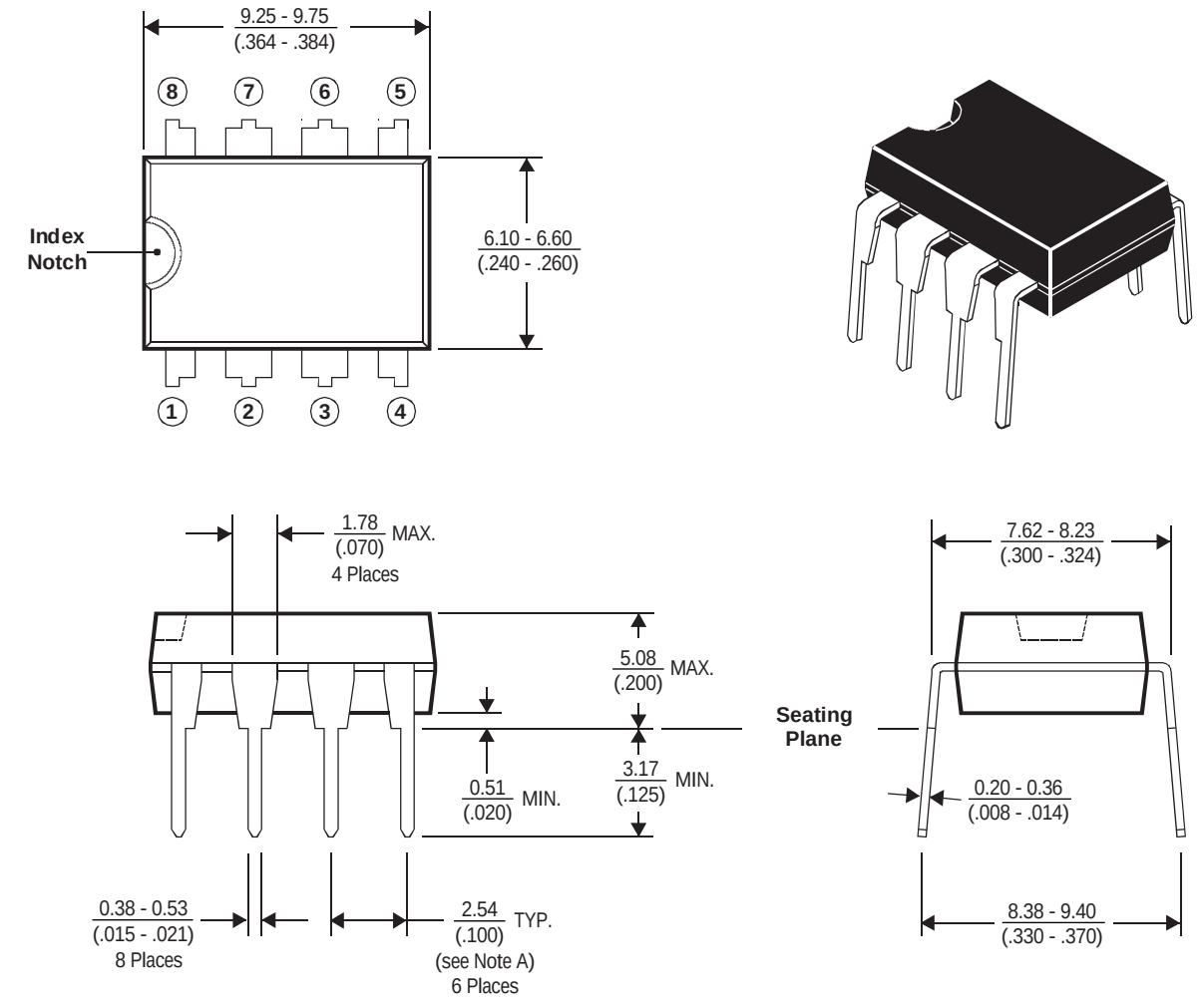
B. 2500 devices are on a reel.

MECHANICAL DATA

P008 Plastic Dual-In-Line Package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions The package is intended for insertion in mounting-hole rows on 7.62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

P008



MDXXCF

NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
B. Dimensions fall within JEDEC MS001 - R-PDIP-T, 0.300" Dual-In-Line Plastic Family.
C. Details of the previous dot index P008 package style, drawing reference MDXXABA, are given in the earlier publications.

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