XIO2000A/XIO2000AI PCI Express to PCI Bus Translation Bridge

Data Manual

Literature Number: SCPS155C
April 2007 Revised October 2008

PRINTED WITH SOY INK

TEXAS INSTRUMENTS

Printed on Recycled Paper

Contents

Section			Page
1	**XIO2000A Features**		**1**
2	**Introduction**		**2**
2.1	Description		2
2.2	Related Documents		2
2.3	Trademarks		2
2.4	Document Conventions		3
2.5	Document History		3
2.6	Ordering Information		3
2.7	Terminal Assignments		4
2.8	Terminal Descriptions		13
3	**Feature/Protocol Descriptions**		**20**
3.1	Power-Up/-Down Sequencing		20
	3.1.1	Power-Up Sequence	20
	3.1.2	Power-Down Sequence	21
3.2	Bridge Reset Features		22
3.3	PCI Express Interface		23
	3.3.1	External Reference Clock	23
	3.3.2	Beacon	24
	3.3.3	Wake	24
	3.3.4	Initial Flow Control Credits	24
	3.3.5	PCI Express Message Transactions	24
3.4	PCI Bus Interface		25
	3.4.1	I/O Characteristics	25
	3.4.2	Clamping Voltage	25
	3.4.3	PCI Bus Clock Run	26
	3.4.4	PCI Bus External Arbiter	26
	3.4.5	MSI Messages Generated from the Serial IRQ Interface	27
	3.4.6	PCI Bus Clocks	28
3.5	Quality of Service and Isochronous Features		28
	3.5.1	PCI Port Arbitration	29
	3.5.2	PCI Isochronous Windows	30
	3.5.3	PCI Express Extended VC With VC Arbitration	31
	3.5.4	128-Phase, WRR PCI Port Arbitration Timing	32
3.6	Configuration Register Translation		33
3.7	PCI Interrupt Conversion to PCI Express Messages		34
3.8	PME Conversion to PCI Express Messages		35
3.9	PCI Express To PCI Bus Lock Conversion		36
3.10	Two-Wire Serial-Bus Interface		37
	3.10.1	Serial-Bus Interface Implementation	38
	3.10.2	Serial-Bus Interface Protocol	38
	3.10.3	Serial-Bus EEPROM Application	40
	3.10.4	Accessing Serial-Bus Devices Through Software	42
3.11	Advanced Error Reporting Registers		42
3.12	Data Error Forwarding Capability		42
3.13	General-Purpose I/O Interface		43
3.14	Set Slot Power Limit Functionality		43
3.15	PCI Express and PCI Bus Power Management		43

4 Classic PCI Configuration Space 45
4.1 Vendor ID Register 46
4.2 Device ID Register 46
4.3 Command Register 47
4.4 Status Register 48
4.5 Class Code and Revision ID Register 49
4.6 Cache Line Size Register 49
4.7 Primary Latency Timer Register 49
4.8 Header Type Register 49
4.9 BIST Register 50
4.10 Device Control Base Address Register 50
4.11 Primary Bus Number Register 50
4.12 Secondary Bus Number Register 51
4.13 Subordinate Bus Number Register 51
4.14 Secondary Latency Timer Register 51
4.15 I/O Base Register 51
4.16 I/O Limit Register 52
4.17 Secondary Status Register 53
4.18 Memory Base Register 54
4.19 Memory Limit Register 54
4.20 Prefetchable Memory Base Register 54
4.21 Prefetchable Memory Limit Register 55
4.22 Prefetchable Base Upper 32-Bit Register 55
4.23 Prefetchable Limit Upper 32-Bit Register 55
4.24 I/O Base Upper 16-Bit Register 56
4.25 I/O Limit Upper 16-Bit Register 56
4.26 Capabilities Pointer Register 56
4.27 Interrupt Line Register 57
4.28 Interrupt Pin Register 57
4.29 Bridge Control Register 57
4.30 Capability ID Register 59
4.31 Next Item Pointer Register 59
4.32 Power Management Capabilities Register 60
4.33 Power Management Control/Status Register 61
4.34 Power Management Bridge Support Extension Register 61
4.35 Power Management Data Register 62
4.36 MSI Capability ID Register 62
4.37 Next Item Pointer Register 62
4.38 MSI Message Control Register 63
4.39 MSI Message Lower Address Register 63
4.40 MSI Message Upper Address Register 64
4.41 MSI Message Data Register 64
4.42 Capability ID Register 64
4.43 Next Item Pointer Register 65
4.44 Subsystem Vendor ID Register 65
4.45 Subsystem ID Register 65
4.46 PCI Express Capability ID Register 65
4.47 Next Item Pointer Register 66
4.48 PCI Express Capabilities Register 66

4.49 Device Capabilities Register 67
4.50 Device Control Register 68
4.51 Device Status Register 69
4.52 Link Capabilities Register 70
4.53 Link Control Register 71
4.54 Link Status Register 72
4.55 Serial-Bus Data Register 72
4.56 Serial-Bus Word Address Register 72
4.57 Serial-Bus Slave Address Register 73
4.58 Serial-Bus Control and Status Register 74
4.59 GPIO Control Register 75
4.60 GPIO Data Register 76
4.61 Control and Diagnostic Register 0 77
4.62 Control and Diagnostic Register 1 78
4.63 Control and Diagnostic Register 2 79
4.64 Subsystem Access Register 79
4.65 General Control Register 80
4.66 Clock Control Register 82
4.67 Clock Mask Register 83
4.68 Clock Run Status Register 84
4.69 Arbiter Control Register 85
4.70 Arbiter Request Mask Register 86
4.71 Arbiter Time-Out Status Register 87
4.72 Serial IRQ Mode Control Register 88
4.73 Serial IRQ Edge Control Register 89
4.74 Serial IRQ Status Register 90
5 PCI Express Extended Configuration Space 92
5.1 Advanced Error Reporting Capability ID Register 93
5.2 Next Capability Offset/Capability Version Register 93
5.3 Uncorrectable Error Status Register 94
5.4 Uncorrectable Error Mask Register 95
5.5 Uncorrectable Error Severity Register 96
5.6 Correctable Error Status Register 97
5.7 Correctable Error Mask Register 98
5.8 Advanced Error Capabilities and Control Register 99
5.9 Header Log Register 99
5.10 Secondary Uncorrectable Error Status Register 100
5.11 Secondary Uncorrectable Error Mask Register 101
5.12 Secondary Uncorrectable Error Severity Register 102
5.13 Secondary Error Capabilities and Control Register 103
5.14 Secondary Header Log Register 104
5.15 Virtual Channel Capability ID Register 104
5.16 Next Capability Offset/Capability Version Register 105
5.17 Port VC Capability Register 1 105
5.18 Port VC Capability Register 2 106
5.19 Port VC Control Register 107
5.20 Port VC Status Register 107
5.21 VC Resource Capability Register (VC0) 108
5.22 VC Resource Control Register (VC0) 109

5.23 VC Resource Status Register (VC0) . . . 110
5.24 VC Resource Capability Register (VC1) . . . 110
5.25 VC Resource Control Register (VC1) . . . 111
5.26 VC Resource Status Register (VC1) . . . 112
5.27 VC Arbitration Table . . . 112
5.28 Port Arbitration Table (VC1) . . . 113
6 Memory-Mapped TI Proprietary Register Space . . . 114
6.1 Device Control Map ID Register . . . 114
6.2 Revision ID Register . . . 115
6.3 Upstream Isochrony Capabilities Register . . . 115
6.4 Upstream Isochrony Control Register . . . 116
6.5 Upstream Isochronous Window 0 Control Register . . . 117
6.6 Upstream Isochronous Window 0 Base Address Register . . . 117
6.7 Upstream Isochronous Window 0 Limit Register . . . 117
6.8 Upstream Isochronous Window 1 Control Register . . . 118
6.9 Upstream Isochronous Window 1 Base Address Register . . . 118
6.10 Upstream Isochronous Window 1 Limit Register . . . 118
6.11 Upstream Isochronous Window 2 Control Register . . . 119
6.12 Upstream Isochronous Window 2 Base Address Register . . . 119
6.13 Upstream Isochronous Window 2 Limit Register . . . 119
6.14 Upstream Isochronous Window 3 Control Register . . . 120
6.15 Upstream Isochronous Window 3 Base Address Register . . . 120
6.16 Upstream Isochronous Window 3 Limit Register . . . 120
6.17 GPIO Control Register . . . 121
6.18 GPIO Data Register . . . 122
6.19 Serial-Bus Data Register . . . 122
6.20 Serial-Bus Word Address Register . . . 123
6.21 Serial-Bus Slave Address Register . . . 123
6.22 Serial-Bus Control and Status Register . . . 124
6.23 Serial IRQ Mode Control Register . . . 125
6.24 Serial IRQ Edge Control Register . . . 126
6.25 Serial IRQ Status Register . . . 127
7 Electrical Characteristics . . . 129
7.1 Absolute Maximum Ratings Over Operating Temperature Ranges † . . . 129
7.2 Recommended Operation Conditions . . . 129
7.3 Nominal Power Consumption . . . 130
7.4 PCI Express Differential Transmitter Output Ranges . . . 131
7.5 PCI Express Differential Receiver Input Ranges . . . 132
7.6 PCI Express Differential Reference Clock Input Ranges . . . 135
7.7 Electrical Characteristics Over Recommended Operating Conditions (PCI Bus) . . . 136
7.8 Electrical Characteristics Over Recommended Operating Conditions (3.3-V I/O) . . . 136
7.9 PCI Clock Timing Requirements Over Recommended Operating Conditions . . . 137
7.10 PCI Bus Timing Requirements Over Recommended Operating Conditions . . . 137
7.11 PCI Bus Parameter Measurement Information . . . 138
7.12 PCI Bus Parameter Measurement Information . . . 139
8 Glossary . . . 140
9 Mechanical Data . . . 141

List of Figures

Figure		*Page*
2−1	XIO2000A GZZ/ZZZ MicroStar BGA™ Package (Bottom View)	5
2−2	XIO2000A ZHH Microstar BGA Package (Bottom View)	8
3−1	XIO2000A Block Diagram	20
3−2	Power-Up Sequence	21
3−3	Power-Down Sequence	22
3−4	3-State Bidirectional Buffer	25
3−5	PCI Bus Timing	33
3−6	Type 0 Configuration Transaction Address Phase Encoding	33
3−7	Type 1 Configuration Transaction Address Phase Encoding	34
3−8	PCI Express Assert_INTx Message	35
3−9	PCI Express Deassert_INTx Message	35
3−10	PCI Express PME Message	35
3−11	Starting A Locked Sequence	36
3−12	Continuing A Locked Sequence	37
3−13	Terminating A Locked Sequence	37
3−14	Serial EEPROM Application	38
3−15	Serial-Bus Start/Stop Conditions and Bit Transfers	39
3−16	Serial-Bus Protocol Acknowledge	39
3−17	Serial-Bus Protocol—Byte Write	39
3−18	Serial-Bus Protocol—Byte Read	40
3−19	Serial-Bus Protocol—Multibyte Read	40
7−1	Load Circuit And Voltage Waveforms	137
7−2	CLK Timing Waveform	139
7−3	$\overline{\text{PRST}}$ Timing Waveforms	139
7−4	Shared Signals Timing Waveforms	139

List of Tables

Table		Page
2−1	XIO2000A GZZ/ZZZ Terminals Sorted Alphanumerically	6
2−2	XIO2000A ZHH Terminals Sorted Alphanumerically	9
2−3	XIO2000A Signal Names Sorted Alphabetically	11
2−4	Power Supply Terminals	14
2−5	Ground Terminals	14
2−6	Combined Power Outputs	14
2−7	PCI Express Terminals	15
2−8	Clock Terminals	15
2−9	PCI System Terminals	16
2−10	Reserved Terminals	17
2−11	Miscellaneous Terminals	18
3−1	Bridge Reset Options	23
3−2	Initial Flow Control Credit Advertisements	24
3−3	Messages Supported by the Bridge	25
3−4	IRQ Interrupt to MSI Message Mapping	27
3−5	Classic PCI Arbiter Registers	29
3−6	Port Number to PCI Bus Device Mapping	29
3−7	128-Phase, WRR Time-Based Arbiter Registers	30
3−8	PCI Isochronous Windows	30
3−9	Hardware-Fixed, Round-Robin Arbiter Registers	31
3−10	32-phase, WRR Arbiter Registers	32
3−11	Type 0 Configuration Transaction IDSEL Mapping	34
3−12	Interrupt Mapping In The Code Field	35
3−13	EEPROM Register Loading Map	41
3−14	Registers Used To Program Serial-Bus Devices	42
3−15	Clocking In Low Power States	44
4−1	Classic PCI Configuration Register Map	45
4−2	Command Register Description	47
4−3	Status Register Description	48
4−4	Class Code and Revision ID Register Description	49
4−5	Device Control Base Address Register Description	50
4−6	I/O Base Register Description	51
4−7	I/O Limit Register Description	52
4−8	Secondary Status Register Description	53
4−9	Memory Base Register Description	54
4−10	Memory Limit Register Description	54
4−11	Prefetchable Memory Base Register Description	54
4−12	Prefetchable Memory Limit Register Description	55
4−13	Prefetchable Base Upper 32-Bit Register Description	55
4−14	Prefetchable Limit Upper 32-Bit Register Description	55
4−15	I/O Base Upper 16-Bit Register Description	56
4−16	I/O Limit Upper 16-Bit Register Description	56
4−17	Bridge Control Register Description	57
4−18	Power Management Capabilities Register Description	60
4−19	Power Management Control/Status Register Description	61
4−20	Power Management Bridge Support Extension Register Description	61
4−21	MSI Message Control Register Description	63

4–22 MSI Message Lower Address Register Description 63
4–23 MSI Message Data Register Description 64
4–24 PCI Express Capabilities Register Description 66
4–25 Device Capabilities Register Description 67
4–26 Device Control Register Description 68
4–27 Device Status Register Description 69
4–28 Link Capabilities Register Description 70
4–29 Link Control Register Description 71
4–30 Link Status Register Description 72
4–31 Serial-Bus Slave Address Register Description 73
4–32 Serial-Bus Control and Status Register Description 74
4–33 GPIO Control Register Description 75
4–34 GPIO Data Register Description 76
4–35 Control and Diagnostic Register 0 Description 77
4–36 Control and Diagnostic Register 1 Description 78
4–37 Control and Diagnostic Register 2 Description 79
4–38 Subsystem Access Register Description 79
4–39 General Control Register Description 80
4–40 Clock Control Register Description 82
4–41 Clock Mask Register Description 83
4–42 Clock Run Status Register Description 84
4–43 Arbiter Control Register Description 85
4–44 Arbiter Request Mask Register Description 86
4–45 Arbiter Time-Out Status Register Description 87
4–46 Serial IRQ Mode Control Register Description 88
4–47 Serial IRQ Edge Control Register Description 89
4–48 Serial IRQ Status Register Description 90
5–1 PCI Express Extended Configuration Register Map 92
5–2 Uncorrectable Error Status Register Description 94
5–3 Uncorrectable Error Mask Register Description 95
5–4 Uncorrectable Error Severity Register Description 96
5–5 Correctable Error Status Register Description 97
5–6 Correctable Error Mask Register Description 98
5–7 Advanced Error Capabilities and Control Register Description 99
5–8 Secondary Uncorrectable Error Status Register Description 100
5–9 Secondary Uncorrectable Error Mask Register Description 101
5–10 Secondary Uncorrectable Error Severity Register Description 102
5–11 Secondary Error Capabilities and Control Register Description 103
5–12 Secondary Header Log Register Description 104
5–13 Port VC Capability Register 1 Description 105
5–14 Port VC Capability Register 2 Description 106
5–15 Port VC Control Register Description 107
5–16 Port VC Status Register Description 107
5–17 VC Resource Capability Register (VC0) Description 108
5–18 VC Resource Control Register (VC0) Description 109
5–19 VC Resource Status Register (VC0) Description 110
5–20 VC Resource Capability Register (VC1) Description 110
5–21 VC Resource Control Register (VC1) Description 111

Table		Page
5–22	VC Resource Status Register (VC1) Description	112
5–23	VC Arbitration Table	112
5–24	VC Arbitration Table Entry Description	112
5–25	Port Arbitration Table	113
5–26	Port Arbitration Table Entry Description	113
6–1	Device Control Memory Window Register Map	114
6–2	Upstream Isochronous Capabilities Register Description	115
6–3	Upstream Isochrony Control Register Description	116
6–4	Upstream Isochronous Window 0 Control Register Description	117
6–5	Upstream Isochronous Window 1 Control Register Description	118
6–6	Upstream Isochronous Window 2 Control Register Description	119
6–7	Upstream Isochronous Window 3 Control Register Description	120
6–8	GPIO Control Register Description	121
6–9	GPIO Data Register Description	122
6–10	Serial-Bus Slave Address Register Description	123
6–11	Serial-Bus Control and Status Register Description	124
6–12	Serial IRQ Mode Control Register Description	125
6–13	Serial IRQ Edge Control Register Description	126
6–14	Serial IRQ Status Register Description	127

1 XIO2000A Features

- Full x1 PCI Express Throughput
- Fully Compliant with *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- Fully Compliant with *PCI Express Base Specification*, Revision 1.0a
- Fully Compliant with *PCI Local Bus Specification*, Revision 2.3
- Extended Virtual Channel (VC) Support Includes a Second VC for Quality-of-Service and Isochronous Applications
- PCI Express Advanced Error Reporting Capability Including ECRC Support
- Support for D1, D2, $D3_{hot}$, and $D3_{cold}$
- Active State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States
- Wake Event and Beacon Support
- Error Forwarding Including PCI Express Data Poisoning and PCI Bus Parity Errors
- Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended, Reference Clock
- Robust Pipeline Architecture To Minimize Transaction Latency
- Full PCI Local Bus 66-MHz/32-Bit Throughput
- Support for Six Subordinate PCI Bus Masters with Internal Configurable, 2-Level Prioritization Scheme
- Low Power Design (<350 mW) Ensures Ease of Implementation
- XIO2000AI Supports Industrial Temperatures at 33-MHz Bus Speeds
- Two Package Options: 15 mm x 15 mm and 12 mm x 12 mm
- Internal PCI Arbiter Supporting Up to 6 External PCI Masters
- Advanced VC Arbitration Options Include VC1 Strict Priority, Hardware-Fixed Round-Robin, and 32-Phase, Weighted Round-Robin
- Advanced PCI Bus Port Arbitration Options Include 128-phase, Weighted Round-Robin Time-Based and 128-phase, Weighted Round-Robin Aggressive Time-Based
- Advanced PCI Isochronous Windows for Memory Space Mapping to a Specified Traffic Class
- Advanced PCI Express Message Signaled Interrupt Generation for Serial IRQ Interrupts from CardBus Applications
- External PCI Bus Arbiter Option
- PCI Bus $\overline{LOCK}$ Support
- Clock Run and Power Override Support
- Six Buffered PCI Clock Outputs (33 MHz or 66 MHz)
- PCI Bus Interface 3.3-V and 5.0-V (33 MHz only at 5.0 V) Tolerance Options
- Integrated AUX Power Switch Drains V_{AUX} Power Only When Main Power Is Off
- Eight 3.3-V, Multifunction, General-Purpose I/O Terminals
- Memory-Mapped EEPROM Serial-Bus Controller Supporting PCI Express Power Budget/Limit Extensions for Add-In Cards
- Compact Footprint, 201-Ball, GZZ MicroStar™ BGA (XIO2000A only), Lead-Free 201-Ball, ZZZ MicroStar™ BGA; 175-Ball ZHC MicroStar BGA; or 175-Ball ZHH MicroStar BGA

MicroStar BGA is a trademark of Texas Instruments.
Other trademarks are the property of their respective owners.

2 Introduction

The Texas Instruments XIO2000A is a PCI Express to PCI local bus translation bridge that provides full PCI Express and PCI local bus functionality and performance.

2.1 Description

The XIO2000A is a single-function PCI Express to PCI translation bridge that is fully compliant to the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. For downstream traffic, the bridge simultaneously supports up to eight posted and four nonposted transactions for each enabled virtual channel (VC). For upstream traffic, up to six posted and four nonposted transactions are simultaneously supported for each VC.

The PCI Express interface is fully compliant to the *PCI Express Base Specification*, Revision 1.0a.

The PCI Express interface supports a x1 link operating at full 250 MB/s packet throughput in each direction simultaneously. Two independent VCs are supported. The second VC is optimized for isochronous traffic types and quality-of-service (QoS) applications. Also, the bridge supports the advanced error reporting capability including extended CRC (ECRC) as defined in the *PCI Express Base Specification*. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency across the bridge. If parity errors are detected, then packet poisoning is supported for both upstream and downstream operations.

The PCI local bus is fully compliant with the *PCI Local Bus Specification* (Revision 2.3) and associated programming model. Also, the bridge supports the standard PCI-to-PCI bridge programming model.

The PCI bus interface is 32-bit and can operate at either 33 MHz or 66 MHz. Also, the PCI interface provides fair arbitration and buffered clock outputs for up to 6 subordinate devices. The bridge has advanced VC arbitration and PCI port arbitration features for upstream traffic. When these arbitration features are fully utilized, bridge throughput performance may be tuned for a variety of complex applications.

Power management (PM) features include active state link PM, PME mechanisms, the beacon and wake protocols, and all conventional PCI D-states. If the active state link PM is enabled, then the link automatically saves power when idle using the L0s and L1 states. PM active state NAK, PM PME, and PME-to-ACK messages are supported. Standard PCI bus power management features provide several low power modes, which enable the host system to further reduce power consumption.

The bridge has additional capabilities including, but not limited to, serial IRQ with MSI messages, serial EEPROM, power override, clock run, and PCI bus $\overline{\text{LOCK}}$. Also, eight general-purpose inputs and outputs (GPIOs) are provided for further system control and customization.

2.2 Related Documents

- *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- *PCI Express Base Specification*, Revision 1.0a
- *PCI Express Card Electromechanical Specification*, Revision 1.0a
- *PCI Local Bus Specification*, Revision 2.3
- *PCI-to-PCI Bridge Architecture Specification*, Revision 1.2
- *PCI Bus Power Management Interface Specification*, Revision 1.1 or 1.2
- *PCI Mobile Design Guide*, Revision 1.1
- *Serialized IRQ Support for PCI Systems*, Revision 6.0
- *PCI Express Jitter and BER White Paper*

2.3 Trademarks

- PCI Express is a trademark of PCI-SIG
- TI and MicroStar BGA are trademarks of Texas Instruments
- Other trademarks are the property of their respective owners

2.4 Document Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, $\overline{\text{GRST}}$), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. Differential signal names end with P, N, +, or − designators. The P or + designators signify the positive signal associated with the differential pair. The N or − designators signify the negative signal associated with the differential pair.
6. RSVD indicates that the referenced item is reserved.
7. The power and ground signals in Figure 2−1 are not subscripted to aid in readability.
8. In Sections 4 through 6, the configuration space for the bridge is defined. For each register bit, the software access method is identified in an access column. The legend for this access column includes the following entries:

   r – read access by software

   u – updates by the bridge internal hardware

   w – write access by software

   c – clear an asserted status bit with a write-back of 1b by software

2.5 Document History

REVISION DATE	REVISION NUMBER	REVISION COMMENTS
05/2004	–	Product preview
08/2005	A	Initial release

2.6 Ordering Information

ORDERING NUMBER	NAME	VOLTAGE	PACKAGE
XIO2000A	PCI-Express to PCI Bridge	3.3-V, 5.0-V tolerant PCI bus I/Os with 3.3-V and 1.5-V power terminals	201-terminal GZZ MicroStar PBGA
XIO2000A	PCI-Express to PCI Bridge	3.3-V, 5.0-V tolerant PCI bus I/Os with 3.3-V and 1.5-V power terminals	201-terminal ZZZ (Lead-Free) MicroStar PBGA
XIO2000A	PCI-Express to PCI Bridge	3.3-V, 5.0-V tolerant PCI bus I/Os with 3.3-V and 1.5-V power terminals	175-terminal ZHH (Lead-Free) MicroStar PBGA
XIO2000A	PCI-Express to PCI Bridge	3.3-V, 5.0-V tolerant PCI bus I/Os with 3.3-V and 1.5-V power terminals	175-terminal ZHC (Lead-Free) MicroStar PBGA
XIO2000AI	PCI-Express to PCI Bridge	3.3-V, 5.0-V tolerant PCI bus I/Os with 3.3-V and 1.5-V power terminals	201-terminal ZZZ (Lead-Free) MicroStar PBGA
XIO2000AI	PCI-Express to PCI Bridge	3.3-V, 5.0-V tolerant PCI bus I/Os with 3.3-V and 1.5-V power terminals	175-terminal ZHH (Lead-Free) MicroStar PBGA
XIO2000AI	PCI-Express to PCI Bridge	3.3-V, 5.0-V tolerant PCI bus I/Os with 3.3-V and 1.5-V power terminals	175-terminal ZHC (Lead-Free) MicroStar PBGA

2.7 Terminal Assignments

The XIO2000A is available in either a 201-ball GZZ/ZZZ MicroStar™ BGA or a 175−ball ZHH/ZHC Microstar package. The XIO2000AI is available in a 201-ball ZZZ MicroStar BGA or a 175-ball ZHH MicroStar package.

Figure 2−1 shows a terminal diagram of the GZZ/ZZZ package, and Table 2−1 lists the GZZ/ZZZ terminals sorted alphanumerically.

Figure 2−2 shows a terminal diagram of the ZHH package, and Table 2−2 lists the ZHH package terminals sorted alphanumerically.

Figure 2−3 shows a terminal diagram of the ZHC package, and Table 2−3 lists the ZHC package terminals sorted alphanumerically.

Table 2−4 shows the terminals by the alphabetically sorted signal names for both packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
U		INTC	PRST	LOCK	GPIO1 // PWR_ OVRD	GPIO3	GPIO6	GPIO7	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	
T	INTB		INTD	SERIRQ	GPIO0 // CLKRUN	GPIO2	GPIO5 // SDA	RSVD	RSVD	RSVD	RSVD	RSVD	VDD_33	RSVD	RSVD		RSVD
R	M66EN	INTA		VSS	VDD_33	VSS	GPIO4 // SCL	RSVD	RSVD	VSS	VSS	VSS	VSS	VDD_33		RSVD	VSS
P	AD30	AD31	CLK				VDD_15	VSS	VDD_33	VDD_33	VDD_33				VDD_15	RSVD	RSVD
N	AD28	AD29	VSS												RSVD	RSVD	GRST
M	AD26	AD27	VDD_33												PME	WAKE	VDD_15 _COMB
L	AD23	C/BE[3]	AD24	AD25			VSS	VSS	VSS	VSS	VSS			VDD_33 _COMB IO	VSSA	REF0_ PCIE	REF1_ PCIE
K	AD20	AD21	AD22	VSS			VSS	VSS	VSS	VSS	VSS			VDD_33 _AUX	VDDA_ 33	VDD_33 _COMB	VSS
J	VCCP	AD19	AD18	VDD_15			VSS	VSS	VSS	VSS	VSS			VDDA_ 15	VDDA_ 15	VSSA	PERST
H	C/BE[2]	AD17	AD16	VDD_33			VSS	VSS	VSS	VSS	VSS			VDD_ 15	VSSA	TXN	TXP
G	FRAME	IRDY	TRDY	VSS			VSS	VSS	VSS	VSS	VSS			VSSA	VDDA_ 15	VSSA	VSS
F	DEVSEL	STOP	PERR												VSSA	VSSA	VDDA_ 15
E	SERR	PAR	VDD_33												VSSA	RXN	RXP
D	C/BE[1]	AD15	VSS				AD3	VSS	VDD_15	VDD_33	VSS				VDDA_ 33	RSVD	RSVD
C	AD14	AD13		AD8	VSS	VDD_33	AD2	CLK OUT0	REQ1	REQ2	GNT3	GNT4	VDD_33	VSS		REF CLK−	REF CLK+
B	AD12		AD10	C/BE[0]	AD7	AD5	AD1	REQ0	CLK OUT1	CLK OUT2	REQ3	REQ4	REQ5	CLK OUT6	CLKRUN _EN		VSSA
A		AD11	AD9	VCCP	AD6	AD4	AD0	GNT0	GNT1	GNT2	CLK OUT3	CLK OUT4	CLK OUT5	GNT5	EXT_ ARB_EN	REFCLK _SEL	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure 2−1. XIO2000A GZZ MicroStar BGA™ Package, XIO2000A/XIO2000AI ZZZ MicroStar BGA™ Package(Bottom View)

Table 2−1. GZZ/ZZZ Terminals Sorted Alphanumerically

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
A02	AD11	C17	REFCLK+	H10	V_{SS}
A03	AD9	D01	C/$\overline{BE[1]}$	H11	V_{SS}
A04	V_{CCP}	D02	AD15	H14	V_{DD_15}
A05	AD6	D03	V_{SS}	H15	V_{SSA}
A06	AD4	D07	AD3	H16	TXN
A07	AD0	D08	V_{SS}	H17	TXP
A08	$\overline{GNT0}$	D09	V_{DD_15}	J01	V_{CCP}
A09	$\overline{GNT1}$	D10	V_{DD_33}	J02	AD19
A10	$\overline{GNT2}$	D11	V_{SS}	J03	AD18
A11	CLKOUT3	D15	V_{DDA_33}	J04	V_{DD_15}
A12	CLKOUT4	D16	RSVD	J07	V_{SS}
A13	CLKOUT5	D17	RSVD	J08	V_{SS}
A14	$\overline{GNT5}$	E01	$\overline{SERR}$	J09	V_{SS}
A15	EXT_ARB_EN	E02	PAR	J10	V_{SS}
A16	REFCLK_SEL	E03	V_{DD_33}	J11	V_{SS}
B01	AD12	E15	V_{SSA}	J14	V_{DDA_15}
B03	AD10	E16	RXN	J15	V_{DDA_15}
B04	C/$\overline{BE[0]}$	E17	RXP	J16	V_{SSA}
B05	AD7	F01	$\overline{DEVSEL}$	J17	$\overline{PERST}$
B06	AD5	F02	$\overline{STOP}$	K01	AD20
B07	AD1	F03	$\overline{PERR}$	K02	AD21
B08	$\overline{REQ0}$	F15	V_{SSA}	K03	AD22
B09	CLKOUT1	F16	V_{SSA}	K04	V_{SS}
B10	CLKOUT2	F17	V_{DDA_15}	K07	V_{SS}
B11	$\overline{REQ3}$	G01	$\overline{FRAME}$	K08	V_{SS}
B12	$\overline{REQ4}$	G02	$\overline{IRDY}$	K09	V_{SS}
B13	$\overline{REQ5}$	G03	$\overline{TRDY}$	K10	V_{SS}
B14	CLKOUT6	G04	V_{SS}	K11	V_{SS}
B15	CLKRUN_EN	G07	V_{SS}	K14	$V_{DD_33_AUX}$
B17	V_{SSA}	G08	V_{SS}	K15	V_{DDA_33}
C01	AD14	G09	V_{SS}	K16	$V_{DD_33_COMB}$
C02	AD13	G10	V_{SS}	K17	V_{SS}
C04	AD8	G11	V_{SS}	L01	AD23
C05	V_{SS}	G14	V_{SSA}	L02	C/$\overline{BE[3]}$
C06	V_{DD_33}	G15	V_{DDA_15}	L03	AD24
C07	AD2	G16	V_{SSA}	L04	AD25
C08	CLKOUT0	G17	V_{SS}	L07	V_{SS}
C09	$\overline{REQ1}$	H01	C/$\overline{BE[2]}$	L08	V_{SS}
C10	$\overline{REQ2}$	H02	AD17	L09	V_{SS}
C11	$\overline{GNT3}$	H03	AD16	L10	V_{SS}
C12	$\overline{GNT4}$	H04	V_{DD_33}	L11	V_{SS}
C13	V_{DD_33}	H07	V_{SS}	L14	$V_{DD_33_COMBIO}$
C14	V_{SS}	H08	V_{SS}	L15	V_{SSA}
C16	REFCLK−	H09	V_{SS}	L16	REF0_PCIE

Table 2−1. GZZ/ZZZ Terminals Sorted Alphanumerically (Continued)

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
L17	REF1_PCIE	P17	RSVD	T09	RSVD
M01	AD26	R01	M66EN	T10	RSVD
M02	AD27	R02	$\overline{\text{INTA}}$	T11	RSVD
M03	V_{DD_33}	R04	V_{SS}	T12	RSVD
M15	$\overline{\text{PME}}$	R05	V_{DD_33}	T13	V_{DD_33}
M16	$\overline{\text{WAKE}}$	R06	V_{SS}	T14	RSVD
M17	$V_{DD_15_COMB}$	R07	GPIO4 // SCL	T15	RSVD
N01	AD28	R08	RSVD	T17	RSVD
N02	AD29	R09	RSVD	U02	$\overline{\text{INTC}}$
N03	V_{SS}	R10	V_{SS}	U03	$\overline{\text{PRST}}$
N15	RSVD	R11	V_{SS}	U04	$\overline{\text{LOCK}}$
N16	RSVD	R12	V_{SS}	U05	GPIO1 // PWR_OVRD
N17	$\overline{\text{GRST}}$	R13	V_{SS}	U06	GPIO3
P01	AD30	R14	V_{DD_33}	U07	GPIO6
P02	AD31	R16	RSVD	U08	GPIO7
P03	CLK	R17	V_{SS}	U09	RSVD
P07	V_{DD_15}	T01	$\overline{\text{INTB}}$	U10	RSVD
P08	V_{SS}	T03	$\overline{\text{INTD}}$	U11	RSVD
P09	V_{DD_33}	T04	SERIRQ	U12	RSVD
P10	V_{DD_33}	T05	GPIO0 // $\overline{\text{CLKRUN}}$	U13	RSVD
P11	V_{DD_33}	T06	GPIO2	U14	RSVD
P15	V_{DD_15}	T07	GPIO5 // SDA	U15	RSVD
P16	RSVD	T08	RSVD	U16	RSVD

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
P	PRST	LOCK	GPIO0// CLKRUN	GPIO1// PWR_OVER	GPIO4 // SCL	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VSSA	RSVD	P
N	INTB	INTC	SERIRQ	GPIO2	GPIO5 // SDA	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VDD_15	VSS	RSVD	N
M	M66EN	INTA	INTD	GPIO3	GPIO6	RSVD	RSVD	VSS	VDD_33	VDD_33	VDD_33	RSVD	RSVD	RSVD	M
L	AD31	AD30	CLK	AD29	VDD_15	GPIO7	RSVD	VDD_33	VSS	RSVD	VSS	$\overline{\text{PME}}$	$\overline{\text{GRST}}$	RSVD	L
K	AD26	AD27	AD28	VDD_33							VSSA	VDD_33_ COMBIO	VDD_15_ COMB	WAKE	K
J	AD23	$\overline{\text{C/BE[3]}}$	AD24	AD25		VDD_33	VDD_33	VSS	VSS		VDDA_33	VDD_33_ AUX	REF1_PCIE	REF0_PCIE	J
H	AD19	AD21	AD20	AD22		VSS	VSS	VSS	VSS		VDDA_15	$\overline{\text{PERST}}$	VDDA_15	VDD_33_ COMB	H
G	VCCP	AD17	AD18	VDD_15		VSS	VSS	VSS	VSS		VSSA	VSSA	TXN	TXP	G
F	$\overline{\text{FRAME}}$	$\overline{\text{C/BE[2]}}$	AD16	VDD_33		VSS	VSS	VSS	VDD_33		VSSA	VDDA_15	VSS	VDD_15	F
E	$\overline{\text{TRDY}}$	$\overline{\text{DEVSEL}}$	$\overline{\text{STOP}}$	$\overline{\text{IRDY}}$							VDDA_15	VSSA	RXN	RXP	E
D	$\overline{\text{SERR}}$	PAR	$\overline{\text{PERR}}$	VDD_33	VDD_33	AD1	CLKOUT0	VDD_15	VDD_33	CLKOUT3	$\overline{\text{GNT4}}$	VSSA	RSVD	RSVD	D
C	$\overline{\text{C/BE[1]}}$	AD15	AD14	AD8	AD7	AD3	GNT0	GNT1	$\overline{\text{REQ2}}$	$\overline{\text{GNT3}}$	$\overline{\text{GNT5}}$	VDDA_33	REFCLK+	REFCLK−	C
B	AD13	AD12	AD10	$\overline{\text{C/BE[0]}}$	AD6	AD4	$\overline{\text{REQ0}}$	CLKOUT1	$\overline{\text{GNT3}}$	CLKOUT4	CLKOUT5	EXT_ARB_EN	CLKRUN_EN	VSSA	B
A		AD11	AD9	VCCP	AD5	AD2	AD0	$\overline{\text{REQ1}}$	CLKOUT2	$\overline{\text{REQ3}}$	$\overline{\text{REQ4}}$	$\overline{\text{REQ5}}$	CLKOUT6	REFCLK_SEL	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 2−2. XIO2000A/XIO2000AI ZHH Microstar BGA™ Package (Bottom View)

Table 2−2. ZHH Terminals Sorted Alphanumerically

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
A02	AD11	D04	V_{DD_33}	H02	AD21
A03	AD9	D05	V_{DD_33}	H03	AD20
A04	V_{CCP}	D06	AD1	H04	AD22
A05	AD5	D07	CLKOUT0	H06	V_{SS}
A06	AD2	D08	V_{DD_15}	H07	V_{SS}
A07	AD0	D09	V_{DD_33}	H08	V_{SS}
A08	$\overline{REQ1}$	D10	CLKOUT3	H09	V_{SS}
A09	CLKOUT2	D11	$\overline{GNT4}$	H11	V_{DDA_15}
A10	$\overline{REQ3}$	D12	V_{SSA}	H12	$\overline{PERST}$
A11	$\overline{REQ4}$	D13	RSVD	H13	V_{DDA_15}
A12	$\overline{REQ5}$	D14	RSVD	H14	$V_{DD_33_COMB}$
A13	CLKOUT6	E01	$\overline{TRDY}$	J01	AD23
A14	REFCLK_SEL	E02	$\overline{DEVSEL}$	J02	C/$\overline{BE[3]}$
B01	AD13	E03	$\overline{STOP}$	J03	AD24
B02	AD12	E04	$\overline{IRDY}$	J04	AD25
B03	AD10	E11	V_{DDA_15}	J06	V_{DD_33}
B04	C/$\overline{BE[0]}$	E12	V_{SSA}	J07	V_{DD_33}
B05	AD6	E13	RXN	J08	V_{SS}
B06	AD4	E14	RXP	J09	V_{SS}
B07	$\overline{REQ0}$	F01	$\overline{FRAME}$	J11	V_{DDA_33}
B08	CLKOUT1	F02	C/$\overline{BE[2]}$	J12	$V_{DD_33_AUX}$
B09	$\overline{GNT2}$	F03	AD16	J13	REF1_PCIE
B10	CLKOUT4	F04	V_{DD_33}	J14	REF0_PCIE
B11	CLKOUT5	F06	V_{SS}	K01	AD26
B12	EXT_ARB_EN	F07	V_{SS}	K02	AD27
B13	CLKRUN_EN	F08	V_{SS}	K03	AD28
B14	V_{SSA}	F09	V_{DD_33}	K04	V_{DD_33}
C01	C/$\overline{BE[1]}$	F11	V_{SSA}	K11	V_{SSA}
C02	AD15	F12	V_{DDA_15}	K12	$V_{DD_33_COMBIO}$
C03	AD14	F13	V_{SS}	K13	$V_{DD_15_COMB}$
C04	AD8	F14	V_{DD_15}	K14	$\overline{WAKE}$
C05	AD7	G01	V_{CCP}	L01	AD31
C06	AD3	G02	AD17	L02	AD30
C07	$\overline{GNT0}$	G03	AD18	L03	CLK
C08	$\overline{GNT1}$	G04	V_{DD_15}	L04	AD29
C09	$\overline{REQ2}$	G06	V_{SS}	L05	V_{DD_15}
C10	$\overline{GNT3}$	G07	V_{SS}	L06	GPIO7
C11	$\overline{GNT5}$	G08	V_{SS}	L07	RSVD
C12	V_{DDA_33}	G09	V_{SS}	L08	V_{DD_33}
C13	REFCLK+	G11	V_{SSA}	L09	V_{SS}
C14	REFCLK−	G12	V_{SSA}	L10	RSVD
D01	$\overline{SERR}$	G13	TXN	L11	V_{SS}
D02	PAR	G14	TXP	L12	$\overline{PME}$
D03	$\overline{PERR}$	H01	AD19	L13	$\overline{GRST}$

Table 2−2. ZHH Terminals Sorted Alphanumerically (Continued)

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
L14	RSVD	N01	$\overline{\text{INTB}}$	P02	$\overline{\text{LOCK}}$
M01	M66EN	N02	$\overline{\text{INTC}}$	P03	GPIO0 // $\overline{\text{CLKRUN}}$
M02	$\overline{\text{INTA}}$	N03	SERIRQ	P04	GPIO1 // PWR_OVER
M03	$\overline{\text{INTD}}$	N04	GPIO2	P05	GPIO4 // SCL
M04	GPIO3	N05	GPIO5 // SDA	P06	RSVD
M05	GPIO6	N06	RSVD	P07	RSVD
M06	RSVD	N07	RSVD	P08	RSVD
M07	RSVD	N08	RSVD	P09	RSVD
M08	V_{SS}	N09	RSVD	P10	RSVD
M09	V_{DD_33}	N10	RSVD	P11	RSVD
M10	V_{DD_33}	N11	RSVD	P12	RSVD
M11	V_{DD_33}	N12	V_{DD_15}	P13	V_{SSA}
M12	RSVD	N13	V_{SS}	P14	RSVD
M13	RSVD	N14	RSVD		
M14	RSVD	P01	$\overline{\text{PRST}}$		

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	VSSA	REFCLK–	REFCLK+	RSVD	RXN	VDD_15	TXP	$\overline{\text{PERST}}$	VDD_33_AUX	REF0_PCIE	$\overline{\text{WAKE}}$	$\overline{\text{PME}}$	RSVD	RSVD	14
13	$\overline{\text{GNT5}}$	CLKRUN_EN	VDDA_33	VDDA_15	RXP	VSS	TXN	VDDA_15	REF1_PCIE	VDD_15_ COMB	$\overline{\text{GRST}}$	RSVD	VDD_15	RSVD	13
12	$\overline{\text{GNT4}}$	$\overline{\text{REQ5}}$	EXT_ARB_EN	RSVD	VSSA	VSSA	VSSA	VDD_33_ COMB	VDD_33_ COM_IO	RSVD	RSVD	VSS	RSVD	VDD_33	12
11	CLKOUT4	$\overline{\text{REQ4}}$	CLKOUT6	REFCLK_SEL	VDDA_15	VSSA	VSSA	VDDA_15	VDDA_33	VSSA	VSSA	RSVD	RSVD	VSS	11
10	$\overline{\text{GNT2}}$	$\overline{\text{GNT3}}$	CLKOUT5	VDD_33							VDD_33	RSVD	RSVD	RSVD	10
9	CLKOUT2	$\overline{\text{REQ2}}$	$\overline{\text{REQ3}}$	CLKOUT3		VDD_33	VSS	VSS	VSS		VDD_33	VSS	RSVD	RSVD	9
8	CLKOUT1	$\overline{\text{REQ1}}$	$\overline{\text{GNT1}}$	VDD_15		VSS	VSS	VSS	VSS		VDD_33	VSS	RSVD	RSVD	8
7	AD0	$\overline{\text{REQ0}}$	$\overline{\text{GNT0}}$	CLKOUT0		VSS	VSS	VSS	VDD_33		RSVD	RSVD	RSVD	RSVD	7
6	AD1	AD2	AD3	VDD_33		VSS	VSS	VSS	VDD_33		GPIO7	GPIO6	RSVD	RSVD	6
5	AD4	AD5	AD6	AD8							VDD_15	GPIO2	GPIO5 // SDA	RSVD	5
4	AD7	VCCP	C/$\overline{\text{BE(0)}}$	VDD_33	C/$\overline{\text{BE(1)}}$	VDD_33	VDD_15	AD22	AD24	AD28	VDD_33	GPIO0 /CLKRUN	GPIO3	GPIO4/SCL	4
3	AD9	AD10	AD14	PAR	$\overline{\text{SERR}}$	$\overline{\text{TRDY}}$	AD17	AD20	AD25	AD29	CLK	$\overline{\text{INTD}}$	SERIRQ	GPIO1/ PWR_OVER	3
2	AD11	AD12	AD15	$\overline{\text{STOP}}$	$\overline{\text{IRDY}}$	C/$\overline{\text{BE(2)}}$	VCCP	AD21	C/$\overline{\text{BE(3)}}$	AD27	AD30	$\overline{\text{INTA}}$	$\overline{\text{INTC}}$	$\overline{\text{LOCK}}$	2
1		AD13	$\overline{\text{PERR}}$	$\overline{\text{DEVSEL}}$	$\overline{\text{FRAME}}$	AD16	AD18	AD19	AD23	AD26	AD31	M66EN	$\overline{\text{INTB}}$	$\overline{\text{PRST}}$	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 2–3. XIO2000A/XIO2000AI ZHC Microstar BGA™ Package (Bottom View)

Table 2−3. ZHC Terminal Names Sorted Alphanumerically

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
A02	AD11	D04	VDD_33	H02	AD21
A03	AD9	D05	AD8	H03	AD20
A04	AD7	D06	VDD_33	H04	AD22
A05	AD4	D07	CLKOUT0	H06	VSS
A06	AD1	D08	VDD_15	H07	VSS
A07	AD0	D09	CLKOUT3	H08	VSS
A08	CLKOUT1	D10	VDD_33	H09	VSS
A09	CLKOUT2	D11	REFCLK_SEL	H11	VDDA_15
A10	$\overline{\text{GNT2}}$	D12	RSVD	H12	VDD_33_COMB
A11	CLKOUT4	D13	VDDA_15	H13	VDDA_15
A12	$\overline{\text{GNT4}}$	D14	RSVD	H14	$\overline{\text{PERST}}$
A13	$\overline{\text{GNT5}}$	E01	$\overline{\text{FRAME}}$	J01	AD23
A14	VSSA	E02	$\overline{\text{IRDY}}$	J02	C/$\overline{\text{BE(3)}}$
B01	AD13	E03	$\overline{\text{SERR}}$	J03	AD25
B02	AD12	E04	C/$\overline{\text{BE[1]}}$	J04	AD24
B03	AD10	E11	VDDA_15	J06	VDD_33
B04	VCCP	E12	VSSA	J07	VDD_33
B05	AD5	E13	RXP	J08	VSS
B06	AD2	E14	RXN	J09	VSS
B07	$\overline{\text{REQ0}}$	F01	AD16	J11	VDDA_33
B08	$\overline{\text{REQ1}}$	F02	C/$\overline{\text{BE[2]}}$	J12	VDD_33_COMB_IO
B09	$\overline{\text{REQ2}}$	F03	$\overline{\text{TRDY}}$	J13	REF1_PCIE
B10	$\overline{\text{GNT3}}$	F04	VDD_33	J14	VDD_33_AUX
B11	$\overline{\text{REQ4}}$	F06	VSS	K01	AD26
B12	$\overline{\text{REQ5}}$	F07	VSS	K02	AD27
B13	CLKRUN_EN	F08	VSS	K03	AD29
B14	REFCLK−	F09	VDD_33	K04	AD28
C01	$\overline{\text{PERR}}$	F11	VSSA	K11	VSSA
C02	AD15	F12	VSSA	K12	RSVD
C03	AD14	F13	VSS	K13	VDD_15_COMB
C04	C/$\overline{\text{BE[0]}}$	F14	VDD_15	K14	REF0_PCIE
C05	AD6	G01	AD18	L01	AD31
C06	AD3	G02	VCCP	L02	AD30
C07	$\overline{\text{GNT0}}$	G03	AD17	L03	CLK
C08	$\overline{\text{GNT1}}$	G04	VDD_15	L04	VDD_33
C09	$\overline{\text{REQ3}}$	G06	VSS	L05	VDD_15
C10	CLKOUT5	G07	VSS	L06	GPIO7
C11	CLKOUT6	G08	VSS	L07	RSVD
C12	EXT_ARB_EN	G09	VSS	L08	VDD_33
C13	VDDA_33	G11	VSSA	L09	VDD_33
C14	REFCLK+	G12	VSSA	L10	VDD_33
D01	$\overline{\text{DEVSEL}}$	G13	TXN	L11	VSSA
D02	$\overline{\text{STOP}}$	G14	TXP	L12	RSVD
D03	PAR	H01	AD19	L13	$\overline{\text{GRST}}$

Figure 2−3. ZHC Terminal Names Sorted Alphanumarically (Continued)

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
L14	$\overline{\text{WAKE}}$	N01	$\overline{\text{INTB}}$	P02	LOCK
M01	M66EN	N02	$\overline{\text{INTC}}$	P03	GPIO1 // PWR_OVER
M02	$\overline{\text{INTA}}$	N03	SERIRQ	P04	GPIO4 // SCL
M03	$\overline{\text{INTD}}$	N04	GPIO3	P05	RSVD
M04	GPIO0 // $\overline{\text{CLKRUN}}$	N05	GPIO5 // SDA	P06	RSVD
M05	GPIO2	N06	RSVD	P07	RSVD
M06	GPIO6	N07	RSVD	P08	RSVD
M07	RSVD	N08	RSVD	P09	RSVD
M08	VSS	N09	RSVD	P10	RSVD
M09	VSS	N10	RSVD	P11	VSS
M10	RSVD	N11	RSVD	P12	VDD_33
M11	RSVD	N12	RSVD	P13	RSVD
M12	VSS	N13	VDD_15	P14	RSVD
M13	RSVD	N14	RSVD		
M14	$\overline{\text{PME}}$	P01	$\overline{\text{PRST}}$		

Table 2−4. XIO2000A/XIO2000AI Signal Names Sorted Alphabetically

SIGNAL NAME	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	SIGNAL NAME	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #
AD0	A07	A07	A07	CLKOUT5	A13	C10	B11
AD1	B07	A06	D06	CLKOUT6	B14	C11	A13
AD2	C07	B06	A06	CLKRUN_EN	B15	B13	B13
AD3	D07	C06	C06	DEVSEL	F01	D01	E02
AD4	A06	A05	B06	EXT_ARB_EN	A15	C12	B12
AD5	B06	B05	A05	FRAME	G01	E01	F01
AD6	A05	C05	B05	GNT0	A08	C07	C07
AD7	B05	A04	C05	GNT1	A09	C08	C08
AD8	C04	D05	C04	GNT2	A10	A10	B09
AD9	A03	A03	A03	GNT3	C11	B10	C10
AD10	B03	B03	B03	GNT4	C12	A12	D11
AD11	A02	A02	A02	GNT5	A14	A13	C11
AD12	B01	B02	B02	GPIO0 // CLKRUN	T05	M04	P03
AD13	C02	B01	B01	GPIO1 // PWR_OVRD	U05	P03	P04
AD14	C01	C03	C03	GPIO2	T06	M05	N04
AD15	D02	C02	C02	GPIO3	U06	N04	M04
AD16	H03	F01	F03	GPIO4 // SCL	R07	P04	P05
AD17	H02	G03	G02	GPIO5 // SDA	T07	N05	N05
AD18	J03	G01	G03	GPIO6	U07	M06	M05
AD19	J02	H01	H01	GPIO7	U08	L06	L06
AD20	K01	H03	H03	GRST	N17	L13	L13
AD21	K02	H02	H02	INTA	R02	M02	M02
AD22	K03	H04	H04	INTB	T01	N01	N01
AD23	L01	J01	J01	INTC	U02	N02	N02
AD24	L03	J04	J03	INTD	T03	M03	M03
AD25	L04	J03	J04	IRDY	G02	E02	E04
AD26	M01	K01	K01	LOCK	U04	P02	P02
AD27	M02	K02	K02	M66EN	R01	M01	M01
AD28	N01	K04	K03	PAR	E02	D03	D02
AD29	N02	K03	L04	PERR	F03	C01	D03
AD30	P01	L02	L02	PERST	J17	H14	H12
AD31	P02	L01	L01	PME	M15	M14	L12
C/BE[0]	B04	C04	B04	PRST	U03	P01	P01
C/BE[1]	D01	E04	C01	REF0_PCIE	L16	K14	J14
C/BE[2]	H01	F02	F02	REF1_PCIE	L17	J13	J13
C/BE[3]	L02	J02	J02	REFCLK_SEL	A16	D11	A14
CLK	P03	L03	L03	REFCLK−	C16	B14	C14
CLKOUT0	C08	D07	D07	REFCLK+	C17	C14	C13
CLKOUT1	B09	A08	B08	REQ0	B08	B07	B07
CLKOUT2	B10	A09	A09	REQ1	C09	B08	A08
CLKOUT3	A11	D09	D10	REQ2	C10	B09	C09
CLKOUT4	A12	A11	B10	REQ3	B11	C09	A10

Table 2−4. XIO2000A/XIO2000AI Signal Names Sorted Alphabetically (Continued)

SIGNAL NAME	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	SIGNAL NAME	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #
$\overline{\text{REQ4}}$	B12	B11	A11	$V_{DD_15_COMB}$	M17	K13	K13
$\overline{\text{REQ5}}$	B13	B12	A12	V_{DD_33}	C06	D04	D04
RSVD	D16	D12	D13	V_{DD_33}	C13	D06	D05
RSVD	D17	D14	D14	V_{DD_33}	D10	D10	D09
RSVD	N15	K12	L07	V_{DD_33}	E03	F04	F04
RSVD	N16	L07	L10	V_{DD_33}	H04	F09	F09
RSVD	P16	L12	L14	V_{DD_33}	M03	J06	J06
RSVD	P17	M07	M14	V_{DD_33}	P09	J07	J07
RSVD	R08	M10	M06	V_{DD_33}	P10	L04	K04
RSVD	R09	M11	P07	V_{DD_33}	P11	L08	L08
RSVD	R16	M13	N14	V_{DD_33}	R05	L09	M09
RSVD	T08	N06	M12	V_{DD_33}	R14	L10	M10
RSVD	T09	N07	M07	V_{DD_33}	T13	P12	M11
RSVD	T10	N08	M13	$V_{DD_33_AUX}$	K14	J14	J12
RSVD	T11	N09	N06	$V_{DD_33_COMB}$	K16	H12	H14
RSVD	T12	N10	N08	$V_{DD_33_COMBIO}$	L14	J12	K12
RSVD	T14	N11	N09	V_{DDA_15}	F17	D13	E11
RSVD	T15	N12	N10	V_{DDA_15}	G15	E11	F12
RSVD	T17	N14	N11	V_{DDA_15}	J14	H11	H11
RSVD	U09	P05	P06	V_{DDA_15}	J15	H13	H13
RSVD	U10	P06	N07	V_{DDA_33}	D15	C13	C12
RSVD	U11	P07	P08	V_{DDA_33}	K15	J11	J11
RSVD	U12	P08	P09	V_{SS}	C05	F06	F06
RSVD	U13	P09	P10	V_{SS}	C14	F07	F07
RSVD	U14	P10	P11	V_{SS}	D03	F08	F08
RSVD	U15	P13	P12	V_{SS}	D08	F13	F13
RSVD	U16	P14	P14	V_{SS}	D11	G06	G06
RXN	E16	E14	E13	V_{SS}	G04	G07	G07
RXP	E17	E13	E14	V_{SS}	G17	G08	G08
SERIRQ	T04	N03	N03	V_{SS}	K04	G09	G09
$\overline{\text{SERR}}$	E01	E03	D01	V_{SS}	K17	H06	H06
$\overline{\text{STOP}}$	F02	D02	E03	V_{SS}	N03	H07	H07
$\overline{\text{TRDY}}$	G03	F03	E01	V_{SS}	P08	H08	H08
TXN	H16	G13	G13	V_{SS}	R04	H09	H09
TXP	H17	G14	G14	V_{SS}	R06	J08	J08
V_{CCP}	A04	B04	A04	V_{SS}	R10	J09	J09
V_{CCP}	J01	G02	G01	V_{SS}	R11	M08	L09
V_{DD_15}	D09	D08	D08	V_{SS}	R12	M09	L11
V_{DD_15}	H14	F14	F14	V_{SS}	R13	M12	M08
V_{DD_15}	J04	G04	G04	V_{SS}	R17	P11	N13
V_{DD_15}	P07	L05	L05	V_{SS}	G07		
V_{DD_15}	P15	N13	N12	V_{SS}	G08		

Table 2−4. XIO2000A/XIO2000AI Signal Names Sorted Alphabetically (Continued)

SIGNAL NAME	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	SIGNAL NAME	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #
V_{SS}	G09			V_{SS}	K11		
V_{SS}	G10			V_{SS}	L07		
V_{SS}	G11			V_{SS}	L08		
V_{SS}	H07			V_{SS}	L09		
V_{SS}	H08			V_{SS}	L10		
V_{SS}	H09			V_{SS}	L11		
V_{SS}	H10			V_{SSA}	B17	A14	B14
V_{SS}	H11			V_{SSA}	E15	E12	D12
V_{SS}	J07			V_{SSA}	F15	F11	E12
V_{SS}	J08			V_{SSA}	F16	F12	F11
V_{SS}	J09			V_{SSA}	G14	G11	G11
V_{SS}	J10			V_{SSA}	G16	G12	G12
V_{SS}	J11			V_{SSA}	H15	K11	K11
V_{SS}	K07			V_{SSA}	J16	L11	P13
V_{SS}	K08			V_{SSA}	L15		
V_{SS}	K09			$\overline{WAKE}$	M16	L14	K14
V_{SS}	K10						

2.8 Terminal Descriptions

Table 2−5 through Table 2−12 give a description of the terminals. These terminals are grouped in tables by functionality. Each table includes the terminal name, terminal number, I/O type, and terminal description.

The following list describes the different input/output cell types that appear in the terminal description tables:

- HS DIFF IN = High speed differential input.
- HS DIFF OUT = High speed differential output.
- PCI BUS = PCI bus 3-state bidirectional buffer with 3.3-V or 5.0-V clamp rail.
- LV CMOS = 3.3-V low voltage CMOS input or output with 3.3-V clamp rail.
- BIAS = Input/output terminals that generate a bias voltage to determine a driver’s operating current.
- Feed through = these terminals connect directly to macros within the part and not through an input or output cell.
- PWR = Power terminal
- GND = Ground terminal

Table 2−5. Power Supply Terminals

SIGNAL	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	EXTERNAL PARTS	DESCRIPTION
V_{CCP}	A04, J01	B04, G02	A04, G01	PWR	Bypass capacitors	5.0-V or 3.3-V PCI bus clamp voltage to set maximum I/O voltage tolerance of the secondary PCI bus signals
V_{DD_15}	D09, H14, J04, P07, P15	D08, F14, G04, L05, N13	D08, F14, G04, L05, N12	PWR	Bypass capacitors	1.5-V digital core power terminals
V_{DDA_15}	F17, J14, J15, G15	D13, E11, H11, H13	E11, F12, H11, H13	PWR	Pi filter	1.5-V analog power terminal
V_{DD_33}	C06, C13, D10, E03, H04, M03, P09, P10, P11, R05, R14, T13	D04, D06, D10, F04, F09, J06, J07, L04, L08, L09, L10, P12	D04, D05, D09, F04, F09, J06, J07, K04, L08, M09, M10, M11	PWR	Bypass capacitors	3.3-V digital I/O power terminals
$V_{DD_33_AUX}$	K14	J14	J12	PWR	Bypass capacitors	3.3-V auxiliary power terminal **Note:** This terminal is connected to V_{SS} through a pulldown resistor if no auxiliary supply is present.
V_{DDA_33}	D15, K15	C13, J11	C12, J11	PWR	Pi filter	3.3-V analog power terminal

Table 2−6. Ground Terminals

SIGNAL	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	DESCRIPTION
V_{SS}	C05, C14, D03, D08, D11, G04, G17, K04, K17, N03, P08, R04, R06, R10, R11, R12, R13, R17	F06, F07, F08, F13, G06, G07, G08, G09, H06, H07, H08, H09, J08, J09, M08, M09, M12, P11	F06, F07, F08, F13, G06, G07, G08, G09, H06, H07, H08, H09, J08, J09, L09, L11, M08, N13	GND	Digital ground terminals
V_{SS}	G07, G08, G09, G10, G11, H07, H08, H09, H10, H11, J07, J08, J09, J10, J11, K07, K08, K09, K10, K11, L07, L08, L09, L10, L11			GND	Ground terminals for thermally-enhanced package
V_{SSA}	B17, E15, F15, F16, G14, G16, H15, J16, L15	A14, E12, F11, F12, G11, G12, K11, L11	B14, D12, E12, F11, G11, G12, K11, P13	GND	Analog ground terminal

Table 2−7. Combined Power Outputs

SIGNAL	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	EXTERNAL PARTS	DESCRIPTION
$V_{DD_15_COMB}$	M17	K13	K13	Feed through	Bypass capacitors	Internally-combined 1.5-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 1.5-V circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power to other devices.
$V_{DD_33_COMB}$	K16	H12	H14	Feed through	Bypass capacitors	Internally-combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power to other devices.
$V_{DD_33_COMBIO}$	L14	J12	K12	Feed through	Bypass capacitors	Internally-combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V input/output circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power to other devices.

Table 2−8. PCI Express Terminals

SIGNAL	GZZ/ ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
$\overline{\text{PERST}}$	J17	H14	H12	I	LV CMOS	$V_{DD_33_COMBIO}$	–	PCI Express reset input. The $\overline{\text{PERST}}$ signal identifies when the system power is stable and generates an internal power on reset. **Note:** The $\overline{\text{PERST}}$ input buffer has hysteresis.
REF0_PCIE REF1_PCIE	L16 L17	K14 J13	J14 J13	I/O	BIAS	–	External resistor	External reference resistor + and − terminals for setting TX driver current. An external resistor is connected between terminals L16 and L17.
RXP RXN	E17 E16	E13 E14	E14 E13	DI	HS DIFF IN	V_{SS}	–	High-speed receive pair. RXP and RXN comprise the differential receive pair for the single PCI Express lane supported.
TXP TXN	H17 H16	G14 G13	G14 G13	DO	HS DIFF OUT	V_{DD_15}	Series capacitors	High-speed transmit pair. TXP and TXN comprise the differential transmit pair for the single PCI Express lane supported.
$\overline{\text{WAKE}}$	M16	L14	K14	O	LV CMOS	$V_{DD_33_COMBIO}$	–	Wake is an active low signal that is driven low to reactivate the PCI Express link hierarchy's main power rails and reference clocks. **Note:** Since $\overline{\text{WAKE}}$ is an open-drain output buffer, a system side pullup resistor is required.

Table 2−9. Clock Terminals

SIGNAL	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
REFCLK_SEL	A16	D11	A14	I	LV CMOS	V_{DD_33}	Pullup or pulldown resistor	Reference clock select. This terminal selects the reference clock input. 0 = 100-MHz differential common reference clock used. 1 = 125-MHz single-ended, reference clock used.
REFCLK+	C17	C14	C13	DI	HS DIFF IN	V_{DD_33}	−	Reference clock. REFCLK+ and REFCLK− comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, use the REFCLK+ input.
REFCLK−	C16	B14	C14	DI	HS DIFF IN	V_{DD_33}	Capacitor to V_{SS} for single-ended mode	Reference clock. REFCLK+ and REFCLK− comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, attach a capacitor from REFCLK− to V_{SS}.
CLK	P03	L03	L03	I	PCI Bus	V_{CCP}	−	PCI clock input. This is the clock input to the PCI bus core.
CLKOUT0 CLKOUT1 CLKOUT2 CLKOUT3 CLKOUT4 CLKOUT5 CLKOUT6	C08 B09 B10 A11 A12 A13 B14	D07 A08 A09 D09 A11 C10 C11	D07 B08 A09 D10 B10 B11 A13	O	PCI Bus	V_{CCP}	−	PCI clock outputs. These clock outputs are used to clock the PCI bus. If the bridge PCI bus clock outputs are used, then CLKOUT6 must be connected to the CLK input.

Table 2−10. PCI System Terminals

SIGNAL	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	P02 P01 N02 N01 M02 M01 L04 L03 L01 K03 K02 K01 J02 J03 H02 H03 D02 C01 C02 B01 A02 B03 A03 C04 B05 A05 B06 A06 D07 C07 B07 A07	L01 L02 K03 K04 K02 K01 J03 J04 J01 H04 H02 H03 H01 G01 G03 F01 C02 C03 B01 B02 A02 B03 A03 D05 A04 C05 B05 A05 C06 B06 A06 A07	L01 L02 L04 K03 K02 K01 J04 J03 J01 H04 H02 H03 H01 G03 G02 F03 C02 C03 B01 B02 A02 B03 A03 C04 C05 B05 A05 B06 C06 A06 D06 A07	I/O	PCI Bus	V_{CCP}	−	PCI address data lines
C/$\overline{BE[3]}$ C/$\overline{BE[2]}$ C/$\overline{BE[1]}$ C/$\overline{BE[0]}$	L02 H01 D01 B04	J02 F02 E04 C04	J02 F02 C01 B04	I/O	PCI Bus	V_{CCP}	−	PCI command byte enables
$\overline{DEVSEL}$	F01	D01	E02	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI device select
$\overline{FRAME}$	G01	E01	F01	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI frame
$\overline{GNT5}$ $\overline{GNT4}$ $\overline{GNT3}$ $\overline{GNT2}$ $\overline{GNT1}$ $\overline{GNT0}$	A14 C12 C11 A10 A09 A08	A13 A12 B10 A10 C08 C07	C11 D11 C10 B09 C08 C07	O	PCI Bus	V_{CCP}	−	PCI grant outputs. These signals are used for arbitration when the PCI bus is the secondary bus and an external arbiter is not used. $\overline{GNT0}$ is used as the $\overline{REQ}$ for the bridge when an external arbiter is used.
$\overline{INTA}$ $\overline{INTB}$ $\overline{INTC}$ $\overline{INTD}$	R02 T01 U02 T03	M02 N01 N02 M03	M02 N01 N02 M03	I	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI interrupts A−D. These signals are interrupt inputs to the bridge on the secondary PCI bus.
$\overline{IRDY}$	G02	E02	E04	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI initiator ready

Table 2−10. PCI System Terminals (Continued)

SIGNAL	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
PAR	E02	D03	D02	I/O	PCI Bus	V_{CCP}	−	PCI bus parity
$\overline{\text{PERR}}$	F03	C01	D03	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI parity error
$\overline{\text{PME}}$	M15	M14	L12	I	LV CMOS	$V_{DD_33_COMBIO}$	Pullup resistor per PCI spec	PCI power management event. This terminal may be used to detect $\overline{\text{PME}}$ events from a PCI device on the secondary bus. **Note:** The $\overline{\text{PME}}$ input buffer has hysteresis.
$\overline{\text{REQ5}}$ $\overline{\text{REQ4}}$ $\overline{\text{REQ3}}$ $\overline{\text{REQ2}}$ $\overline{\text{REQ1}}$ $\overline{\text{REQ0}}$	B13 B12 B11 C10 C09 B08	B12 B11 C09 B09 B08 B07	A12 A11 A10 C09 A08 B07	I	PCI Bus	V_{CCP}	If unused, a weak pullup resistor per PCI spec	PCI request inputs. These signals are used for arbitration on the secondary PCI bus when an external arbiter is not used. $\overline{\text{REQ0}}$ is used as the $\overline{\text{GNT}}$ for the bridge when an external arbiter is used.
$\overline{\text{PRST}}$	U03	P01	P01	O	PCI Bus	V_{CCP}	−	PCI reset. This terminal is an output to the secondary PCI bus.
$\overline{\text{SERR}}$	E01	E03	D01	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI system error
$\overline{\text{STOP}}$	F02	D02	E03	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI stop
$\overline{\text{TRDY}}$	G03	F03	E01	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	PCI target ready

Table 2−11. Reserved Terminals

SIGNAL	GZZ/ZZZ BALL #	ZHC BALL #	ZHH BALL #	I/O TYPE	DESCRIPTION
RSVD	N15, N16, P16, R08, T08, T10, T11, T12, T14, T15, T17, U09, U11, U12, U13, U14, U15, U16	K12, L07, L12, M10, M11, M13, N06, N08, N09, N10, N11, P05, P06, P08, P09, P10, P13, P14	L07, L10, L14, M06, M12, M13, N06, N08, N09, N10, N11, P06, P08, P09, P10, P11, P12, P14	O	Reserved, do not connect to external signals.
RSVD	R16	N12	N14	I	Must be connected to V_{DD_33}.
RSVD	D16, D17, P17, R09, T09, U10	D12, D14, M07, N07, N14, P07	D13, D14, M14, P07, M07, N07	I	Must be connected to V_{SS}.

Table 2−12. Miscellaneous Terminals

SIGNAL	GZZ/ ZZZ BALL	ZHC BALL	ZHH BALL	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
CLKRUN_EN	B15	B13	B13	I	LV CMOS	V_{DD_33}	Optional pullup resistor	Clock run enable 0 = Clock run support disabled 1 = Clock run support enabled **Note:** The CLKRUN_EN input buffer has an internal active pulldown.
EXT_ARB_EN	A15	C12	B12	I	LV CMOS	V_{DD_33}	Optional pullup resistor	External arbiter enable 0 = Internal arbiter enabled 1 = External arbiter enabled **Note:** The EXT_ARB_EN input buffer has an internal active pulldown.
GPIO0 // CLKRUN	T05	M04	P03	I/O	LV CMOS	V_{DD_33}	Optional pullup resistor	General-purpose I/O 0/clock run. This terminal functions as a GPIO controlled by bit 0 (GPIO0_DIR) in the GPIO control register (see Section 4.59) or the clock run terminal. This terminal is used as clock run input when the bridge is placed in clock run mode. **Note:** In clock run mode, an external pullup resistor is required to prevent the CLKRUN signal from floating. **Note:** This terminal has an internal active pullup resistor.
GPIO1 // PWR_OVRD	U05	P03	P04	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 1/power override. This terminal functions as a GPIO controlled by bit 1 (GPIO1_DIR) in the GPIO control register (see Section 4.59) or the power override output terminal. GPIO1 becomes PWR_OVRD when bits 22:20 (POWER_OVRD) in the general control register are set to 001b or 011b (see Section 4.65). **Note:** This terminal has an internal active pullup resistor.
GPIO2	T06	M05	N04	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 2. This terminal functions as a GPIO controlled by bit 2 (GPIO2_DIR) in the GPIO control register (see Section 4.59). **Note:** When PERST is deasserted, this terminal must be a 1b to enable the PCI Express 1.0a compatibility mode. **Note:** This terminal has an internal active pullup resistor.
GPIO3	U06	N04	M04	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 3. This terminal functions as a GPIO controlled by bit 3 (GPIO3_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
GPIO4 // SCL	R07	P04	P05	I/O	LV CMOS	V_{DD_33}	Optional pullup resistor	GPIO4 or serial-bus clock. This terminal functions as serial-bus clock if a pullup resistor is detected on SDA. If a pulldown resistor is detected on SDA, this terminal functions as GPIO4. **Note:** In serial-bus mode, an external pullup resistor is required to prevent the SCL signal from floating. **Note:** This terminal has an internal active pullup resistor.

Table 2−12. Miscellaneous Terminals (Continued)

SIGNAL	GZZ ZZZ BALL	ZHC BALL	ZHH BALL	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
GPIO5 // SDA	T07	N05	N05	I/O	LV CMOS	V_{DD_33}	Pullup or Pulldown resistor	GPIO5 or serial-bus data. This terminal functions as serial-bus data if a pullup resistor is detected on SDA. If a pulldown resistor is detected on SDA, this terminal functions as GPIO5. **Note:** In serial-bus mode, an external pullup resistor is required to prevent the SDA signal from floating.
GPIO6	U07	M06	M05	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 6. This terminal functions as a GPIO controlled by bit 6 (GPIO6_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
GPIO7	U08	L06	L06	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 7. This terminal functions as a GPIO controlled by bit 7 (GPIO7_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
$\overline{\text{GRST}}$	N17	L13	L13	I	LV CMOS	$V_{DD_33_COMBIO}$	–	Global reset input. Asynchronously resets all logic in device, including sticky bits and power management state machines. **Note:** The $\overline{\text{GRST}}$ input buffer has both hysteresis and an internal active pullup.
$\overline{\text{LOCK}}$	U04	P02	P02	I/O	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	This terminal functions as PCI $\overline{\text{LOCK}}$ when bit 12 (LOCK_EN) is set in the general control register (see Section 4.65). **Note:** In lock mode, an external pullup resistor is required to prevent the $\overline{\text{LOCK}}$ signal from floating.
M66EN	R01	M01	M01	I	PCI Bus	V_{CCP}	Pullup resistor per PCI spec	66-MHz mode enable 0 = Secondary PCI bus and clock outputs operate at 33 MHz 1 = Secondary PCI bus and clock outputs operate at 66 MHz **Note:** If the PCI bus clock is always 33 MHz, then this terminal is connected to V_{SS}. **Note:** The XIO2000AI industrial temperature device does not support 66 MHz operation so for the XIO2000AI, this pin must be grounded for proper operation.
SERIRQ	T04	N03	N03	I/O	PCI Bus	V_{CCP}	Pullup or pulldown resistor	Serial IRQ interface. This terminal functions as a serial IRQ interface if a pullup is detected when $\overline{\text{PERST}}$ is deasserted. If a pulldown is detected, then the serial IRQ interface is disabled.

3 Feature/Protocol Descriptions

This chapter provides a high-level overview of all significant device features. Figure 3−1 shows a simplified block diagram of the basic architecture of the PCI-Express to PCI Bridge. The top of the diagram is the PCI Express interface and the PCI bus interface is located at the bottom of the diagram.

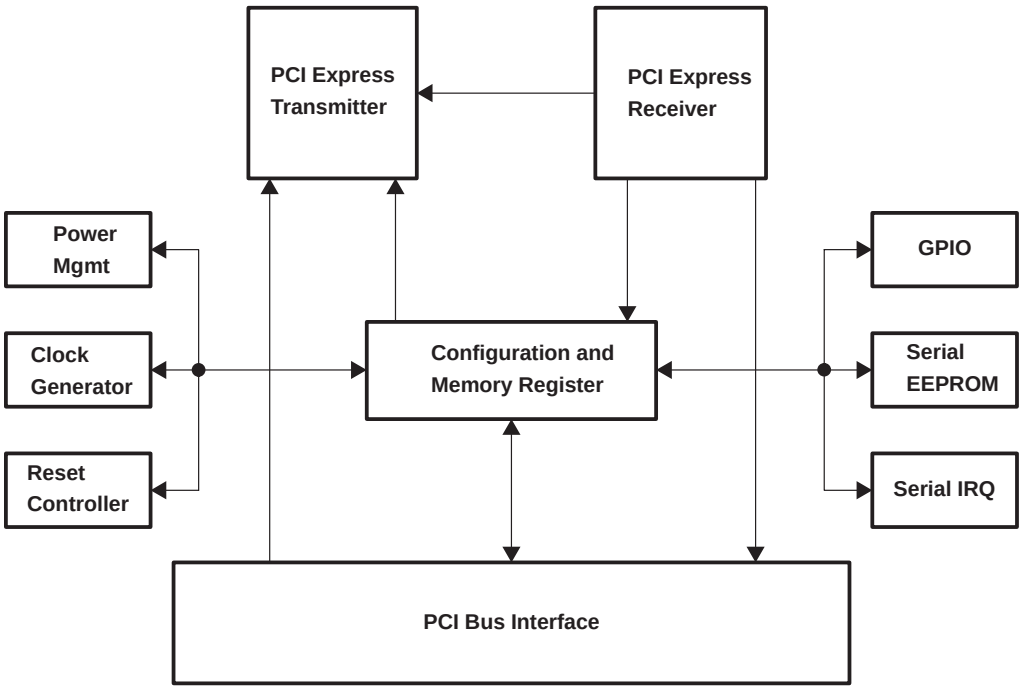


Figure 3−1. XIO2000A Block Diagram

3.1 Power-Up/-Down Sequencing

The bridge contains both 1.5-V and 3.3-V power terminals. In addition, a V_{AUX} supply exists to support the $D3_{cold}$ state. The clamping voltage (V_{CCP}) can be either 3.3-V or 5.0-V, depending on the PCI bus interface requirements. The following power-up and power-down sequences describe how power is applied to these terminals.

In addition, the bridge has three resets: $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, and an internal power-on reset. These resets are fully described in Section 3.2. The following power-up and power-down sequences describe how $\overline{\text{PERST}}$ is applied to the bridge.

The application of the PCI Express reference clock (REFCLK) is important to the power-up/-down sequence and is included in the following power-up and power-down descriptions.

3.1.1 Power-Up Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Apply 1.5-V and 3.3-V voltages.
3. Apply V_{CCP} clamp voltage.
4. Apply a stable PCI Express reference clock.
5. To meet PCI Express specification requirements, $\overline{\text{PERST}}$ cannot be deasserted until the following two delay requirements are satisfied:
   - Wait a minimum of 100 µs after applying a stable PCI Express reference clock. The 100-µs limit satisfies the requirement for stable device clocks by the deassertion of $\overline{\text{PERST}}$.
   - Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the deassertion of $\overline{\text{PERST}}$.

See the power-up sequencing diagram in Figure 3−2.

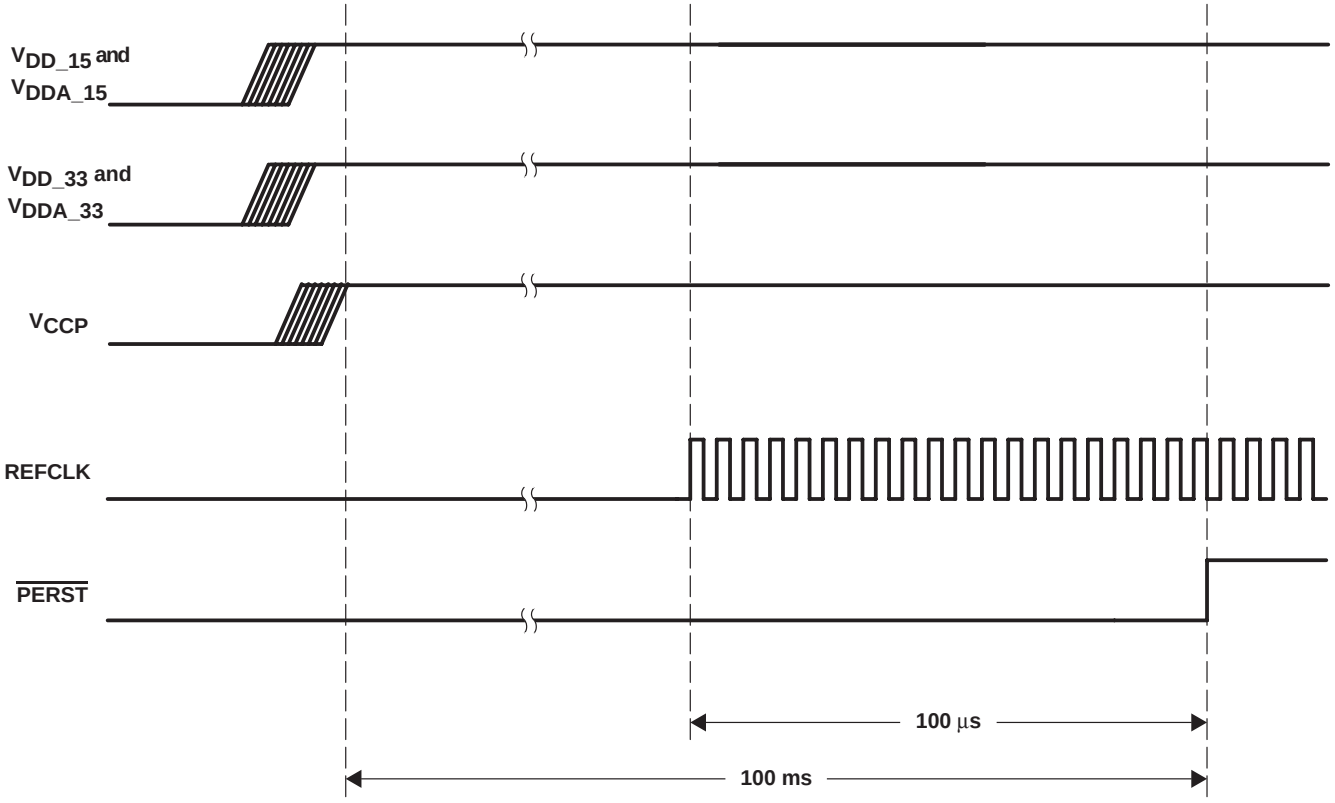


Figure 3−2. Power-Up Sequence

3.1.2 Power-Down Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Remove the reference clock.
3. Remove V_{CCP} clamp voltage.
4. Remove 3.3-V and 1.5-V voltages.

Please see the power-down sequencing diagram in Figure 3−3. If the $V_{DD_33_AUX}$ terminal is to remain powered after a system shutdown, then the bridge power-down sequence is exactly the same as shown in Figure 3−3.

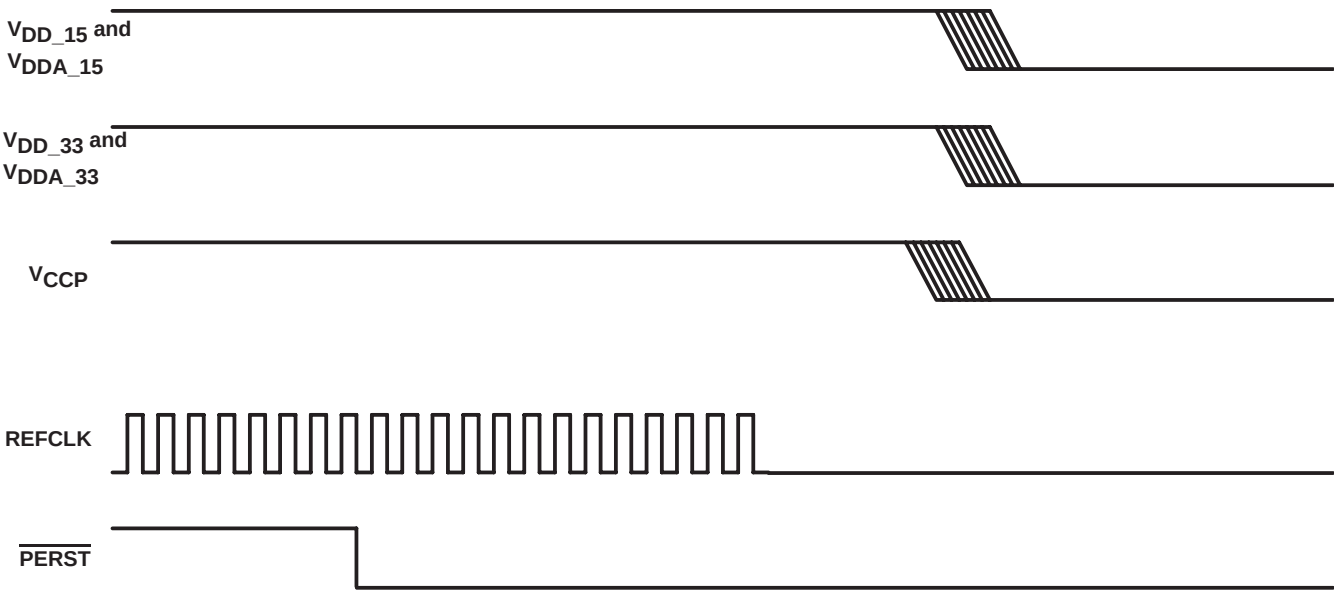


Figure 3−3. Power-Down Sequence

3.2 Bridge Reset Features

There are five bridge reset options that include internally-generated power-on reset, resets generated by asserting input terminals, and software-initiated resets that are controlled by sending a PCI Express hot reset or setting a configuration register bit. Table 3−1 identifies these reset sources and describes how the bridge responds to each reset.

Table 3−1. Bridge Reset Options

RESET OPTION	XIO2000A FEATURE	RESET RESPONSE
Bridge internally-generated power-on reset	During a power-on cycle, the bridge asserts an internal reset and monitors the $V_{DD_15_COMB}$ (M17) terminal. When this terminal reaches 90% of the nominal input voltage specification, power is considered stable. After stable power, the bridge monitors the PCI Express reference clock (REFCLK) and waits 10 µs after active clocks are detected. Then, internal power-on reset is deasserted.	When the internal power-on reset is asserted, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the bridge asserts PCI bus reset ($\overline{PRST}$).
Global reset input $\overline{GRST}$ (N17)	When $\overline{GRST}$ is asserted low, an internal power-on reset occurs. This reset is asynchronous and functions during both normal power states and V_{AUX} power states.	When $\overline{GRST}$ is asserted low, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the bridge asserts PCI bus reset ($\overline{PRST}$). When the rising edge of $\overline{GRST}$ occurs, the bridge samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The bridge starts link training within 80 ms after $\overline{GRST}$ is deasserted.
PCI Express reset input $\overline{PERST}$ (J17)	This bridge input terminal is used by an upstream PCI Express device to generate a PCI Express reset and to signal a system power good condition. When $\overline{PERST}$ is asserted low, the bridge generates an internal PCI Express reset as defined in the PCI Express specification. When $\overline{PERST}$ transitions from low to high, a system power good condition is assumed by the bridge. **Note:** The system must assert $\overline{PERST}$ before power is removed, before REFCLK is removed, or before REFCLK becomes unstable.	When $\overline{PERST}$ is asserted low, all control register bits that are not sticky are reset. Within the configuration register maps, the sticky bits are indicated by the ☆ symbol. Also, all state machines that are not associated with sticky functionality or V_{AUX} power management are reset. In addition, the bridge asserts PCI bus reset ($\overline{PRST}$). When the rising edge of $\overline{PERST}$ occurs, the bridge samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The bridge starts link training within 80 ms after $\overline{PERST}$ is deasserted.
PCI Express training control hot reset	The bridge responds to a training control hot reset received on the PCI Express interface. After a training control hot reset, the PCI Express interface enters the DL_DOWN state.	In the DL_DOWN state, all remaining configuration register bits and state machines are reset. All remaining bits exclude sticky bits and EEPROM loadable bits. All remaining state machines exclude sticky functionality, EEPROM functionality, and V_{AUX} power management. Within the configuration register maps, the sticky bits are indicated by the ☆ symbol and the EEPROM loadable bits are indicated by the † symbol. In addition, the bridge asserts PCI bus reset ($\overline{PRST}$).
PCI bus reset $\overline{PRST}$ (U03)	System software has the ability to assert and deassert the $\overline{PRST}$ terminal on the secondary PCI bus interface. This terminal is the PCI bus reset.	When bit 6 (SRST) in the bridge control register at offset 3Eh (see Section 4.29) is asserted, the bridge asserts the $\overline{PRST}$ terminal. A 0 in the SRST bit deasserts the $\overline{PRST}$ terminal.

3.3 PCI Express Interface

3.3.1 External Reference Clock

The bridge requires either a differential, 100-MHz common clock reference or a single-ended, 125-MHz clock reference. The selected clock reference must meet all *PCI Express Electrical Specification* requirements for frequency tolerance, spread spectrum clocking, and signal electrical characteristics.

If the REFCLK_SEL (A16) input is connected to V_{SS}, then a differential, 100-MHz common clock reference is expected by the bridge. If the A16 terminal is connected to V_{DD_33}, then a single-ended, 125-MHz clock reference is expected by the bridge.

When the single-ended, 125-MHz clock reference option is enabled, the single-ended clock signal is connected to the REFCLK+ (C17) terminal. The REFCLK− (C16) terminal is connected to one side of an external capacitor with the other side of the capacitor connected to V_{SS}.

When using a single-ended reference clock, care must be taken to ensure interoperability from a system jitter standpoint. The *PCI Express Base Specification* does not ensure interoperability when using a differential reference clock commonly used in PC applications along with a single-ended clock in a noncommon clock architecture. System jitter budgets will have to be verified to ensure interoperability. See the *PCI Express Jitter and BER White Paper* from the PCI-SIG.

3.3.2 Beacon

The bridge supports the PCI Express in-band beacon feature. Beacon is driven on the upstream PCI Express link by the bridge to request the reapplication of main power when in the L2 link state. To enable the beacon feature, bit 10 (BEACON_ENABLE) in the general control register at offset D4h is asserted. See Section 4.65, *General Control Register*, for details.

If the bridge is in the L2 link state and beacon is enabled, when a secondary PCI bus device asserts $\overline{\text{PME}}$, then the bridge outputs the beacon signal on the upstream PCI Express link. The beacon signal frequency is approximately 500 kHz ± 50% with a differential peak-to-peak amplitude of 500 mV and no de-emphasis. Once the beacon is activated, the bridge continues to send the beacon signal until main power is restored as indicated by $\overline{\text{PERST}}$ going inactive. At this time, the beacon signal is deactivated.

3.3.3 Wake

The bridge supports the PCI Express sideband $\overline{\text{WAKE}}$ feature. $\overline{\text{WAKE}}$ is an active low signal driven by the bridge to request the reapplication of main power when in the L2 link state. Since $\overline{\text{WAKE}}$ is an open-collector output, a system-side pullup resistor is required to prevent the signal from floating.

When the bridge is in the L2 link state and $\overline{\text{PME}}$ is received from a device on the secondary PCI bus, the $\overline{\text{WAKE}}$ signal is asserted low as a wakeup mechanism. Once $\overline{\text{WAKE}}$ is asserted, the bridge drives the signal low until main power is restored as indicated by $\overline{\text{PERST}}$ going inactive. At this time, $\overline{\text{WAKE}}$ is deasserted.

3.3.4 Initial Flow Control Credits

The bridge flow control credits are initialized using the rules defined in the *PCI Express Base Specification*. Table 3−2 identifies the initial flow control credit advertisement for the bridge. The initial advertisement is exactly the same when a second virtual channel (VC) is enabled.

Table 3−2. Initial Flow Control Credit Advertisements

CREDIT TYPE	INITIAL ADVERTISEMENT
Posted request headers (PH)	8
Posted request data (PD)	128
Nonposted header (NPH)	4
Nonposted data (NPD)	4
Completion header (CPLH)	0 (infinite)
Completion data (CPLD)	0 (infinite)

3.3.5 PCI Express Message Transactions

PCI Express messages are both initiated and received by the bridge. Table 3−3 outlines message support within the bridge.

Table 3−3. Messages Supported by the Bridge

MESSAGE	SUPPORTED	BRIDGE ACTION
Assert_INTx	Yes	Transmitted upstream
Deassert_INTx	Yes	Transmitted upstream
PM_Active_State_Nak	Yes	Received and processed
PM_PME	Yes	Transmitted upstream
PME_Turn_Off	Yes	Received and processed
PME_TO_Ack	Yes	Transmitted upstream
ERR_COR	Yes	Transmitted upstream
ERR_NONFATAL	Yes	Transmitted upstream
ERR_FATAL	Yes	Transmitted upstream
Unlock	Yes	Received and processed
Set_Slot_Power_Limit	Yes	Received and processed
Hot plug messages	No	Discarded
Advanced switching messages	No	Discarded
Vendor defined type 0	No	Unsupported request
Vendor defined type 1	No	Discarded

All supported message transactions are processed per the *PCI Express Base Specification*.

3.4 PCI Bus Interface

3.4.1 I/O Characteristics

Figure 3−4 shows a 3-state bi-directional buffer that represents the I/O cell design for the PCI bus. Section 7.7, *Electrical Characteristics over Recommended Operating Conditions*, provides the electrical characteristics of the PCI bus I/O cell.

NOTE: The PCI bus interface on the bridge meets the ac specifications of the *PCI Local Bus Specification*. Additionally, PCI bus terminals (input or I/O) must be held high or low to prevent them from floating.

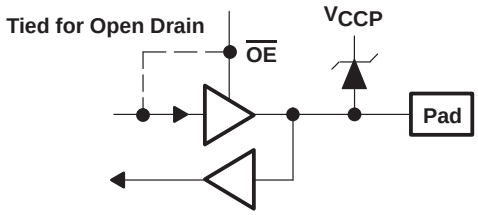


Figure 3−4. 3-State Bidirectional Buffer

3.4.2 Clamping Voltage

In the bridge, the PCI bus I/O drivers are powered from the V_{DD_33} power rail. Plus, the I/O driver cell is tolerant to input signals with 5.0-V peak-to-peak amplitudes.

For PCI bus interfaces operating at 66 MHz, all devices are required to output only 3.3-V peak-to-peak signal amplitudes. For PCI bus interfaces operating at 33-MHz, devices may output either 3.3-V or 5.0-V peak-to-peak signal amplitudes. The bridge accommodates both signal amplitudes.

Each PCI bus I/O driver cell has a clamping diode connected to the V_{CCP} voltage rail that protects the cell from excessive input voltage. If the PCI signaling is 3.3-V, then V_{CCP} (A04, J01) is connected to a 3.3-V power supply. If the PCI signaling is 5.0 V, then V_{CCP} (A04, J01) is connected to a 5.0-V power supply.

The PCI bus signals attached to the V_{CCP} clamping voltage are identified in the following list:

- In Table 2−9, *Clock Terminals*, the terminal names include CLK and CLKOUT6:0.
- In Table 2−10, *PCI System Terminals*, all terminal names except for $\overline{\text{PME}}$
- In Table 2−12, *Miscellaneous Terminals*, the terminal names include SERIRQ, M66EN, and $\overline{\text{LOCK}}$.

3.4.3 PCI Bus Clock Run

The bridge supports the clock run protocol as specified in the *PCI Mobile Design Guide*. When the clock run protocol is enabled, the bridge assumes the role of the central resource master.

To enable the clock run function, terminal B15 (CLKRUN_EN) is asserted high. Then, terminal T05 (GPIO0) is enabled as the $\overline{\text{CLKRUN}}$ signal. An external pullup resistor must be provided to prevent the $\overline{\text{CLKRUN}}$ signal from floating. To verify the operational status of the PCI bus clocks, bit 0 (SEC_CLK_STATUS) in the clock run status register at offset DAh (see Section 4.68) is read.

Since the bridge has several unique features associated with the PCI bus interface, the system designer must consider the following interdependencies between these features and the $\overline{\text{CLKRUN}}$ feature:

1. If the system designer chooses to generate the PCI bus clock externally, then the CLKRUN mode of the bridge must be disabled. The central resource function within the bridge only operates as a $\overline{\text{CLKRUN}}$ master and does not support the $\overline{\text{CLKRUN}}$ slave mode.
2. If the central resource function has stopped the PCI bus clocks, then the bridge still detects INTx state changes and will generate and send PCI Express messages upstream.
3. If the serial IRQ interface is enabled and the central resource function has stopped the PCI bus clocks, then any PCI bus device that needs to report an IRQ interrupt asserts $\overline{\text{CLKRUN}}$ to start the bus clocks.
4. When a PCI bus device asserts $\overline{\text{CLKRUN}}$, the central resource function turns on PCI bus clocks for a minimum of 512 cycles.
5. If the serial IRQ function detects an IRQ interrupt, then the central resource function keeps the PCI bus clocks running until the IRQ interrupt is cleared by software.
6. If the central resource function has stopped the PCI bus clocks and the bridge receives a downstream transaction that is forwarded to the PCI bus interface, then the bridge asserts $\overline{\text{CLKRUN}}$ to start the bus clocks.
7. The central resource function is reset by PCI bus reset ($\overline{\text{PRST}}$) assuring that clocks are present during PCI bus resets.

3.4.4 PCI Bus External Arbiter

The bridge supports an external arbiter for the PCI bus. Terminal A15 (EXT_ARB_EN), when asserted high, enables the use of an external arbiter.

When an external arbiter is enabled, $\overline{\text{GNT0}}$ is connected to the external arbiter as the $\overline{\text{REQ}}$ for the bridge. Likewise, $\overline{\text{REQ0}}$ is connected to the external arbiter as the $\overline{\text{GNT}}$ for the bridge.

All internal port arbitration features are disabled when an external arbiter is enabled. 128-phase, weighted round-robin (WRR) time-based arbitration, bus parking, arbiter time-out, tier select, and request masking modes have no effect if an external arbiter is enabled.

3.4.5 MSI Messages Generated from the Serial IRQ Interface

When properly configured, the bridge converts PCI bus serial IRQ interrupts into PCI Express message signaled interrupts (MSI). classic PCI configuration register space is provided to enable this feature. The following list identifies the involved configuration registers:

1. Command register at offset 04h, bit 2 (MASTER_ENB) is asserted (see Section 4.3).
2. MSI message control register at offset 62h, bits 0 (MSI_EN) and 6:4 (MM_EN) enable single and multiple MSI messages, respectively (see Section 4.38).
3. MSI message address register at offsets 64h and 68h specifies the message memory address. A nonzero address value in offset 68h initiates 64-bit addressing (see Section 4.40).
4. MSI message data register at offset 6Ch specifies the system interrupt message (see Section 4.41).
5. Serial IRQ mode control register at offset E0h specifies the serial IRQ bus format (see Section 4.72).
6. Serial IRQ edge control register at offset E2h selects either level or edge mode interrupts (see Section 4.73).
7. Serial IRQ status register at offset E4h reports level mode interrupt status (see Section 4.74).

A PCI Express MSI is generated based on the settings in the serial IRQ edge control register. If the system is configured for edge mode, then an MSI message is sent when the corresponding serial IRQ interface sample phase transitions from low to high. If the system is configured for level mode, then an MSI message is sent when the corresponding IRQ status bit in the serial IRQ status register changes from low to high.

The bridge has a dedicated SERIRQ terminal (T04) for all PCI bus devices that support serialized interrupts. This SERIRQ interface is synchronous to the PCI bus clock input (CLK) frequency. The bridge always generates a 17-phase serial IRQ stream. Internally, the bridge detects only 16 IRQ interrupts, IRQ0 frame through IRQ15 frame. The $\overline{\text{IOCHCK}}$ frame is not monitored by the serial IRQ state machine and never generates an IRQ interrupt or MSI message.

The multiple message enable (MM_EN) field determines the number of unique MSI messages that are sent upstream on the PCI Express link. From 1 message to 16 messages, in powers of 2, are selectable. If fewer than 16 messages are selected, then the mapping from IRQ interrupts to MSI messages is aliased. Table 3−4 illustrates the IRQ interrupt to MSI message mapping based on the number of enabling messages.

Table 3−4. IRQ Interrupt to MSI Message Mapping

IRQ INTERRUPT	1 MESSAGE ENABLED	2 MESSAGES ENABLED	4 MESSAGES ENABLED	8 MESSAGES ENABLED	16 MESSAGES ENABLED
IRQ0	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #0
IRQ1	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #1	MSI MSG #1
IRQ2	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #2	MSI MSG #2
IRQ3	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #3	MSI MSG #3
IRQ4	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #4	MSI MSG #4
IRQ5	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #5	MSI MSG #5
IRQ6	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #6	MSI MSG #6
IRQ7	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #7	MSI MSG #7
IRQ8	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #8
IRQ9	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #1	MSI MSG #9
IRQ10	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #2	MSI MSG #10
IRQ11	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #3	MSI MSG #11
IRQ12	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #4	MSI MSG #12
IRQ13	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #5	MSI MSG #13
IRQ14	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #6	MSI MSG #14
IRQ15	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #7	MSI MSG #15

The MSI message format is compatible with the PCI Express request header format for 32-bit and 64-bit memory write transactions. The system message and message number fields are included in bytes 0 and 1 of the data payload.

3.4.6 PCI Bus Clocks

The bridge has seven PCI bus clock outputs and one PCI bus clock input. Up to six PCI bus devices are supported by the bridge.

Terminal R01 (M66EN) selects the operating frequency of the PCI bus clock outputs. When this input is asserted high, the PCI bus clocks operate at 66-MHz. When this input is deasserted low, the PCI bus clocks operate at 33-MHz. The clock control register at offset D8h provides 7 control bits to individually enable or disable each PCI bus clock output (see Section 4.66). The register default is enabled for all 7 outputs.

The PCI bus clock (CLK) input provides the clock to the internal PCI bus core and serial IRQ core. When the internal PCI bus clock source is selected, PCI bus clock output 6 (CLKOUT6) is connected to the PCI bus clock input (CLK). When an external PCI bus clock source is selected, the external clock source is connected to the PCI bus clock input (CLK). For external clock mode, all seven CLKOUT6:0 terminals must be disabled using the clock control register at offset D8h (see Section 4.66).

3.5 Quality of Service and Isochronous Features

The bridge has standard and advanced features that provide a robust solution for quality-of-service (QoS) and isochronous applications. These features are best described by divided them into the following three categories:

- PCI port arbitration. PCI port arbitration determines which bus master is granted the next transaction cycle on the PCI bus. The three PCI port arbitration options are the classic PCI arbiter, the 128-phase, WRR time-based arbiter, and the 128-phase, WRR aggressive time-based arbiter. The power-up register default is the classic PCI arbiter. The advanced time-based arbiter features are provided to support isochronous applications.
- PCI isochronous windows. There are four separate windows that allow PCI bus-initiated memory transactions to be labeled with a PCI Express traffic class (TC) beyond the default TC0. Each window designates a range of PCI memory space that is mapped to a specified TC label. The power-up register default is all four windows disabled.
- PCI Express extended VC with VC arbitration. With an extended VC, system software can map a particular TC to a specific VC. The differentiated traffic on the second VC then uses dedicated system resources to support a QoS environment. VC arbitration is provided to gate traffic to the upstream PCI Express link. The three VC arbitration options include strict priority, hardware-fixed round-robin, and 32-phase WRR. The power-up register default is strict priority with the second VC disabled.

When configuring these standard and advanced features, the following rules must be followed:

1. The default mode is classic PCI arbiter with the PCI isochronous windows disabled and the second VC disabled. The bridge performs default PCI bus arbitration without any arbiter-related configuration register setup.
2. If a second VC is enabled, then at least one PCI isochronous window must be configured to map upstream transactions to the second VC.
3. If a second VC is enabled, then any VC arbiter option interacts with any PCI port arbiter option.
4. To enable the PCI isochronous windows it is not required to enable a second VC. The memory space to traffic mapping always uses VC0 for all upstream traffic.
5. When programming the upstream isochronous window base and limit registers, the 32-bit base/limit address must be DWORD aligned and the limit address must be greater than the base address.

The following sections describe in detail the standard and advanced bridge features for QoS and isochronous applications.

3.5.1 PCI Port Arbitration

The internal PCI port arbitration logic supports up to six external PCI bus devices plus the bridge. Three options exist when configuring the bridge arbiter for these seven bus devices: classic PCI arbiter, 128-phase, WRR time-based arbiter, and 128-phase, WRR aggressive time-based arbiter.

3.5.1.1 Classic PCI Arbiter

The classic PCI arbiter is configured through the classic PCI configuration space at offset DCh. Table 3−5 identifies and describes the registers associated with classic PCI arbitration mode.

Table 3−5. Classic PCI Arbiter Registers

PCI OFFSET	REGISTER NAME	DESCRIPTION
Classic PCI configuration register DCh	Arbiter control (see Section 4.69)	Contains a two-tier priority scheme for the bridge and six PCI bus devices. The bridge defaults to the high priority tier. The six PCI bus devices default to the low priority tier. A bus parking control bit (bit 7, PARK) is provided.
Classic PCI configuration register DDh	Arbiter request mask (see Section 4.70)	Six mask bits provide individual control to block each PCI Bus $\overline{\text{REQ}}$ input. Bit 7 (ARB_TIMEOUT) in the arbiter request mask register enables generating timeout status if a PCI device does not respond within 16 PCI bus clocks. Bit 6 (AUTO_MASK) in the arbiter request mask register automatically masks a PCI bus $\overline{\text{REQ}}$ if the device does not respond after $\overline{\text{GNT}}$ is issued. The AUTO_MASK bit is cleared to disable any automatically generated mask.
Classic PCI configuration register DEh	Arbiter time-out status (see Section 4.71)	When bit 7 (ARB_TIMEOUT) in the arbiter request mask register (see Section 4.70) is asserted, timeout status for each PCI bus device is reported in this register.

3.5.1.2 128-Phase, WRR Time-Based Arbiter

The 128-phase, WRR time-based arbiter is configured through the PCI express VC extended configuration space at offset 150h and the device control memory window register map.

The 128-phase, WRR time-based arbiter periodically asserts $\overline{\text{GNT}}$ to a PCI master device based on entries within a port arbitration table. There are actually two port arbitration tables within the bridge. The first table is accessed through the PCI Express VC extended configuration register space using configuration read/write transactions. The second table is internal and is used by the PCI bus arbiter to make $\overline{\text{GNT}}$ decisions. A configuration register load function exists to transfer the contents of the configuration register table to the internal table.

The port arbitration table uses a 4-bit field to identify the secondary bus master that receives $\overline{\text{GNT}}$ during each phase of the time-based WRR arbitration. For the arbiter to recognize a bus master $\overline{\text{REQ}}$ and to generate $\overline{\text{GNT}}$, software must allocate at least three consecutive phases to the same port number.

Table 3−6 defines the mapping relationship of the PCI bus devices to a port number in the port arbitration table.

Table 3−6. Port Number to PCI Bus Device Mapping

PORT NUMBER	$\overline{\text{GNT}}$	PCI DEVICE
0000b	Internal $\overline{\text{GNT}}$ for PCI master state machine	Internal $\overline{\text{REQ}}$ from PCI master state machine
0001b	External $\overline{\text{GNT0}}$	External $\overline{\text{REQ0}}$
0010b	External $\overline{\text{GNT1}}$	External $\overline{\text{REQ1}}$
0011b	External $\overline{\text{GNT2}}$	External $\overline{\text{REQ2}}$
0100b	External $\overline{\text{GNT3}}$	External $\overline{\text{REQ3}}$
0101b	External $\overline{\text{GNT4}}$	External $\overline{\text{REQ4}}$
0110b	External $\overline{\text{GNT5}}$	External $\overline{\text{REQ5}}$
0111b−1111b	Reserved	–

To enable the 128-phase, WRR time-based arbiter, two configuration registers must be written. Bit 1 (PORTARB_LEVEL_1_EN) in the upstream isochrony control register at offset 04h (see Section 6.4) within the device control memory window register map must be asserted. The VC1 resource control register at offset 170h within the PCI Express VC extended configuration space has a PORT_ARB_SELECT field that must be set to 100b (see Section 5.22).

Table 3−7 identifies and describes the registers associated with 128-phase, WWR time-based arbitration mode.

Table 3−7. 128-Phase, WRR Time-Based Arbiter Registers

REGISTER OFFSET	REGISTER NAME	DESCRIPTION
PCI Express VC extended configuration registers 1C0h to 1FCh	Port arbitration table (see Section 5.28)	16-doubleword sized configuration registers that are the registered version of the 128-phase, WRR port arbitration table. Each port arbitration table entry is a 4-bit field.
PCI Express VC extended configuration register 170h	VC1 resource control (see Section 5.25)	Bits 19:17 (PORT_ARB_SELECT) equal to 100b define the port arbitration mechanism as 128-phase WRR. Bit 16 (LOAD_PORT_TABLE), when written with a 1b, transfers the port arbitration table configuration register values to the internal registers used by the PCI bus arbiter.
PCI Express VC extended configuration register 176h	VC1 resource status (see Section 5.26)	Bit 0 (PORT_TABLE_STATUS) equal to 1b indicates that the port arbitration table configuration registers were updated but not loaded into the internal arbitration table.
Device control memory window register 04h	Upstream isochrony control (see Section 6.4)	Bit 1 (PORTARB_LEVEL_1_EN) must be asserted to enable the 128-phase, WRR time-based arbiter.

3.5.1.3 128-Phase, WRR Aggressive Time-Based Arbiter

The last option for PCI port arbitration is 128-phase, WRR aggressive time-based arbitration mode. This arbitration mode performs the same as isochronous mode arbitration, but with one difference. When an isochronous timing event occurs, the PCI bus arbiter deliberately stops a secondary bus master in the middle of the transaction to assure that isochrony is preserved. The register setup for this arbitration option is the same as the 128-phase, WRR time-based arbiter option with the following addition. Bit 2 (PORTARB_LEVEL_2_EN) in the device control memory window upstream isochrony control register at offset 04h must be asserted (see Section 6.4).

3.5.2 PCI Isochronous Windows

The bridge has four separate windows that allow PCI bus-initiated memory transactions to be labeled with a PCI Express traffic class (TC) beyond the default TC0. Each window designates a range of PCI memory space that is mapped to a specified TC label. This advance feature is configured through the device control memory window register map.

Table 3−8 identifies and describes the registers associated with isochronous arbitration mode.

Table 3−8. PCI Isochronous Windows

REGISTER OFFSET	REGISTER NAME	DESCRIPTION
Device control memory window register 08h	Upstream isochronous window 0 control (see Section 6.5)	Bits 3:1 (ISOC_WINDOW_EN) indicate that memory addresses within the base and limit addresses are mapped to a specific traffic class ID. Bit 0 (TC_ID) identifies the specific traffic class ID. **Note:** Memory-mapped register space exists for four upstream windows. Only window 0 is included in this table.
Device control memory window register 0Ch	Upstream isochronous window 0 base address (see Section 6.6)	Window 0 base address
Device control memory window register 10h	Upstream isochronous window 0 limit address (see Section 6.7)	Window 0 limit address

3.5.3 PCI Express Extended VC With VC Arbitration

When a second VC is enabled, the bridge has three arbitration options that determine which VC is granted access to the upstream PCI Express link. These three arbitration modes include strict priority, hardware-fixed round-robin, and 32-phase WRR. The default mode is strict priority. For all three arbitration modes, if the second VC is disabled, then VC0 is always granted.

To map upstream transactions to the extended VC, the following registers must be programmed:

1. Bit 0 (ISOC_ENABLE) is asserted in the upstream isochrony control register at device control memory window register offset 04h (see Section 6.4).
2. At least one PCI isochronous window register set must be programmed. Please see Section 3.5.2 for a description on how to program this advanced feature.
3. The traffic class ID selected for the PCI isochronous window(s) must be assigned to the extended VC. This is accomplished by asserting the corresponding bit in the TC_VC_MAP field in the VC resource control register (VC1) at PCI Express extended register offset 170h (see Section 5.25).
4. The extended VC must be enabled. This is accomplished by asserting bit 31 (VC_EN) and programming bits 26:24 (VC_ID) in the VC resource control register (VC1) at PCI Express extended register offset 170h.

3.5.3.1 Strict Priority Arbitration Mode

Strict priority arbitration always grants VC1 traffic over VC0 traffic. If the traffic on VC1 uses 100% of the upstream link bandwidth, then VC0 traffic is blocked. This mode is enabled when bit 25 (STRICT_PRIORITY_EN) in the general control register at offset D4h equals 1b (see Section 4.65).

For applications that require QoS or isochronous operation, this arbitration mode is recommended. In this mode, all traffic on VC1 is assured access to the upstream link and VC0 traffic is best effort with a lower priority.

3.5.3.2 Hardware-Fixed, Round-Robin Arbitration

Hardware-fixed, round-robin arbitration alternates between VC0 and the second VC. Over an extended period of time, if both VCs are heavily loaded with equal data payloads, each VC is granted approximately 50% of the upstream link bandwidth. The PCI configuration registers described in Table 3−9 configure the hardware-fixed, round-robin arbitration mode.

Table 3−9. Hardware-Fixed, Round-Robin Arbiter Registers

PCI OFFSET	REGISTER NAME	DESCRIPTION
Classic PCI configuration register D4h	General control (see Section 4.65)	Bit 25 (STRICT_PRIORITY_EN) equal to 0b enables either hardware-fixed, round-robin or 32-phase, WRR arbitration mode.
Classic PCI configuration register 15Ch	Port VC control (see Section 5.19)	Bits 3:1 (VC_ARB_SELECT) equal to 000b enables hardware-fixed, round-robin arbitration mode.

3.5.3.3 32-Phase, WRR Arbitration Mode

When the second upstream VC is enabled, the VC arbiter selects the next PCI Express upstream link transaction based on entries within a VC arbitration table. There are actually two VC arbitration tables within the bridge. The first table is accessed through the extended PCI Express configuration register space using configuration read/write transactions. The second table is internal and is used by the VC arbiter to make selection decisions. A configuration register load function exists to transfer the contents of the configuration register table to the internal table.

The VC arbitration table uses a 4-bit field to identify the VC that is selected during each arbiter cycle. Bits 2:0 of this 4-bit field are loaded with the VC_ID assigned to each VC. For the arbiter to recognize a VC request, the software must allocate only 1 phase to the same VC_ID.

The PCI configuration registers described in Table 3−10 configure the 32-phase, WRR arbitration mode.

Table 3−10. 32-phase, WRR Arbiter Registers

PCI OFFSET	REGISTER NAME	DESCRIPTION
Classic PCI configuration register D4h	General control (see Section 4.65)	Bit 25 (STRICT_PRIORITY_EN) equal to 0b enables either hardware-fixed, round-robin or 32-phase, WRR arbitration mode.
PCI Express VC extended configuration register 15Ch	Port VC control (see Section 5.19)	Bit 0 (LOAD_VC_TABLE) when written with a 1b transfers the VC arbitration table configuration register values to the internal registers used by the VC arbiter. Bits 3:1 (VC_ARB_SELECT) equal to 001b enables 32-phase, WRR arbitration mode.
PCI Express VC extended configuration register 15Eh	Port VC status (see Section 5.20)	Bit 0 (VC_TABLE_STATUS) equal to 1b indicates that the VC arbitration table configuration registers were updated but not loaded into the internal arbitration table.
PCI Express VC extended configuration registers 180h to 18Ch	VC arbitration table (see Section 5.27)	4-doubleword sized configuration registers that are the registered version of the 32-phase, WRR VC arbitration table. Each VC arbitration table entry is a 4-bit field.

3.5.4 128-Phase, WRR PCI Port Arbitration Timing

This section includes a timing diagram that illustrates the 128-phase, WRR time-based arbiter timing for the bridge and three PCI bus devices. This timing diagram assumes aggressive mode since the transfer associated with device #1 is stopped to start a device #0 transfer. The PCI bus cycle where device #1 is stopped is indicated by the ‡ symbol. Device #1 then waits until its next port arbitration table cycle to finish the transfer.

The signal waveforms associated with bridge $\overline{\text{REQ}}$, bridge $\overline{\text{GNT}}$, ISOC reference clock, and port arbitration table entry are internal to the bridge. These internal bridge signals are included here to help clarify the operation of the PCI port arbiter in 128-phase, WRR time-based arbitration mode. The remaining $\overline{\text{REQ}}$, $\overline{\text{GNT}}$, and PCI bus signals are all external to the bridge.

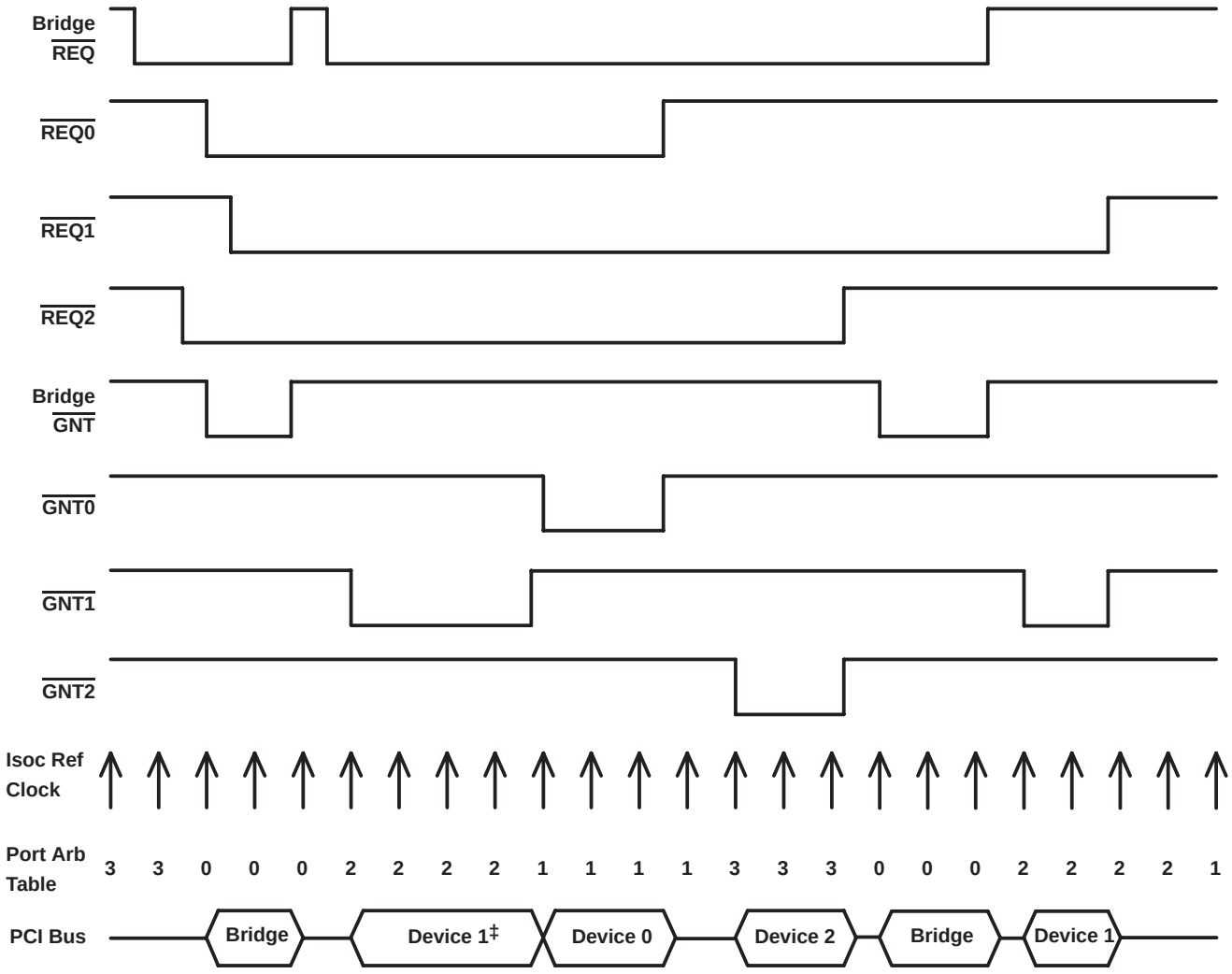


Figure 3−5. PCI Bus Timing

3.6 Configuration Register Translation

PCI Express configuration register transactions received by the bridge are decoded based on the transaction's destination ID. These configuration transactions can be broken into three subcategories: type 0 transactions, type 1 transactions that target the secondary bus, and type 1 transactions that target a downstream bus other than the secondary bus.

PCI Express type 0 configuration register transactions always target the configuration space and are never passed on to the secondary interface.

Type 1 configuration register transactions that target a device on the secondary bus are converted to type 0 configuration register transactions on the PCI bus. Figure 3−6 shows the address phase of a type 0 configuration transaction on the PCI bus as defined by the PCI specification.

31 16	15 11	10 8	7 2	1	0
IDSEL	Reserved	Function Number	Register Number	0	0

Figure 3−6. Type 0 Configuration Transaction Address Phase Encoding

In addition, the bridge converts the destination ID device number to one of the AD[31:16] lines as the IDSEL signal. The implemented IDSEL signal mapping is shown in Table 3−11.

Table 3−11. Type 0 Configuration Transaction IDSEL Mapping

DEVICE NUMBER	AD[31:16]
00000	0000 0000 0000 0001
00001	0000 0000 0000 0010
00010	0000 0000 0000 0100
00011	0000 0000 0000 1000
00100	0000 0000 0001 0000
00101	0000 0000 0010 0000
00110	0000 0000 0100 0000
00111	0000 0000 1000 0000
01000	0000 0001 0000 0000
01001	0000 0010 0000 0000
01010	0000 0100 0000 0000
01011	0000 1000 0000 0000
01100	0001 0000 0000 0000
01101	0010 0000 0000 0000
01110	0100 0000 0000 0000
01111	1000 0000 0000 0000
1xxxx	0000 0000 0000 0000

Type 1 configuration registers transactions that target a downstream bus other then the secondary bus are output on the PCI bus as type 1 PCI configuration transactions. Figure 3−7 shows the address phase of a type 1 configuration transaction on the PCI bus as defined by the PCI specification.

31 24	23 16	15 11	10 8	7 2	1	0
Reserved	Bus Number	Device Number	Function Number	Register Number	0	1

Figure 3−7. Type 1 Configuration Transaction Address Phase Encoding

3.7 PCI Interrupt Conversion to PCI Express Messages

The bridge converts interrupts from the PCI bus sideband interrupt signals to PCI Express interrupt messages.

PCI Express Assert_INTx messages are generated when one of the PCI bus $\overline{\text{INT[A:D]}}$ input terminals transitions low. The requester ID portion of the Assert_INTx message uses the value stored in the primary bus number register (see Section 4.11) as the bus number, 0 as the device number, and 0 as the function number. The tag field for each Assert_INTx message is 00h. The lower two bits in the code field indicate the asserted interrupt signal.

PCI Express Deassert_INTx messages are generated when one of the PCI bus $\overline{\text{INT[A:D]}}$ input terminals transitions high. The requester ID portion of the Deassert_INTx message uses the value stored in the primary bus number register as the bus number, 0 as the device number, and 0 as the function number. The Tag field for each Deassert_INTx message is 00h. The lower two bits in the code field indicate the deasserted interrupt signal.

Table 3−12, Figure 3−8, and Figure 3−9 illustrate the format for both the assert and deassert INTx messages.

Table 3−12. Interrupt Mapping In The Code Field

INTERRUPT	CODE FIELD
$\overline{\text{INTA}}$	00
$\overline{\text{INTB}}$	01
$\overline{\text{INTC}}$	10
$\overline{\text{INTD}}$	11

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0>	R	Fmt		Type					R	TC			Reserved				T D	E P	Attr		R				Length							
		0	1	1	0	1	0	0		0	0	0							0	0					0	0	0	0	0	0	0	0
Byte 4>	Requester ID																Tag								Code							
																									0	0	1	0	0	0	x	x
Byte 8> Byte 12>	Reserved																															

Figure 3−8. PCI Express ASSERT_INTX Message

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0>	R	Fmt		Type					R	TC			Reserved				T D	E P	Attr		R				Length							
		0	1	1	0	1	0	0		0	0	0							0	0					0	0	0	0	0	0	0	0
Byte 4>	Requester ID																Tag								Code							
																									0	0	1	0	0	1	x	x
Byte 8> Byte 12>	Reserved																															

Figure 3−9. PCI Express DEASSERT_INTX Message

3.8 $\overline{\text{PME}}$ Conversion to PCI Express Messages

When the PCI bus $\overline{\text{PME}}$ input transitions low, the bridge generates and sends a PCI Express PME message upstream. The requester ID portion of the PME message uses the stored value in the secondary bus number register as the bus number, 0 as the device number, and 0 as the function number. The Tag field for each PME message is 00h. A PME message is sent periodically until the $\overline{\text{PME}}$ signal transitions high.

Figure 3−10 illustrates the format for a PCI Express PME message.

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0>	R	Fmt		Type					R	TC			Reserved				T D	E P	Attr		R				Length							
		0	1	1	0	0	0	0		0	0	0							0	0					0	0	0	0	0	0	0	0
Byte 4>	Requester ID																Tag								Code							
																									0	0	0	1	1	0	0	0
Byte 8> Byte 12>	Reserved																															

Figure 3−10. PCI Express PME Message

3.9 PCI Express To PCI Bus Lock Conversion

The bus-locking protocol defined in the *PCI Express Base Specification* and *PCI Local Bus Specification* is provided on the bridge as an additional compatibility feature. The PCI bus $\overline{\text{LOCK}}$ signal is a dedicated output that is enabled by setting bit 12 in the general control register at offset D4h. See Section 4.65, *General Control Register*, for details.

NOTE: The use of $\overline{\text{LOCK}}$ is only supported by PCI-Express to PCI Bridges in the downstream direction (away from the root complex).

PCI Express locked-memory read request transactions are treated the same as PCI Express memory read transactions except that the bridge returns a completion for a locked-memory read. Also, the bridge uses the PCI $\overline{\text{LOCK}}$ protocol when initiating the memory read transaction on the PCI bus.

When a PCI Express locked-memory read request transaction is received and the bridge is not already locked, the bridge arbitrates for use of the $\overline{\text{LOCK}}$ terminal by asserting $\overline{\text{REQ}}$. If the bridge receives $\overline{\text{GNT}}$ and the $\overline{\text{LOCK}}$ terminal is high, then the bridge drives the $\overline{\text{LOCK}}$ terminal low after the address phase of the first locked-memory read transaction to take ownership of $\overline{\text{LOCK}}$. The bridge continues to assert $\overline{\text{LOCK}}$ except during the address phase of locked transactions. If the bridge receives $\overline{\text{GNT}}$ and the $\overline{\text{LOCK}}$ terminal is low, then the bridge deasserts its $\overline{\text{REQ}}$ and waits until $\overline{\text{LOCK}}$ is high and the bus is idle before re-arbitrating for the use of $\overline{\text{LOCK}}$.

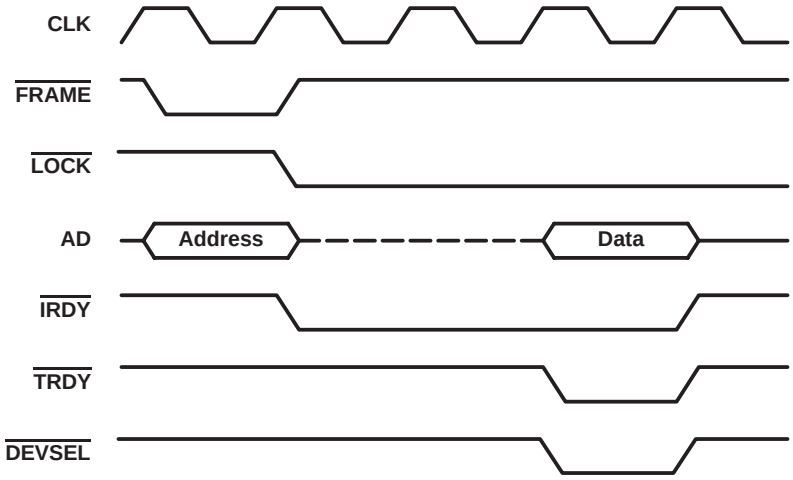


Figure 3−11. Starting A Locked Sequence

Once the bridge has ownership of $\overline{\text{LOCK}}$, the bridge initiates the lock read as a memory read transaction on the PCI bus. When the target of the locked-memory read returns data, the bridge is considered locked and all transactions not associated with the locked sequence are blocked by the bridge.

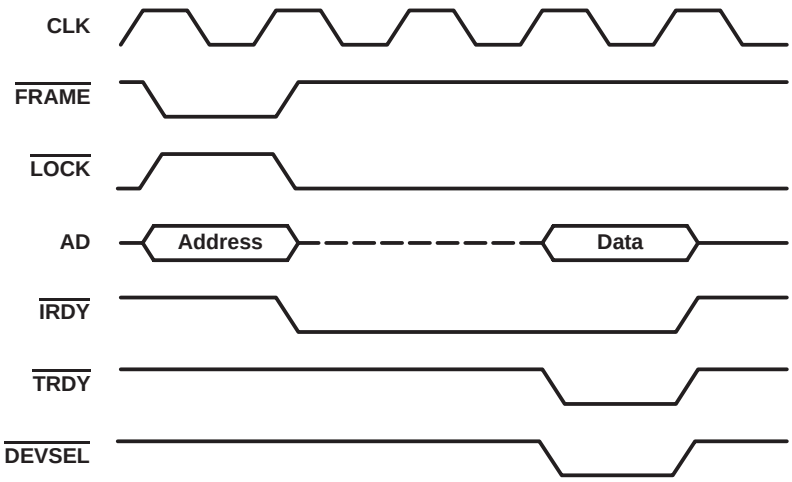


Figure 3−12. Continuing A Locked Sequence

Because PCI Express does not have a unique locked-memory write request packet, all PCI Express memory write requests that are received while the bridge is locked are considered part of the locked sequence and are transmitted to PCI as locked-memory write transactions. In addition, all traffic mapped to VC1 is allowed to pass.

The bridge terminates the locked sequence when an unlock message is received from PCI Express and all previous locked transactions have been completed.

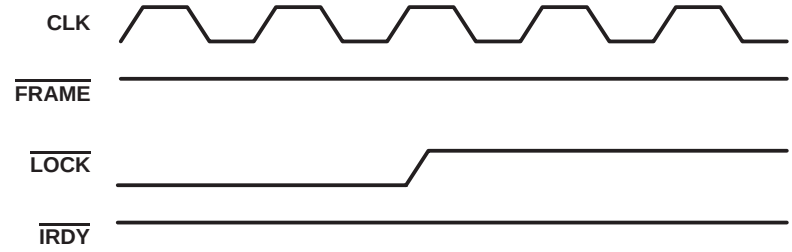


Figure 3−13. Terminating A Locked Sequence

In the erroneous case that a normal downstream memory read request is received during a locked sequence, the bridge responds with an unsupported request completion status. Please note that this condition must never occur, because the PCI Express specification requires the root complex to block normal memory read requests at the source. All locked sequences that end successfully or with an error condition must be immediately followed by an unlock message. This unlock message is required to return the bridge to a known unlocked state.

3.10 Two-Wire Serial-Bus Interface

The bridge provides a two-wire serial-bus interface to load subsystem identification information and specific register defaults from an external EEPROM. The serial-bus interface signals (SCL and SDA) are shared with two of the GPIO terminals (4 and 5). If the serial bus interface is enabled, then the GPIO4 and GPIO5 terminals are disabled. If the serial bus interface is disabled, then the GPIO terminals operate as described in Section 3.13.

3.10.1 Serial-Bus Interface Implementation

To enable the serial-bus interface, a pullup resistor must be implemented on the SDA signal. At the rising edge of $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$, whichever occurs later in time, the SDA terminal is checked for a pullup resistor. If one is detected, then bit 3 (SBDETECT) in the serial-bus control and status register (see Section 4.58) is set. Software may disable the serial-bus interface at any time by writing a 0b to the SBDETECT bit. If no external EEPROM is required, then the serial-bus interface is permanently disabled by attaching a pulldown resistor to the SDA signal.

The bridge implements a two-terminal serial interface with 1 clock signal (SCL) and 1 data signal (SDA). The SCL signal is a unidirectional output from the bridge and the SDA signal is bidirectional. Both are open-drain signals and require pullup resistors. The bridge is a bus master device and drives SCL at approximately 60 kHz during data transfers and places SCL in a high-impedance state (0 frequency) during bus idle states. The serial EEPROM is a bus slave device and must acknowledge a slave address equal to A0h. Figure 3−14 illustrates an example application implementing the two-wire serial bus.

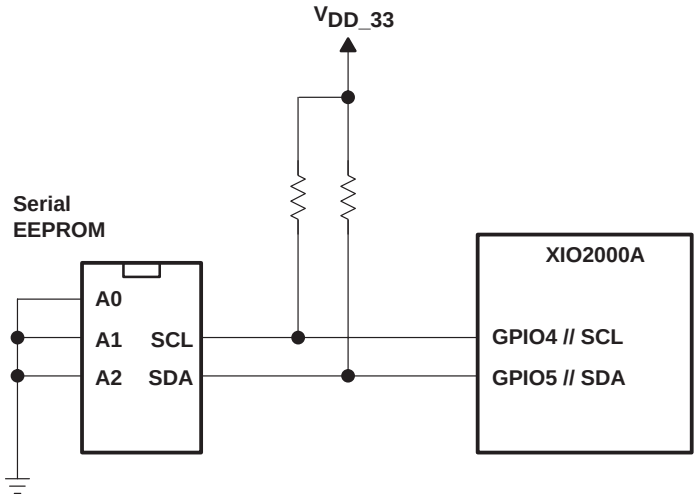


Figure 3−14. Serial EEPROM Application

3.10.2 Serial-Bus Interface Protocol

All data transfers are initiated by the serial-bus master. The beginning of a data transfer is indicated by a start condition, which is signaled when the SDA line transitions to the low state while SCL is in the high state, as illustrated in Figure 3−15. The end of a requested data transfer is indicated by a stop condition, which is signaled by a low-to-high transition of SDA while SCL is in the high state, as shown in Figure 3−15. Data on SDA must remain stable during the high state of the SCL signal, as changes on the SDA signal during the high state of SCL are interpreted as control signals, that is, a start or stop condition.

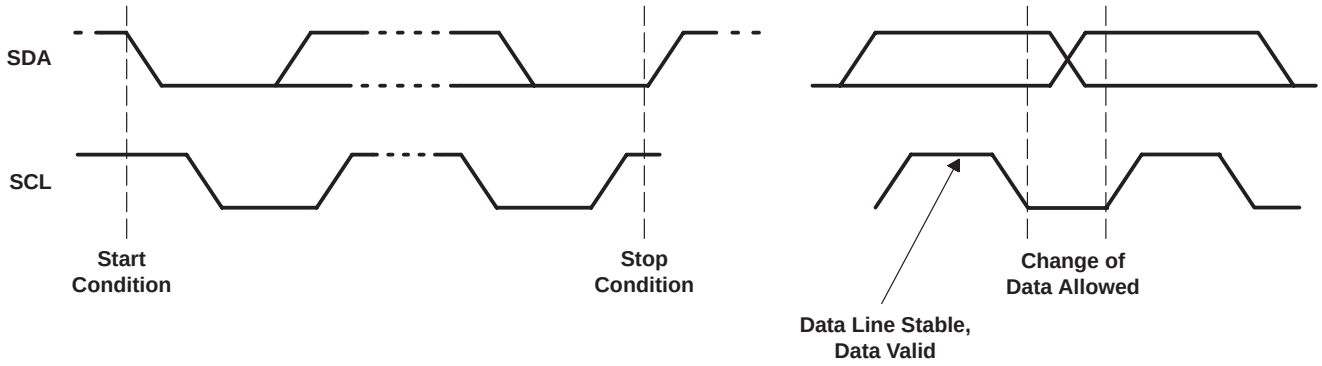


Figure 3−15. Serial-Bus Start/Stop Conditions and Bit Transfers

Data is transferred serially in 8-bit bytes. During a data transfer operation, the exact number of bytes that are transmitted is unlimited. However, each byte must be followed by an acknowledge bit to continue the data transfer operation. An acknowledge (ACK) is indicated by the data byte receiver pulling the SDA signal low, so that it remains low during the high state of the SCL signal. Figure 3−16 illustrates the acknowledge protocol.

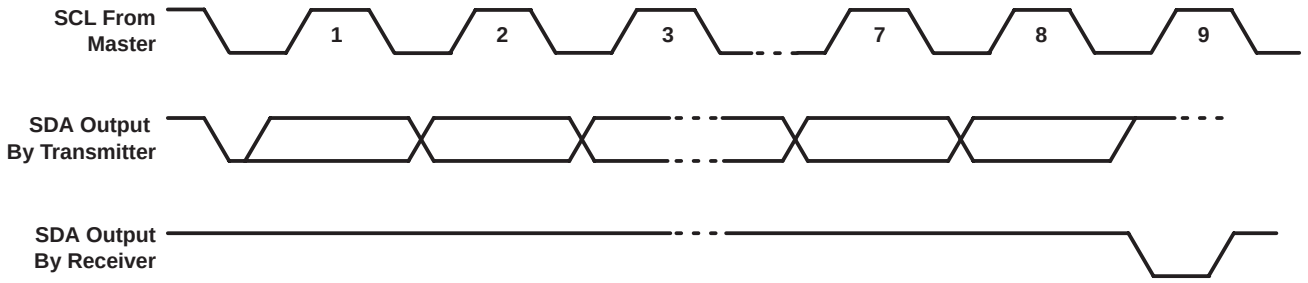


Figure 3−16. Serial-Bus Protocol Acknowledge

The bridge performs three basic serial-bus operations: single byte reads, single byte writes, and multibyte reads. The single byte operations occur under software control. The multibyte read operations are performed by the serial EEPROM initialization circuitry immediately after a PCI Express reset. See Section 3.10.3, *Serial-Bus EEPROM Application*, for details on how the bridge automatically loads the subsystem identification and other register defaults from the serial-bus EEPROM.

Figure 3−17 illustrates a single byte write. The bridge issues a start condition and sends the 7-bit slave device address and the R/$\overline{W}$ command bit is equal to 0b. A 0b in the R/$\overline{W}$ command bit indicates that the data transfer is a write. The slave device acknowledges if it recognizes the slave address. If no acknowledgment is received by the bridge, then bit 1 (SB_ERR) is set in the serial-bus control and status register (PCI offset B3h, see Section 4.58). Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then the bridge delivers the data byte MSB first and expects a final acknowledgment before issuing the stop condition.

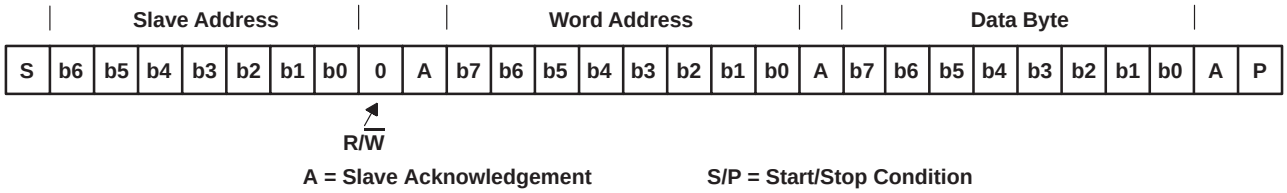


Figure 3−17. Serial-Bus Protocol—Byte Write

Figure 3−18 illustrates a single byte read. The bridge issues a start condition and sends the 7-bit slave device address and the R/$\overline{W}$ command bit is equal to 0b (write). The slave device acknowledges if it recognizes the slave address. Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then, the bridge issues a restart condition followed by the 7-bit slave address and the R/$\overline{W}$ command bit is equal to 1b (read). Once again, the slave device responds with an acknowledge. Next, the slave device sends the 8-bit data byte, MSB first. Since this is a 1-byte read, the bridge responds with no acknowledge (logic high) indicating the last data byte. Finally, the bridge issues a stop condition.

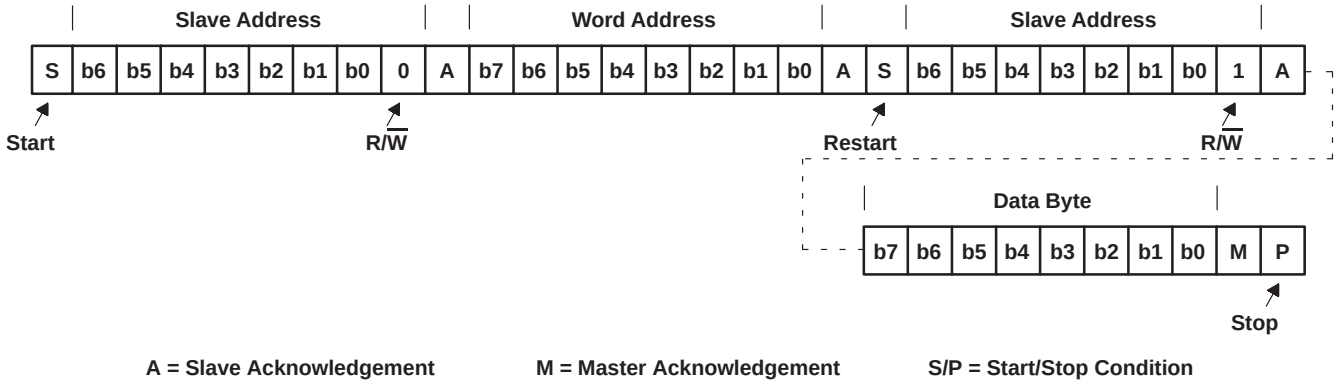


Figure 3−18. Serial-Bus Protocol—Byte Read

Figure 3−19 illustrates the serial interface protocol during a multi-byte serial EEPROM download. The serial-bus protocol starts exactly the same as a 1-byte read. The only difference is that multiple data bytes are transferred. The number of transferred data bytes is controlled by the bridge master. After each data byte, the bridge master issues acknowledge (logic low) if more data bytes are requested. The transfer ends after a bridge master no acknowledge (logic high) followed by a stop condition.

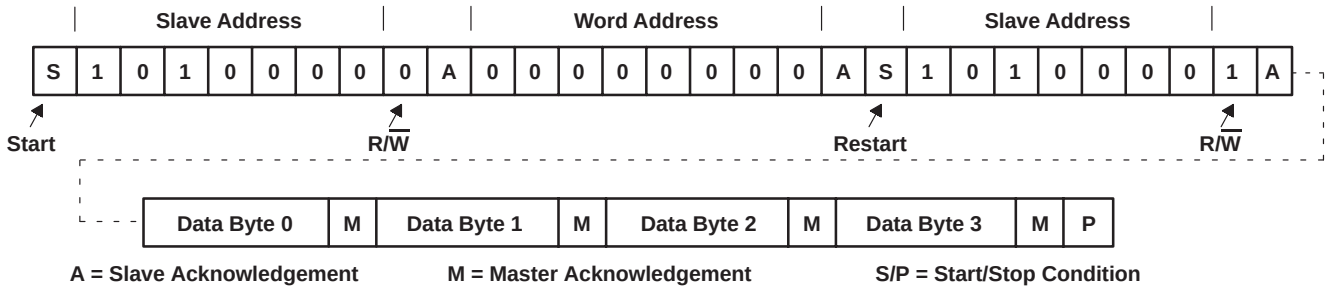


Figure 3−19. Serial-Bus Protocol—Multibyte Read

Bit 7 (PROT_SEL) in the serial-bus control and status register changes the serial-bus protocol. Each of the three previous serial-bus protocol figures illustrates the PROT_SEL bit default (logic low). When this control bit is asserted, the word address and corresponding acknowledge are removed from the serial-bus protocol. This feature allows the system designer a second serial-bus protocol option when selecting external EEPROM devices.

3.10.3 Serial-Bus EEPROM Application

The registers and corresponding bits that are loaded through the EEPROM are provided in Table 3−13.

Table 3−13. EEPROM Register Loading Map

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION
00h	PCI-Express to PCI bridge function indicator (00h)
01h	Number of bytes to download (1Eh)
02h	PCI 84h, subsystem vendor ID, byte 0
03h	PCI 85h, subsystem vendor ID, byte 1
04h	PCI 86h, subsystem ID, byte 0
05h	PCI 87h, subsystem ID, byte 1
06h	PCI D4h, general control, byte 0
07h	PCI D5h, general control, byte 1
08h	PCI D6h, general control, byte 2
09h	PCI D7h, general control, byte 3
0Ah	PCI D8h, clock control
0Bh	PCI D9h, clock mask
0Ch	Reserved—no bits loaded
0Dh	PCI DCh, arbiter control
0Eh	PCI DDh, arbiter request mask
0Fh	PCI C0h, control and diagnostic register 0 byte 0
10h	PCI C1h, control and diagnostic register 0 byte 1
11h	PCI C2h, control and diagnostic register 0 byte 2
12h	PCI C3h, control and diagnostic register 0 byte 3
13h	PCI C4h, control and diagnostic register 1 byte 0
14h	PCI C5h, control and diagnostic register 1 byte 1
15h	PCI C6h, control and diagnostic register 1 byte 2
16h	PCI C7h, control and diagnostic register 1 byte 3
17h	PCI C8h, control and diagnostic register 2 byte 0
18h	PCI C9h, control and diagnostic register 2 byte 1
19h	PCI CAh, control and diagnostic register 2 byte 2
1Ah	PCI CBh, control and diagnostic register 2 byte 3
1Bh	Reserved—no bits loaded
1Ch	Reserved—no bits loaded
1Dh	PCI E0h, serial IRQ mode control
1Eh	PCI E2h, serial IRQ edge control, byte 0
1Fh	PCI E3h, serial IRQ edge control, byte 1
20h	End-of-list indicator (80h)

This format must be explicitly followed for the bridge to correctly load initialization values from a serial EEPROM. All byte locations must be considered when programming the EEPROM.

The serial EEPROM is addressed by the bridge at slave address 1010 000b. This slave address is internally hardwired and cannot be changed by the system designer. Therefore, all three hardware address bits for the EEPROM are tied to V_{SS} to achieve this address. The serial EEPROM in the sample application circuit (Figure 3−14) assumes the 1010b high-address nibble. The lower three address bits are terminal inputs to the chip, and the sample application shows these terminal inputs tied to V_{SS}.

During an EEPROM download operation, bit 4 (ROMBUSY) in the serial-bus control and status register is asserted. After the download is finished, bit 0 (ROM_ERR) in the serial-bus control and status register may be monitored to verify a successful download.

3.10.4 Accessing Serial-Bus Devices Through Software

The bridge provides a programming mechanism to control serial-bus devices through system software. The programming is accomplished through a doubleword of PCI configuration space at offset B0h. Table 3−14 lists the registers that program a serial-bus device through software.

Table 3−14. Registers Used To Program Serial-Bus Devices

PCI OFFSET	REGISTER NAME	DESCRIPTION
B0h	Serial-bus data (see Section 4.55)	Contains the data byte to send on write commands or the received data byte on read commands.
B1h	Serial-bus word address (see Section 4.56)	The content of this register is sent as the word address on byte writes or reads. When bit 7 (PROT_SEL) in the serial-bus control and status register (offset B3h, see Section 4.58) is set to 1b and the quick command protocol is selected, this word address is ignored.
B2h	Serial-bus slave address (see Section 4.57)	Write transactions to this register initiate a serial-bus transaction. The slave device address and the R/$\overline{W}$ command selector are programmed through this register.
B3h	Serial-bus control and status (see Section 4.58)	Serial interface enable, busy, and error status are communicated through this register. In addition, the protocol-select (PROT_SEL) bit and serial-bus test (SBTEST) bit are programmed through this register.

To access the serial EEPROM through the software interface, the following steps are performed:

1. The control and status byte is read to verify the EEPROM interface is enabled (SBDETECT asserted) and not busy (REQBUSY and ROMBUSY deasserted).
2. The serial-bus word address is loaded. If the access is a write, then the data byte is also loaded.
3. The serial-bus slave address and R/$\overline{W}$ command selector byte is written.
4. REQBUSY is monitored until this bit is deasserted.
5. SB_ERR is checked to verify that the serial-bus operation completed without error. If the operation is a read, then the serial-bus data byte is now valid.

3.11 Advanced Error Reporting Registers

In the extended PCI Express configuration space, the bridge supports the advanced error reporting capabilities structure. For the PCI Express interface, both correctable and uncorrectable error status is provided. For the PCI bus interface, secondary uncorrectable error status is provided. All uncorrectable status bits have corresponding mask and severity control bits. For correctable status bits, only mask bits are provided.

Both the primary and secondary interfaces include first error pointer and header log registers. When the first error is detected, the corresponding bit position within the uncorrectable status register is loaded into the first error pointer register. Likewise, the header information associated with the first failing transaction is loaded into the header log. To reset this first error control logic, the corresponding status bit in the uncorrectable status register is cleared by a writeback of 1b.

For systems that require high data reliability, ECRC is fully supported on the PCI Express interface. The primary side advanced error capabilities and control register has both ECRC generation and checking enable control bits. When the checking bit is asserted, all received TLPs are checked for a valid ECRC field. If the generation bit is asserted, then all transmitted TLPs contain a valid ECRC field.

3.12 Data Error Forwarding Capability

The bridge supports the transfer of data errors in both directions.

If a downstream PCI Express transaction with a data payload is received that targets the PCI bus and the EP bit is set indicating poisoned data, then the bridge must ensure that this information is transferred to the PCI bus. To do this, the bridge forces a parity error on each PCI bus data phase by inverting the parity bit calculated for each double-word of data.

If the bridge is the target of a PCI transaction that is forwarded to the PCI Express interface and a data parity error is detected, then this information is passed to the PCI Express interface. To do this, the bridge sets the EP bit in the upstream PCI Express header.

3.13 General-Purpose I/O Interface

Up to eight general-purpose input/output (GPIO) terminals are provided for system customization. These GPIO terminals are 3.3-V tolerant.

The exact number of GPIO terminals varies based on implementing the clock run, power override, and serial EEPROM interface features. These features share four of the eight GPIO terminals. When any of the three shared functions are enabled, the associated GPIO terminal is disabled.

All eight GPIO terminals are individually configurable as either inputs or outputs by writing the corresponding bit in the GPIO control register at offset B4h. A GPIO data register at offset B6h exists to either read the logic state of each GPIO input or to set the logic state of each GPIO output. The power-up default state for the GPIO control register is input mode.

3.14 Set Slot Power Limit Functionality

The *PCI Express Specification* provides a method for devices to limit internal functionality and save power based on the value programmed into the captured slot power limit scale (CSPLS) and capture slot power limit value (CSPLV) fields of the PCI Express device capabilities register at offset 94h. See Section 4.49, *Device Capabilities Register*, for details. The bridge writes these fields when a set slot power limit message is received on the PCI Express interface.

After the deassertion of $\overline{\text{PERST}}$, the bridge compares the information in the CSPLS and CSPLV fields of the device capabilities register with the minimum power scale (MIN_POWER_SCALE) and minimum power value (MIN_POWER_VALUE) fields in the general control register at offset D4h. See Section 4.65, *General Control Register*, for details. If the CSPLS and CSPLV fields are less than the MIN_POWER_SCALE and MIN_POWER_VALUE fields, respectively, then the bridge takes the appropriate action that is defined below.

The power usage action is programmable within the bridge. The general control register includes a 3-bit PWR_OVRD field. This field is programmable to the following five options:

1. Ignore slot power limit fields
2. Assert the PWR_OVRD terminal (U05)
3. Disable secondary clocks as specified by the clock mask register at offset D9h.
4. Disable secondary clocks as specified by the clock mask register and assert the PWR_OVRD terminal
5. Respond with unsupported request to all transactions except type 0/1 configuration transactions and set slot power limit messages

3.15 PCI Express and PCI Bus Power Management

The bridge supports both software-directed power management and active state power management through standard PCI configuration space. Software-directed registers are located in the power management capabilities structure located at offset 50h. Active state power management control registers are located in the PCI Express capabilities structure located at offset 90h.

During software-directed power management state changes, the bridge initiates link state transitions to L1 or L2/L3 after a configuration write transaction places the device in a low power state. The power management state machine is also responsible for gating internal clocks based on the power state. Table 3−15 identifies the relationship between the D-states and bridge clock operation.

Table 3−15. Clocking In Low Power States

CLOCK SOURCE	D0/L0	D1/L1	D2/L1	D3/L2/L3
PCI express reference clock input (REFCLK)	On	On	On	On/Off
PCI clock input (CLK)	On	Off	Off	Off
Secondary PCI bus clock outputs (CLKOUT6:0)	On	On	On	On/Off

The link power management (LPM) state machine manages active state power by monitoring the PCI Express transaction activity. If no transactions are pending and the transmitter has been idle for at least the minimum time required by the *PCI Express Specification*, then the LPM state machine transitions the link to either the L0s or L1 state. By reading the bridge's L0s and L1 exit latency in the link capabilities register, the system software may make an informed decision relating to system performance versus power savings. The ASLPMC field in the link control register provides an L0s-only option, L1-only option, or both L0s and L1 option.

Finally, the bridge generates the PM_Active_State_Nak Message if a PM_Active_State_Request_L1 DLLP is received on the PCI Express interface and the link cannot be transitioned to L1.

4 Classic PCI Configuration Space

The programming model of the XIO2000A PCI-Express to PCI bridge is compliant to the classic PCI-to-PCI bridge programming model. The PCI configuration map uses the type 1 PCI bridge header.

All bits marked with a ☆ are sticky bits and are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a † are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4−1. Classic PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		000h
Status		Command		004h
Class code			Revision ID	008h
BIST	Header type	Latency timer	Cache line size	00Ch
Device control base address				010h
Reserved				014h
Secondary latency timer	Subordinate bus number	Secondary bus number	Primary bus number	018h
Secondary status		I/O limit	I/O base	01Ch
Memory limit		Memory base		020h
Prefetchable memory limit		Prefetchable memory base		024h
Prefetchable base upper 32 bits				028h
Prefetchable limit upper 32 bits				02Ch
I/O limit upper 16 bits		I/O base upper 16 bits		030h
Reserved			Capabilities pointer	034h
Reserved				038h
Bridge control		Interrupt pin	Interrupt line	03Ch
Reserved				040h−04Ch
Power management capabilities		Next item pointer	PM CAP ID	050h
PM data	PMCSR_BSE	Power management CSR		054h
Reserved				058h−05Ch
MSI message control		Next item pointer	MSI CAP ID	060h
MSI message address				064h
MSI upper message address				068h
Reserved		MSI message data		06Ch
Reserved				070h−07Ch
Reserved		Next item pointer	SSID/SSVID CAP ID	080h
Subsystem ID†		Subsystem vendor ID†		084h
Reserved				088h−08Ch
PCI Express capabilities register		Next item pointer	PCI Express capability ID	090h
Device capabilities				094h
Device status		Device control		098h
Link capabilities				09Ch
Link status		Link control		0A0h
Reserved				0A4h−0ACh
Serial-bus control and status†	Serial-bus slave address†	Serial-bus word address†	Serial-bus data†	0B0h

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4−1. PCI Express Configuration Register Map (Continued)

REGISTER NAME				OFFSET
GPIO data†		GPIO control†		0B4h
Reserved				0B8h−0BCh
Control and diagnotic register 0†				0C0h
Control and diagnotic register 1†				0C4h
Control and diagnotic register 2†				0C8h
Reserved				0CCh
Subsystem access†				0D0h
General control†				0D4h
Reserved	Clock run status†	Clock mask†	Clock control†	0D8h
Reserved	Arbiter time-out status	Arbiter request mask†	Arbiter control†	0DCh
Serial IRQ edge control†		Reserved	Serial IRQ mode control†	0E0h
Reserved		Serial IRQ status		0E4h
Reserved				0E8h−0FCh

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.1 Vendor ID Register

This 16-bit read-only register contains the value 104Ch, which is the vendor ID assigned to Texas Instruments.

PCI register offset: 00h
Register type: Read-only
Default value: 104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.2 Device ID Register

This 16-bit read-only register contains the value 8231h, which is the device ID assigned by TI for the bridge.

PCI register offset: 02h
Register type: Read-only
Default value: 8231h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1

4.3 Command Register

The command register controls how the bridge behaves on the PCI Express interface. See Table 4−2 for a complete description of the register contents.

PCI register offset: 04h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−2. Command Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	RSVD	R	Reserved. Returns 00000b when read.
10	INT_DISABLE	R	$\overline{\text{INTx}}$ disable. This bit enables device specific interrupts. Since the bridge does not generate any internal interrupts, this bit is read-only 0b.
9	FBB_ENB	R	Fast back-to-back enable. The bridge does not generate fast back-to-back transactions; therefore, this bit returns 0b when read.
8	SERR_ENB	RW	$\overline{\text{SERR}}$ enable bit. When this bit is set, the bridge can signal fatal and nonfatal errors on the PCI Express interface on behalf of $\overline{\text{SERR}}$ assertions detected on the PCI bus. 0 = Disable the reporting of nonfatal errors and fatal errors (default) 1 = Enable the reporting of nonfatal errors and fatal errors
7	STEP_ENB	R	Address/data stepping control. The bridge does not support address/data stepping, and this bit is hardwired to 0b.
6	PERR_ENB	RW	Controls the setting of bit 8 (DATAPAR) in the status register (offset 06h, see Section 4.4) in response to a received poisoned TLP from PCI Express. A received poisoned TLP is forwarded with bad parity to conventional PCI regardless of the setting of this bit. 0 = Disables the setting of the master data parity error bit (default) 1 = Enables the setting of the master data parity error bit
5	VGA_ENB	R	VGA palette snoop enable. The bridge does not support VGA palette snooping; therefore, this bit returns 0b when read.
4	MWI_ENB	RW	Memory write and invalidate enable. When this bit is set, the bridge translates PCI Express memory write requests into memory write and invalidate transactions on the PCI interface. 0 = Disable the promotion to memory write and invalidate (default) 1 = Enable the promotion to memory write and invalidate
3	SPECIAL	R	Special cycle enable. The bridge does not respond to special cycle transactions; therefore, this bit returns 0b when read.
2	MASTER_ENB	RW	Bus master enable. When this bit is set, the bridge is enabled to initiate transactions on the PCI Express interface. 0 = PCI Express interface cannot initiate transactions. The bridge must disable the response to memory and I/O transactions on the PCI interface (default). 1 = PCI Express interface can initiate transactions. The bridge can forward memory and I/O transactions from PCI secondary interface to the PCI Express interface.
1	MEMORY_ENB	RW	Memory space enable. Setting this bit enables the bridge to respond to memory transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream memory transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream memory transactions. The bridge can forward memory transactions to the PCI interface.
0	IO_ENB	RW	I/O space enable. Setting this bit enables the bridge to respond to I/O transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream I/O transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream I/O transactions. The bridge can forward I/O transactions to the PCI interface.

4.4 Status Register

The status register provides information about the PCI Express interface to the system. See Table 4−3 for a complete description of the register contents.

PCI register offset: 06h
Register type: Read-only, Read/Clear
Default value: 0010h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 4−3. Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit is set when the PCI Express interface receives a poisoned TLP. This bit is set regardless of the state of bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3). 0 = No parity error detected 1 = Parity error detected
14	SYS_ERR	RCU	Signaled system error. This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL message and bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set. 0 = No error signaled 1 = ERR_FATAL or ERR_NONFATAL signaled
13	MABORT	RCU	Received master abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-unsupported-request status. 0 = Unsupported request not received on the PCI Express interface 1 = Unsupported request received on the PCI Express interface
12	TABORT_REC	RCU	Received target abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-completer-abort status. 0 = Completer abort not received on the PCI Express interface 1 = Completer abort received on the PCI Express interface
11	TABORT_SIG	RCU	Signaled target abort. This bit is set when the PCI Express interface completes a request with completer abort status. 0 = Completer abort not signaled on the PCI Express interface 1 = Completer abort signaled on the PCI Express interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are read-only 00b, because they do not apply to PCI Express.
8	DATAPAR	RCU	Master data parity error. This bit is set if bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3) is set and the bridge receives a completion with data marked as poisoned on the PCI Express interface or poisons a write request received on the PCI Express interface. 0 = No uncorrectable data error detected on the primary interface 1 = Uncorrectable data error detected on the primary interface
7	FBB_CAP	R	Fast back-to-back capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
4	CAPLIST	R	Capabilities list. This bit returns 1b when read, indicating that the bridge supports additional PCI capabilities.
3	INT_STATUS	R	Interrupt status. This bit reflects the interrupt status of the function. This bit is read-only 0b since the bridge does not generate any interrupts internally.
2:0	RSVD	R	Reserved. Returns 000b when read.

4.5 Class Code and Revision ID Register

This read-only register categorizes the base class, subclass, and programming interface of the bridge. The base class is 06h, identifying the device as a bridge. The subclass is 04h, identifying the function as a PCI-to-PCI bridge, and the programming interface is 00h. Furthermore, the TI device revision is indicated in the lower byte (03h). See Table 4−4 for a complete description of the register contents.

PCI register offset: 08h
Register type: Read-only
Default value: 0604 0003

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Table 4−4. Class Code and Revision ID Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	BASECLASS	R	Base class. This field returns 06h when read, which classifies the function as a bridge device.
23:16	SUBCLASS	R	Subclass. This field returns 04h when read, which classifies the function as a PCI-to-PCI bridge.
15:8	PGMIF	R	Programming interface. This field returns 00h when read.
7:0	CHIPREV	R	Silicon revision. This field returns the silicon revision of the function.

4.6 Cache Line Size Register

This read/write cache line size register is used by the bridge to determine how much data to prefetch when handling delayed read transactions. The value in this register must be programmed to a power of 2. Any written odd value (bit 0 = 1b) or value greater than 32 DWORDs is treated as 0 DWORDs.

PCI register offset: 0Ch
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.7 Primary Latency Timer Register

This read-only register has no meaningful context for a PCI Express device and returns the value 00h when read.

PCI register offset: 0Dh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.8 Header Type Register

This read-only register indicates that this function has a type one PCI header. Bit 7 of this register is 0b indicating that the bridge is a single-function device.

PCI register offset: 0Eh
Register type: Read-only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.9 BIST Register

Since the bridge does not support a built-in self test (BIST), this read-only register returns the value of 00h when read.

PCI register offset: 0Fh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.10 Device Control Base Address Register

This register programs the memory base address that acesses the device control registers. By default, this register is read only. If bit 5 of the Control and Diagnostic Register 2 (offset C8h) is set, then the bits 31:12 of this register become read/write. See Table 4−5 for a complete description of the register contents.

PCI register offset: 10h
Register type: Read-only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−5. Device Control Base Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:12	ADDRESS	R,R/W	Memory base address. The memory address field for the bridge uses 20 read/write bits indicating that 4096 bytes is the amount of memory space that is reserved. These bits are read only if Register C8h bit 5 is clear. If bit 5 is set, then these bits become Read/Write.
11:4	RSVD	R	Reserved. These bits are read-only and return 00h when read.
3	PRE_FETCH	R	Prefetchable. This bit is read-only 0b indicating that this memory window is not prefetchable.
2:1	MEM_TYPE	R	Memory type. This field is read-only 00b indicating that this window can be located anywhere in the 32-bit address space.
0	MEM_IND	R	Memory space indicator. This field returns 0b indicating that memory space is used.

4.11 Primary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI Express interface is connected to.

PCI register offset: 18h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.12 Secondary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI interface is connected to. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 19h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.13 Subordinate Bus Number Register

This read/write register specifies the bus number of the highest number PCI bus segment that is downstream of the bridge. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 1Ah
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.14 Secondary Latency Timer Register

This read/write register specifies the secondary bus latency timer for the bridge, in units of PCI clock cycles.

PCI register offset: 1Bh
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.15 I/O Base Register

This read/write register specifies the lower limit of the I/O addresses that the bridge forwards downstream. See Table 4−6 for a complete description of the register contents.

PCI register offset: 1Ch
Register type: Read-only, Read/Write
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4−6. I/O Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOBASE	RW	I/O base. Defines the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be 000h. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O base upper 16 bits register (offset 30h, see Section 4.24).
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

4.16 I/O Limit Register

This read/write register specifies the upper limit of the I/O addresses that the bridge forwards downstream. See Table 4−7 for a complete description of the register contents.

PCI register offset: 1Dh
Register type: Read-only, Read/Write
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4−7. I/O Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOLIMIT	RW	I/O limit. Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O limit upper 16 bits register (offset 32h, see Section 4.25).
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

4.17 Secondary Status Register

The secondary status register provides information about the PCI bus interface. See Table 4−8 for a complete description of the register contents.

PCI register offset: 1Eh
Register type: Read-only, Read/Clear
Default value: 02X0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	1	0	x	0	0	0	0	0

Table 4−8. Secondary Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit reports the detection of an uncorrectable address, attribute, or data error by the bridge on its secondary interface. This bit must be set when any of the following three conditions are true: • The bridge detects an uncorrectable address or attribute error as a potential target. • The bridge detects an uncorrectable data error when it is the target of a write transaction. • The bridge detects an uncorrectable data error when it is the master of a read transaction (immediate read data). The bit is set irrespective of the state of bit 0 (PERR_EN) in the bridge control register at offset 3Eh (see Section 4.29). 0 = Uncorrectable address, attribute, or data error not detected on secondary interface 1 = Uncorrectable address, attribute, or data error detected on secondary interface
14	SYS_ERR	RCU	Received system error. This bit is set when the bridge detects an $\overline{\text{SERR}}$ assertion. 0 = No error asserted on the PCI interface 1 = $\overline{\text{SERR}}$ asserted on the PCI interface
13	MABORT	RCU	Received master abort. This bit is set when the PCI interface of the bridge reports the detection of a master abort termination by the bridge when it is the master of a transaction on its secondary interface. 0 = Master abort not received on the PCI interface 1 = Master abort received on the PCI interface
12	TABORT_REC	RCU	Received target abort. This bit is set when the PCI interface of the bridge receives a target abort. 0 = Target abort not received on the PCI interface 1 = Target abort received on the PCI interface
11	TABORT_SIG	RCU	Signaled target abort. This bit reports the signaling of a target abort termination by the bridge when it responds as the target of a transaction on its secondary interface. 0 = Target abort not signaled on the PCI interface 1 = Target abort signaled on the PCI interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are 01b indicating that this is a medium speed decoding device.
8	DATAPAR	RCU	Master data parity error. This bit is set if the bridge is the bus master of the transaction on the PCI bus, bit 0 (PERR_EN) in the bridge control register (offset 3Eh see Section 4.29) is set, and the bridge either asserts $\overline{\text{PERR}}$ on a read transaction or detects $\overline{\text{PERR}}$ asserted on a write transaction. 0 = No data parity error detected on the PCI interface 1 = Data parity error detected on the PCI interface
7	FBB_CAP	R	Fast back-to-back capable. This bit returns a 1b when read indicating that the secondary PCI interface of bridge supports fast back-to-back transactions.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. The bridge can operate at a maximum CLK frequency of 66 MHz; therefore, this bit reflects the state of the M66EN terminal.
4:0	RSVD	R	Reserved. Returns 00000b when read.

4.18 Memory Base Register

This read/write register specifies the lower limit of the memory addresses that the bridge forwards downstream. See Table 4−9 for a complete description of the register contents.

PCI register offset: 20h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−9. Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMBASE	RW	Memory base. Defines the lowest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h.
3:0	RSVD	R	Reserved. Returns 0h when read.

4.19 Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the bridge forwards downstream. See Table 4−10 for a complete description of the register contents.

PCI register offset: 22h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−10. Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMLIMIT	RW	Memory limit. Defines the highest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh.
3:0	RSVD	R	Reserved. Returns 0h when read.

4.20 Prefetchable Memory Base Register

This read/write register specifies the lower limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4−11 for a complete description of the register contents.

PCI register offset: 24h
Register type: Read-only, Read/Write
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4−11. Prefetchable Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PREBASE	RW	Prefetchable memory base. Defines the lowest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base upper 32 bits register (offset 28h, see Section 4.22) specifies bits [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.21 Prefetchable Memory Limit Register

This read/write register specifies the upper limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4−12 for a complete description of the register contents.

PCI register offset: 26h
Register type: Read-only, Read/Write
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4−12. Prefetchable Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PRELIMIT	RW	Prefetchable memory limit. Defines the highest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable limit upper 32 bits register (offset 2Ch, see Section 4.23) specifies bits [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.22 Prefetchable Base Upper 32-Bit Register

This read/write register specifies the upper 32 bits of the prefetchable memory base register. See Table 4−13 for a complete description of the register contents.

PCI register offset: 28h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−13. Prefetchable Base Upper 32-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PREBASE	RW	Prefetchable memory base upper 32 bits. Defines the upper 32 bits of the lowest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

4.23 Prefetchable Limit Upper 32-Bit Register

This read/write register specifies the upper 32 bits of the prefetchable memory limit register. See Table 4−14 for a complete description of the register contents.

PCI register offset: 2Ch
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−14. Prefetchable Limit Upper 32-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PRELIMIT	RW	Prefetchable memory limit upper 32 bits. Defines the upper 32 bits of the highest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

4.24 I/O Base Upper 16-Bit Register

This read/write register specifies the upper 16 bits of the I/O base register. See Table 4−15 for a complete description of the register contents.

PCI register offset: 30h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−15. I/O Base Upper 16-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOBASE	RW	I/O base upper 16 bits. Defines the upper 16 bits of the lowest address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be 00000h.

4.25 I/O Limit Upper 16-Bit Register

This read/write register specifies the upper 16 bits of the I/O limit register. See Table 4−16 for a complete description of the register contents.

PCI register offset: 32h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−16. I/O Limit Upper 16-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOLIMIT	RW	I/O limit upper 16 bits. Defines the upper 16 bits of the top address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be FFFFFh.

4.26 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header where the PCI power management block resides. Since the PCI power management registers begin at 50h, this register is hardwired to 50h.

PCI register offset: 34h
Register type: Read-only
Default value: 50h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	1	0	0	0	0

4.27 Interrupt Line Register

This read/write register is programmed by the system and indicates to the software which interrupt line the bridge has assigned to it. The default value of this register is FFh, indicating that an interrupt line has not yet been assigned to the function. Since the bridge does not generate interrupts internally, this register is a scratch pad register.

PCI register offset: 3Ch
Register type: Read/Write
Default value: FFh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1

4.28 Interrupt Pin Register

The interrupt pin register is read-only 00h indicating that the bridge does not generate internal interrupts. While the bridge does not generate internal interrupts, it does forward interrupts from the secondary interface to the primary interface.

PCI register offset: 3Dh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.29 Bridge Control Register

The bridge control register provides extensions to the command register that are specific to a bridge. See Table 4−17 for a complete description of the register contents.

PCI register offset: 3Eh
Register type: Read-only, Read/Write, Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−17. Bridge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11	DTSERR	RW	Discard timer $\overline{\text{SERR}}$ enable. Applies only in conventional PCI mode. This bit enables the bridge to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the primary interface when the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge. The severity is selectable only if advanced error reporting is supported. 0 = Do not generate ERR_NONFATAL or ERR_FATAL on the primary interface as a result of the expiration of the secondary discard timer. Note that an error message can still be sent if advanced error reporting is supported and bit 10 (DISCARD_TIMER_MASK) in the secondary uncorrectable error mask register (offset 130h, see Section 5.11) is clear (default). 1 = Generate ERR_NONFATAL or ERR_FATAL on the primary interface if the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge
10	DTSTATUS	RCU	Discard timer status. This bit indicates if a discard timer expires and a delayed transaction is discarded. 0 = No discard timer error 1 = Discard timer error

Table 4−17. Bridge Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
9	SEC_DT	RW	Selects the number of PCI clocks that the bridge waits for a master on the secondary interface to repeat a delayed transaction request. The counter starts once the delayed completion (the completion of the delayed transaction on the primary interface) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the delayed transaction with the initiating master on the secondary bus). If the master does not repeat the transaction before the counter expires, then the bridge deletes the delayed transaction from its queue and sets the discard timer status bit. 0 = The secondary discard timer counts 2^{15} PCI clock cycles (default) 1 = The secondary discard timer counts 2^{10} PCI clock cycles
8	PRI_DEC	R	Primary discard timer. This bit has no meaning in PCI Express and is hardwired to 0b.
7	FBB_EN	RW	Fast back-to-back enable. This bit allows software to enable fast back-to-back transactions on the secondary PCI interface. 0 = Fast back-to-back transactions are disabled (default) 1 = Secondary interface fast back-to-back transactions are enabled
6	SRST	RW	Secondary bus reset. This bit is set when software wishes to reset all devices downstream of the bridge. Setting this bit causes the $\overline{\text{PRST}}$ terminal on the secondary interface to be asserted. 0 = Secondary interface is not in reset state (default) 1 = Secondary interface is in the reset state
5	MAM	RW	Master abort mode. This bit controls the behavior of the bridge when it receives a master abort or an unsupported request. 0 = Do not report master aborts. Returns FFFF FFFFh on reads and discards data on writes (default). 1 = Respond with an unsupported request on PCI Express when a master abort is received on PCI. Respond with target abort on PCI when an unsupported request completion on PCI Express is received. This bit also enables error signaling on master abort conditions on posted writes.
4	VGA16	RW	VGA 16-bit decode. This bit enables the bridge to provide full 16-bit decoding for VGA I/O addresses. This bit only has meaning if the VGA enable bit is set. 0 = Ignore address bits [15:10] when decoding VGA I/O addresses (default) 1 = Decode address bits [15:10] when decoding VGA I/O addresses
3	VGA	RW	VGA enable. This bit modifies the response by the bridge to VGA compatible addresses. If this bit is set, then the bridge decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A 0000h to 000B FFFFh • I/O addresses in the first 64 KB of the I/O address space (address bits [31:16] are 0000h) and where address bits [9:0] are in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – address bits [15:10] may possess any value and are not used in the decoding) If this bit is set, then forwarding of VGA addresses is independent of the value of bit 2 (ISA), the I/O address and memory address ranges defined by the I/O base and limit registers, the memory base and limit registers, and the prefetchable memory base and limit registers of the bridge. The forwarding of VGA addresses is qualified by bits 0 (IO_ENB) and 1 (MEMORY_ENB) in the command register (offset 04h, see Section 4.3). 0 = Do not forward VGA compatible memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges (default) 1 = Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the I/O enable and memory enable bits are set) independent of the I/O and memory address ranges and independent of the ISA enable bit

Table 4−17. Bridge Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2	ISA	RW	ISA enable. This bit modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, then the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1 KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1K block. 0 = Forward downstream all I/O addresses in the address range defined by the I/O base and I/O limit registers (default) 1 = Forward upstream ISA I/O addresses in the address range defined by the I/O base and I/O limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1-KB block)
1	SERR_EN	RW	SERR enable. This bit controls forwarding of system error events from the secondary interface to the primary interface. The bridge forwards system error events when: • This bit is set • Bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set • $\overline{\text{SERR}}$ is asserted on the secondary interface 0 = Disable the forwarding of system error events (default) 1 = Enable the forwarding of system error events
0	PERR_EN	RW	Parity error response enable. Controls the bridge's response to data, uncorrectable address, and attribute errors on the secondary interface. Also, the bridge always forwards data with poisoning, from conventional PCI to PCI Express on an uncorrectable conventional PCI data error, regardless of the setting of this bit. 0 = Ignore uncorrectable address, attribute, and data errors on the secondary interface (default) 1 = Enable uncorrectable address, attribute, and data error detection and reporting on the secondary interface

4.30 Capability ID Register

This read-only register identifies the linked list item as the register for PCI power management. The register returns 01h when read.

PCI register offset: 50h
Register type: Read-only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.31 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 60h pointing to the MSI capabilities registers.

PCI register offset: 51h
Register type: Read-only
Default value: 60h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	0	0	0	0	0

4.32 Power Management Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI power management. See Table 4−18 for a complete description of the register contents.

PCI register offset: 52h
Register type: Read-only
Default value: 0602h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0

Table 4−18. Power Management Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	PME_SUPPORT	R	$\overline{\text{PME}}$ support. This 5-bit field indicates the power states from which the bridge may assert $\overline{\text{PME}}$. Because the bridge never generates a $\overline{\text{PME}}$ except on a behalf of a secondary device, this field is read-only and returns 00000b.
10	D2_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D2 device power state.
9	D1_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D1 device power state.
8:6	AUX_CURRENT	R	3.3 V_{AUX} auxiliary current requirements. This field returns 000b since the bridge does not generate $\overline{\text{PME}}$ from $D3_{cold}$.
5	DSI	R	Device specific initialization. This bit returns 0b when read, indicating that the bridge does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Returns 0b when read.
3	PME_CLK	R	$\overline{\text{PME}}$ clock. This bit returns 0b indicating that the PCI clock is not needed to generate $\overline{\text{PME}}$.
2:0	PM_VERSION	R	Power management version. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.65) is 0b, then this field returns 010b indicating revision 1.1 compatibility. If PCI_PM_VERSION_CTRL is 1b, then this field returns 011b indicating revision 1.2 compatibility.

4.33 Power Management Control/Status Register

This register determines and changes the current power state of the bridge. No internal reset is generated when transitioning from the $D3_{hot}$ state to the D0 state. See Table 4−19 for a complete description of the register contents.

PCI register offset: 54h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−19. Power Management Control/Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PME_STAT	R	$\overline{\text{PME}}$ status. This bit is read-only and returns 0b when read.
14:13	DATA_SCALE	R	Data scale. This 2-bit field returns 00b when read since the bridge does not use the data register.
12:9	DATA_SEL	R	Data select. This 4-bit field returns 0h when read since the bridge does not use the data register.
8	PME_EN	RW	$\overline{\text{PME}}$ enable. This bit has no function and acts as scratchpad space. The default value for this bit is 0b.
7:4	RSVD	R	Reserved. Returns 0h when read.
3	NO_SOFT_RESET	R	No soft reset. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.65) is 0b, then this bit returns 0b for compatibility with version 1.1 of the *PCI Power Management Specification*. If PCI_PM_VERSION_CTRL is 1b, then this bit returns 1b indicating that no internal reset is generated and the device retains its configuration context when transitioning from the $D3_{hot}$ state to the D0 state.
2	RSVD	R	Reserved. Returns 0b when read.
1:0	PWR_STATE	RW	Power state. This 2-bit field determines the current power state of the function and sets the function into a new power state. This field is encoded as follows: 00 = D0 (default) 01 = D1 10 = D2 11 = $D3_{hot}$

4.34 Power Management Bridge Support Extension Register

This read-only register indicates to host software what the state of the secondary bus will be when the bridge is placed in D3. See Table 4−20 for a complete description of the register contents.

PCI register offset: 56h
Register type: Read-only
Default value: 40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4−20. Power Management Bridge Support Extension Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	BPCC	R	Bus power/clock control enable. This bit indicates to the host software if the bus secondary clocks are stopped when the bridge is placed in D3. The state of the BPCC bit is controlled by bit 11 (BPCC_E) in the general control register (offset D4h, see Section 4.65). 0 = The secondary bus clocks are not stopped in D3 1 = The secondary bus clocks are stopped in D3
6	BSTATE	R	B2/B3 support. This bit is read-only 1b indicating that the bus state in D3 is B2.
5:0	RSVD	R	Reserved. Returns 00 0000b when read.

4.35 Power Management Data Register

The read-only register is not applicable to the bridge and returns 00h when read.

PCI register offset: 57h
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.36 MSI Capability ID Register

This read-only register identifies the linked list item as the register for message signaled interrupts capabilities. The register returns 05h when read.

PCI register offset: 60h
Register type: Read-only
Default value: 05h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	1

4.37 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 80h pointing to the subsystem ID capabilities registers.

PCI register offset: 61h
Register type: Read-only
Default value: 80h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0

4.38 MSI Message Control Register

This register controls the sending of MSI messages. See Table 4−21 for a complete description of the register contents.

PCI register offset: 62h
Register type: Read-only, Read/Write
Default value: 0088h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

Table 4−21. MSI Message Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7	64CAP	R	64-bit message capability. This bit is read-only 1b indicating that the bridge supports 64-bit MSI message addressing.
6:4	MM_EN	RW	Multiple message enable. This bit indicates the number of distinct messages that the bridge is allowed to generate. 000 = 1 message (default) 001 = 2 messages 010 = 4 messages 011 = 8 messages 100 = 16 messages 101 = Reserved 110 = Reserved 111 = Reserved
3:1	MM_CAP	R	Multiple message capabilities. This field indicates the number of distinct messages that bridge is capable of generating. This field is read-only 100b indicating that the bridge can signal 1 interrupt for each IRQ supported on the serial IRQ stream up to a maximum of 16 unique interrupts.
0	MSI_EN	RW	MSI enable. This bit enables MSI interrupt signaling. MSI signaling must be enabled by software for the bridge to signal that a serial IRQ has been detected. 0 = MSI signaling is prohibited (default) 1 = MSI signaling is enabled

4.39 MSI Message Lower Address Register

This register contains the lower 32 bits of the address that a MSI message writes to when a serial IRQ is detected. See Table 4−22 for a complete description of the register contents.

PCI register offset: 64h
Register type: Read-only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−22. MSI Message Lower Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:2	ADDRESS	RW	System specified message address
1:0	RSVD	R	Reserved. Returns 00b when read.

4.40 MSI Message Upper Address Register

This register contains the upper 32 bits of the address that a MSI message writes to when a serial IRQ is detected. If this register contains 0000 0000h, then 32-bit addressing is used; otherwise, 64-bit addressing is used.

PCI register offset: 68h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.41 MSI Message Data Register

This register contains the data that software programmed the bridge to send when it send a MSI message. See Table 4−23 for a complete description of the register contents.

PCI register offset: 6Ch
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−23. MSI Message Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MSG	RW	System specific message. This field contains the portion of the message that the bridge forwards unmodified.
3:0	MSG_NUM	RW	Message number. This portion of the message field may be modified to contain the message number is multiple messages are enable. The number of bits that are modifiable depends on the number of messages enabled in the message control register. 1 message = No message data bits can be modified (default) 2 messages = Bit 0 can be modified 4 messages = Bits 1:0 can be modified 8 messages = Bits 2:0 can be modified 16 messages = Bits 3:0 can be modified

4.42 Capability ID Register

This read-only register identifies the linked list item as the register for subsystem ID and subsystem vendor ID capabilities. The register returns 0Dh when read.

PCI register offset: 80h
Register type: Read-only
Default value: 0Dh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	1	0	1

4.43 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 90h pointing to the PCI Express capabilities registers.

PCI register offset: 81h
Register type: Read-only
Default value: 90h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	1	0	0	0	0

4.44 Subsystem Vendor ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: 84h
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.45 Subsystem ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: 86h
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.46 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express capabilities. The register returns 10h when read.

PCI register offset: 90h
Register type: Read-only
Default value: 10h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0

4.47 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 00h indicating no additional capabilities are supported.

PCI register offset: 91h
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.48 PCI Express Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI Express. See Table 4−24 for a complete description of the register contents.

PCI register offset: 92h
Register type: Read-only
Default value: 0071h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1

Table 4−24. PCI Express Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:14	RSVD	R	Reserved. Returns 00b when read.
13:9	INT_NUM	R	Interrupt message number. This field is used for MSI support and is implemented as read-only 00000b in the bridge.
8	SLOT	R	Slot implemented. This bit is not valid for the bridge and is read-only 0b.
7:4	DEV_TYPE	R	Device/port type. This read-only field returns 7h indicating that the device is a PCI Express-to-PCI bridge.
3:0	VERSION	R	Capability version. This field returns 1h indicating revision 1 of the PCI Express capability.

4.49 Device Capabilities Register

The device capabilities register indicates the device specific capabilities of the bridge. See Table 4−25 for a complete description of the register contents.

PCI register offset: 94h
Register type: Read-only
Default value: 0000 0D82

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	1	1	0	1	1	0	0	0	0	0	1	0

Table 4−25. Device Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:28	RSVD	R	Reserved. Returns 0h when read.
27:26	CSPLS	RU	Captured slot power limit scale. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 9:8 are written to this field. The value in this field specifies the scale used for the slot power limit. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x
25:18	CSPLV	RU	Captured slot power limit value. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 7:0 are written to this field. The value in this field in combination with the slot power limit scale value (bits 27:26) specifies the upper limit of power supplied to the slot. The power limit is calculated by multiplying the value in this field by the value in the slot power limit scale field.
17:15	RSVD	R	Reserved. Returns 000b when read.
14	PIP	R	Power indicator present. This bit is hardwired to 0b indicating that a power indicator is not implemented.
13	AIP	R	Attention indicator present. This bit is hardwired to 0b indicating that an attention indicator is not implemented.
12	ABP	R	Attention button present. This bit is hardwired to 0b indicating that an attention button is not implemented.
11:9	EP_L1_LAT	RU	Endpoint L1 acceptable latency. This field indicates the maximum acceptable latency for a transition from L1 to L0 state. This field can be programmed by writing to the L1_LATENCY field (bits 15:13) in the general control register (offset D4h, see Section 4.65). The default value for this field is 110b which indicates a range from 32 μs to 64 μs. This field cannot be programmed to be less than the latency for the PHY to exit the L1 state.
8:6	EP_L0S_LAT	RU	Endpoint L0s acceptable latency. This field indicates the maximum acceptable latency for a transition from L0s to L0 state. This field can be programmed by writing to the L0s_LATENCY field (bits 18:16) in the general control register (offset D4h, see Section 4.65). The default value for this field is 110b which indicates a range from 2 μs to 4 μs. This field cannot be programmed to be less than the latency for the PHY to exit the L0s state.
5	ETFS	R	Extended tag field supported. This field indicates the size of the tag field not supported.
4:3	PFS	R	Phantom functions supported. This field is read-only 00b indicating that function numbers are not used for phantom functions.
2:0	MPSS	R	Maximum payload size supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 010b indicating the maximum payload size for a TLP is 512 bytes.

4.50 Device Control Register

The device control register controls PCI Express device specific parameters. See Table 4−26 for a complete description of the register contents.

PCI register offset: 98h
Register type: Read-only, Read/Write
Default value: 2800h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Table 4−26. Device Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	CFG_RTRY_ENB	RW	Configuration retry status enable. When this read/write bit is set to 1b, the bridge returns a completion with completion retry status on PCI Express if a configuration transaction forwarded to the secondary interface did not complete within the implementation specific time-out period. When this bit is set to 0b, the bridge does not generate completions with completion retry status on behalf of configuration transactions. The default value of this bit is 0b.
14:12	MRRS	RW	Maximum read request size. This field is programmed by host software to set the maximum size of a read request that the bridge can generate. The bridge uses this field in conjunction with the cache line size register (offset 0Ch, see Section 4.6) to determine how much data to fetch on a read request. This field is encoded as: 000 = 128B 001 = 256B 010 = 512B (default) 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
11	ENS	RW	Enable no snoop. Controls the setting of the no snoop flag within the TLP header for upstream memory transactions mapped to any traffic class mapped to a virtual channel (VC) other than VC0 through the upstream decode windows. 0 = No snoop field is 0b 1 = No snoop field is 1b (default)
10☆	APPE	RW	Auxiliary power PM enable. This bit has no effect in the bridge. 0 = AUX power is disabled (default) 1 = AUX power is enabled
9	PFE	R	Phantom function enable. Since the bridge does not support phantom functions, this bit is read-only 0b.
8	ETFE	R	Extended tag field enable. Since the bridge does not support extended tags, this bit is read-only 0b.
7:5	MPS	RW	Maximum payload size. This field is programmed by host software to set the maximum size of posted writes or read completions that the bridge can initiate. This field is encoded as: 000 = 128B (default) 001 = 256B 010 = 512B 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
4	ERO	R	Enable relaxed ordering. Since the bridge does not support relaxed ordering, this bit is read-only 0b.

☆This bit is sticky and must retain its value when the bridge is powered by V_{AUX}.

Table 4−26. Device Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
3	URRE	RW	Unsupported request reporting enable. If this bit is set, then the bridge sends an ERR_NONFATAL message to the root complex when an unsupported request is received. 0 = Do not report unsupported requests to the root complex (default) 1 = Report unsupported requests to the root complex
2	FERE	RW	Fatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_FATAL messages to the root complex when a system error event occurs. 0 = Do not report fatal errors to the root complex (default) 1 = Report fatal errors to the root complex
1	NFERE	RW	Nonfatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_NONFATAL messages to the root complex when a system error event occurs. 0 = Do not report nonfatal errors to the root complex (default) 1 = Report nonfatal errors to the root complex
0	CERE	RW	Correctable error reporting enable. If this bit is set, then the bridge is enabled to send ERR_COR messages to the root complex when a system error event occurs. 0 = Do not report correctable errors to the root complex (default) 1 = Report correctable errors to the root complex

4.51 Device Status Register

The device status register provides PCI Express device specific information to the system. See Table 4−27 for a complete description of the register contents.

PCI register offset: 9Ah
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−27. Device Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:6	RSVD	R	Reserved. Returns 00 0000 0000b when read.
5	PEND	RU	Transaction pending. This bit is set when the bridge has issued a nonposted transaction that has not been completed.
4	APD	RU	AUX power detected. This bit indicates that AUX power is present. 0 = No AUX power detected 1 = AUX power detected
3	URD	RCU	Unsupported request detected. This bit is set by the bridge when an unsupported request is received.
2	FED	RCU	Fatal error detected. This bit is set by the bridge when a fatal error is detected.
1	NFED	RCU	Nonfatal error detected. This bit is set by the bridge when a nonfatal error is detected.
0	CED	RCU	Correctable error detected. This bit is set by the bridge when a correctable error is detected.

4.52 Link Capabilities Register

The link capabilities register indicates the link specific capabilities of the bridge. See Table 4−28 for a complete description of the register contents.

PCI register offset: 9Ch
Register type: Read-only
Default value: 0002 XC11h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	x	x	x	1	1	0	0	0	0	0	1	0	0	0	1

Table 4−28. Link Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_NUM	R	Port number. This field indicates port number for the PCI Express link. This field is read-only 00h indicating that the link is associated with port 0.
23:18	RSVD	R	Reserved. Returns 00 0000b when read.
17:15	L1_LATENCY	R	L1 exit latency. This field indicates the time that it takes to transition from the L1 state to the L0 state. Bit 6 (CCC) in the link control register (offset A0h, see Section 4.53) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of this field is determined by bits 20:18 (L1_EXIT_LAT_ASYNC) of the control and diagnostic register 1 (offset C4h, see Section 4.62). For an asynchronous reference clock, the value of this field is determined by bits 17:15 (L1_EXIT_LAT_COMMON) of the control and diagnostic register 1 (offset C4h, see Section 4.62).
14:12	L0S_LATENCY	R	L0s exit latency. This field indicates the time that it takes to transition from the L0s state to the L0 state. Bit 6 (CCC) in the link control register (offset A0h, see Section 4.53) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of 011b indicates that the L1 exit latency falls between 256 ns to less than 512 ns. For an asynchronous reference clock, the value of 100b indicates that the L1 exit latency falls between 512 ns to less than 1 µs.
11:10	ASLPMS	R	Active state link PM support. This field indicates the level of active state power management that the bridge supports. The value 11b indicates support for both L0s and L1 through active state power management.
9:4	MLW	R	Maximum link width. This field is encoded 00 0001b to indicate that the bridge only supports a 1x PCI Express link.
3:0	MLS	R	Maximum link speed. This field is encoded 1h to indicate that the bridge supports a maximum link speed of 2.5 Gb/s.

4.53 Link Control Register

The link control register controls link specific behavior. See Table 4−29 for a complete description of the register contents.

PCI register offset: A0h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−29. Link Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7	ES	RW	Extended synch. This bit forces the bridge to extend the transmission of FTS ordered sets and an extra TS2 when exiting from L1 prior to entering to L0. 0 = Normal synch (default) 1 = Extended synch
6	CCC	RW	Common clock configuration. When this bit is set, it indicates that the bridge and the device at the opposite end of the link are operating with a common clock source. A value of 0b indicates that the bridge and the device at the opposite end of the link are operating with separate reference clock sources. The bridge uses this common clock configuration information to report the L0s and L1 exit latencies. 0 = Reference clock is asynchronous (default) 1 = Reference clock is common
5	RL	R	Retrain link. This bit has no function and is read-only 0b.
4	LD	R	Link disable. This bit has no function and is read-only 0b.
3	RCB	RW	Read completion boundary. This bit is an indication of the RCB of the root complex. The state of this bit has no affect on the bridge, since the RCB of the bridge is fixed at 128 bytes. 0 = 64 bytes (default) 1 = 128 bytes
2	RSVD	R	Reserved. Returns 0b when read.
1:0	ASLPMC	RW	Active state link PM control. This field enables and disables the active state PM. 00 = Active state PM disabled (default) 01 = L0s entry enabled 10 = L1 entry enabled 11 = L0s and L1 entry enabled

4.54 Link Status Register

The link status register indicates the current state of the PCI Express link. See Table 4−30 for a complete description of the register contents.

PCI register offset: A2h
Register type: Read-only
Default value: X011h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	x	0	0	0	0	0	0	0	1	0	0	0	1

Table 4−30. Link Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:13	RSVD	R	Reserved. Returns 000b when read.
12	SCC	R	Slot clock configuration. This bit indicates that the bridge uses the same physical reference clock that the platform provides on the connector. If the bridge uses an independent clock irrespective of the presence of a reference on the connector, then this bit must be cleared. 0 = Independent 125-MHz reference clock is used 1 = Common 100-MHz reference clock is used
11	LT	R	Link training. This bit has no function and is read-only 0b.
10	TE	R	Retrain link. This bit has no function and is read-only 0b.
9:4	NLW	R	Negotiated link width. This field is read-only 00 0001b indicating the lane width is 1x.
3:0	LS	R	Link speed. This field is read-only 1h indicating the link speed is 2.5 Gb/s.

4.55 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.57) that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) of the serial-bus control and status register (offset B3h, see Section 4.58) is cleared. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: B0h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.56 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to the serial-bus device. The word address is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.57) that initiates the bus cycle. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: B1h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.57 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the slave address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle is a read or a write cycle. Writing to this register initiates the cycle on the serial interface. See Table 4−31 for a complete description of the register contents.

PCI register offset: B2h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−31. Serial-Bus Slave Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1†	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0†	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle. 0 = A single byte write is requested (default) 1 = A single byte read is requested

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.58 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial bus. See Table 4−32 for a complete description of the register contents.

PCI register offset: B3h
Register type: Read-only, Read/Write, Read/Clear
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−32. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial-bus (default) 1 = Only the slave address is sent on the serial-bus
6	RSVD	R	Reserved. Returns 0b when read.
5†	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progress
4†	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. 0 = No EEPROM activity 1 = EEPROM download in progress
3†	SBDETECT	RWU	Serial EEPROM detected. This bit enables the serial-bus interface. The value of this bit controls whether the GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals or as serial-bus signals. This bit is automatically set to 1b when a serial EEPROM is detected. **Note:** A serial EEPROM is only detected once following $\overline{\text{PERST}}$. 0 = No EEPROM present, EEPROM load process does not happen. GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals. 1 = EEPROM present, EEPROM load process takes place. GPIO4//SCL and GPIO5//SDA terminals are configured as serial-bus signals.
2†	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz
1†	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0†	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 = No error 1 = EEPROM load error

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.59 GPIO Control Register

This register controls the direction of the eight GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO4 (SCL), and GPIO5 (SDA). See Table 4−33 for a complete description of the register contents.

PCI register offset: B4h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−33. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7†	GPIO7_DIR	RW	GPIO 7 data direction. This bit selects whether GPIO7 is in input or output mode. 0 = Input (default) 1 = Output
6†	GPIO6_DIR	RW	GPIO 6 data direction. This bit selects whether GPIO6 is in input or output mode. 0 = Input (default) 1 = Output
5†	GPIO5_DIR	RW	GPIO 5 data direction. This bit selects whether GPIO5 is in input or output mode. 0 = Input (default) 1 = Output
4†	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3†	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2†	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
1†	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0†	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.60 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO4 (SCL), and GPIO5 (SDA). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. See Table 4−34 for a complete description of the register contents.

PCI register offset: B6h
Register type: Read-only, Read/Write
Default value: 00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Table 4−34. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7†	GPIO7_DATA	RW	GPIO 7 data. This bit reads the state of GPIO7 when in input mode or changes the state of GPIO7 when in output mode.
6†	GPIO6_DATA	RW	GPIO 6 data. This bit reads the state of GPIO6 when in input mode or changes the state of GPIO6 when in output mode.
5†	GPIO5_DATA	RW	GPIO 5 data. This bit reads the state of GPIO5 when in input mode or changes the state of GPIO5 when in output mode.
4†	GPIO4_DATA	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3†	GPIO3_DATA	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2†	GPIO2_DATA	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1†	GPIO1_DATA	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0†	GPIO0_DATA	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.61 Control and Diagnostic Register 0

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4−35 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C0h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−35. Control and Diagnostic Register 0 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24†	PRI_BUS_NUM	R	This field contains the captured primary bus number
23:19†	PRI_DEVICE_ NUM	R	This field contains the captured primary device number
18:16	RSVD	R	Reserved. Returns 000b when read.
15:14†	RSVD	RW	Reserved. Bits 15:14 default to 00b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 00b.
13:12	RSVD	R	Reserved. Returns 00b when read.
11:8†	RSVD	RW	Reserved. Bits 11:8 default to 0000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0000b.
7	RSVD	R	Reserved. Returns 0b when read.
6†	PREFETCH_4X	RW	Prefetch 4X enable. This bit sets the prefetch behavior for upstream memory read multiple transactions. If bit 24 (FORCE_MRM) in the general control register (offset D4h, see Section 4.65) is set, then all upstream memory read transactions will prefetch the indicated number of cache lines. If bit 19 (READ_PREFETCH_DIS) in the general control register (offset D4h, see Section 4.65) is set, then this bit has no effect and only 1 DWORD will be fetched. 0 = The bridge will prefetch up to 2 cache lines, as defined in the cache line size register (offset 0Ch, see Section 4.6) for upstream memory read multiple (MRM) transactions (default) 1 = The bridge device will prefetch up to 4 cache lines, as defined in the cache line size register (offset 0Ch, see Section 4.6) for upstream memory read multiple (MRM) transactions.
5:4†	UP_REQ_BUF _VALUE	RW	PCI upstream req−res buffer threshold value. The value in this field controls the buffer space that must be available for the bridge to accept a PCI bus transaction. If the cache line size is not valid, then the bridge will use 8 DW for calculating the threshold value 00 = 1 Cacheline + 4 DW (default) 01 = 1 Cacheline + 8 DW 10 = 1 Cacheline + 12 DW 11 = 2 Cachelines + 4 DW
3†	UP_REQ_BUF _CTRL	RW	PCI upstream req-res buffer threshold control. This bit enables the PCI upstream req-res buffer threshold control mode of the bridge. 0 = PCI upstream req-res buffer threshold control mode disabled (default) 1 = PCI upstream req-res buffer threshold control mode enabled
2†	CFG_ACCESS _MEM_REG	RW	Configuration access to memory-mapped registers. When this bit is set, the bridge allows configuration access to memory-mapped configuration registers.
1†	RSVD	RW	Reserved. Bit 1 defaults to 0b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0b.
0	RSVD	R	Reserved. Returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.62 Control and Diagnostic Register 1

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4−36 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C4h
Register type: Read/Write
Default value: 0012 0108h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0

Table 4−36. Control and Diagnostic Register 1 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
32:21	RSVD	R	Reserved. Returns 000h when read.
20:18†	L1_EXIT_LAT_ ASYNC	RW	L1 exit latency for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is set, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 9Ch, see Section 4.52). This field defaults to 100b.
17:15†	L1_EXIT_LAT_ COMMON	RW	L1 exit latency for common clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is clear, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 9Ch, see Section 4.52). This field defaults to 100b.
14:11†	RSVD	RW	Reserved. Bits 14:11 default to 0000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0000b.
10†	SBUS_RESET _MASK	RW	Secondary bus reset bit mask. When this bit is set, the bridge masks the reset caused by bit 6 (SRST) of the bridge control register (offset 3Eh, see Section 4.29). This bit defaults to 0b.
9:6†	L1ASPM_ TIMER	RW	L1ASPM entry timer. This field specifies the value (in 512-ns ticks) of the L1ASPM entry timer. This field defaults to 0100b.
5:2†	L0s_TIMER	RW	L0s entry timer. This field specifies the value (in 62.5-MHz clock ticks) of the L0s entry timer. This field defaults to 0010b.
1:0†	RSVD	RW	Reserved. Bits 1:0 default to 00b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00b.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.63 Control and Diagnostic Register 2

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4−37 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C8h
Register type: Read/Write
Default value: 3214 6000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−37. Control and Diagnostic Register 2 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24†	N_FTS_ ASYNC_CLK	RW	N_FTS for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is clear, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field shall default to 32h.
23:16†	N_FTS_ COMMON_ CLK	RW	N_FTS for common clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is set, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field defaults to 14h.
15:13	PHY_REV	R	PHY revision number
12:8†	LINK_NUM	RW	Link number
7:6	RSVD	R	Reserved. Returns 00b when read.
5:0	BAROWE	RW	BAR 0 Write Enable. When this bit is clear (default), the Base Address at offset 10h is read only and writes to that register will have no effect. When this bit is set, then bits 31:12 of the Base Address Register becomes writeable allowing the address of the 4K window to the Memory Mapped TI Proprietary Registers to be changed.
4:0†	RSVD	RW	Reserved. Bits 4:0 default to 00000b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00000b.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.64 Subsystem Access Register

The contents of this read/write register are aliased to the subsystem vendor ID and subsystem ID registers at PCI offsets 84h and 86h. See Table 4−38 for a complete description of the register contents.

PCI register offset: D0h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−38. Subsystem Access Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:16†	SubsystemID	RW	Subsystem ID. The value written to this field is aliased to the subsystem ID register at PCI offset 86h (see Section 4.45).
15:0†	SubsystemVendorID	RW	Subsystem vendor ID. The value written to this field is aliased to the subsystem vendor ID register at PCI offset 84h (see Section 4.44).

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.65 General Control Register

This read/write register controls various functions of the bridge. See Table 4−39 for a complete description of the register contents.

PCI register offset: D4h
Register type: Read-only, Read/Write
Default value: 8206 C000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−39. General Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:30†	CFG_RETRY_CNTR	RW	Configuration retry counter. Configures the amount of time that a configuration request must be retried on the secondary PCI bus before it may be completed with configuration retry status on the PCI Express side. 00 = 25 µs 01 = 1 ms 10 = 25 ms (default) 11 = 50 ms
29:28	RSVD	R	Reserved. Returns 00b when read.
27†	LOW_POWER_EN	RW	Low-power enable. When this bit is set, the half-ampitude, no preemphasis mode for the PCI Express TX drivers is enabled. The default for this bit is 0b.
26†	PCI_PM_VERSION_CTRL	RW	PCI power management version control. This bit controls the value reported in bits 2:0 (PM_VERSION) in the power management capabilities register (offset 52h, see Section 4.32). It also controls the value of bit 3 (NO_SOFT_RESET) in the power management control/status register (offset 54h, see Section 4.33). 0 = Version fields reports 010b and NO_SOFT_RESET reports 0b for Power Management 1.1 compliance (default) 1 = Version fields reports 011b and NO_SOFT_RESET reports 1b for Power Management 1.2 compliance
25†	STRICT_PRIORITY_EN	RW	Strict priority enable. When this bit is set and bits 6:4 (LOW_PRIORITY_COUNT) in the port VC capability register 1 (offset 154h, see Section 5.17) are 000b, meaning that strict priority VC arbitration is used, the extended VC always receives priority over VC0 at the PCI Express port. 0 = The default LOW_PRIORITY_COUNT is 001b 1 = The default LOW_PRIORITY_COUNT is 000b (default)
24†	FORCE_MRM	RW	Force memory read multiple 0 = Memory read multiple transactions are disabled (default) 1 = All upstream memory read transactions initiated on the PCI bus are treated as though they are memory read multiple transactions where prefetching is supported
23†	ASPM_CTRL_DEF_OVRD	RW	Active state power management control default override. This bit determines the power-up default for bits 1:0 (ASLPMC) of the link control register (offset A0h, see Section 4.53) in the PCI Express capability structure. 0 = Power-on default indicates that active state power management is disabled (00b) (default) 1 = Power-on default indicates that active state power management is enabled for L0s and L1 (11b)
22:20†	POWER_OVRD	RW	Power override. This bit field determines how the bridge responds when the slot power limit is less than the amount of power required by the bridge and the devices behind the bridge. 000 = Ignore slot power limit (default) 001 = Assert the PWR_OVRD terminal 010 = Disable secondary clocks selected by the clock mask register 011 = Disable secondary clocks selected by the clock mask register and assert the PWR_OVRD terminal 100 = Respond with unsupported request to all transactions except for configuration transactions (type 0 or type 1) and set slot power limit messages 101, 110, 111 = Reserved

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4−39. General Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
19†	READ_ PREFETCH_ DIS	RW	Read prefetch disable. This bit controls the prefetch functionality on PCI memory read transactions. 0 = Prefetch to the next cache line boundary on a burst read (default) 1 = Fetch only a single DWORD on a burst read
18:16†	L0s_LATENCY	RW	L0s maximum exit latency. This field programs the maximum acceptable latency when exiting the L0s state. This sets bits 8:6 (EP_L0S_LAT) in the device capabilities register (offset 94h, see Section 4.49). 000 = Less than 64 ns 001 = 64 ns up to less than 128 ns 010 = 128 ns up to less than 256 ns 011 = 256 ns up to less than 512 ns 100 = 512 ns up to less than 1 μs 101 = 1 μs up to less than 2 μs 110 = 2 μs to 4 μs (default) 111 = More than 4 μs
15:13†	L1_LATENCY	RW	L1 maximum exit latency. This field programs the maximum acceptable latency when exiting the L1 state. This sets bits 11:9 (EP_L1_LAT) in the device capabilities register (offset 94h, see Section 4.49). 000 = Less than 1 μs 001 = 1 μs up to less than 2 μs 010 = 2 μs up to less than 4 μs 011 = 4 μs up to less than 8 μs 100 = 8 μs up to less than 16 μs 101 = 16 μs up to less than 32 μs 110 = 32 μs to 64 μs (default) 111 = More than 64 μs
12†	VC_CAP_EN	RW	VC capability structure enable. This bit enables the VC capability structure by changing the next offset field of the advanced error reporting capability register at offset 102h. 0 = VC capability structure disabled (offset field = 000h) 1 = VC capability structure enabled (offset field = 150h)
11☆	BPCC_E	RW	Bus power clock control enable. This bit controls whether the secondary bus PCI clocks are stopped when the bridge is placed in the D3 state. It is assumed that if the secondary bus clocks are required to be active, that a reference clock continues to be provided on the PCI Express interface. 0 = Secondary bus clocks are not stopped in D3 (default) 1 = Secondary bus clocks are stopped on D3
10☆	BEACON_ ENABLE	RW	Beacon enable. This bit controls the mechanism for waking up the physical PCI Express link when in L2. 0 = $\overline{\text{WAKE}}$ mechanism is used exclusively. Beacon is not used (default). 1 = Beacon and $\overline{\text{WAKE}}$ mechanisms are used
9:8†	MIN_POWER_ SCALE	RW	Minimum power scale. This value is programmed to indicate the scale of bits 7:0 (MIN_POWER_VALUE). 00 = 1.0x (default) 01 = 0.1x 10 = 0.01x 11 = 0.001x
7:0†	MIN_POWER_ VALUE	RW	Minimum power value. This value is programmed to indicate the minimum power requirements. This value is multiplied by the minimum power scale field (bits 9:8) to determine the minimum power requirements for the bridge. The default is 00h, because this feature is only usable when the system implementer adds the PCI devices' power consumption to the bridge power consumption and reprograms this field with an EEPROM or the system BIOS.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

☆These bits are sticky and must retain their value when the bridge is powered by V_{AUX}.

4.66 Clock Control Register

This register enables and disables the PCI clock outputs (CLKOUT). See Table 4−40 for a complete description of the register contents.

PCI register offset: D8h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−40. Clock Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	RSVD	R	Reserved. Returns 0b when read.
6†	CLOCK6_DISABLE	RW	Clock output 6 disable. This bit disables secondary CLKOUT6. 0 = Clock enabled (default) 1 = Clock disabled
5†	CLOCK5_DISABLE	RW	Clock output 5 disable. This bit disables secondary CLKOUT5. 0 = Clock enabled (default) 1 = Clock disabled
4†	CLOCK4_DISABLE	RW	Clock output 4 disable. This bit disables secondary CLKOUT4. 0 = Clock enabled (default) 1 = Clock disabled
3†	CLOCK3_DISABLE	RW	Clock output 3 disable. This bit disables secondary CLKOUT3. 0 = Clock enabled (default) 1 = Clock disabled
2†	CLOCK2_DISABLE	RW	Clock output 2 disable. This bit disables secondary CLKOUT2. 0 = Clock enabled (default) 1 = Clock disabled
1†	CLOCK1_DISABLE	RW	Clock output 1 disable. This bit disables secondary CLKOUT1. 0 = Clock enabled (default) 1 = Clock disabled
0†	CLOCK0_DISABLE	RW	Clock output 0 disable. This bit disables secondary CLKOUT0. 0 = Clock enabled (default) 1 = Clock disabled

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.67 Clock Mask Register

This register selects which PCI bus clocks are disabled when bits 22:20 (POWER_OVRD) in the general control register (offset D4h, see Section 4.65) are set to 010h or 011h. This register has no effect on the clock outputs if the POWER_OVRD bits are not set to 010h or 011h or if the slot power limit is greater than the power required. See Table 4−41 for a complete description of the register contents.

PCI register offset: D9h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−41. Clock Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	RSVD	R	Reserved. Returns 0b when read.
6†	CLOCK6_MASK	RW	Clock output 6 mask. This bit disables PCI bus CLKOUT6 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
5†	CLOCK5_MASK	RW	Clock output 5 mask. This bit disables PCI bus CLKOUT5 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
4†	CLOCK4_MASK	RW	Clock output 4 mask. This bit disables PCI bus CLKOUT4 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
3†	CLOCK3_MASK	RW	Clock output 3 mask. This bit disables PCI bus CLKOUT3 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
2†	CLOCK2_MASK	RW	Clock output 2 mask. This bit disables PCI bus CLKOUT2 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
1†	CLOCK1_MASK	RW	Clock output 1 mask. This bit disables PCI bus CLKOUT1 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
0†	CLOCK0_MASK	RW	Clock output 0 mask. This bit disables PCI bus CLKOUT0 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.68 Clock Run Status Register

The clock run status register indicates the state of the PCI clock-run features in the bridge. See Table 4−42 for a complete description of the register contents.

PCI register offset: DAh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−42. Clock Run Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1	RSVD	R	Reserved. Returns 000 0000b when read.
0†	SEC_CLK_STATUS	RU	Secondary clock status. This bit indicates the status of the PCI bus secondary clock outputs. 0 = Secondary clock running 1 = Secondary clock stopped

† This bit is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.69 Arbiter Control Register

The arbiter control register controls the bridge internal arbiter. The arbitration scheme used is a two-tier rotational arbitration. The bridge is the only secondary bus master that defaults to the higher priority arbitration tier. See Table 4−43 for a complete description of the register contents.

PCI register offset: DCh
Register type: Read/Write
Default value: 40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4−43. Arbiter Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	PARK	RW	Bus parking mode. This bit determines where the internal arbiter parks the secondary bus. When this bit is set, the arbiter parks the secondary bus on the bridge. When this bit is cleared, the arbiter parks the bus on the last device mastering the secondary bus. 0 = Park the secondary bus on the last secondary bus master (default) 1 = Park the secondary bus on the bridge
6†	BRIDGE_TIER_SEL	RW	Bridge tier select. This bit determines in which tier the bridge is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
5†	TIER_SEL5	RW	$\overline{\text{GNT5}}$ tier select. This bit determines in which tier $\overline{\text{GNT5}}$ is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
4†	TIER_SEL4	RW	$\overline{\text{GNT4}}$ tier select. This bit determines in which tier $\overline{\text{GNT4}}$ is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
3†	TIER_SEL3	RW	$\overline{\text{GNT3}}$ tier select. This bit determines in which tier $\overline{\text{GNT3}}$ is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
2†	TIER_SEL2	RW	$\overline{\text{GNT2}}$ tier select. This bit determines in which tier $\overline{\text{GNT2}}$ is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
1†	TIER_SEL1	RW	$\overline{\text{GNT1}}$ tier select. This bit determines in which tier $\overline{\text{GNT1}}$ is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
0†	TIER_SEL0	RW	$\overline{\text{GNT0}}$ tier select. This bit determines in which tier $\overline{\text{GNT0}}$ is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)

† Thes bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.70 Arbiter Request Mask Register

The arbiter request mask register enables and disables support for requests from specific masters on the secondary bus. The arbiter request mask register also controls if a request input is automatically masked on an arbiter time-out. See Table 4−44 for a complete description of the register contents.

PCI register offset: DDh
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−44. Arbiter Request Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	ARB_TIMEOUT	RW	Arbiter time-out. This bit enables the arbiter time-out feature. The arbiter time-out is defined as the number of PCI clocks after the PCI bus has gone idle for a device to assert $\overline{\text{FRAME}}$ before the arbiter assumes the device will not respond. 0 = Arbiter time disabled (default) 1 = Arbiter time-out set to 16 PCI clocks
6†	AUTO_MASK	RW	Automatic request mask. This bit enables automatic request masking when an arbiter time-out occurs. 0 = Automatic request masking disabled (default) 1 = Automatic request masking enabled
5†	REQ5_MASK	RW	Request 5 ($\overline{\text{REQ5}}$) mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 5. 0 = Use request 5 (default) 1 = Ignore request 5
4†	REQ4_MASK	RW	Request 4 ($\overline{\text{REQ4}}$) mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 4. 0 = Use request 4 (default) 1 = Ignore request 4
3†	REQ3_MASK	RW	Request 3 ($\overline{\text{REQ3}}$) mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 3. 0 = Use request 3 (default) 1 = Ignore request 3
2†	REQ2_MASK	RW	Request 2 ($\overline{\text{REQ2}}$) mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 2. 0 = Use request 2 (default) 1 = Ignore request 2
1†	REQ1_MASK	RW	Request 1 ($\overline{\text{REQ1}}$) mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 1. 0 = Use request 1 (default) 1 = Ignore request 1
0†	REQ0_MASK	RW	Request 0 ($\overline{\text{REQ0}}$) mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use request 0 (default) 1 = Ignore request 0

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.71 Arbiter Time-Out Status Register

The arbiter time-out status register contains the status of each request (request 5–0) time-out. The time-out status bit for the respective request is set if the device did not assert $\overline{\text{FRAME}}$ after the arbiter time-out value. See Table 4−45 for a complete description of the register contents.

PCI register offset: DEh
Register type: Read/Clear
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−45. Arbiter Time-Out Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:6	RSVD	R	Reserved. Returns 00b when read.
5	REQ5_TO	RCU	Request 5 time-out status 0 = No time-out 1 = Time-out has occurred
4	REQ4_TO	RCU	Request 4 time-out status 0 = No time-out 1 = Time-out has occurred
3	REQ3_TO	RCU	Request 3 time-out status 0 = No time-out 1 = Time-out has occurred
2	REQ2_TO	RCU	Request 2 time-out status 0 = No time-out 1 = Time-out has occurred
1	REQ1_TO	RCU	Request 1 time-out status 0 = No time-out 1 = Time-out has occurred
0	REQ0_TO	RCU	Request 0 time-out status 0 = No time-out 1 = Time-out has occurred

NOTE: If bit 6 (AUTO_MASK) in the arbiter request mask register (offset DDh, see Section 4.70) is asserted and a PCI bus request time-out is detected, then the request time-out status bits require a special reset sequence. First, the AUTO_MASK bit must be cleared to 0b. Then, the REQ[5:0]_TO bit will clear after a write-back of 1b.

4.72 Serial IRQ Mode Control Register

This register controls the behavior of the serial IRQ controller. See Table 4−46 for a complete description of the register contents.

PCI register offset: E0h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4−46. Serial IRQ Mode Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	R	Reserved. Returns 0h when read.
3:2†	START_WIDTH	RW	Start frame pulse width. Sets the width of the start frame for a SERIRQ stream. 00 = 4 clocks (default) 01 = 6 clocks 10 = 8 clocks 11 = Reserved
1†	POLLMODE	RW	Poll mode. This bit selects between continuous and quiet mode. 0 = Continuous mode (default) 1 = Quiet mode
0†	DRIVEMODE	RW	Drive mode. This bit selects the behavior of the serial IRQ controller during the recovery cycle. 0 = Drive high (default) 1 = 3-state

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.73 Serial IRQ Edge Control Register

This register controls the edge mode or level mode for each IRQ in the serial IRQ stream. See Table 4−47 for a complete description of the register contents.

PCI register offset: E2h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−47. Serial IRQ Edge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15†	IRQ15_MODE	RW	IRQ 15 edge mode 0 = Edge mode (default) 1 = Level mode
14†	IRQ14_MODE	RW	IRQ 14 edge mode 0 = Edge mode (default) 1 = Level mode
13†	IRQ13_MODE	RW	IRQ 13 edge mode 0 = Edge mode (default) 1 = Level mode
12†	IRQ12_MODE	RW	IRQ 12 edge mode 0 = Edge mode (default) 1 = Level mode
11†	IRQ11_MODE	RW	IRQ 11 edge mode 0 = Edge mode (default) 1 = Level mode
10†	IRQ10_MODE	RW	IRQ 10 edge mode 0 = Edge mode (default) 1 = Level mode
9†	IRQ9_MODE	RW	IRQ 9 edge mode 0 = Edge mode (default) 1 = Level mode
8†	IRQ8_MODE	RW	IRQ 8 edge mode 0 = Edge mode (default) 1 = Level mode
7†	IRQ7_MODE	RW	IRQ 7 edge mode 0 = Edge mode (default) 1 = Level mode
6†	IRQ6_MODE	RW	IRQ 6 edge mode 0 = Edge mode (default) 1 = Level mode
5†	IRQ5_MODE	RW	IRQ 5 edge mode 0 = Edge mode (default) 1 = Level mode
4†	IRQ4_MODE	RW	IRQ 4 edge mode 0 = Edge mode (default) 1 = Level mode
3†	IRQ3_MODE	RW	IRQ 3 edge mode 0 = Edge mode (default) 1 = Level mode
2†	IRQ2_MODE	RW	IRQ 2 edge mode 0 = Edge mode (default) 1 = Level mode

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4−47. Serial IRQ Edge Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
1†	IRQ1_MODE	RW	IRQ 1 edge mode 0 = Edge mode (default) 1 = Level mode
0†	IRQ0_MODE	RW	IRQ 0 edge mode 0 = Edge mode (default) 1 = Level mode

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.74 Serial IRQ Status Register

This register indicates when a level mode IRQ is signaled on the serial IRQ stream. After a level mode IRQ is signaled, a write-back of 1b to the asserted IRQ status bit re-arms the interrupt. IRQ interrupts that are defined as edge mode in the serial IRQ edge control register are not reported in this status register. See Table 4−48 for a complete description of the register contents.

PCI register offset: E4h
Register type: Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4−48. Serial IRQ Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	IRQ15	RCU	IRQ 15 asserted. This bit indicates that the IRQ15 has been asserted. 0 = Deasserted 1 = Asserted
14	IRQ14	RCU	IRQ 14 asserted. This bit indicates that the IRQ14 has been asserted. 0 = Deasserted 1 = Asserted
13	IRQ13	RCU	IRQ 13 asserted. This bit indicates that the IRQ13 has been asserted. 0 = Deasserted 1 = Asserted
12	IRQ12	RCU	IRQ 12 asserted. This bit indicates that the IRQ12 has been asserted. 0 = Deasserted 1 = Asserted
11	IRQ11	RCU	IRQ 11 asserted. This bit indicates that the IRQ11 has been asserted. 0 = Deasserted 1 = Asserted
10	IRQ10	RCU	IRQ 10 asserted. This bit indicates that the IRQ10 has been asserted. 0 = Deasserted 1 = Asserted
9	IRQ9	RCU	IRQ 9 asserted. This bit indicates that the IRQ9 has been asserted. 0 = Deasserted 1 = Asserted
8	IRQ8	RCU	IRQ 8 asserted. This bit indicates that the IRQ8 has been asserted. 0 = Deasserted 1 = Asserted
7	IRQ7	RCU	IRQ 7 asserted. This bit indicates that the IRQ7 has been asserted. 0 = Deasserted 1 = Asserted

Table 4−48. Serial IRQ Status Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
6	IRQ6	RCU	IRQ 6 asserted. This bit indicates that the IRQ6 has been asserted. 0 = Deasserted 1 = Asserted
5	IRQ5	RCU	IRQ 5 asserted. This bit indicates that the IRQ5 has been asserted. 0 = Deasserted 1 = Asserted
4	IRQ4	RCU	IRQ 4 asserted. This bit indicates that the IRQ4 has been asserted. 0 = Deasserted 1 = Asserted
3	IRQ3	RCU	IRQ 3 asserted. This bit indicates that the IRQ3 has been asserted. 0 = Deasserted 1 = Asserted
2	IRQ2	RCU	IRQ 2 asserted. This bit indicates that the IRQ2 has been asserted. 0 = Deasserted 1 = Asserted
1	IRQ1	RCU	IRQ 1 asserted. This bit indicates that the IRQ1 has been asserted. 0 = Deasserted 1 = Asserted
0	IRQ0	RCU	IRQ 0 asserted. This bit indicates that the IRQ0 has been asserted. 0 = Deasserted 1 = Asserted

5 PCI Express Extended Configuration Space

The programming model of the PCI Express extended configuration space is compliant to the *PCI Express Base Specification* and the *PCI Express to PCI/PCI-X Bridge Specification* programming models. The PCI Express extended configuration map uses the PCI Express advanced error reporting capability and PCI Express virtual channel (VC) capability headers.

All bits marked with a ☆ are sticky bits and are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a † are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 5−1. PCI Express Extended Configuration Register Map

REGISTER NAME		OFFSET
Next capability offset / capability version	PCI Express advanced error reporting capabilities ID	100h
Uncorrectable error status register†		104h
Uncorrectable error mask register†		108h
Uncorrectable error severity register†		10Ch
Correctable error status register†		110h
Correctable error mask†		114h
Advanced error capabilities and control†		118h
Header log register†		11Ch
Header log register†		120h
Header log register†		124h
Header log register†		128h
Secondary uncorrectable error status†		12Ch
Secondary uncorrectable error mask†		130h
Secondary uncorrectable error severity register†		134h
Secondary error capabilities and control register†		138h
Secondary header log register†		13Ch
Secondary header log register†		140h
Secondary header log register†		144h
Secondary header log register†		148h
Reserved		14Ch
Next capability offset / capability version	PCI express virtual channel extended capabilities ID	150h
Port VC capability register 1		154h
Port VC capability register 2		158h
Port VC status register	Port VC control register	15Ch
VC resource capability register (VC0)		160h
VC resource control register (VC0)		164h
VC resource status register (VC0)	Reserved	168h
VC resource capability register (VC1)		16Ch
VC resource control register (VC1)		170h
VC resource status register (VC1)	Reserved	174h
Reserved		178h – 17Ch
VC arbitration table (phase 7 − phase 0)		180h
VC arbitration table (phase 15 − phase 8)		184h
VC arbitration table (phase 23 − phase 16)		188h

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 5−1. PCI Express Extended Configuration Register Map (Continued)

REGISTER NAME	OFFSET
VC arbitration table (phase 31 − phase 24)	18Ch
Reserved	190h – 1BCh
Port arbitration table for VC1 (phase 7 – phase 0)	1C0h
Port arbitration table for VC1 (phase 15 – phase 8)	1C4h
Port arbitration table for VC1 (phase 23 – phase 16)	1C8h
Port arbitration table for VC1 (phase 31 – phase 24)	1CCh
Port arbitration table for VC1 (phase 39 – phase 32)	1D0h
Port arbitration table for VC1 (phase 47 – phase 40)	1D4h
Port arbitration table for VC1 (phase 55 – phase 48)	1D8h
Port arbitration table for VC1 (phase 63 – phase 56)	1DCh
Port arbitration table for VC1 (phase 71 – phase 64)	1E0h
Port arbitration table for VC1 (phase 79 – phase 72)	1E4h
Port arbitration table for VC1 (phase 87 – phase 80)	1E8h
Port arbitration table for VC1 (phase 95 – phase 88)	1ECh
Port arbitration table for VC1 (phase 103 – phase 96)	1F0h
Port arbitration table for VC1 (phase 111 – phase 104)	1F4h
Port arbitration table for VC1 (phase 119 – phase 112)	1F8h
Port arbitration table for VC1 (phase 127 – phase 120)	1FCh
Reserved	200h – FFCh

5.1 Advanced Error Reporting Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express advanced error reporting capabilities. The register returns 0001h when read.

PCI Express extended register offset: 100h
Register type: Read-only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

5.2 Next Capability Offset/Capability Version Register

This read-only register identifies the next location in the PCI Express extended capabilities link list. If bit 12 (VC_CAP_EN) in the general control register (offset D4h, see Section 4.65) is 0b, then the upper 12 bits in this register are 000h, indicating the end of the linked list. If VC_CAP_EN is 1b, then the upper 12 bits in this register are 150h, indicating the existance of the VC capability structure at offset 150h. The four least significant bits identify the revision of the current capability block as 1h.

PCI Express extended register offset: 102h
Register type: Read-only
Default value: XX01h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	x	0	x	0	x	0	0	0	0	0	0	0	1

5.3 Uncorrectable Error Status Register

The uncorrectable error status register reports the status of individual errors as they occur on the primary PCI Express interface. Software may only clear these bits by writing a 1b to the desired location. See Table 5−2 for a complete description of the register contents.

PCI Express extended register offset: 104h
Register type: Read-only, Read/Clear
Default value: 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−2. Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20†	UR_ERROR	RCU	Unsupported request error. This bit is asserted when an unsupported request is received.
19†	ECRC_ERROR	RCU	Extended CRC error. This bit is asserted when an extended CRC error is detected.
18†	MAL_TLP	RCU	Malformed TLP. This bit is asserted when a malformed TLP is detected.
17†	RX_OVERFLOW	RCU	Receiver overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued.
16†	UNXP_CPL	RCU	Unexpected completion. This bit is asserted when a completion packet is received that does not correspond to an issued request.
15†	CPL_ABORT	RCU	Completer abort. This bit is asserted when the bridge signals a completer abort.
14†	CPL_TIMEOUT	RCU	Completion time-out. This bit is asserted when no completion has been received for an issued request before the time-out period.
13†	FC_ERROR	RCU	Flow control error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation.
12†	PSN_TLP	RCU	Poisoned TLP. This bit is asserted when a poisoned TLP is received.
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4†	DLL_ERROR	RCU	Data link protocol error. This bit is asserted if a data link-layer protocol error is detected.
3:0	RSVD	R	Reserved. Returns 0h when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.4 Uncorrectable Error Mask Register

The uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5−3 for a complete description of the register contents.

PCI Express extended register offset: 108h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−3. Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20†	UR_ERROR_MASK	RW	Unsupported request error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
19†	ECRC_ERROR_MASK	RW	Extended CRC error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
18†	MAL_TLP_MASK	RW	Malformed TLP mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
17†	RX_OVERFLOW_MASK	RW	Receiver overflow mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
16†	UNXP_CPL_MASK	RW	Unexpected completion mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
15†	CPL_ABORT_MASK	RW	Completer abort mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
14†	CPL_TIMEOUT_MASK	RW	Completion time-out mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
13†	FC_ERROR_MASK	RW	Flow control error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
12†	PSN_TLP_MASK	RW	Poisoned TLP mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4†	DLL_ERROR_MASK	RW	Data link protocol error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
3:0	RSVD	R	Reserved. Returns 0h when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.5 Uncorrectable Error Severity Register

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5−4 for a complete description of the register contents.

PCI Express extended register offset: 10Ch
Register type: Read-only, Read/Write
Default value: 0006 2011h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1

Table 5−4. Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20†	UR_ERROR_SEVR	RW	Unsupported request error severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
19†	ECRC_ERROR_SEVR	RW	Extended CRC error severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
18†	MAL_TLP_SEVR	RW	Malformed TLP severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
17†	RX_OVERFLOW_SEVR	RW	Receiver overflow severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
16†	UNXP_CPL_SEVR	RW	Unexpected completion severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
15†	CPL_ABORT_SEVR	RW	Completer abort severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
14†	CPL_TIMEOUT_SEVR	RW	Completion time-out severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
13†	FC_ERROR_SEVR	RW	Flow control error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
12†	PSN_TLP_SEVR	RW	Poisoned TLP severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4†	DLL_ERROR_SEVR	RW	Data link protocol error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
3:1	RSVD	R	Reserved. Return 000b when read.
0	RSVD	R	Reserved. Returns 1b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.6 Correctable Error Status Register

The correctable error status register reports the status of individual errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5−5 for a complete description of the register contents.

PCI Express extended register offset: 110h
Register type: Read-only, Read/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−5. Correctable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:13	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
12†	REPLAY_TMOUT	RCU	Replay timer time-out. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged.
11:9	RSVD	R	Reserved. Returns 000b when read.
8†	REPLAY_ROLL	RCU	REPLAY_NUM rollover. This bit is asserted when the replay counter rolls over after a pending request or completion has not been acknowledged.
7†	BAD_DLLP	RCU	Bad DLLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a DLLP.
6†	BAD_TLP	RCU	Bad TLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a TLP.
5:1	RSVD	R	Reserved. Returns 00000b when read.
0†	RX_ERROR	RCU	Receiver error. This bit is asserted when an 8b/10b error is detected by the PHY at any time.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.7 Correctable Error Mask Register

The correctable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5−6 for a complete description of the register contents.

PCI Express extended register offset: 114h
Register type: Read-only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−6. Correctable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:13	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
12†	REPLAY_TMOUT_MASK	RW	Replay timer time-out mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
11:9	RSVD	R	Reserved. Returns 000b when read.
8†	REPLAY_ROLL_MASK	RW	REPLAY_NUM rollover mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
7†	BAD_DLLP_MASK	RW	Bad DLLP error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
6†	BAD_TLP_MASK	RW	Bad TLP error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
5:1	RSVD	R	Reserved. Returns 00000b when read.
0†	RX_ERROR_MASK	RW	Receiver error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.8 Advanced Error Capabilities and Control Register

The advanced error capabilities and control register allows the system to monitor and control the advanced error reporting capabilities. See Table 5−7 for a complete description of the register contents.

PCI Express extended register offset: 118h
Register type: Read-only, Read/Write
Default value: 0000 00A0h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 5−7. Advanced Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:9	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000 0000b when read.
8†	ECRC_CHK_EN	RW	Extended CRC check enable 0 = Extended CRC checking is disabled 1 = Extended CRC checking is enabled
7	ECRC_CHK_CAPABLE	R	Extended CRC check capable. This read-only bit returns a value of 1b indicating that the bridge is capable of checking extended CRC information.
6†	ECRC_GEN_EN	RW	Extended CRC generation enable 0 = Extended CRC generation is disabled 1 = Extended CRC generation is enabled
5	ECRC_GEN_CAPABLE	R	Extended CRC generation capable. This read-only bit returns a value of 1b indicating that the bridge is capable of generating extended CRC information.
4:0†	FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the uncorrectable error status register (offset 104h, see Section 5.3) corresponding to the class of the first error condition that was detected.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.9 Header Log Register

The header log register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header). Each DWORD is stored with the least significant byte representing the earliest transmitted. These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI Express extended register offset: 11Ch, 120h, 124h, and 128h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.10 Secondary Uncorrectable Error Status Register

The secondary uncorrectable error status register reports the status of individual PCI bus errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5−8 for a complete description of the register contents.

PCI Express extended register offset: 12Ch
Register type: Read-only, Read/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−8. Secondary Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13†	BRIDGE_ERROR	R	Internal bridge error. This error bit is associated with a PCI-X error and returns 0b when read.
12†	SERR_DETECT	RCU	$\overline{\text{SERR}}$ assertion detected. This bit is asserted when the bridge detects the assertion of $\overline{\text{SERR}}$ on the secondary bus.
11†	PERR_DETECT	RCU	$\overline{\text{PERR}}$ assertion detected. This bit is asserted when the bridge detects the assertion of $\overline{\text{PERR}}$ on the secondary bus.
10†	DISCARD_TIMER	RCU	Delayed transaction discard timer expired. This bit is asserted when the discard timer expires for a pending delayed transaction that was initiated on the secondary bus.
9†	UNCOR_ADDR	RCU	Uncorrectable address error. This bit is asserted when the bridge detects a parity error during the address phase of an upstream transaction.
8†	ATTR_ERROR	R	Uncorrectable attribute error. This error bit is associated with a PCI-X error and returns 0b when read.
7†	UNCOR_DATA	RCU	Uncorrectable data error. This bit is asserted when the bridge detects a parity error during a data phase of an upstream write transaction, or when the bridge detects the assertion of $\overline{\text{PERR}}$ when forwarding read completion data to a PCI device.
6†	SC_MSG_DATA	R	Uncorrectable split completion message data error. This error bit is associated with a PCI-X error and returns 0b when read.
5†	SC_ERROR	R	Unexpected split completion error. This error bit is associated with a PCI-X error and returns 0b when read.
4	RSVD	R	Reserved. Returns 0b when read.
3†	MASTER_ABORT	RCU	Received master abort. This bit is asserted when the bridge receives a master abort on the PCI interface.
2†	TARGET_ABORT	RCU	Received target abort. This bit is asserted when the bridge receives a target abort on the PCI interface.
1†	SC_MSTR_ABORT	R	Master abort on split completion. This error bit is associated with a PCI-X error and returns 0b when read.
0	RSVD	R	Reserved. Returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.11 Secondary Uncorrectable Error Mask Register

The secondary uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5−9 for a complete description of the register contents.

PCI Express extended register offset: 130h
Register type: Read-only, Read/Write
Default value: 0000 17A8h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	1	0	1	1	1	1	0	1	0	1	0	0	0

Table 5−9. Secondary Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13†	BRIDGE_ERROR_MASK	RW	Internal bridge error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
12†	SERR_DETECT_MASK	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is unmasked 1 = Error condition is masked (default)
11†	PERR_DETECT_MASK	RW	$\overline{\text{PERR}}$ assertion detected 0 = Error condition is unmasked (default) 1 = Error condition is masked
10†	DISCARD_TIMER_MASK	RW	Delayed transaction discard timer expired 0 = Error condition is unmasked 1 = Error condition is masked (default)
9†	UNCOR_ADDR_MASK	RW	Uncorrectable address error 0 = Error condition is unmasked 1 = Error condition is masked (default)
8†	ATTR_ERROR_MASK	RW	Uncorrectable attribute error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
7†	UNCOR_DATA_MASK	RW	Uncorrectable data error 0 = Error condition is unmasked 1 = Error condition is masked (default)
6†	SC_MSG_DATA_MASK	RW	Uncorrectable split completion message data error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
5†	SC_ERROR_MASK	RW	Unexpected split completion error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3†	MASTER_ABORT_MASK	RW	Received master abort 0 = Error condition is unmasked 1 = Error condition is masked (default)
2†	TARGET_ABORT_MASK	RW	Received target abort 0 = Error condition is unmasked (default) 1 = Error condition is masked
1†	SC_MSTR_ABORT_MASK	RW	Master abort on split completion. This mask bit is associated with a PCI-X error and has no effect on the bridge.
0	RSVD	R	Reserved. Returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.12 Secondary Uncorrectable Error Severity Register

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5−10 for a complete description of the register contents.

PCI Express extended register offset: 134h
Register type: Read-only, Read/Write
Default value: 0000 1340h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0

Table 5−10. Secondary Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13†	BRIDGE_ERROR_SEVR	RW	Internal bridge error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
12†	SERR_DETECT_SEVR	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
11†	PERR_DETECT_SEVR	RW	$\overline{\text{PERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
10†	DISCARD_TIMER_SEVR	RW	Delayed transaction discard timer expired 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
9†	UNCOR_ADDR_SEVR	RW	Uncorrectable address error 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
8†	ATTR_ERROR_SEVR	RW	Uncorrectable attribute error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
7†	UNCOR_DATA_SEVR	RW	Uncorrectable data error 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
6†	SC_MSG_DATA_SEVR	RW	Uncorrectable split completion message data error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
5†	SC_ERROR_SEVR	RW	Unexpected split completion error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3†	MASTER_ABORT_SEVR	RW	Received master abort 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
2†	TARGET_ABORT_SEVR	RW	Received target abort 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
1†	SC_MSTR_ABORT_SEVR	RW	Master abort on split completion. This severity bit is associated with a PCI-X error and has no effect on the bridge.
0	RSVD	R	Reserved. Returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.13 Secondary Error Capabilities and Control Register

The secondary error capabilities and control register allows the system to monitor and control the secondary advanced error reporting capabilities. See Table 5−11 for a complete description of the register contents.

PCI Express extended register offset: 138h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−11. Secondary Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:5	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000 0000 0000b when read.
4:0†	SEC_FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the secondary uncorrectable error status register (offset 12Ch, see Section 5.10) corresponding to the class of the first error condition that was detected.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.14 Secondary Header Log Register

The secondary header log register stores the transaction address and command for the PCI bus cycle that led to the most recently detected error condition. Offset 13Ch accesses register bits 31:0. Offset 140h accesses register bits 63:32. Offset 144h accesses register bits 95:64. Offset 148h accesses register bits 127:96. See Table 5−12 for a complete description of the register contents.

PCI Express extended register offset: 13Ch, 140h, 144h, and 148h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−12. Secondary Header Log Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
127:64†	ADDRESS	RU	Transaction address. The 64-bit value transferred on AD[31:0] during the first and second address phases. The first address phase is logged to 95:64 and the second address phase is logged to 127:96. In the case of a 32-bit address, bits 127:96 are set to 0000 0000h.
63:44	RSVD	R	Reserved. Returns 00000h when read.
43:40†	UPPER_CMD	RU	Transaction command upper. Contains the status of the C/$\overline{BE}$ terminals during the second address phase of the PCI transaction that generated the error if using a dual-address cycle.
39:36†	LOWER_CMD	RU	Transaction command lower. Contains the status of the C/$\overline{BE}$ terminals during the first address phase of the PCI transaction that generated the error.
35:0	TRANS_ATTRIBUTE	R	Transaction attribute. Because the bridge does not support the PCI-X attribute transaction phase, these bits have no function, and return 0 0000 0000h when read.

† These bits are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

5.15 Virtual Channel Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express VC capabilities. The register returns 0002h when read.

PCI Express extended register offset: 150h
Register type: Read-only
Default value: 0002h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

5.16 Next Capability Offset/Capability Version Register

This read-only register returns the value 000h to indicate that this extended capability block represents the end of the linked list of extended capability structures. The four least significant bits identify the revision of the current capability block as 1h.

PCI Express extended register offset: 152h
Register type: Read-only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

5.17 Port VC Capability Register 1

The first port VC capability register provides information to software regarding the VC capabilities support by the bridge. See Table 5−13 for a complete description of the register contents.

PCI Express extended register offset: 154h
Register type: Read-only
Default value: 0000 08X1h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	1	0	0	0	0	0	0	x	0	0	0	1

Table 5−13. Port VC Capability Register 1 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:12	RSVD	R	Reserved. Returns 00000h when read.
11:10	PORT_TABLE_SIZE	R	Port arbitration table entry size. This read-only field returns a value of 10b to indicate that the field size within the port arbitration table is four bits. This is necessary to allow as many as six secondary PCI bus masters.
9:8	REF_CLK	R	Reference clock. This read-only field returns a value of 00b to indicate than an internal 100-ns timer is used for time-based, WRR port arbitration.
7	RSVD	R	Reserved. Returns 0b when read.
6:4	LOW_PRIORITY_COUNT	RU	Low priority extended VC count. When bit 25 (STRICT_PRIORITY_EN) in the general control register (offset D4h, see Section 4.65) is 0b, the default LOW_PRIORITY_COUNT is 001b. When STRICT_PRIORITY_EN is 1b, the default LOW_PRIORITY_COUNT is 000b. When STRICT_PRIORITY_EN is set, strict priority VC arbitration is used and the extended VC always receives priority over VC0 at the PCI Express port.
3	RSVD	R	Reserved. Returns 0b when read.
2:0	EXT_VC_COUNT	R	Extended VC count. This read-only field returns a value of 001b to indicate support for one extended VC.

5.18 Port VC Capability Register 2

The second port VC capability register provides information to software regarding the VC arbitration schemes supported by the bridge. See Table 5−14 for a complete description of the register contents.

PCI Express extended register offset: 158h
Register type: Read-only
Default value: 0X00 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x

Table 5−14. Port VC Capability Register 2 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	VC_ARB_ TBL_OFFSET	RU	VC arbitration table offset. If bits 6:4 (LOW_PROIRITY_COUNT) in the port VC capability register 1 (offset 154h, see Section 5.17) are 000b, then this field returns 00h when read. Otherwise, this read-only field returns the value 03h to indicate that the VC arbitration table begins 48 bytes from the top of the VC capability structure. When this field equals 00h, the VC arbitration table is a scratch pad and has no effect in the bridge.
23:8	RSVD	R	Reserved. Returns 0000h when read.
7:0	VC_ARB_CAP	RU	VC arbitration capability. This 8-bit encoded field indicates support for the various schemes that are supported for VC arbitration. The field is encoded as follows: Bit 0 = Hardware fixed arbitration (round-robin) Bit 1 = WRR with 32 phases Bit 2 = WRR with 64 phases Bit 3 = WRR with 128 phases Bit 4 = Reserved Bit 5 = Reserved Bit 6 = Reserved Bit 7 = Reserved If bits 6:4 (LOW_PROIRITY_COUNT) in the port VC capability register 1 (offset 154h, see Section 5.17) are 000b, then this field returns 00h when read. Otherwise, this field returns 03h to indicate that hardware-fixed round-robin and WRR with 32 phases are both supported.

5.19 Port VC Control Register

The port VC control register allows software to configure the VC arbitration options within the bridge. See Table 5−15 for a complete description of the register contents.

PCI Express extended register offset: 15Ch
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−15. Port VC Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	VC_ARB _SELECT	RW	VC arbitration select. This read/write field allows software to define the mechanism used for VC arbitration by the bridge. The value written to this field indicates the bit position within bits 7:0 (VC_ARB_CAP) in the port VC capability register 2 (offset 158h, see Section 5.18) that corresponds to the selected arbitration scheme. Values that may be written to this field include: 000 = Hardware-fixed round-robin (default) 001 = WRR with 32 phases All other values are reserved for arbitrations schemes that are not supported by the bridge.
0	LOAD_VC _TABLE	RW	Load VC arbitration table. When software writes a 1b to this bit, the bridge applies the values written in the VC arbitration table within the extended configuration space to the actual VC arbitration tables used by the device for arbitration. This bit always returns 0b when read.

5.20 Port VC Status Register

The port VC status register allows software to monitor the status of the VC arbitration table. See Table 5−16 for a complete description of the register contents.

PCI Express extended register offset: 15Eh
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−16. Port VC Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:1	RSVD	R	Reserved. Returns 000 0000 0000 0000b when read.
0	VC_TABLE_STATUS	RU	VC arbitration table status. This bit is automatically set by hardware when any modification is made to the VC arbitration table entries within the extended configuration space. This bit is cleared by hardware after software has requested a VC arbitration table refresh and the refresh has been completed.

5.21 VC Resource Capability Register (VC0)

The VC resource capability register for VC0 provides information to software regarding the port and arbitration schemes supported by the bridge. See Table 5−17 for a complete description of the register contents.

PCI Express extended register offset: 160h
Register type: Read-only
Default value: 0000 0001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 5−17. VC Resource Capability Register (VC0) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_ARB_TBL_OFFSET	R	Port arbitration table offset. This read-only field returns the value 00h to indicate that no port arbitration table is required for this VC.
23	RSVD	R	Reserved. Returns 0b when read.
22:16	MAX_TIME_SLOTS	R	Maximum time slots. This read-only field returns the value 000 0000b because there is no support for time-based, WRR arbitration on this VC.
15	REJECT_SNOOP	R	Reject snoop transactions. This bit only has meaningful context for root ports; therefore, returns 0b when read.
14	ADV_SWITCHING	R	Advanced packet switching. This read-only bit returns 0b to indicate that the use of this VC is not limited to AS traffic.
13:8	RSVD	R	Reserved. Returns 00 0000b when read.
7:0	PORT_ARB_CAP	R	Port arbitration capability. This 8-bit encoded field indicates support for the various schemes that are supported for port (secondary PCI device) arbitration. The field is encoded as follows: Bit 0 = Hardware fixed arbitration (round-robin) Bit 1 = WRR with 32 phases Bit 2 = WRR with 64 phases Bit 3 = WRR with 128 phases Bit 4 = Time-based WRR with 128 phases Bit 5 = WRR with 256 phases Bits 6 and 7 = Reserved The returned value of 01h indicates that only hardware-fixed, round-robin arbitration is support for this VC.

5.22 VC Resource Control Register (VC0)

The VC resource control register for VC0 allows software to control VC0 and the associated port and arbitration schemes supported by the bridge. See Table 5−18 for a complete description of the register contents.

PCI Express extended register offset: 164h
Register type: Read-only, Read/Write
Default value: 8000 00FFh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Table 5−18. VC Resource Control Register (VC0) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31	VC_EN	R	VC enable. This field is internally hardwired to 1b to indicate that this VC resource is always enabled.
30:27	RSVD	R	Reserved. Returns 0h when read.
26:24	VC_ID	R	Virtual channel ID. This field is internally hardwired to 000b to indicate that this VC resource is always used for VC0.
23:20	RSVD	R	Reserved. Returns 0h when read.
19:17	PORT_ARB_SELECT	R	Port arbitration select. This read-only field returns 000b when read, because only hardware-fixed, round-robin arbitration is supported for this VC.
16	LOAD_PORT_TABLE	R	Load port arbitration table. This read-only bit returns 0b when read, because no port arbitration table is supported for this VC.
15:8	RSVD	R	Reserved. Returns 00h when read.
7:0	TC_VC_MAP	RW	TC/VC map. This field indicates all of the traffic classes that are mapped to this VC. A 1b in any bit position indicates that the corresponding traffic class is enabled for this VC. A 0b indicates that the corresponding traffic class is mapped to a different VC. The following table is used: Bit 0 = Traffic class 0 (This bit is read-only and returns a value of 1b) Bit 1 = Traffic class 1 Bit 2 = Traffic class 2 Bit 3 = Traffic class 3 Bit 4 = Traffic class 4 Bit 5 = Traffic class 5 Bit 6 = Traffic class 6 Bit 7 = Traffic class 7 The default value of FFh indicates that all eight traffic classes are initially mapped to VC0.

5.23 VC Resource Status Register (VC0)

The VC resource status register allows software to monitor the status of the port arbitration table for this VC. See Table 5−19 for a complete description of the register contents.

PCI Express extended register offset: 16Ah
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−19. VC Resource Status Register (VC0) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:2	RSVD	R	Reserved. Returns 00 0000 0000 0000b when read.
1	VC_PENDING	RU	VC negotiation pending. This bit is asserted when VC negotiation is in progress following a request by software to enable or disable the VC or at startup for VC0.
0	PORT_TABLE_STATUS	RU	Port arbitration table status. This bit is automatically set by hardware when any modification is made to the port arbitration table entries for this VC within the extended configuration space. This bit is cleared by hardware after software has requested a port arbitration table refresh and the refresh has been completed.

5.24 VC Resource Capability Register (VC1)

The VC resource capability register for VC1 provides information to software regarding the port and arbitration schemes supported by the bridge. See Table 5−20 for a complete description of the register contents.

PCI Express extended register offset: 16Ch
Register type: Read-only
Default value: 077F 0011h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Table 5−20. VC Resource Capability Register (VC1) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_ARB_ TBL_OFFSET	R	Port arbitration table offset. This read-only field returns the value 07h to indicate that the port arbitration table for this VC begins 112 bytes from the top of the VC capability structure.
23	RSVD	R	Reserved. Returns 0b when read.
22:16	MAX_TIME_ SLOTS	R	Maximum time slots. The read-only field returns the value 111 1111b to indicate that all 128 slots are supported for time-based WRR.
15	REJECT_ SNOOP	R	Reject snoop transactions. This bit only has meaningful context for root ports; therefore, returns 0b when read.
14	ADV_ SWITCHING	R	Advanced packet switching. This read-only bit returns the value 0b to indicate that the use of this VC is not limited to AS traffic.
13:8	RSVD	R	Reserved. Return 00 0000b when read.
7:0	PORT_ ARB_CAP	R	Port arbitration capability. This 8-bit encoded field indicates support for the various schemes that are supported for port (secondary PCI device) arbitration. The field is encoded as follows: Bit 0 = Hardware fixed arbitration (round-robin) Bit 1 = WRR with 32 phases Bit 2 = WRR with 64 phases Bit 3 = WRR with 128 phases Bit 4 = Time-based WRR with 128 phases Bit 5 = WRR with 256 phases Bits 6 and 7 = Reserved The returned value of 11h indicates that hardware-fixed round-robin and time-based WRR with 128 phases are both supported.

5.25 VC Resource Control Register (VC1)

The VC resource control register for VC1 allows software to control the second VC and associated port and arbitration schemes supported by the bridge. See Table 5−21 for a complete description of the register contents.

PCI Express extended register offset: 170h
Register type: Read-only, Read/Write
Default value: 0100 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−21. VC Resource Control Register (VC1) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31	VC_EN	RW	VC enable. This bit is used by software to enable this VC resource. Writing a 1b to this bit causes the bridge to begin VC negotiation and set bit 1 (VC_PENDING) in the VC resource status register for this VC (offset 176h, see Section 5.26). The default value for this bit is 0b.
30:27	RSVD	R	Reserved. Returns 0h when read.
26:24	VC_ID	RW	Virtual channel ID. This field allows software to assign a VC ID to this VC resource. Valid values range from 001b to 111b, because the value 000b is hardware-fixed to VC0 within the device. The default value for this field is 001b.
23:20	RSVD	R	Reserved. Returns 0h when read.
19:17	PORT_ARB _SELECT	RW	Port arbitration select. This read/write field allows software to define the mechanism used for port arbitration by the bridge on this VC. The value written to this field indicates the bit position within bits 7:0 (PORT_ARB_CAP) in the VC resource capability register for this VC (offset 16Ch, see Section 5.24) that corresponds to the selected arbitration scheme. Values that may be written to this field include: 000 = Hardware-fixed round-robin (default) 100 = Time-based WRR with 128 phases All other values are reserved for arbitrations schemes that are not supported by the bridge.
16	LOAD_PORT _TABLE	RW	Load port arbitration table. When software writes a 1b to this bit, the bridge applies the values written in the port arbitration table for this VC within the extended configuration space to the actual port arbitration tables used by the device for arbitration on this VC. This bit always returns 0b when read.
15:8	RSVD	R	Reserved. Returns 00h when read.
7:0	TC_VC_MAP	RW	TC/VC map. This field indicates all of the traffic classes that are mapped to this VC. A 1b in any bit position indicates that the corresponding traffic class is enabled for this VC. A 0b indicates that the corresponding traffic class is mapped to a different VC. The following table is used: Bit 0 = Traffic class 0 (This bit is read only and returns a value of 0b) Bit 1 = Traffic class 1 Bit 2 = Traffic class 2 Bit 3 = Traffic class 3 Bit 4 = Traffic class 4 Bit 5 = Traffic class 5 Bit 6 = Traffic class 6 Bit 7 = Traffic class 7 The default value of 00h indicates that none of the eight traffic classes are initially mapped to this VC.

5.26 VC Resource Status Register (VC1)

The VC resource status register allows software to monitor the status of the port arbitration table for this VC. See Table 5−22 for a complete description of the register contents.

PCI Express extended register offset: 176h
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5−22. VC Resource Status Register (VC1) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:2	RSVD	R	Reserved. Returns 00 0000 0000 0000b when read.
1	VC_PENDING	RU	VC negotiation pending. This bit is asserted when VC negotiation is in progress following a request by software to enable the second VC.
0	PORT_TABLE _STATUS	RU	Port arbitration table status. This bit is automatically set by hardware when any modification is made to the port arbitration table entries for this VC within the extended configuration space. This bit is cleared by hardware after software has requested a port arbitration table refresh and the refresh has been completed.

5.27 VC Arbitration Table

The VC arbitration table is provided to allow software to define round-robin weighting for traffic targeting the PCI Express port. The table is divided into 32 phases. See Table 5−24 for a complete description of the register contents.

PCI Express extended register offset: 180h – 18Ch
Register type: Read-only, Read/Write
Default value: 0000 0000h

Table 5−23. VC Arbitration Table

REGISTER FORMAT								OFFSET
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	180h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	184h
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	188h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	18Ch

Each phase consists of a four-bit field as indicated below.

BIT NUMBER	3	2	1	0
RESET STATE	0	0	0	0

Table 5−24. VC Arbitration Table Entry Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
3	RSVD	R	Reserved. Returns 0b when read.
2:0	VC_ARB_ID	RW	Virtual channel ID. This 3-bit field is used by software to identify the VC ID that must be allocated this slot of arbitration bandwidth depending upon the VC arbitration scheme enabled. The default value for this field is 000b.

5.28 Port Arbitration Table (VC1)

The port arbitration table is provided to allow software to define round-robin weighting for traffic entering the PCI interface. The table is divided into 128 phases.

PCI Express extended register offset: 1C0h – 1FCh
Register type: Read/Write
Default value: 0000 0000h

Table 5−25. Port Arbitration Table

REGISTER FORMAT								OFFSET
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	1C0h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	1C4h
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	1C8h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	1CCh
Phase 39	Phase 38	Phase 37	Phase 36	Phase 35	Phase 34	Phase 33	Phase 32	1D0h
Phase 47	Phase 46	Phase 45	Phase 44	Phase 43	Phase 42	Phase 41	Phase 40	1D4h
Phase 55	Phase 54	Phase 53	Phase 52	Phase 51	Phase 50	Phase 49	Phase 48	1D8h
Phase 63	Phase 62	Phase 61	Phase 60	Phase 59	Phase 58	Phase 57	Phase 56	1DCh
Phase 71	Phase 70	Phase 69	Phase 68	Phase 67	Phase 66	Phase 65	Phase 64	1E0h
Phase 79	Phase 78	Phase 77	Phase 76	Phase 75	Phase 74	Phase 73	Phase 72	1E4h
Phase 87	Phase 86	Phase 85	Phase 84	Phase 83	Phase 82	Phase 81	Phase 80	1E8h
Phase 95	Phase 94	Phase 93	Phase 92	Phase 91	Phase 90	Phase 89	Phase 88	1ECh
Phase 103	Phase 102	Phase 101	Phase 100	Phase 99	Phase 98	Phase 97	Phase 96	1F0h
Phase 111	Phase 110	Phase 109	Phase 108	Phase 107	Phase 106	Phase 105	Phase 104	1F4h
Phase 119	Phase 118	Phase 117	Phase 116	Phase 115	Phase 114	Phase 113	Phase 112	1F8h
Phase 127	Phase 126	Phase 125	Phase 124	Phase 123	Phase 122	Phase 121	Phase 120	1FCh

Each phase consists of a four-bit field as indicated below.

BIT NUMBER	3	2	1	0
RESET STATE	0	0	0	0

Table 5−26. Port Arbitration Table Entry Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
3:0	PORT_SELECT	RW	Port arbitration select. This 4-bit field is used by software to identify the port ID (secondary PCI device) that must be allocated to this slot of arbitration bandwidth depending upon the port arbitration scheme enabled. The default value for this field is 0h.

6 Memory-Mapped TI Proprietary Register Space

The programming model of the memory-mapped TI proprietary register space is unique to this device. These custom registers are specifically designed to provide enhanced features associated with upstream isochronous applications.

All bits marked with a ☆ are sticky bits and are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a † are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$ or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 6−1. Device Control Memory Window Register Map

REGISTER NAME				OFFSET
Upstream isochrony capabilities		Revision ID	Device control map ID	00h
Reserved		Upstream isochrony control		04h
Reserved		Upstream isochronous window 0 control		08h
Upstream isochronous window 0 base address				0Ch
Upstream isochronous window 0 limit				10h
Reserved		Upstream isochronous window 1 control		14h
Upstream isochronous window 1 base address				18h
Upstream isochronous window 1 limit				1Ch
Reserved		Upstream isochronous window 2 control		20h
Upstream isochronous window 2 base address				24h
Upstream isochronous window 2 limit				28h
Reserved		Upstream isochronous window 3 control		2Ch
Upstream isochronous window 3 base address				30h
Upstream isochronous window 3 limit				34h
Reserved				38h−3Ch
GPIO data†		GPIO control†		40h
Serial-bus control and status†	Serial-bus slave address†	Serial-bus word address†	Serial-bus data†	44h
Serial IRQ edge control†		Reserved	Serial IRQ mode control†	48h
Reserved		Serial IRQ status		4Ch

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.1 Device Control Map ID Register

The device control map ID register identifies the TI proprietary layout for this device control map. The value 01h identifies this as a PCI Express-to-PCI bridge supporting upstream isochronous capabilities.

Device control memory window register offset: 00h
Register type: Read-only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

6.2 Revision ID Register

The revision ID register identifies the revision of the TI proprietary layout for this device control map. The value 00h identifies the revision as the initial layout.

Device control memory window register offset: 01h
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.3 Upstream Isochrony Capabilities Register

The upstream isochronous capabilities register provides software information regarding the capabilities supported by this bridge. See Table 6−2 for a complete description of the register contents.

Device control memory window register offset: 02h
Register type: Read-only
Default value: 0004h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Table 6−2. Upstream Isochronous Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:0	ISOC_WINDOW_COUNT	R	Isochronous window count. This 4-bit field indicates the number of isochronous address windows supported. The value 0100b indicates that 4 separate windows are supported by the bridge.

6.4 Upstream Isochrony Control Register

The upstream isochrony control register allows software to control bridge isochronous behavior. See Table 6−3 for a complete description of the register contents.

Device control memory window register offset: 04h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−3. Upstream Isochrony Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:3	RSVD	R	Reserved. Returns 0 0000 0000 0000b when read.
2	PORTARB_LEVEL_2_EN	RW	Port arbitration level 2 enable. This bit is only valid if PORTARB_LEVEL_1_EN is set to 1b, because this enhances the behavior enabled through the assertion of that bit. If PORTARB_LEVEL_1_EN is clear, then this bit is read-only and returns 0b when read. 0 = Arbiter behavior follows PORTARB_LEVEL_1_EN rules (default) 1 = Aggressive mode. The arbiter deliberately stops secondary bus masters in the middle of their transaction to assure that isochrony is preserved.
1	PORTARB_LEVEL_1_EN	RW	Port arbitration level 1 enable. 0 = Arbiter behavior is controlled only by the arbiter control registers within the classic PCI configuration space (default) 1 = Values programmed within the port arbitration table for extended VCs impact the arbiter's decision to assert $\overline{GNT}$ to any particular bus master. Programmed values in the arbiter control registers within the classic PCI configuration space have no effect when this bit is asserted.
0	ISOC_ENABLE	RW	Isochronous enable. Global enable bit for the upstream isochronous capability of the bridge. 0 = Mapping of upstream traffic to TCs other than TC0 prohibited (default) 1 = Mapping of upstream traffic to TCs other than TC0 permitted

6.5 Upstream Isochronous Window 0 Control Register

The upstream isochronous window 0 control register allows software to identify the traffic class (TC) associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6−4 for a complete description of the register contents.

Device control memory window register offset: 08h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−4. Upstream Isochronous Window 0 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable. 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.6 Upstream Isochronous Window 0 Base Address Register

The upstream isochronous window 0 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 0Ch
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.7 Upstream Isochronous Window 0 Limit Register

The upstream isochronous window 0 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 10h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.8 Upstream Isochronous Window 1 Control Register

The upstream isochronous window 1 control register allows software to identify the TC associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6−5 for a complete description of the register contents.

Device control memory window register offset: 14h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−5. Upstream Isochronous Window 1 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable. 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.9 Upstream Isochronous Window 1 Base Address Register

The upstream isochronous window 1 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 18h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.10 Upstream Isochronous Window 1 Limit Register

The upstream isochronous window 1 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 1Ch
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.11 Upstream Isochronous Window 2 Control Register

The upstream isochronous window 2 control register allows software to identify the TC associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6−6 for a complete description of the register contents.

Device control memory window register offset: 20h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−6. Upstream Isochronous Window 2 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable. 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.12 Upstream Isochronous Window 2 Base Address Register

The upstream isochronous window 2 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 24h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.13 Upstream Isochronous Window 2 Limit Register

The upstream isochronous window 2 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 28h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.14 Upstream Isochronous Window 3 Control Register

The upstream isochronous window 3 control register allows software to identify the TC associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6−7 for a complete description of the register contents.

Device control memory window register offset: 2Ch
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−7. Upstream Isochronous Window 3 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable. 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.15 Upstream Isochronous Window 3 Base Address Register

The upstream isochronous window 3 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 30h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.16 Upstream Isochronous Window 3 Limit Register

The upstream isochronous window 3 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 34h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.17 GPIO Control Register

This register controls the direction of the eight GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO4 (SCL), and GPIO5 (SDA). This register is an alias of the GPIO control register in the classic PCI configuration space (offset B4h, see Section 4.59). See Table 6−8 for a complete description of the register contents.

Device control memory window register offset: 40h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−8. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7†	GPIO7_DIR	RW	GPIO 7 data direction. This bit selects whether GPIO7 is in input or output mode. 0 = Input (default) 1 = Output
6†	GPIO6_DIR	RW	GPIO 6 data direction. This bit selects whether GPIO6 is in input or output mode. 0 = Input (default) 1 = Output
5†	GPIO5_DIR	RW	GPIO 5 data direction. This bit selects whether GPIO5 is in input or output mode. 0 = Input (default) 1 = Output
4†	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3†	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2†	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
1†	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0†	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.18 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO4 (SCL), and GPIO5 (SDA). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. This register is an alias of the GPIO data register in the classic PCI configuration space (offset B6h, see Section 4.60). See Table 6−9 for a complete description of the register contents.

Device control memory window register offset: 42h
Register type: Read-only, Read/Write
Default value: 00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Table 6−9. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7†	GPIO7_Data	RW	GPIO 7 data. This bit reads the state of GPIO7 when in input mode or changes the state of GPIO7 when in output mode.
6†	GPIO6_Data	RW	GPIO 6 data. This bit reads the state of GPIO6 when in input mode or changes the state of GPIO6 when in output mode.
5†	GPIO5_Data	RW	GPIO 5 data. This bit reads the state of GPIO5 when in input mode or changes the state of GPIO5 when in output mode.
4†	GPIO4_Data	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3†	GPIO3_Data	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2†	GPIO2_Data	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1†	GPIO1_Data	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0†	GPIO0_Data	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.19 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) in the serial-bus control and status register (offset 47h, see Section 6.22) is cleared. This register is an alias for the serial-bus data register in the PCI header (offset B0h, see Section 4.55). This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Device control memory window register offset: 44h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.20 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to on the serial-bus interface. The word address is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. This register is an alias for the serial-bus word address register in the PCI header (offset B1h, see Section 4.56). This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Device control memory window register offset: 45h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.21 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle will be a read or a write cycle. Writing to this register initiates the cycle on the serial interface. This register is an alias for the serial-bus slave address register in the PCI header (offset B2h, see Section 4.57). See Table 6−10 for a complete description of the register contents.

Device control memory window register offset: 46h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6−10. Serial-Bus Slave Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1†	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0†	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle. 0 = A single byte write is requested (default) 1 = A single byte read is requested

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.22 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial-bus. This register is an alias for the serial-bus control and status register in the PCI header (offset B3h, see Section 4.58). See Table 6−11 for a complete description of the register contents.

Device control memory window register offset: 47h
Register type: Read-only, Read/Write, Read/Clear
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6−11. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial-bus (default) 1 = Only the slave address is sent on the serial-bus
6	RSVD	R	Reserved. Returns 0b when read.
5†	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progress
4†	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. 0 = No EEPROM activity 1 = EEPROM download in progress
3†	SBDETECT	RWU	Serial EEPROM detected. This bit enables the serial-bus interface. The value of this bit controls whether the GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals or as serial-bus signals. This bit is automatically set to 1b when a serial EEPROM is detected. **Note:** A serial EEPROM is only detected once following $\overline{\text{PERST}}$. 0 = No EEPROM present, EEPROM load process does not happen. GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals. 1 = EEPROM present, EEPROM load process takes place. GPIO4//SCL and GPIO5//SDA terminals are configured as serial-bus signals.
2†	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz
1†	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0†	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 = No Error 1 = EEPROM load error

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.23 Serial IRQ Mode Control Register

This register controls the behavior of the serial IRQ controller. This register is an alias for the serial IRQ mode control register in the classic PCI configuration space (offset E0h, see Section 4.72). See Table 6−12 for a complete description of the register contents.

Device control memory window register offset: 48h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6−12. Serial IRQ Mode Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	R	Reserved. Returns 0h when read.
3:2†	START_WIDTH	RW	Start frame pulse width. Used to set the width of the start frame for a SERIRQ stream. 00 = 4 clocks (default) 01 = 6 clocks 10 = 8 clocks 11 = Reserved
1†	POLLMODE	RW	Poll mode. This bit selects between continuous and quiet mode. 0 = Continuous mode (default) 1 = Quiet mode
0†	DRIVEMODE	RW	Drive mode. This bit selects the behavior of the serial IRQ controller during the recovery cycle. 0 = Drive high (default) 1 = Tri-state

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.24 Serial IRQ Edge Control Register

This register controls the edge mode of each IRQ in the serial IRQ stream. This register is an alias for the serial IRQ edge control register in the classic PCI configuration space (offset E2h, see Section 4.73). See Table 6−13 for a complete description of the register contents.

Device control memory window register offset: 4Ah
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−13. Serial IRQ Edge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15†	IRQ15_MODE	RW	IRQ 15 edge mode 0 = Edge mode (default) 1 = Level mode
14†	IRQ14_MODE	RW	IRQ 14 edge mode 0 = Edge mode (default) 1 = Level mode
13†	IRQ13_MODE	RW	IRQ 13 edge mode 0 = Edge mode (default) 1 = Level mode
12†	IRQ12_MODE	RW	IRQ 12 edge mode 0 = Edge mode (default) 1 = Level mode
11†	IRQ11_MODE	RW	IRQ 11 edge mode 0 = Edge mode (default) 1 = Level mode
10†	IRQ10_MODE	RW	IRQ 10 edge mode 0 = Edge mode (default) 1 = Level mode
9†	IRQ9_MODE	RW	IRQ 9 edge mode 0 = Edge mode (default) 1 = Level mode
8†	IRQ8_MODE	RW	IRQ 8 edge mode 0 = Edge mode (default) 1 = Level mode
7†	IRQ7_MODE	RW	IRQ 7 edge mode 0 = Edge mode (default) 1 = Level mode
6†	IRQ6_MODE	RW	IRQ 6 edge mode 0 = Edge mode (default) 1 = Level mode
5†	IRQ5_MODE	RW	IRQ 5 edge mode 0 = Edge mode (default) 1 = Level mode
4†	IRQ4_MODE	RW	IRQ 4 edge mode 0 = Edge mode (default) 1 = Level mode

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 6−13. Serial IRQ Edge Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
3†	IRQ3_MODE	RW	IRQ 3 edge mode 0 = Edge mode (default) 1 = Level mode
2†	IRQ2_MODE	RW	IRQ 2 edge mode 0 = Edge mode (default) 1 = Level mode
1†	IRQ1_MODE	RW	IRQ 1 edge mode 0 = Edge mode (default) 1 = Level mode
0†	IRQ0_MODE	RW	IRQ 0 edge mode 0 = Edge mode (default) 1 = Level mode

† These bits are reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset.

6.25 Serial IRQ Status Register

This register indicates when a level mode IRQ is signaled on the serial IRQ stream. After a level mode IRQ is signaled, a write-back of 1b to the asserted IRQ status bit re-arms the interrupt. IRQ interrupts that are defined as edge mode in the serial IRQ edge control register are not reported in this status register.

This register is an alias for the serial IRQ status register in the classic PCI configuration space (offset E4h, see Section 4.74). See Table 6−14 for a complete description of the register contents.

Device control memory window register offset: 4Ch
Register type: Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6−14. Serial IRQ Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	IRQ15	RCU	IRQ 15 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
14	IRQ14	RCU	IRQ 14 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
13	IRQ13	RCU	IRQ 13 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
12	IRQ12	RCU	IRQ 12 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
11	IRQ11	RCU	IRQ 11 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
10	IRQ10	RCU	IRQ 10 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
9	IRQ9	RCU	IRQ 9 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted

Table 6−14. Serial IRQ Status Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
8	IRQ8	RCU	IRQ 8 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
7	IRQ7	RCU	IRQ 7 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
6	IRQ6	RCU	IRQ 6 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
5	IRQ5	RCU	IRQ 5 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
4	IRQ4	RCU	IRQ 4 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
3	IRQ3	RCU	IRQ 3 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
2	IRQ2	RCU	IRQ 2 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
1	IRQ1	RCU	IRQ 1 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted
0	IRQ0	RCU	IRQ 0 asserted. This bit indicates that the IRQ has been asserted. 0 = Deasserted 1 = Asserted

7 Electrical Characteristics

7.1 Absolute Maximum Ratings Over Operating Temperature Ranges †

Supply voltage range:	V_{DD_33}	–0.5 V to 3.6 V
	V_{DD_15}	–0.5 V to 1.65 V
	V_{CCP}	–0.5 V to 5.25 V
Input voltage range,	V_I: PCI	–0.5 V to V_{CCP} + 0.5 V
	V_I: PCI Express (RX)	–0.6 V to 0.6 V
	V_I: PCI Express REFCLK (single-ended)	–0.5 V to V_{DD_33} + 0.5 V
	V_I: PCI Express REFCLK (differential)	–0.5 V to V_{DD_15} + 0.5 V
	V_I: Miscellaneous 3.3-V IO	–0.5 V to V_{DD_33} + 0.5 V
Output voltage range:	V_O: PCI	–0.5 V to V_{DD_33} + 0.5 V
	V_O: PCI Express (TX)	–0.5 V to V_{DD_15} + 0.5V
	V_O: Miscellaneous 3.3-V IO	–0.5 V to V_{DD_33} + 0.5 V
Input clamp current, (V_I < 0 or V_I > V_{DD}) (see Note 1)		±20 mA
Output clamp current, (V_O < 0 or V_O > V_{DD}) (see Note 2)		±20 mA
Human body model (HBM) ESD performance		1500 V
Charged device model (CDM) ESD performance		500 V
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies for external input and bidirectional buffers. V_I < 0 or V_I > V_{DD} or V_I > V_{CCP}.
2. Applies to external output and bidirectional buffers. V_O < 0 or V_O > V_{DD} or V_O > V_{CCP}.

7.2 Recommended Operation Conditions

			OPERATION	MIN	NOM	MAX	UNITS
V_{DD_15} V_{DDA_15}	Supply voltage		1.5 V	1.35	1.5	1.65	V
V_{DD_33} V_{DDA_33} $V_{DDA_33_AUX}$	Supply voltage		3.3 V	3	3.3	3.6	V
V_{CCP}	PCI bus clamping rail voltage		3.3 V	3	3.3	3.6	V
			5.0 V	4.75	5	5.25	
T_A	Operating ambient temperature range	XIO2000A (Commercial)		0	25	70	°C
		XIO2000AI (Industrial)		–40	25	85	°C
T_J	Virtual junction temperature (Note 3)			0	25	115	°C

NOTE 3: The junction temperature reflects simulated conditions. The customer is responsible for verifying junction temperature.

7.3 Nominal Power Consumption

DEVICES	POWER STATE	VOLTS	AMPERES	WATTS
No downstream	D0 idle	1.5	0.159	0.239
		3.3	0.019	0.063
		Totals:	0.178	0.301
One downstream	D0 idle	1.5	0.159	0.239
		3.3	0.026	0.086
		Totals:	0.185	0.324
One downstream	D0 active	1.5	0.159	0.239
		3.3	0.026	0.086
		Totals:	0.185	0.324
Two downstream	D0 idle	1.5	0.159	0.239
		3.3	0.032	0.106
		Totals:	0.191	0.344
Two downstream	D0 active	1.5	0.159	0.239
		3.3	0.032	0.106
		Totals:	0.191	0.344

NOTES: 4. D0 idle power state: Downstream PCI device is in PCI state D0. Downstream device driver is loaded. Downstream device is not actively transferring data.
D0 active power state: Downstream PCI device is in PCI state D0. Downstream device driver is loaded. Downstream device is acitvely trasferring data.

5. Downstream device 1: Texas Instruments TSB43AB22a OHCI controller.
Downstream device 2: Texas Instruments TSB43AB22a OHCI controller.
No ASPM was used during power consumption testing.
Unused PCI clocks were disabled via XIO2000A PCI register 0xD8.

7.4 PCI Express Differential Transmitter Output Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
UI Unit interval	TXP, TXN	399.88	400	400.12	ps	Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations. See Note 6.
$V_{TX-DIFFp-p}$ Differential peak-to-peak output voltage	TXP, TXN	0.8		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TXP} - V_{TXN}\|$ See Note 7.
$V_{TX-DE-RATIO}$ De-emphasized differential output voltage (ratio)	TXP, TXN	−3.0	−3.5	−4.0	dB	This is the ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 7.
T_{TX-EYE} Minimum TX eye width	TXP, TXN	0.75			UI	The maximum transmitter jitter can be derived as $T_{TXMAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI See Notes 7 and 8.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ Maximum time between the jitter median and maximum deviation from the median	TXP, TXN			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI. See Notes 7 and 8.
$T_{TX-RISE}$, $T_{TX-FALL}$ P/N TX output rise/fall time	TXP, TXN	0.125			UI	See Notes 7 and 10.
$V_{TX-CM-ACp}$ RMS ac peak common mode output voltage	TXP, TXN			20	mV	$V_{TX-CM-ACp} = RMS(\|V_{TXP} + V_{TXN}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ See Note 7.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$ Absolute delta of dc common mode voltage during L0 and electrical idle	TXP, TXN	0		100	mV	$\|V_{TX-CM-DC} - V_{TX-CM-Idle-DC}\| \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during electrical idle] See Note 7.
$V_{TX-CM-DC-LINE-DELTA}$ Absolute delta of dc common mode voltage between P and N	TXP, TXN	0		25	mV	$\|V_{TXP-CM-DC} - V_{TXN-CM-DC}\| \leq 25$ mV when $V_{TXP-CM-DC} = DC_{(avg)}$ of $\|V_{TXP}\|$ $V_{TXN-CM-DC} = DC_{(avg)}$ of $\|V_{TXN}\|$ See Note 7.
$V_{TX-IDLE-DIFFp}$ Electrical idle differential peak output voltage	TXP, TXN	0		20	mV	$V_{TX-IDLE-DIFFp} = \|V_{TXP-Idle} - V_{TXN-Idle}\| \leq 20$ mV See Note 7.
$V_{TX-RCV-DETECT}$ The amount of voltage change allowed during receiver detection	TXP, TXN			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
$V_{TX-DC-CM}$ The TX dc common mode voltage	TXP, TXN	0		3.6	V	The allowed dc common mode voltage under any condition

PCI Express Differential Transmitter Output Ranges (continued)

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
$I_{TX-SHORT}$ TX short circuit current limit	TXP, TXN			90	mA	The total current the transmitter can provide when shorted to its ground.
$T_{TX-IDLE-MIN}$ Minimum time spent in electrical idle	TXP, TXN	50			UI	Minimum time a transmitter must be in electrical idle. Utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
$T_{TX-IDLE-SET-to-IDLE}$ Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	TXP, TXN			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
$T_{TX-IDLE-to-DIFF-DATA}$ Maximum time to transition to valid TX specifications after leaving an electrical idle condition	TXP, TXN			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX-DIFF}$ Differential return loss	TXP, TXN	10			dB	Measured over 50 MHz to 1.25 GHz. See Note 9.
RL_{TX-CM} Common mode return loss	TXP, TXN	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 9.
$Z_{TX-DIFF-DC}$ DC differential TX impedance	TXP, TXN	80	100	120	Ω	TX dc differential mode low impedance
Z_{TX-DC} Transmitter dc impedance	TXP, TXN	40			Ω	Required TXP as well as TXN dc impedance during all states
C_{TX} AC coupling capacitor	TXP, TXN	75		200	nF	All transmitters are ac-coupled and are required on the PWB.

NOTES: 6. No test load is necessarily associated with this value.

7. Specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive TX UIs.
8. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
9. The transmitter input impedance results in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the P and N line. Note that the series capacitors C_{TX} is optional for the return loss measurement.
10. Measured between 20% and 80% at transmitter package terminals into a test load for both V_{TXP} and V_{TXN}.

7.5 PCI Express Differential Receiver Input Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
UI Unit interval	RXP, RXN	399.88	400	400.12	ps	Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations. See Note 11.
$V_{RX-DIFFp-p}$ Differential input peak-to-peak voltage	RXP, RXN	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\lvert V_{RXP} - V_{RXN}\rvert$ See Note 12.
T_{RX-EYE} Minimum receiver eye width	RXP, RXN	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver is derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI See Notes 12 and 13.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ Maximum time between the jitter median and maximum deviation from the median.	RXP, RXN			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI. See Notes 12 and 13.
$V_{RX-CM-ACp}$ AC peak common mode input voltage	RXP, RXN			150	mV	$V_{RX-CM-ACp} = RMS(\lvert V_{RXP} + V_{RXN}\rvert/2 - V_{RX-CM-DC})$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RXP} + V_{RXN}\rvert/2$ See Note 12.
$RL_{RX-DIFF}$ Differential return loss	RXP, RXN	10			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and −300 mV, respectively. See Note 14.
RL_{RX-CM} Common mode return loss	RXP, RXN	6			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and −300 mV, respectively. See Note 14.
$Z_{RX-DIFF-DC}$ DC differential input impedance	RXP, RXN	80	100	120	Ω	RX dc differential mode impedance See Note 15.
Z_{RX-DC} DC input impedance	RXP, RXN	40	50	60	Ω	Required RXP as well as RXN dc impedance (50 Ω ±20% tolerance) See Notes 12 and 15.
$Z_{RX-HIGH-IMP-DC}$ Powered down dc input impedance	RXP, RXN	200K			Ω	Required RXP as well as RXN dc impedance when the receiver terminations do not have power. See Note 16.
$V_{RX-IDLE-DET-DIFFp-p}$ Electrical idle detect threshold	RXP, RXN	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RXP} - V_{RXN}\rvert$ measured at the receiver package terminals
$T_{RX-IDLE-DET-DIFF-ENTER-TIME}$ Unexpected electrical idle enter detect threshold integration time	RXP, RXN			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTER-TIME}$ to signal an unexpected idle condition.

NOTES: 11. No test load is necessarily associated with this value.

12. Specified at the measurement point and measured over any 250 consecutive UIs. A test load must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs is used as a reference for the eye diagram.

13. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs must be used as the reference for the eye diagram.
14. The receiver input impedance results in a differential return loss greater than or equal to 15 dB with the P line biased to 300 mV and the N line biased to −300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the P and N line (i.e., as measured by a Vector Network Analyzer with 50-Ω probes). The series capacitors C_{TX} is optional for the return loss measurement.
15. Impedance during all link training status state machine (LTSSM) states. When transitioning from a PCI Express reset to the detect state (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on the unconfigured lane of a port.
16. The RX dc common mode impedance that exists when no power is present or PCI Express reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

7.6 PCI Express Differential Reference Clock Input Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
$f_{IN-DIFF}$ Differential input frequency	REFCLK+ REFCLK−		100		MHz	The input frequency is 100 MHz + 300 ppm and − 2800 ppm including SSC-dictated variations.
f_{IN-SE} Single-ended input frequency	REFCLK+		125		MHz	The input frequency is 125 MHz ± 300 ppm.
$V_{RX-DIFFp-p}$ Differential input peak-to-peak voltage	REFCLK+ REFCLK−	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\lvert V_{REFCLK+} - V_{REFCLK-}\rvert$
V_{IH-SE}	REFCLK+	$0.7\ V_{DDA_33}$		V_{DDA_33}	V	Single-ended, reference clock mode high-level input voltage
V_{IL-SE}	REFCLK+	0		$0.3\ V_{DDA_33}$	V	Single-ended, reference clock mode low-level input voltage
$V_{RX-CM-ACp}$ AC peak common mode input voltage	REFCLK+ REFCLK−			140	mV	$V_{RX-CM-ACp} = RMS(\lvert V_{REFCLK+} + V_{REFCLK-}\rvert/2 - V_{RX-CM-DC})$ $V_{RX-CM-DC} = DC_{(avg)}\ of\ \lvert V_{REFCLK+} + V_{REFCLK-}\rvert/2$
Duty cycle	REFCLK+ REFCLK−	40%		60%		Differential and single-ended waveform input duty cycle
$Z_{RX-DIFF-DC}$ DC differential input impedance	REFCLK+ REFCLK−		20		kΩ	REFCLK+/− dc differential mode impedance
Z_{RX-DC} DC input impedance	REFCLK+ REFCLK−		20		kΩ	REFCLK+ dc single-ended mode impedance

NOTE 17: The XIO2000A is compliant with the defined system jitter models for a PCI-Express reference clock and associated TX/RX link. These system jitter models are described in the *PCI-Express Jitter Modeling*, Revision 1.0RD document. Any usage of the XIO2000A in a system configuration that does not conform to the defined system jitter models requires the system designer to validate the system jitter budgets.

7.7 Electrical Characteristics Over Recommended Operating Conditions (PCI Bus)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNITS
V_{IH}	High-level input voltage (Note 18)	V_{CCP} = 3.3 V		0.5 V_{DD_33}	V_{CCP}	V
		V_{CCP} = 5.0 V		0.5 V_{DD_33}	V_{CCP}	
V_{IL}	Low-level input voltage (Note 18)	V_{CCP} = 3.3 V		0	0.3 V_{DD_33}	V
		V_{CCP} = 5.0 V		0	0.3 V_{DD_33}	
V_I	Input voltage			0	V_{CCP}	V
V_O	Output voltage (Note 19)			0	V_{DD_33}	V
t_t	Input transition time (t_{rise} and t_{fall})			1	4	ns
V_{OH}	High-level output voltage (Note 19)	V_{DD_33}	I_{OH} = −32 mA	0.7 V_{DD_33}		V
V_{OL}	Low-level output voltage (Note 19)	V_{DD_33}	I_{OL} = 32 mA		0.18 V_{DD_33}	V
I_{OZ}	High-impedance, output current (Note 19)	V_{CCP} = 3.3 V	V_I = 0 to V_{CCP}		±10	µA
		V_{CCP} = 5.0 V	V_I = 0 to V_{CCP}		±70	
I_I	Input current (Note 18)	V_{CCP} = 3.3 V	V_I = 0 to V_{CCP}		±10	µA
		V_{CCP} = 5.0 V	V_I = 0 to V_{CCP}		±70	

NOTES: 18. Applies to external inputs and bidirectional buffers.
19. Applies to external outputs and bidirectional buffers.

Note: This table applies to CLK, CLKOUT6:0, AD31:0, C/$\overline{BE}$[3:0], $\overline{DEVSEL}$, $\overline{FRAME}$, $\overline{GNT}$5:0, $\overline{INTD}$:A, $\overline{IRDY}$, PAR, $\overline{PERR}$, $\overline{REQ}$5:0, $\overline{PRST}$, $\overline{SERR}$, $\overline{STOP}$, $\overline{TRDY}$, SERIRQ, M66EN, and $\overline{LOCK}$ terminals.

7.8 Electrical Characteristics Over Recommended Operating Conditions (3.3-V I/O)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNITS
V_{IH}	High-level input voltage (Note 20)	V_{DD_33}		0.7V_{DD_33}	V_{DD_33}	V
V_{IL}	Low-level input voltage (Note 20)	V_{DD_33}		0	0.3 V_{DD_33}	V
V_I	Input voltage			0	V_{DD_33}	V
V_O	Output voltage (Note 21)			0	V_{DD_33}	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis (Note 23)				0.13V_{DD_33}	V
V_{OH}	High-level output voltage	V_{DD_33}	I_{OH} = −4 mA	0.8V_{DD_33}		V
V_{OL}	Low-level output voltage	V_{DD_33}	I_{OL} = 4 mA		0.22V_{DD_33}	V
I_{OZ}	High-impedance, output current (Note 21)	V_{DD_33}	V_I = 0 to V_{DD_33}		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown (Note 24)	V_{DD_33}	V_I = 0 to V_{DD_33}		±100	µA
I_I	Input current (Note 22)	V_{DD_33}	V_I = 0 to V_{DD_33}		±1	µA

NOTES: 20. Applies to external inputs and bidirectional buffers.
21. Applies to external outputs and bidirectional buffers.
22. Applies to external input buffers.
23. Applies to $\overline{PERST}$, $\overline{GRST}$, and PME.
24. Applies to $\overline{GRST}$ (pullup), EXT_ARB_EN (pulldown), CLKRUN_EN (pulldown), and most GPIO (pullup).

Note: This table applies to $\overline{PERST}$, $\overline{WAKE}$, REFCLK_SEL, $\overline{PME}$, CLKRUN_EN, EXT_ARB_EN, $\overline{GRST}$, GPIO7:0, and all RSVD input terminals.

7.9 PCI Clock Timing Requirements Over Recommended Operating Conditions

PARAMETER		33 MHZ		66 MHZ		UNITS
		MIN	MAX	MIN	MAX	
t_c	Cycle time, CLK	30	∞	15	30	ns
t_{wH}	Pulse duration (width), CLK high	11		6		ns
t_{wL}	Pulse duration (width), CLK low	11		6		ns
t_{rise} t_{fall}	Slew rate, CLK	1.5	4	1.5	4	V/ns
t_{dc}	CLKOUT6:0 duty cycle	40%	60%	40%	60%	
t_{skew}	CLKOUT6:0 skew between clock outputs		0.5		0.5	ns
t_{su}	Setup time, CLKOUT6:0 stable before $\overline{PRST}$ is deasserted		100		100	µs

7.10 PCI Bus Timing Requirements Over Recommended Operating Conditions

PARAMETER		TEST CONDITION	33 MHZ		66 MHZ		UNITS
			MIN	MAX	MIN	MAX	
t_{pd}	CLK to shared signal valid propagation delay time	C_L = 50 pF		11			ns
		C_L = 30 pF				6	
t_{pd}	CLK to shared signal invalid propagation delay time	C_L = 50 pF	2				ns
		C_L = 30 pF			1		
t_{on}	Enable time, high-impedance-to-active delay time from CLK	C_L = 50 pF	2				ns
		C_L = 30 pF			1		
t_{off}	Disable time, active-to-high-impedance delay time from CLK	C_L = 50 pF		28			ns
		C_L = 30 pF				14	
t_{su}	Setup time on shared signals before CLK valid (rising edge)		7		3		ns
t_h	Hold time on shared signals after CLK valid (rising edge)		0		0		ns

Note: The PCI shared signals are AD31:0, C/$\overline{BE3:0}$, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, IDSEL, $\overline{DEVSEL}$, $\overline{LOCK}$, SERIRQ, PAR, $\overline{PERR}$, $\overline{SERR}$, and $\overline{CLKRUN}$.

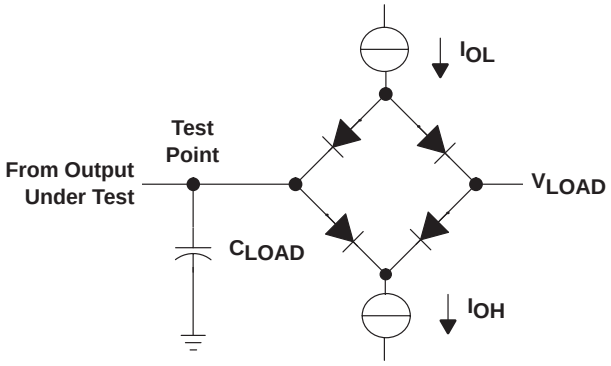
7.11 PCI Bus Parameter Measurement Information

LOAD CIRCUIT PARAMETERS

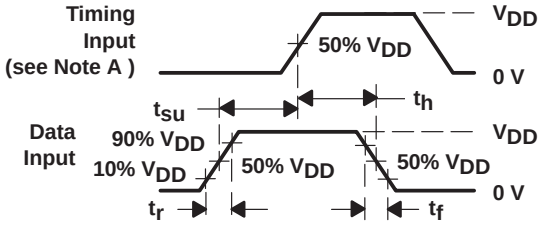
TIMING PARAMETER		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	30/50	12	−12	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	30/50	12	−12	1.5
	t_{PLZ}				
t_{pd}		30/50	12	−12	‡

† C_{LOAD} includes the typical load-circuit distributed capacitance.

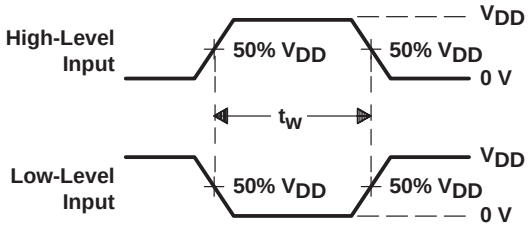
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}}$ = 50 Ω, where V_{OL} = 0.6 V, I_{OL} = 12 mA



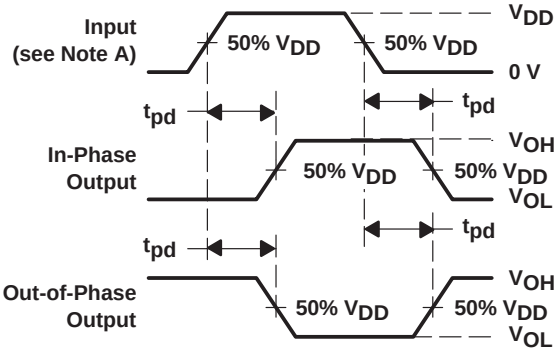
LOAD CIRCUIT



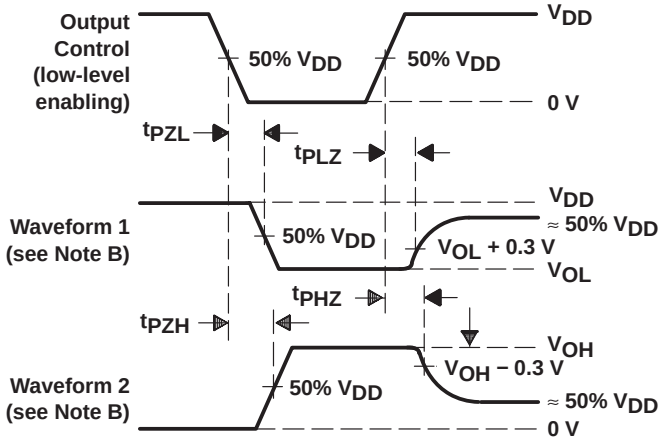
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, $t_r \le 6$ ns, $t_f \le 6$ ns.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 7−1. Load Circuit And Voltage Waveforms

7.12 PCI Bus Parameter Measurement Information

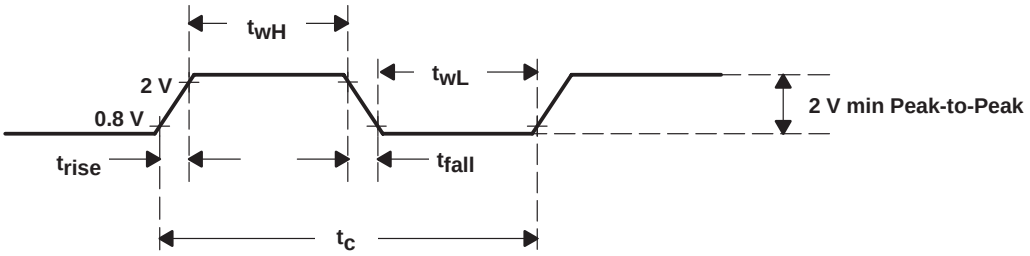


Figure 7−2. CLK Timing Waveform

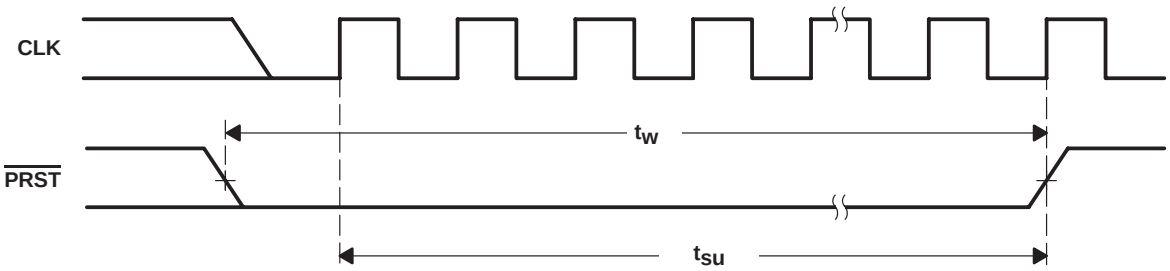


Figure 7−3. PRST Timing Waveforms

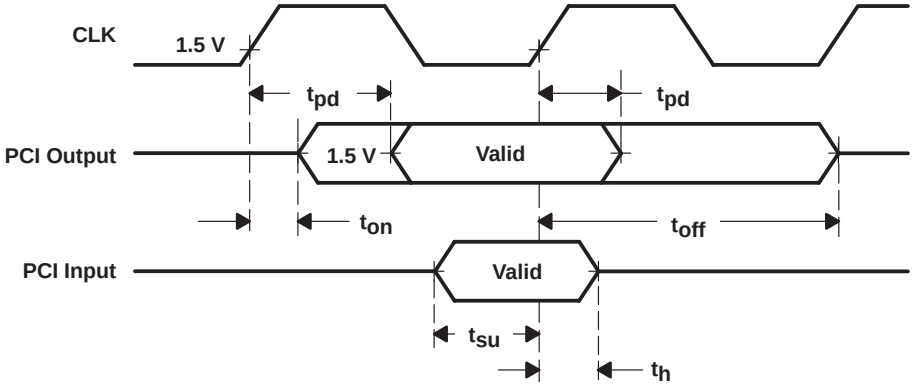


Figure 7−4. Shared Signals Timing Waveforms

8 Glossary

ACRONYM	DEFINITION
BIST	Built-in self test
ECRC	End-to-end cyclic redundancy code
EEPROM	Electrically erasable programmable read-only memory
GP	General purpose
GPIO	General-purpose input output
ID	Identification
IF	Interface
IO	Input output
I2S	Inter IC sound
LPM	Link power management
LSB	Least significant bit
MSB	Most significant bit
MSI	Message signaled interrupts
PCI	Peripheral component interface
PME	PCI power management event
QoS	Quality-of-service
RX	Receive
SCL	Serial-bus clock
SDA	Serial-bus data
TC	Traffic class
TLP	Transaction layer packet or protocol
TX	Transmit
VC	Virtual channel
WRR	Weighted round-robin

9 Mechanical Data

The XIO2000A/XIO2000AI devices is available in the 175−ball lead−free (Pb atomic number 82) Microstar BGA package (ZHH), the 175-ball lead-free (Pb atomic number 82) MicroStar BGA package ZHC, the 201-ball MicroStar BGA package (GZZ – XIO2000A Only,) or the 201-ball lead-free (Pb atomic number 82) MicroStar BGA package (ZZZ). The following figures show the mechanical dimensions for the packages. The GZZ and ZZZ packages are mechanically identical.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XIO2000AZAV	Active	Production	NFBGA (ZAV) | 201	126 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	XIO2000A
XIO2000AZAV.A	Active	Production	NFBGA (ZAV) | 201	126 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	XIO2000A
XIO2000AZAY	Obsolete	Production	NFBGA (ZAY) | 175	-	-	Call TI	Call TI	0 to 70	XIO2000A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

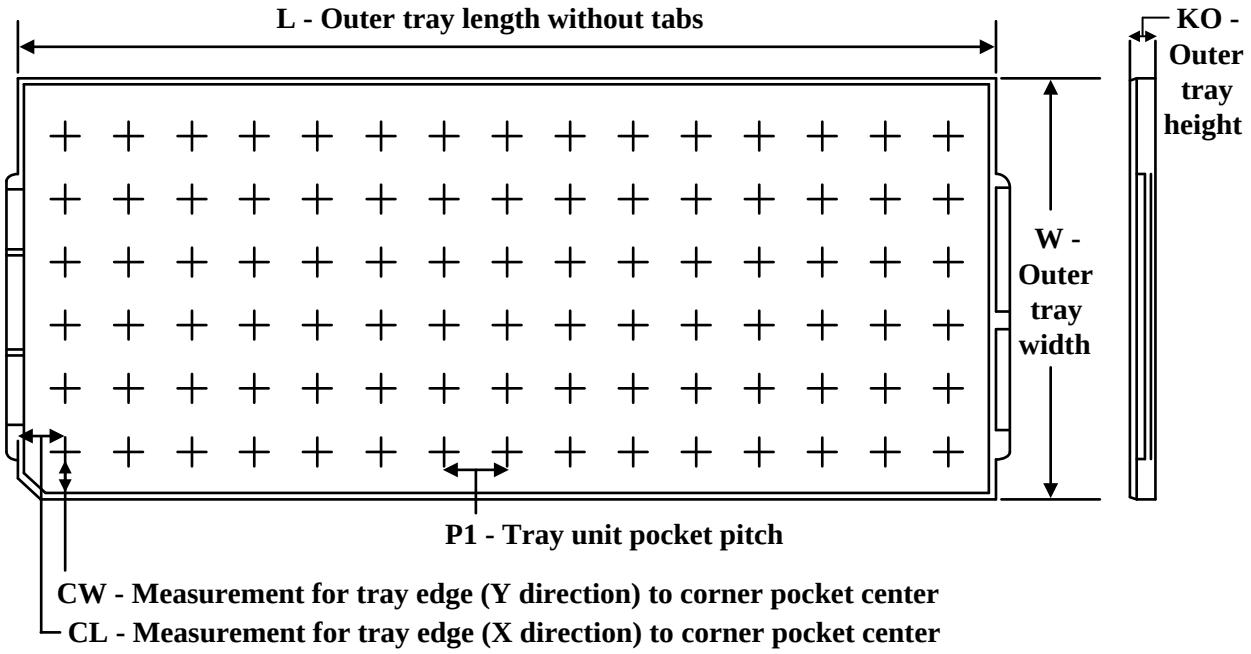
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

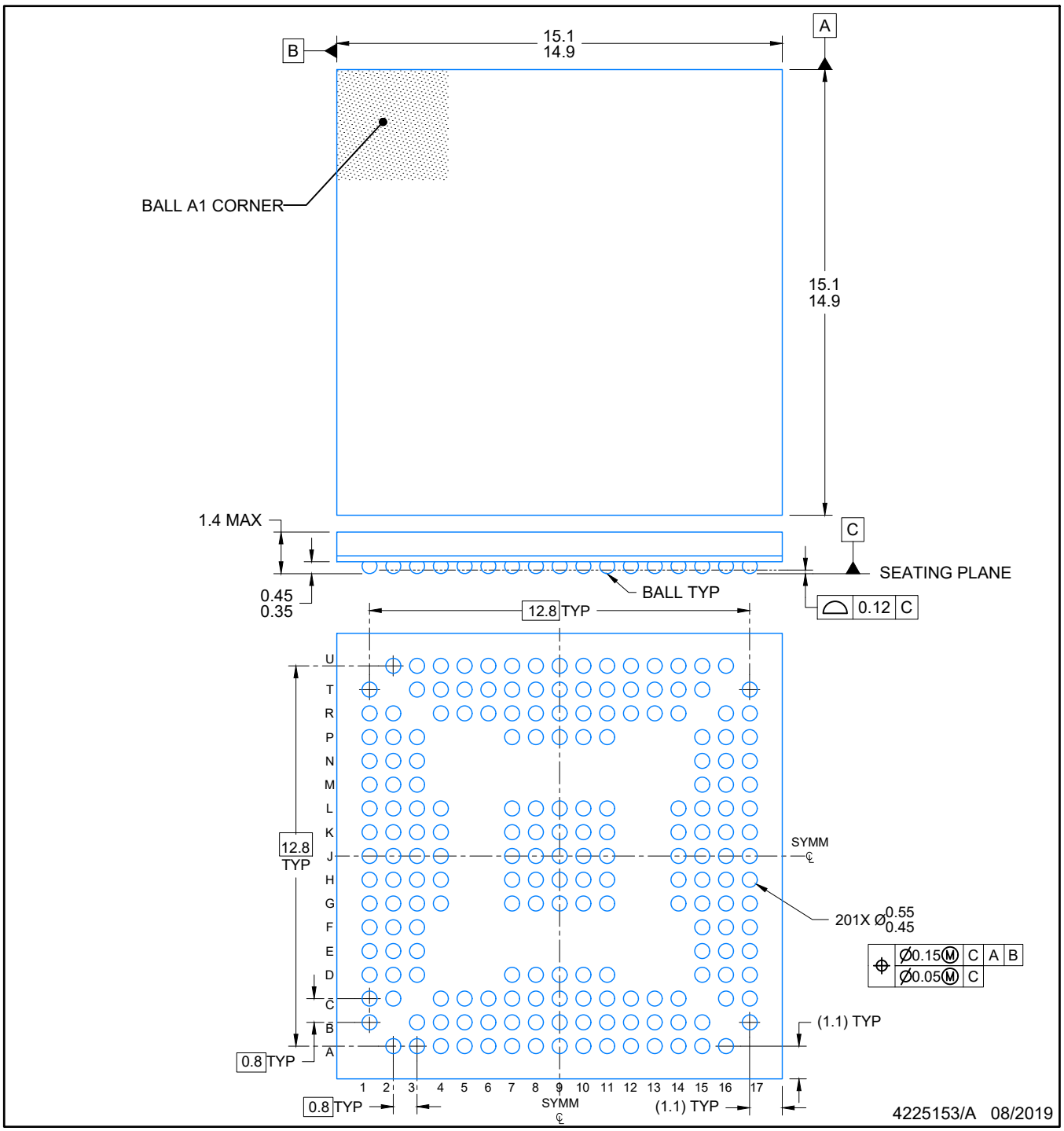
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
XIO2000AZAV	ZAV	NFBGA	201	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35
XIO2000AZAV.A	ZAV	NFBGA	201	126	7 X 18	150	315	135.9	7620	17.2	11.3	16.35

PACKAGE OUTLINE

ZAV0201A

NFBGA - 1.4 mm max height

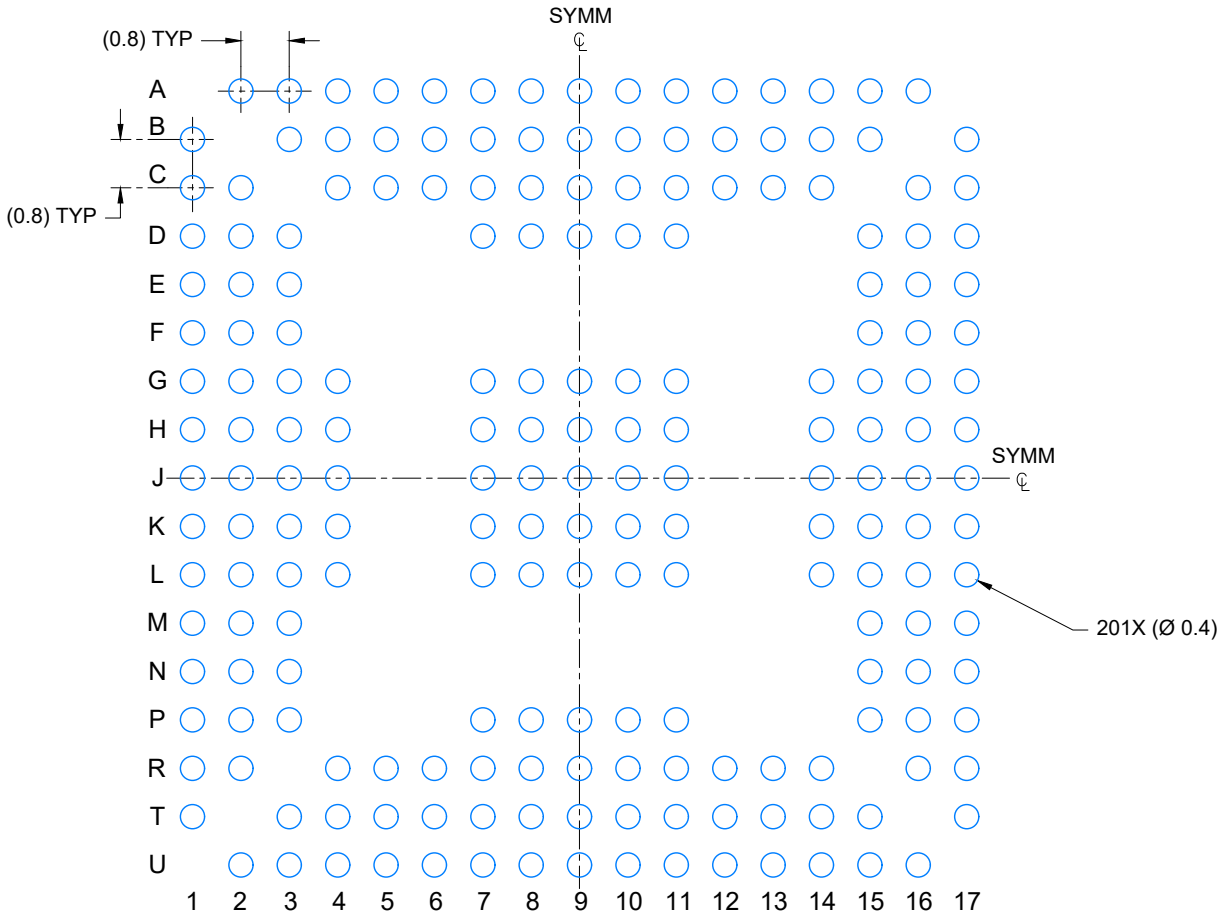
PLASTIC BALL GRID ARRAY



NOTES:

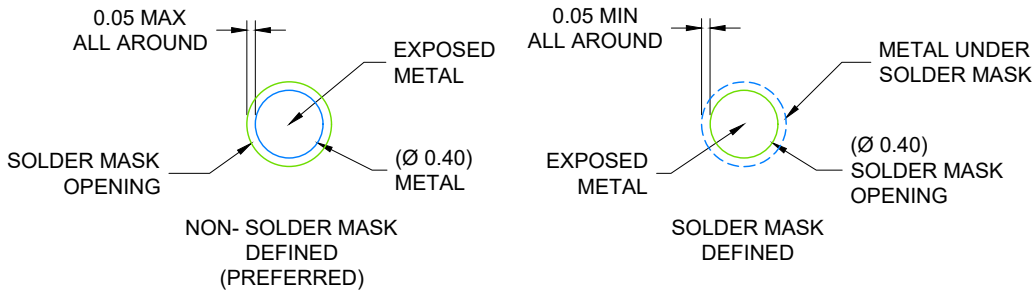
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 8X



SOLDER MASK DETAILS

NOT TO SCALE

4225153/A 08/2019

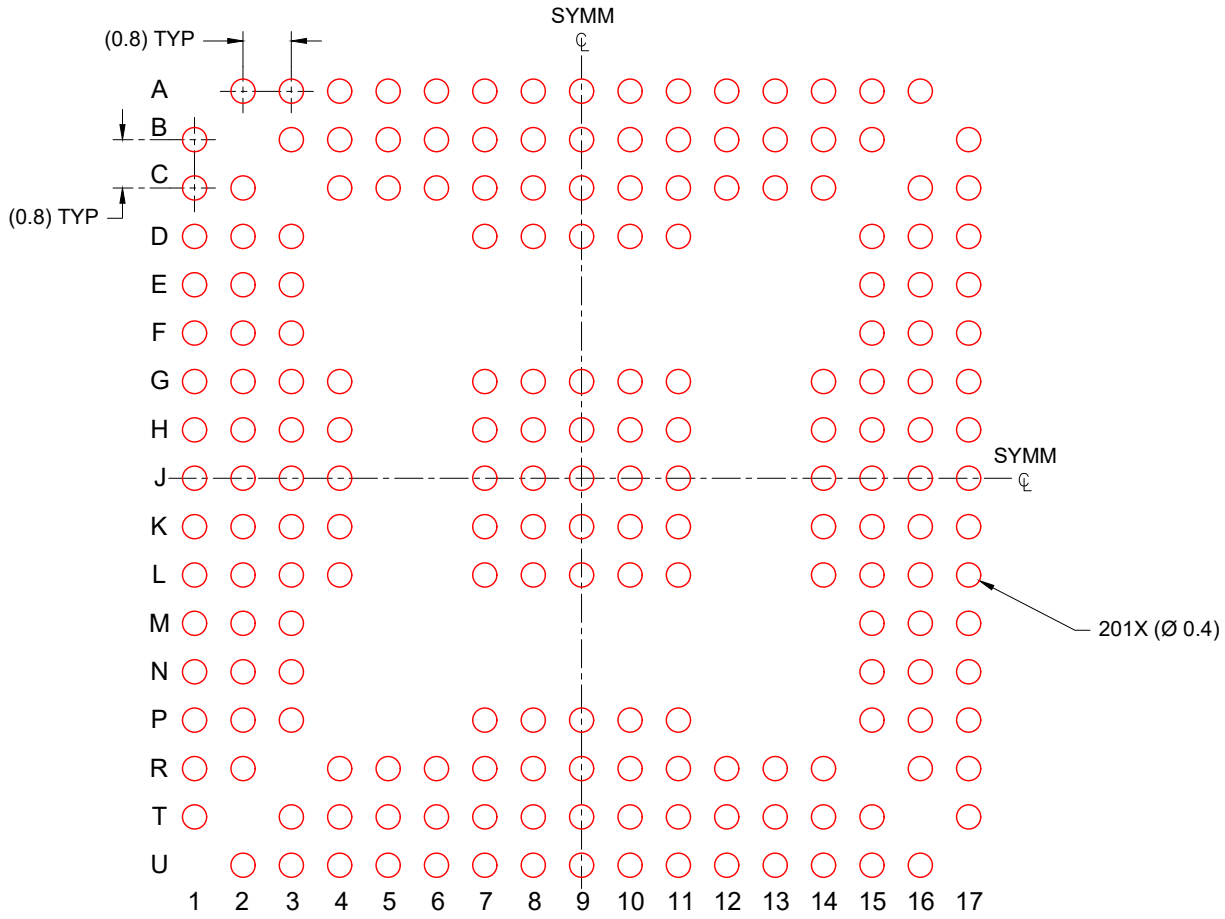
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 18X

4225153/A 08/2019

NOTES: (continued)

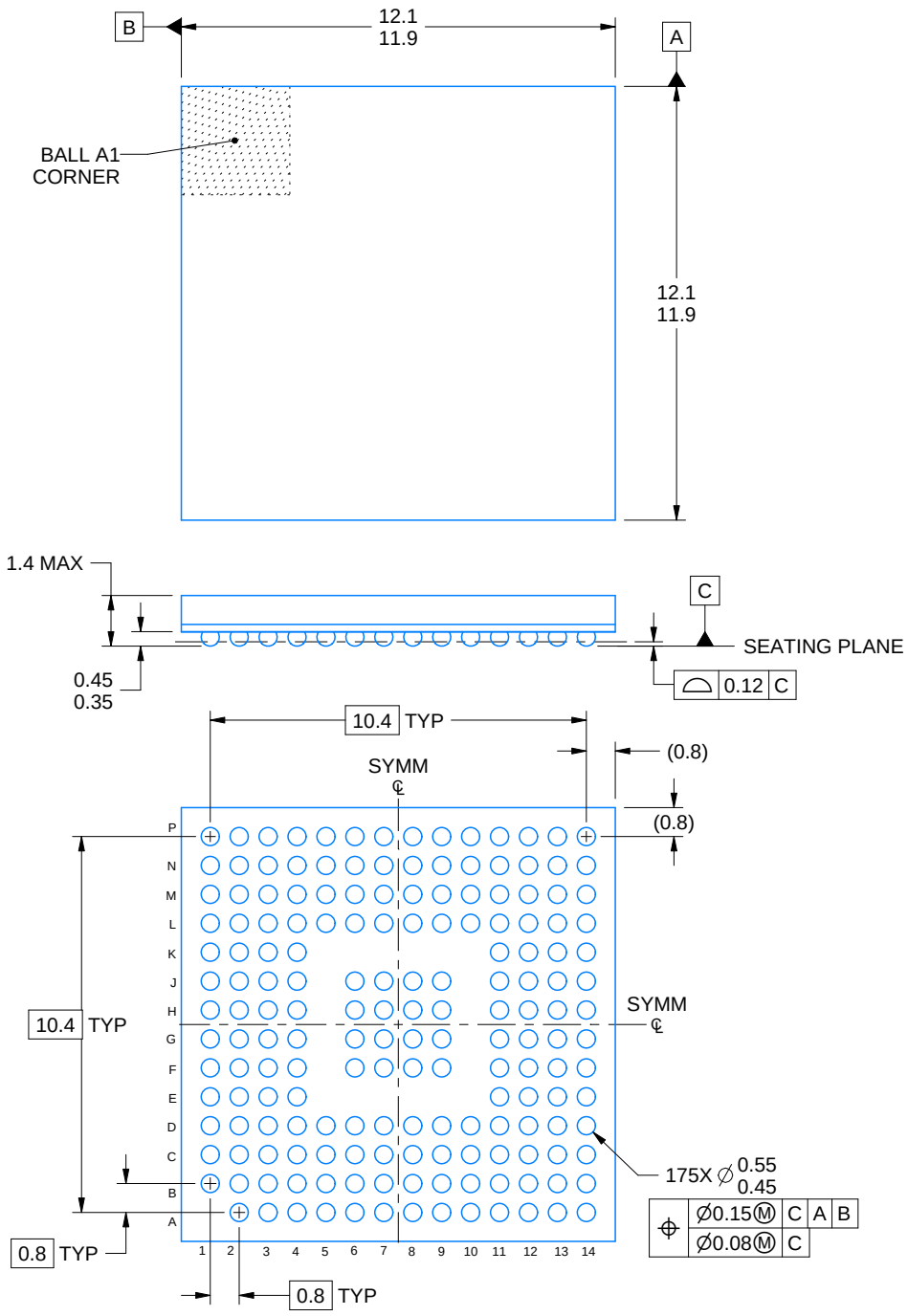
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZAY0175A

NFBGA - 1.4 mm max height

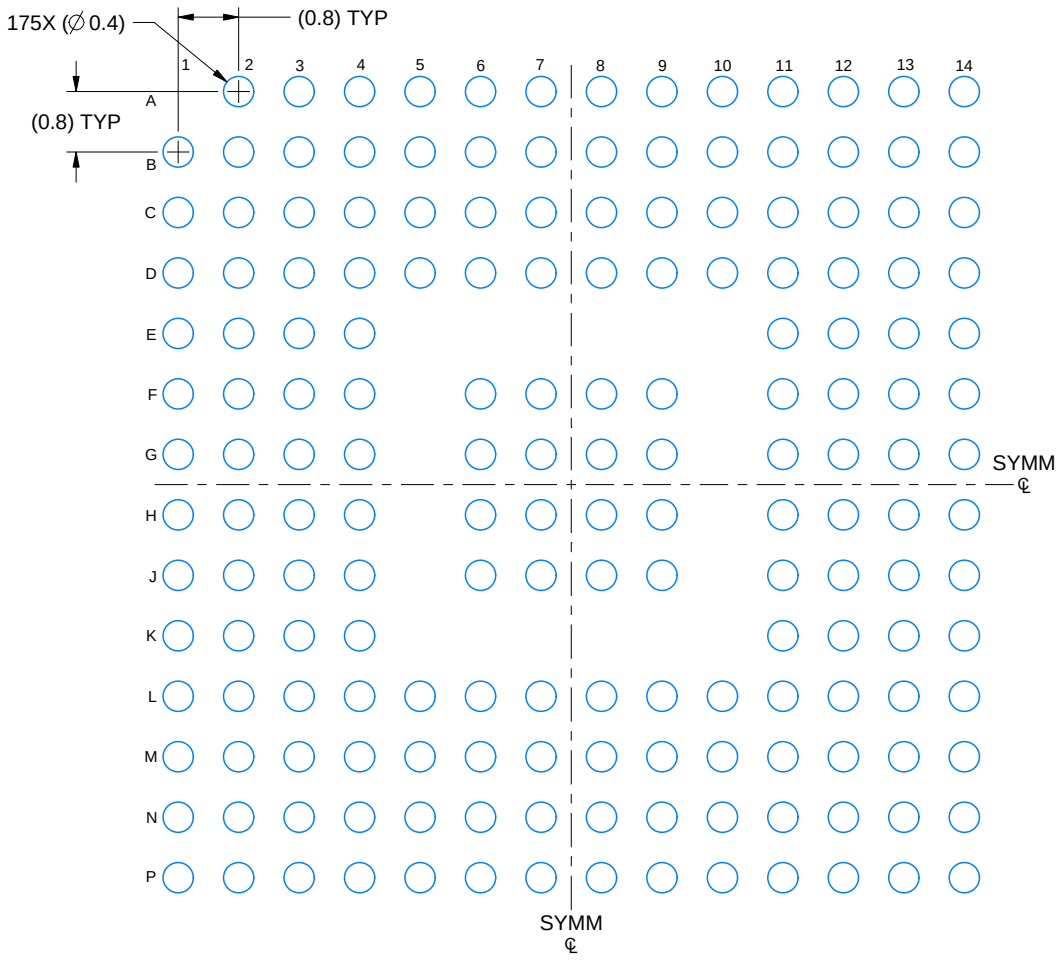
PLASTIC BALL GRID ARRAY



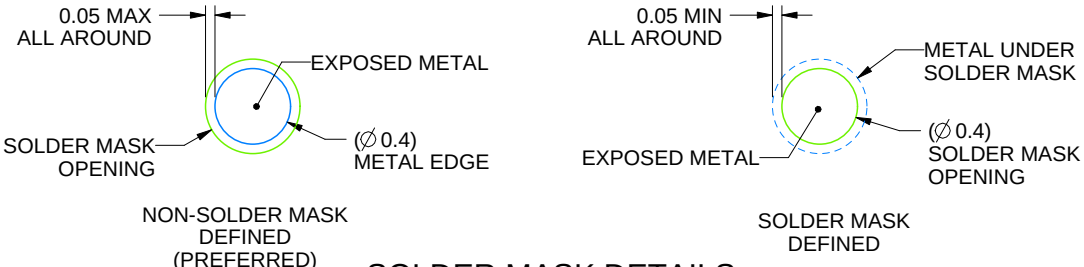
4219814/A 05/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

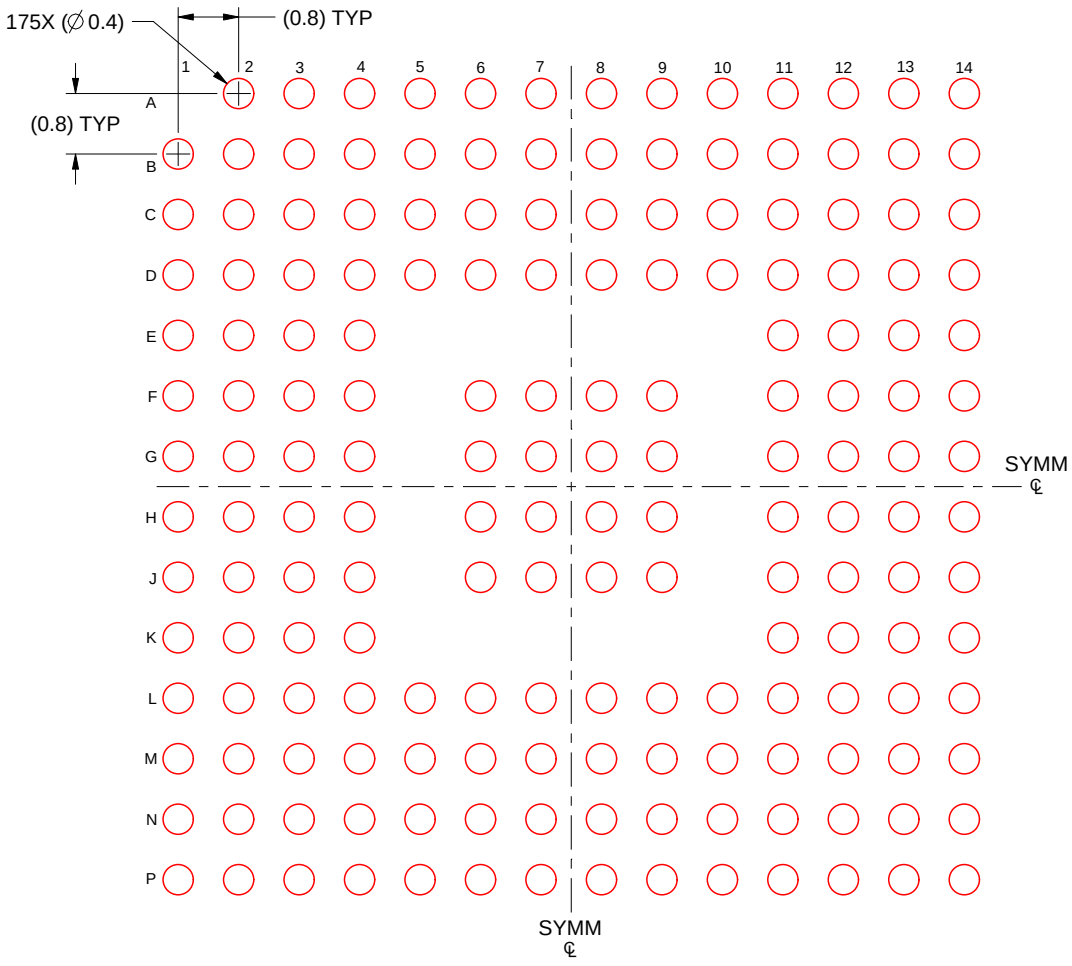


SOLDER MASK DETAILS
NOT TO SCALE

4219814/A 05/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4219814/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025