TEXAS INSTRUMENTS

THVD2410
THVD2450

SLLSF20A – JULY 2019 – REVISED OCTOBER 2019

THVD24x0 ±70-V Fault-Protected 3.3-V to 5-V RS-485 Transceivers With IEC ESD

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A and TIA/EIA-422B standards
- 3-V to 5.5-V supply voltage
- Differential output exceeds 2.1 V for PROFIBUS compatibility with 5-V supply
- Bus I/O protection
  - ±70-V DC bus fault
  - ±16-kV HBM ESD
  - ±12-kV IEC 61000-4-2 contact discharge
  - ±12-kV IEC 61000-4-2 air-gap discharge
  - ±4-kV IEC 61000-4-4 fast transient burst
- Half-duplex devices available in two speed grades
  - THVD2410: 500 kbps
  - THVD2450: 50 Mbps
- Extended ambient temperature range: -40°C to 125°C
- Extended operational common-mode range: ±25 V
- Enhanced receiver hysteresis for noise immunity
- Low power consumption
  - Low shutdown supply current: < 1 µA
  - Current during operation: < 5.6 mA
- Glitch-free power-up/down for hot plug-in capability
- Open, short, and idle bus failsafe
- Thermal shutdown
- 1/8 unit load (up to 256 bus nodes)
- Small VSON and VSSOP packages to save board space or SOIC for drop-in compatibility

2 Applications

- Motor drives
- Factory automation & control
- HVAC systems
- Building automation
- Grid infrastructure
- Electricity meters
- Process analytics
- Video surveillance

3 Description

THVD2410 and THVD2450 are ±70-V fault-protected, half-duplex, RS-422/RS-485 transceivers operating on a single 3-V to 5.5-V supply. Bus interface pins are protected against overvoltage conditions during all modes of operation ensuring robust communication in rugged industrial environments.

These devices feature integrated IEC ESD protection, eliminating the need for external system-level protection components. Extended ±25-V input common-mode range guarantees reliable data communication over longer cable run lengths and/or in the presence of large ground loop voltages. Enhanced 250-mV receiver hysteresis ensures high noise rejection. In addition, the receiver fail-safe feature guarantees a logic high when the inputs are open or shorted together.

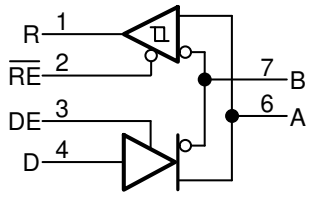
THVD24x0 devices are available in small VSSOP and VSON packages for space-constrained applications. These devices are characterized over ambient free-air temperatures from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THVD2410 THVD2450	VSON (8)	3.00 mm × 3.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

THVD2410 and THVD2450 Simplified Schematic



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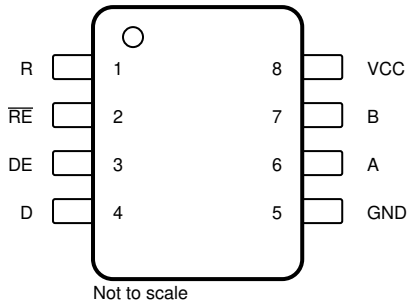
4 Revision History

Changes from Original (July 2019) to Revision A **Page**

- Deleted *Application*: Seismic test equipment ... 1
- Deleted the product preview note from THVD2410 in the *Device Information* table ... 1

5 Pin Configuration and Functions

THVD2410, THVD2450 Devices
8-Pin D (SOIC) and DGK (VSSOP) Packages
Top View



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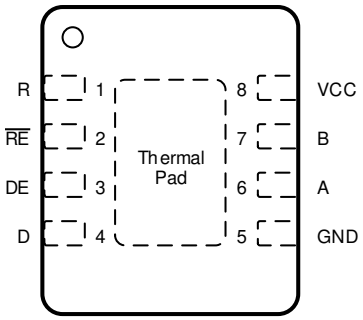
THVD2410, THVD2450 Devices
8-Pin DRB Package (VSON)
Top View



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Pin Functions

PIN				I/O	DESCRIPTION
NAME	D	DGK	DRB		
A	6	6	6	Bus input/output	Bus I/O port, A (complementary to B)
B	7	7	7	Bus input/output	Bus I/O port, B (complementary to A)
D	4	4	4	Digital input	Driver data input
DE	3	3	3	Digital input	Driver enable, active high (2-MΩ internal pull-down)
GND	5	5	5	Ground	Device ground
R	1	1	1	Digital output	Receive data output
V_{CC}	8	8	8	Power	3.3-V to 5-V supply
$\overline{RE}$	2	2	2	Digital input	Receiver enable, active low (2-MΩ internal pull-up)
Thermal Pad	—	—	—	—	No electrical connection. Should be connected to GND plane for optimal thermal performance

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.5	7	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	–70	70	V
Input voltage	Range at any logic pin (D, DE, or $\overline{RE}$)	–0.3	5.7	V
Receiver output current	I_O	–24	24	mA
Storage temperature	T_{stg}	–65	170	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±16,000	V
			All pins except bus terminals and GND	±8,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±12,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±12,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)(1)		–25		25	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2			V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)				0.8	V
V_{ID}	Differential input voltage		–25		25	V
I_O	Output current, driver		–60		60	mA
I_{OR}	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate	THVD2410			500	kbps
		THVD2450			50	Mbps
T_A	Operating ambient temperature		-40		125	°C
T_J	Junction temperature		-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.5 Thermal Information

THERMAL METRIC(1)		THVD2410 THVD2450 D (SOIC) 8 PINS	THVD2410 THVD2450 DGK (VSSOP) 8 PINS	THVD2410 THVD2450 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.9	164.0	47.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.1	49.5	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.1	85.5	20.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.1	5.1	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.2	83.7	20.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	5.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Dissipation

PARAMETER		TEST CONDITIONS			VALUE	UNIT
P_D	Driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125 °C, random data (PRBS7) at signaling rate	Unterminated R_L = 300 Ω, C_L = 50 pF (driver)	THVD2410	500 kbps	130	mW
			THVD2450	50 Mbps	340	
		RS-422 load R_L = 100 Ω, C_L = 50 pF (driver)	THVD2410	500 kbps	170	mW
			THVD2450	50 Mbps	340	
		RS-485 load R_L = 54 Ω, C_L = 50 pF (driver)	THVD2410	500 kbps	240	mW
			THVD2450	50 Mbps	370	

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver								
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, –25 V ≤ V_{test} ≤ 25 V (See Figure 10)			1.5	3.3		V
		R_L = 60 Ω, –25 V ≤ V_{test} ≤ 25 V, 4.5 V ≤ V_{CC} ≤ 5.5 V (See Figure 10)			2.1	3.3		V
		R_L = 100 Ω (See Figure 11)			2	4		V
		R_L = 54 Ω (See Figure 11)			1.5	3.3		V
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage	R_L = 54 Ω or 100 Ω (See Figure 11)			–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 11)			1	V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 11)			–50		50	mV
I_{OS}	Short-circuit output current	DE = V_{CC}, -70 V ≤ (V_A or V_B) ≤ 70 V			–250		250	mA
Receiver								
I_I	Bus input current	DE = 0 V, V_{CC} = 0 V or 5.5 V	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V		75	125	µA
				V_I = 25 V		150	250	
				V_I = –7 V	–100	–40		
				V_I = –25 V	–250	–150		
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of ± 25 V			40	125	200	mV
V_{TH-}	Negative-going input threshold voltage(1)				–200	–125	-40	mV
V_{HYS}	Input hysteresis					250		mV
V_{TH_FSH}	Input fail-safe threshold				–40		40	mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1 MHz				50		pF
V_{OH}	Output high voltage	I_{OH} = –8 mA			V_{CC} – 0.4	V_{CC} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8 mA				0.2	0.4	V
I_{OZ}	Output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}			–1		1	µA
Logic								
I_{IN}	Input current (DE)	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}					5	µA
I_{IN}	Input current (D, $\overline{RE}$)	3 V ≤ V_{CC} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{CC}			–5			µA
Thermal Protection								
T_{SHDN}	Thermal shutdown threshold	Temperature rising			150	170		°C
T_{HYS}	Thermal shutdown hysteresis					10		°C
Supply								
I_{CC}	Supply current (quiescent)	Driver and receiver enabled		$\overline{RE}$ = 0 V, DE = V_{CC}, No load		3.5	5.6	mA
		Driver enabled, receiver disabled		$\overline{RE}$ = V_{CC}, DE = V_{CC}, No load		2.5	4.4	mA
		Driver disabled, receiver enabled		$\overline{RE}$ = 0 V, DE = 0 V, No load		1.8	2.4	mA
		Driver and receiver disabled		$\overline{RE}$ = V_{CC}, DE = 0 V, D = open, No load		0.1	1	µA

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than $V_{TH–}$.

6.8 Switching Characteristics

500-kbps device (THVD2410) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 12	240	280	600	ns
t_{PHL}, t_{PLH}	Propagation delay				275	350	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					10	ns
t_{PHZ}, t_{PLZ}	Disable time		See Figure 13 and Figure 14		45	95	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			175	270	ns
		$\overline{RE}$ = V_{CC}			1.5	4	µs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{CC}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See Figure 15		13	20	ns
t_{PHL}, t_{PLH}	Propagation delay				50	80	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					7	ns
t_{PHZ}, t_{PLZ}	Disable time				30	40	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = V_{CC}	See Figure 16		90	120	ns
		DE = 0 V	See Figure 17		2	4	µs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See Figure 18	7	10	18	µs
$t_{D(FSO)}$	Delay to exit fail-safe operation			35	45	60	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See Figure 17	50		500	ns

6.9 Switching Characteristics

50-Mbps device (THVD2450) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 12		5	7	ns
t_{PHL}, t_{PLH}	Propagation delay			5	10	16	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					3.5	ns
t_{PHZ}, t_{PLZ}	Disable time		See Figure 13 and Figure 14		11	30	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ = 0 V			8	25	ns
		$\overline{RE}$ = V_{CC}			1.5	4	µs
t_{SHDN}	Time to shutdown	$\overline{RE}$ = V_{CC}		50		500	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See Figure 15		2	6	ns
t_{PHL}, t_{PLH}	Propagation delay				40	55	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					4	ns
t_{PHZ}, t_{PLZ}	Disable time				7	15	ns
$t_{PZH(1)}$, $t_{PZL(1)}$, $t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	DE = V_{CC}	See Figure 16		50	70	ns
		DE = 0 V	See Figure 17		2	4	µs
$t_{D(OFS)}$	Delay to enter fail-safe operation	C_L = 15 pF	See Figure 18	7	10	18	µs
$t_{D(FSO)}$	Delay to exit fail-safe operation			25	35	50	ns
t_{SHDN}	Time to shutdown	DE = 0 V	See Figure 17	50		500	ns

6.10 Typical Characteristics

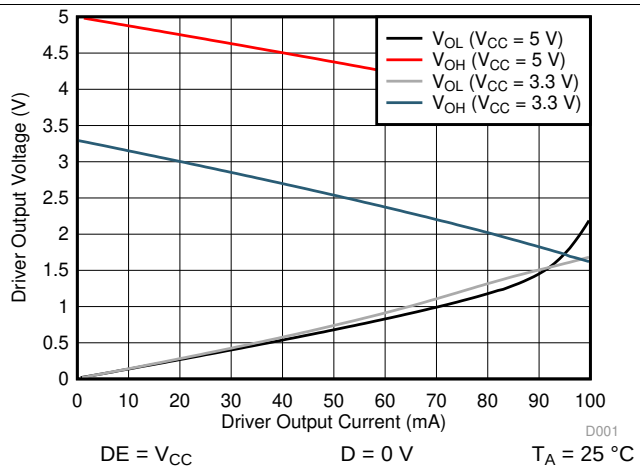


Figure 1. Driver Output Voltage vs Driver Output Current

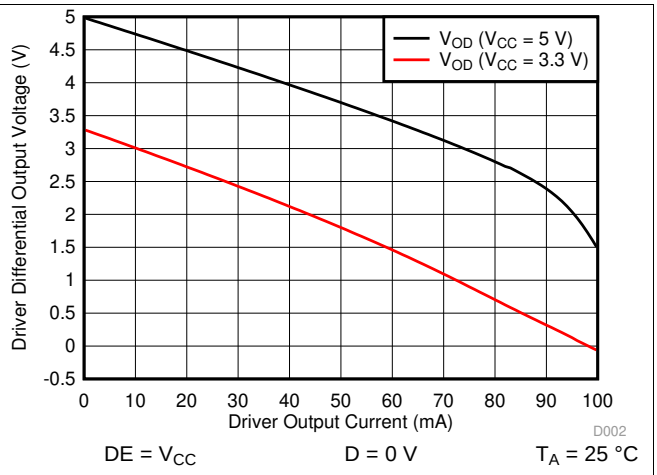


Figure 2. Driver Differential Output voltage vs Driver Output Current

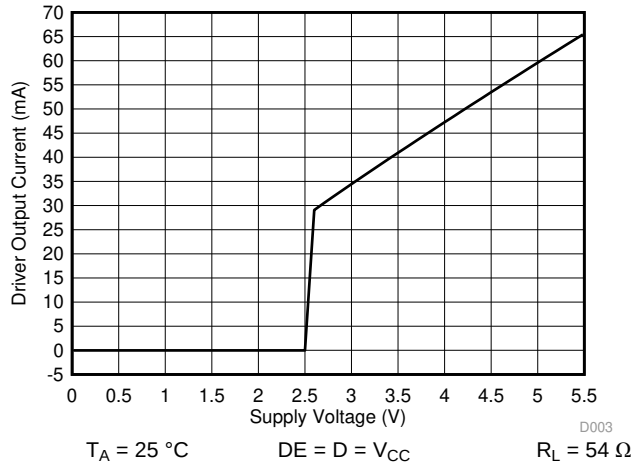


Figure 3. Driver Output Current vs Supply Voltage

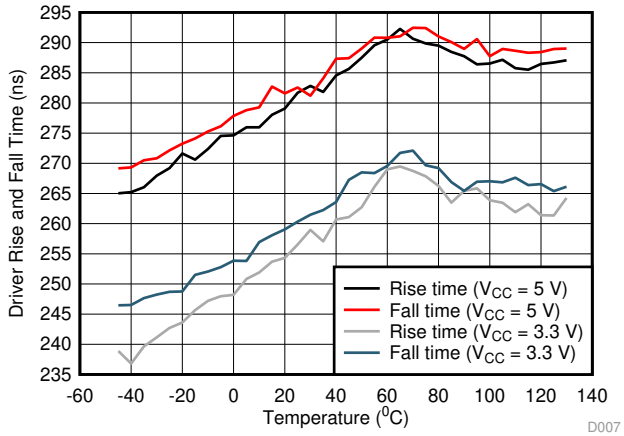


Figure 4. THVD2410 Driver Rise or Fall Time vs Temperature

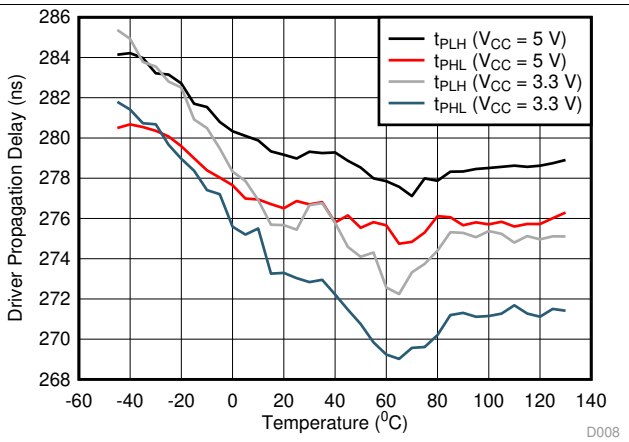


Figure 5. THVD2410 Driver Propagation Delay vs Temperature

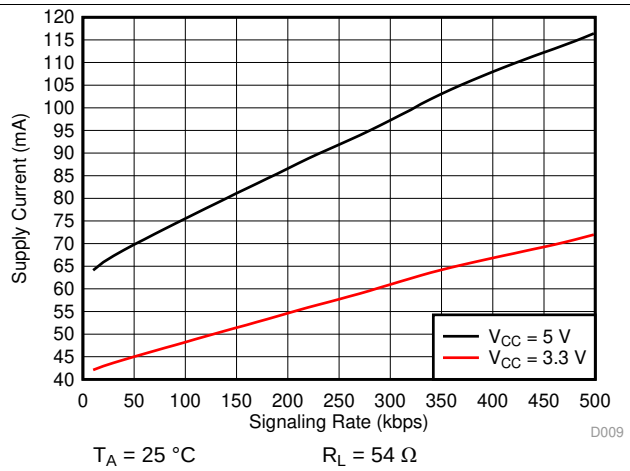


Figure 6. THVD2410 Supply Current vs Signal Rate

Typical Characteristics (continued)

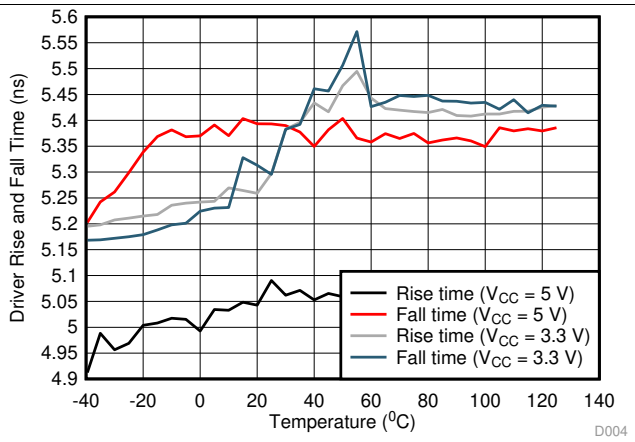


Figure 7. THVD2450 Driver Rise or Fall Time vs Temperature

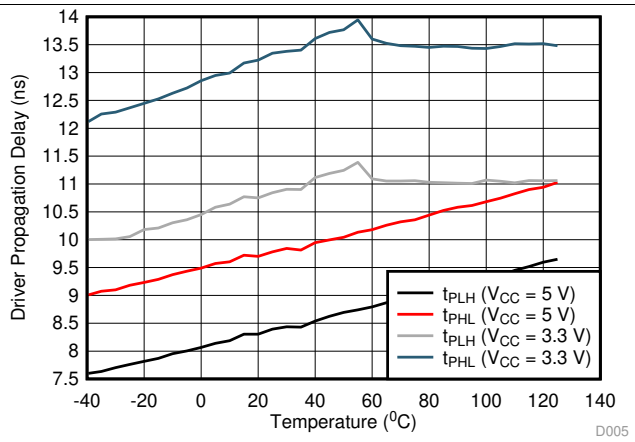
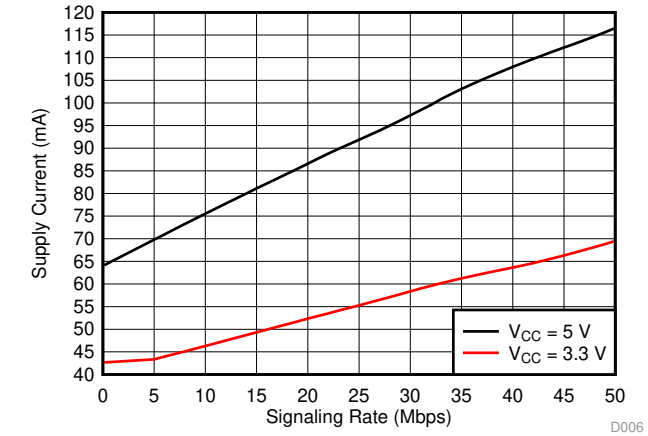


Figure 8. THVD2450 Driver Propagation Delay vs Temperature



T_A = 25 °C R_L = 54 Ω

Figure 9. THVD2450 Supply Current vs Signal Rate

7 Parameter Measurement Information

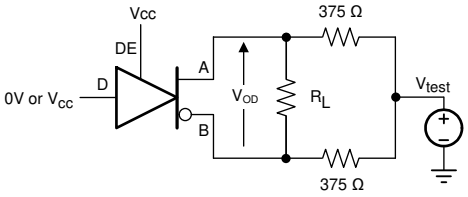


Figure 10. Measurement of Driver Differential Output Voltage With Common-Mode Load

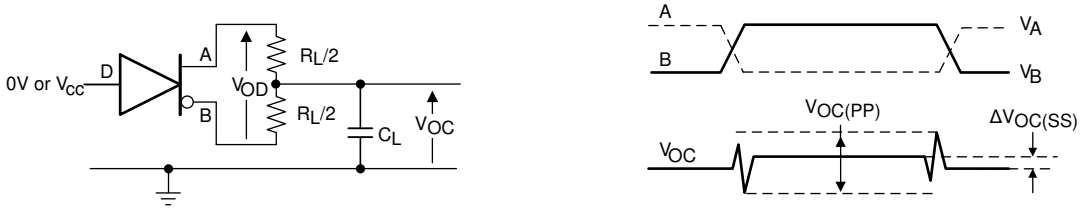


Figure 11. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

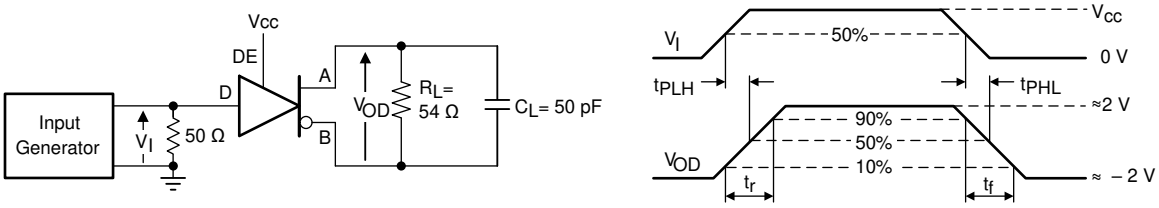


Figure 12. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

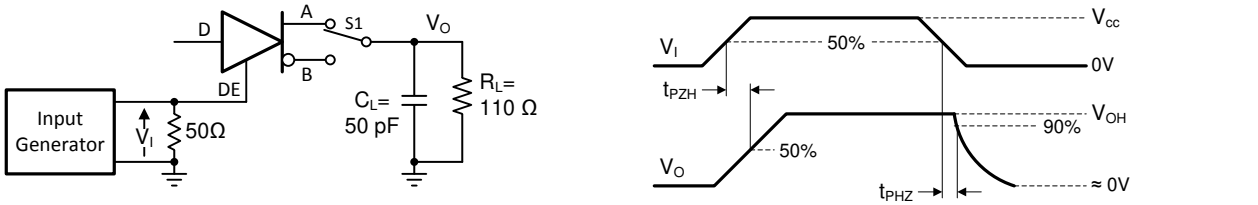


Figure 13. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

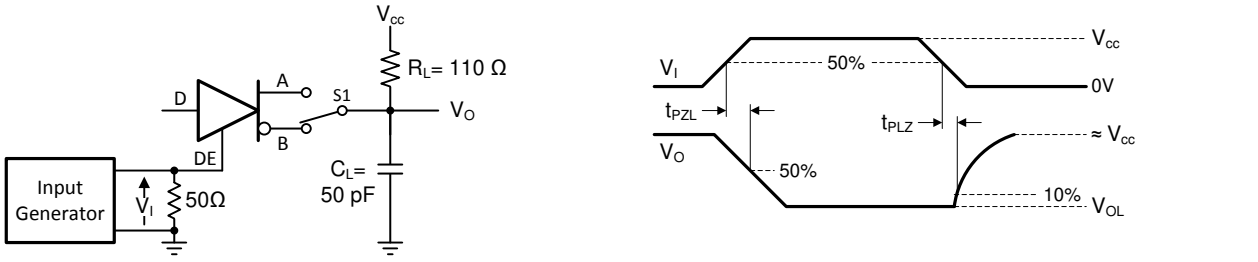


Figure 14. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

Parameter Measurement Information (continued)

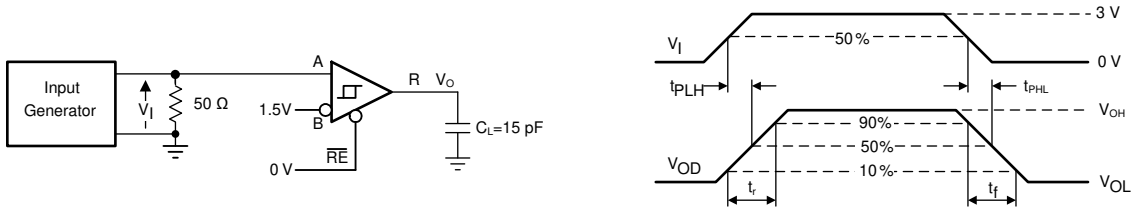


Figure 15. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

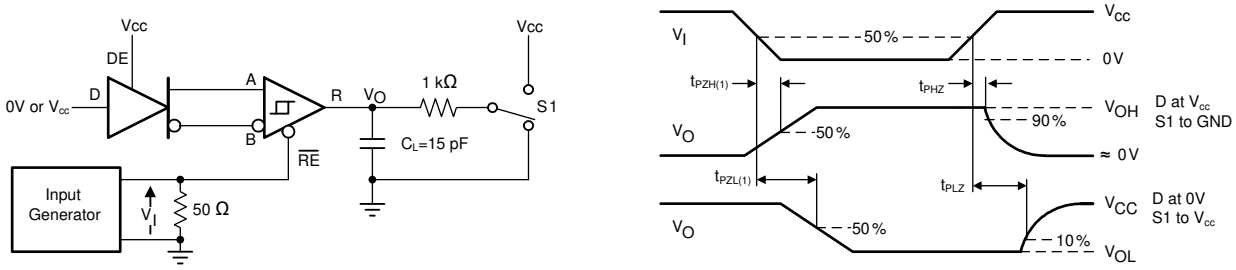


Figure 16. Measurement of Receiver Enable/Disable Times With Driver Enabled

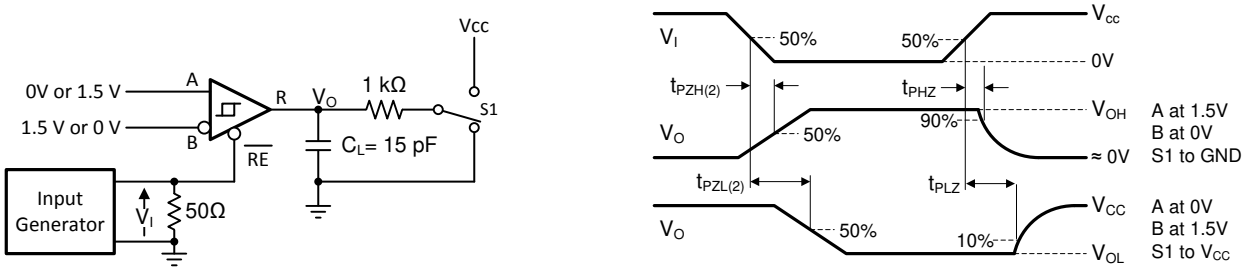


Figure 17. Measurement of Receiver Enable Times With Driver Disabled

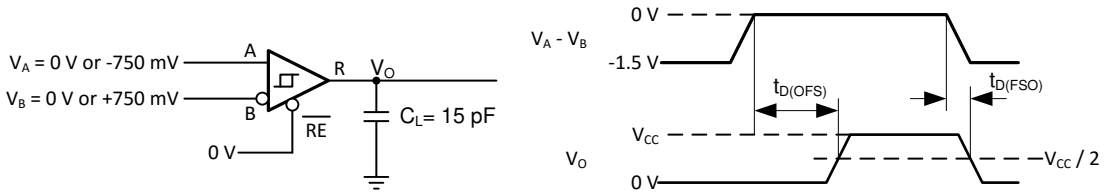


Figure 18. Measurement of Fail-Safe Delay

8 Detailed Description

8.1 Overview

THVD2410 and THVD2450 are fault-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 500 kbps and 50 Mbps respectively. The devices have active-high driver enables and active-low receiver enables. A shutdown current of less than 1 µA can be achieved by disabling both driver and receiver.

8.2 Functional Block Diagrams

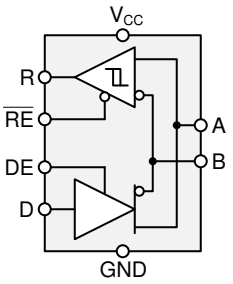


Figure 19. THVD2410 and THVD2450 Block Diagram

8.3 Feature Description

8.3.1 ±70-V Fault Protection

THVD24x0 transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7 V to +12 V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, THVD24x0 devices are protected up to ±70 V without the need for any external components.

8.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV. THVD24x0 ESD structures help to limit voltage excursions and recover from them quickly that they allow EFT Criterion A at the system level (no data loss when transient noise is present).

8.3.3 Driver Overvoltage and Overcurrent Protection

The THVD24x0 drivers are protected against any DC supply shorts in the range of -70 V to +70 V. The devices internally limit the short circuit current to ±250 mA in order to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than ±5 mA if the output fault voltage exceeds |±25 V|.

All devices feature thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation.

8.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD24x0 feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250 mV (typical) hysteresis ensures excellent noise immunity.

Feature Description (continued)

8.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH\_FSH}|$.

8.3.6 Low-Power Shutdown Mode

Driving DE low and $\overline{RE}$ high for longer than 500 ns puts the devices into the shutdown mode. If either DE goes high or $\overline{RE}$ goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50 ns. This feature prevents the devices from accidentally going into shutdown mode due to skew between DE and $\overline{RE}$.

8.4 Device Functional Modes

8.4.1 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

THVD2410 and THVD2450 are fault-protected, half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For these devices, the driver and receiver enable pins allow for the configuration of different operating modes.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

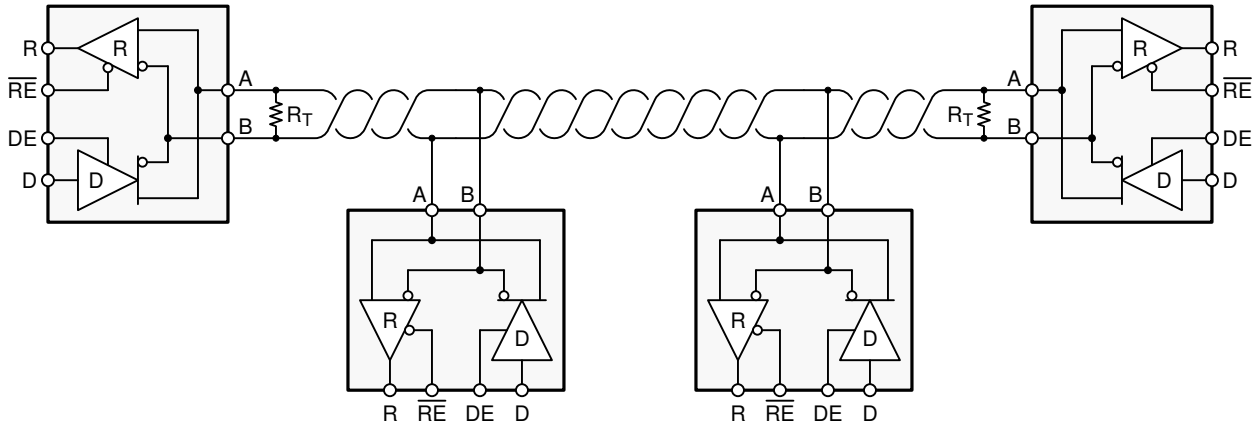


Figure 20. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

Typical Application (continued)

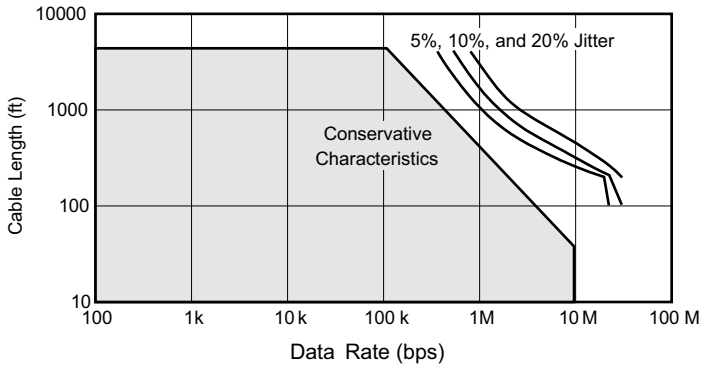


Figure 21. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50 Mbps for the THVD2450) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the THVD24x0 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

Typical Application (continued)

9.2.1.4 Transient Protection

The bus pins of the THVD24x0 transceivers include on-chip ESD protection against ±30-kV HBM and ±12-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

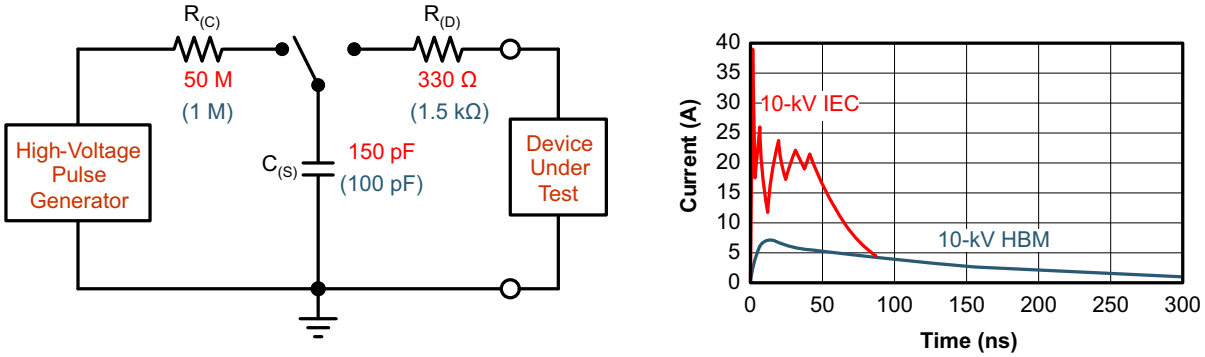


Figure 22. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 23 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

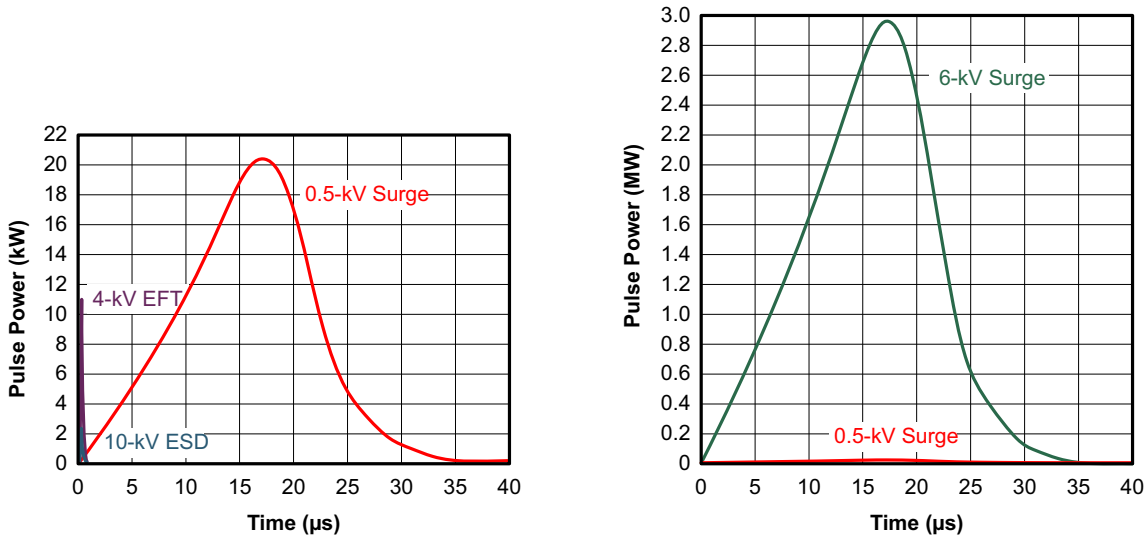


Figure 23. Power Comparison of ESD, EFT, and Surge Transients

Typical Application (continued)

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 24 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

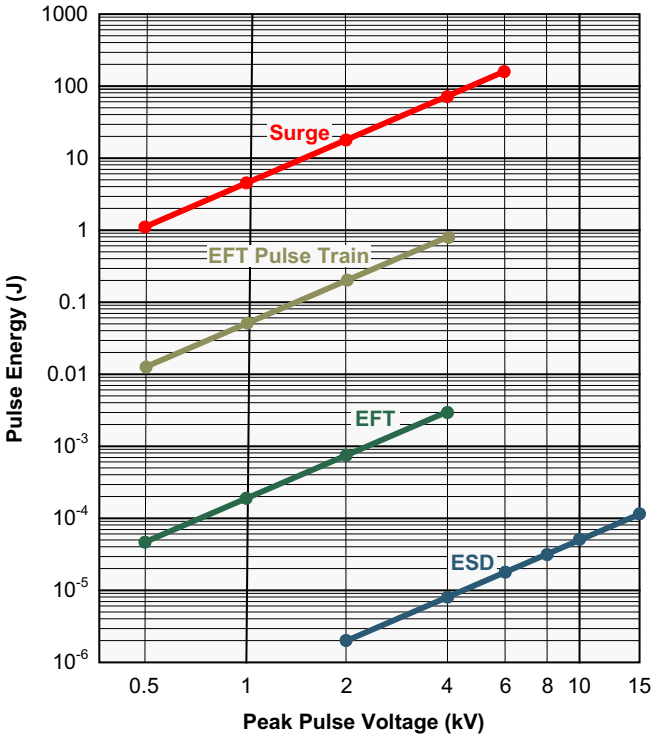


Figure 24. Comparison of Transient Energies

Typical Application (continued)

9.2.2 Detailed Design Procedure

Figure 25 suggests a protection circuit against 1 kV surge (IEC 61000-4-5) transients. Table 3 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30 V. This ensures the protection diodes do not conduct if a direct RS-485 bus shorts to 24-V DC industrial power rail.

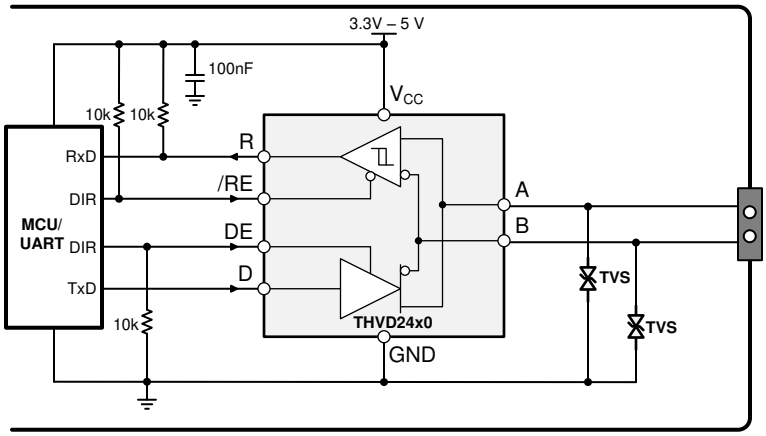


Figure 25. Transient Protection Against Surge Transients for Half-Duplex Devices

Table 3. Components List(1)

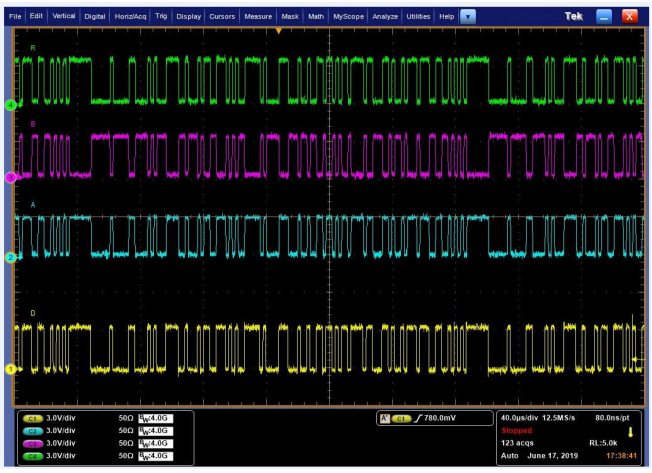
DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 transceiver	THVD24x0	TI
TVS	Bidirectional 400-W transient suppressor	SMAJ30CA	Littelfuse

(1) See Device Support

9.2.3 Application Curves

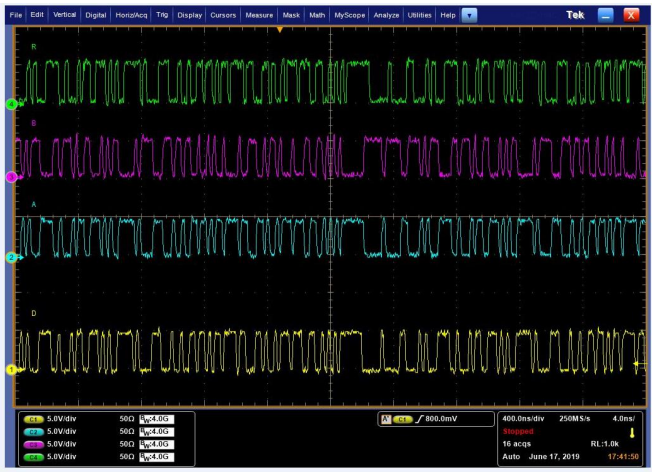
THVD2410 V_{CC} = 5 V R_L = 50 Ω
Random (PRBS7) data at 500 kbps

Figure 26. THVD2410 Waveforms at V_{CC} = 5 V



THVD2410 V_{CC} = 3.3 V R_L = 50 Ω
Random (PRBS7) data at 500 kbps

Figure 27. THVD2410 Waveforms at V_{CC} = 3.3 V



THVD2450 V_{CC} = 5 V R_L = 50 Ω
Random (PRBS7) data at 50 Mbps

Figure 28. THVD2450 Waveforms at V_{CC} = 5 V

THVD2450 V_{CC} = 3.3 V R_L = 50 Ω
Random (PRBS7) data at 50 Mbps

Figure 29. THVD2450 Waveforms at V_{CC} = 3.3 V

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

11.2 Layout Example

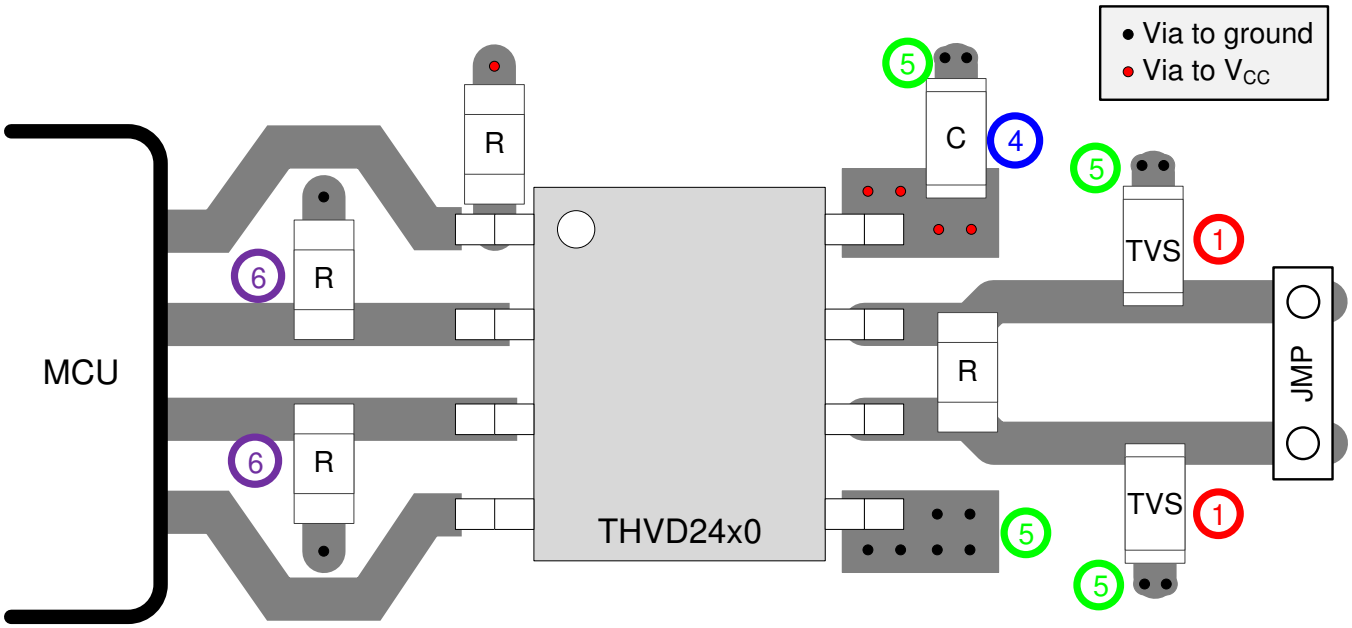


Figure 30. Half-Duplex Layout Example

12 Device and Documentation Support

12.1 Device Support

12.2 Third-Party Products Disclaimer

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12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
THVD2410	Click here	Click here	Click here	Click here	Click here
THVD2450	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document..

12.5 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.6 Trademarks

E2E is a trademark of Texas Instruments.

12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD2410DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2410	Samples
THVD2410DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410	Samples
THVD2410DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2410	Samples
THVD2450DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2450	Samples
THVD2450DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450	Samples
THVD2450DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

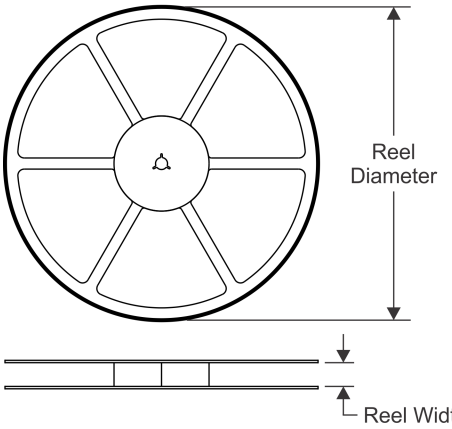
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

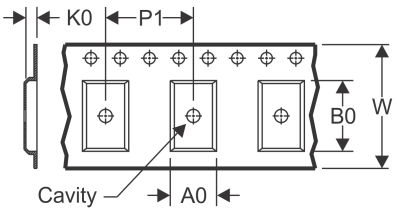
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

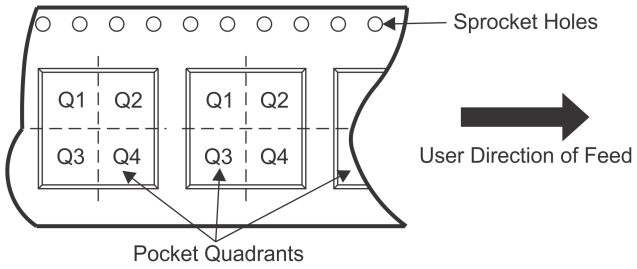


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

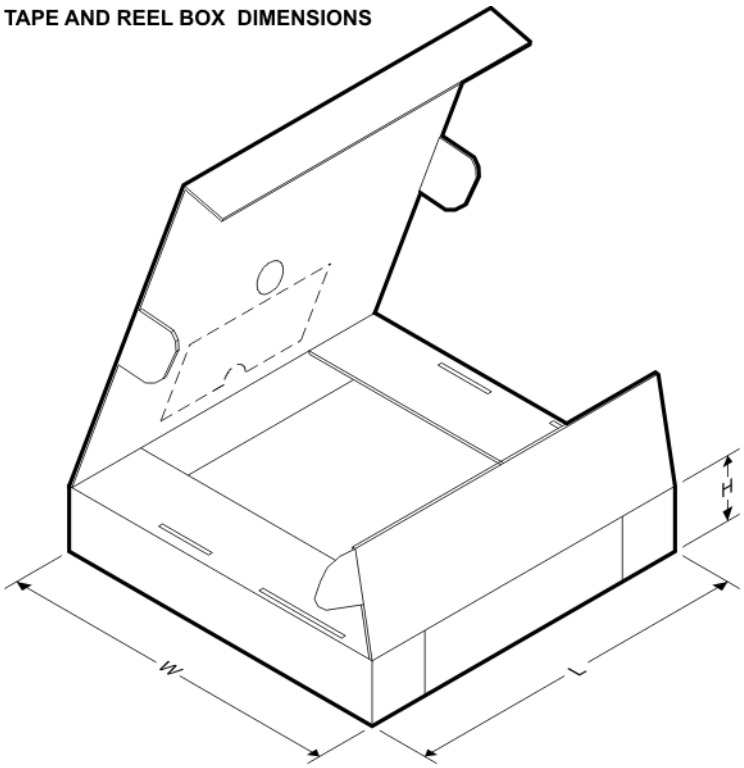
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD2410DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD2410DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD2410DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2450DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THVD2450DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD2450DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD2410DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
THVD2410DR	SOIC	D	8	2500	367.0	367.0	35.0
THVD2410DRBR	SON	DRB	8	3000	367.0	367.0	35.0
THVD2450DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
THVD2450DR	SOIC	D	8	2500	367.0	367.0	35.0
THVD2450DRBR	SON	DRB	8	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

DRB 8

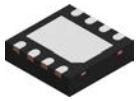
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

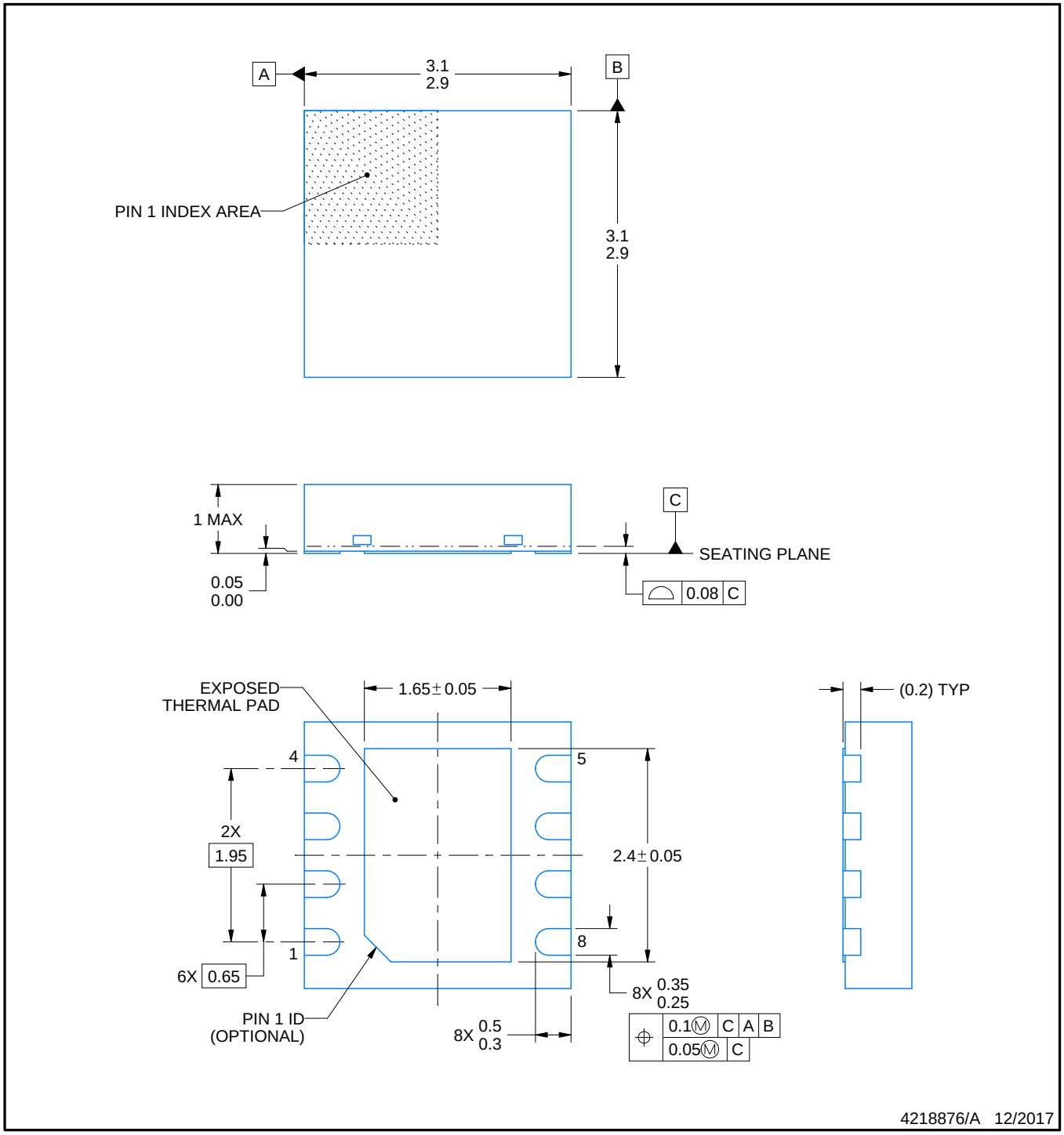
DRB0008B



PACKAGE OUTLINE

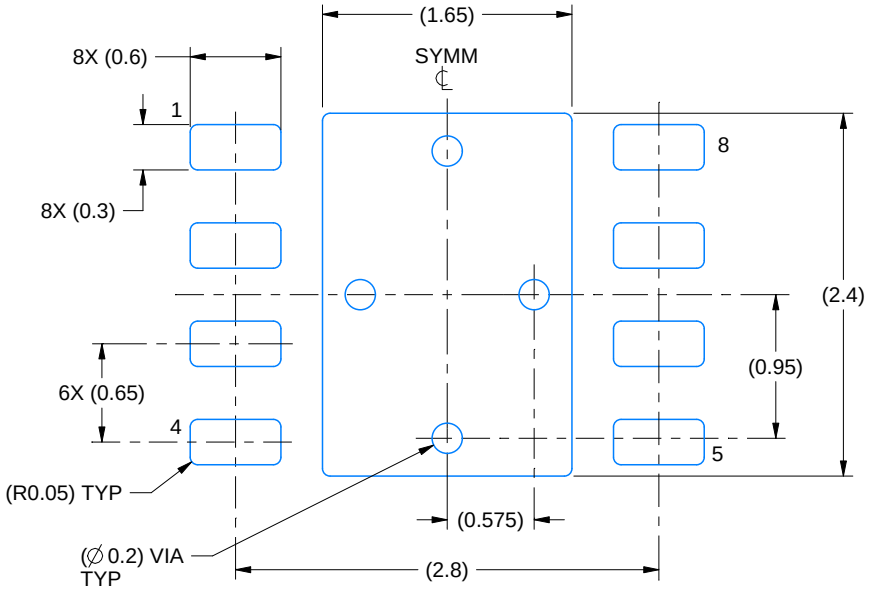
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

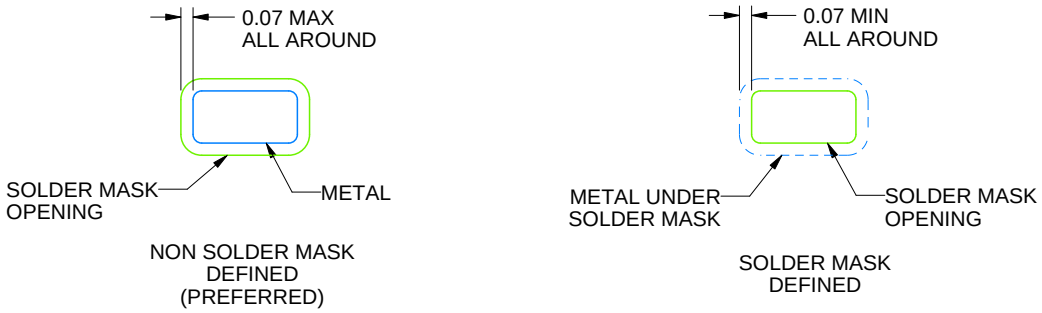


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

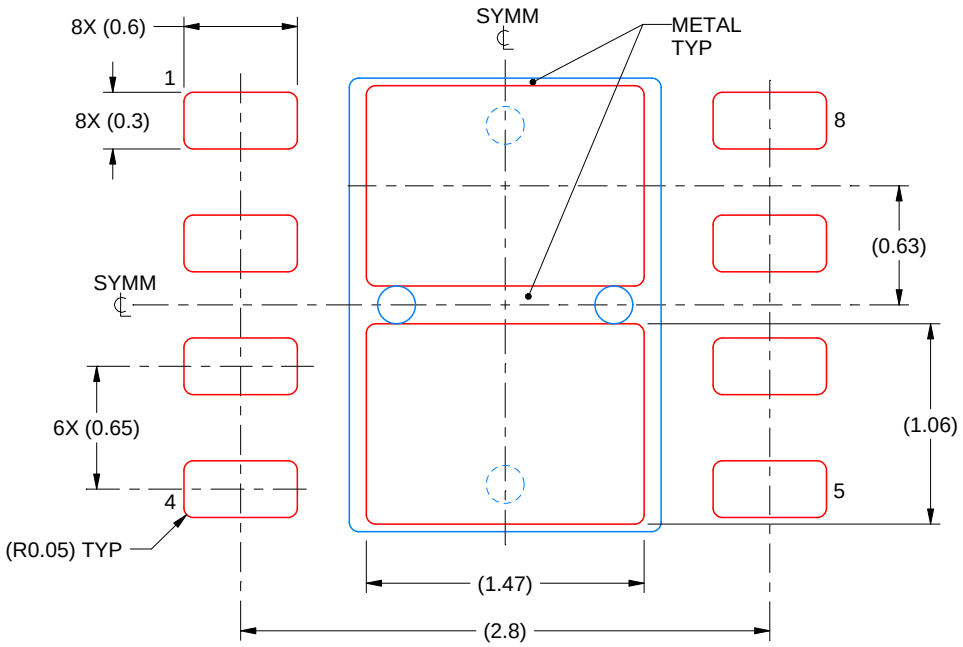


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



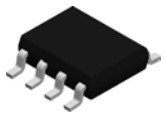
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

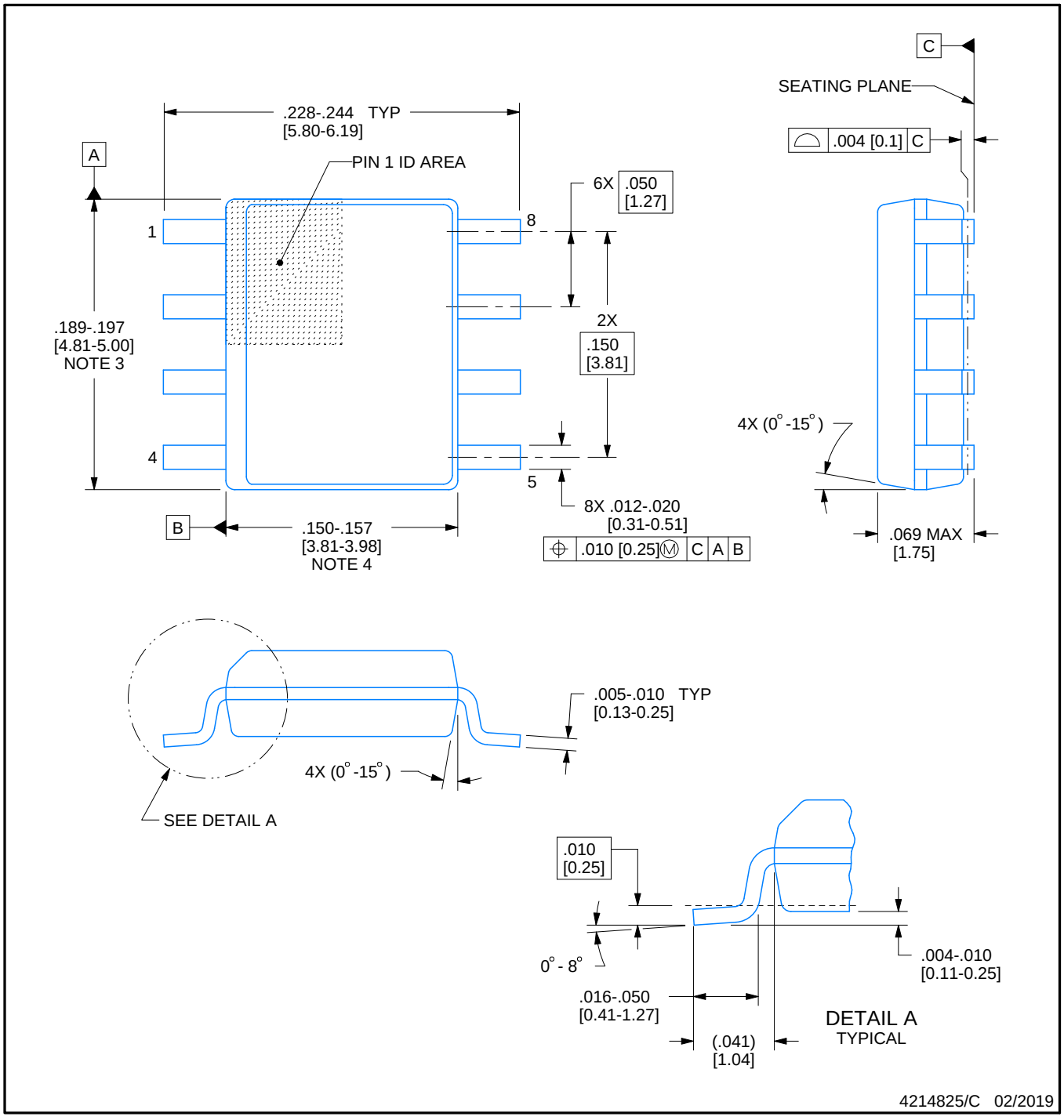


PACKAGE OUTLINE

D0008A

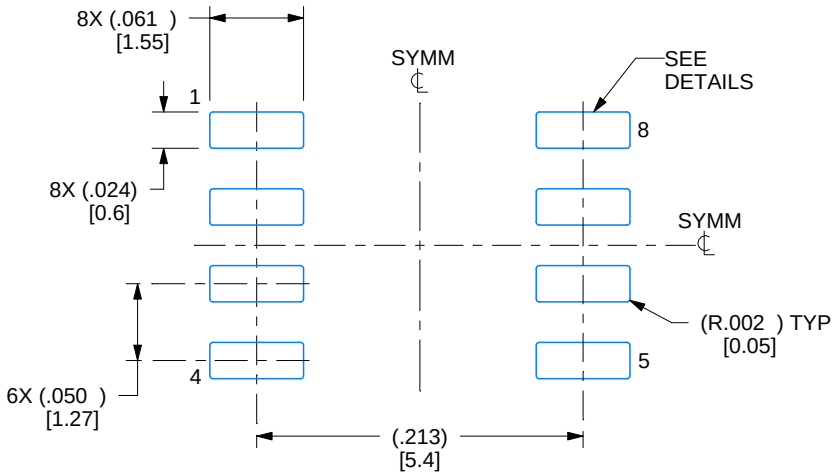
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

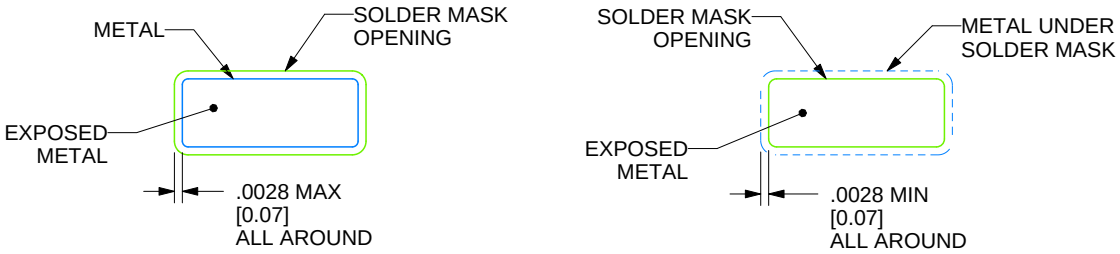


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

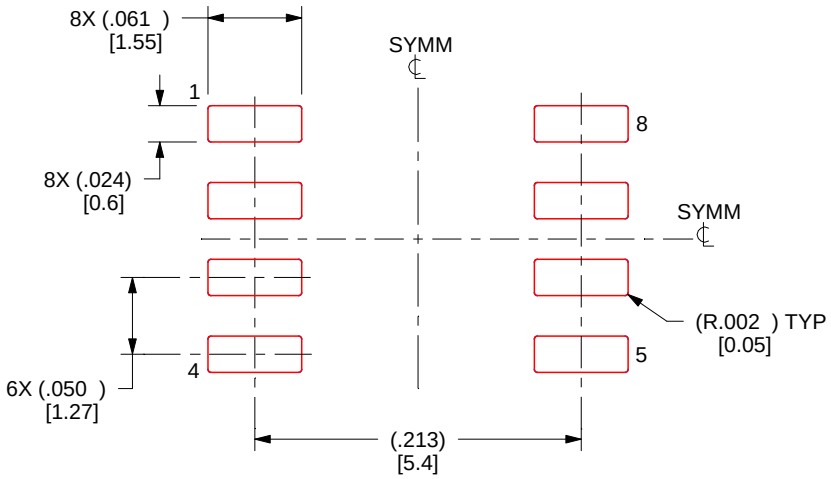
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



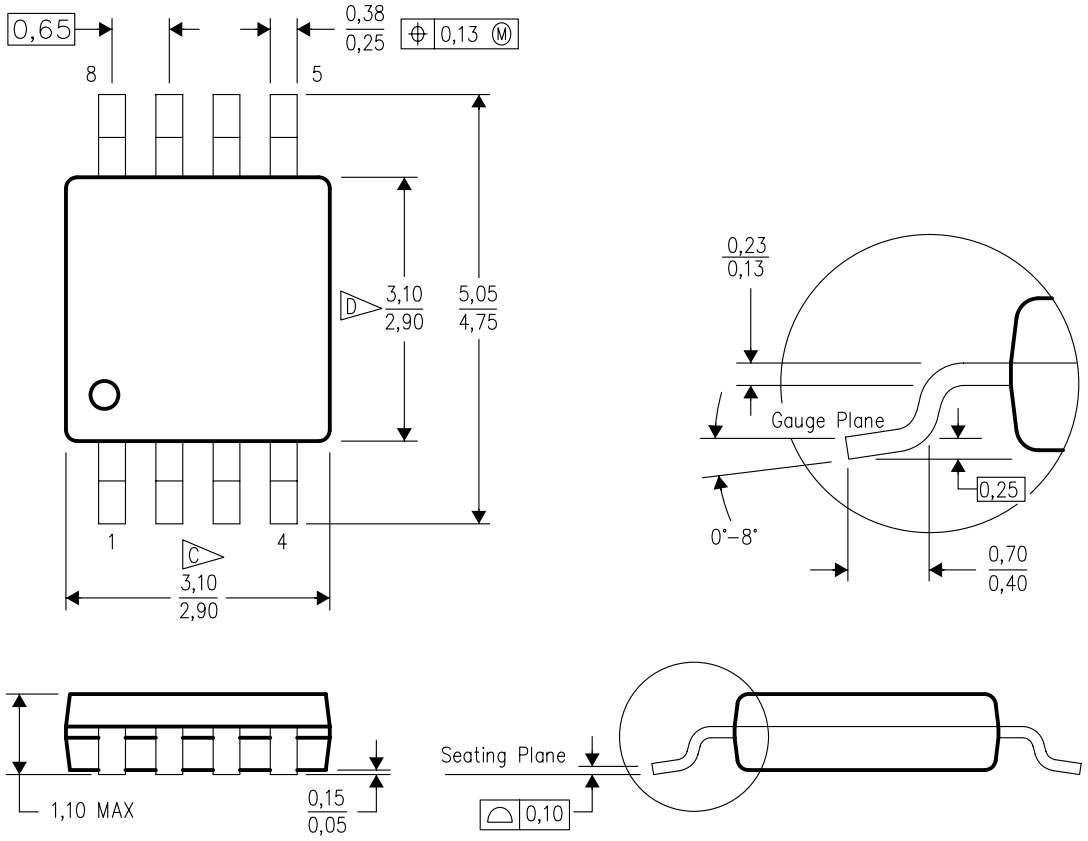
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

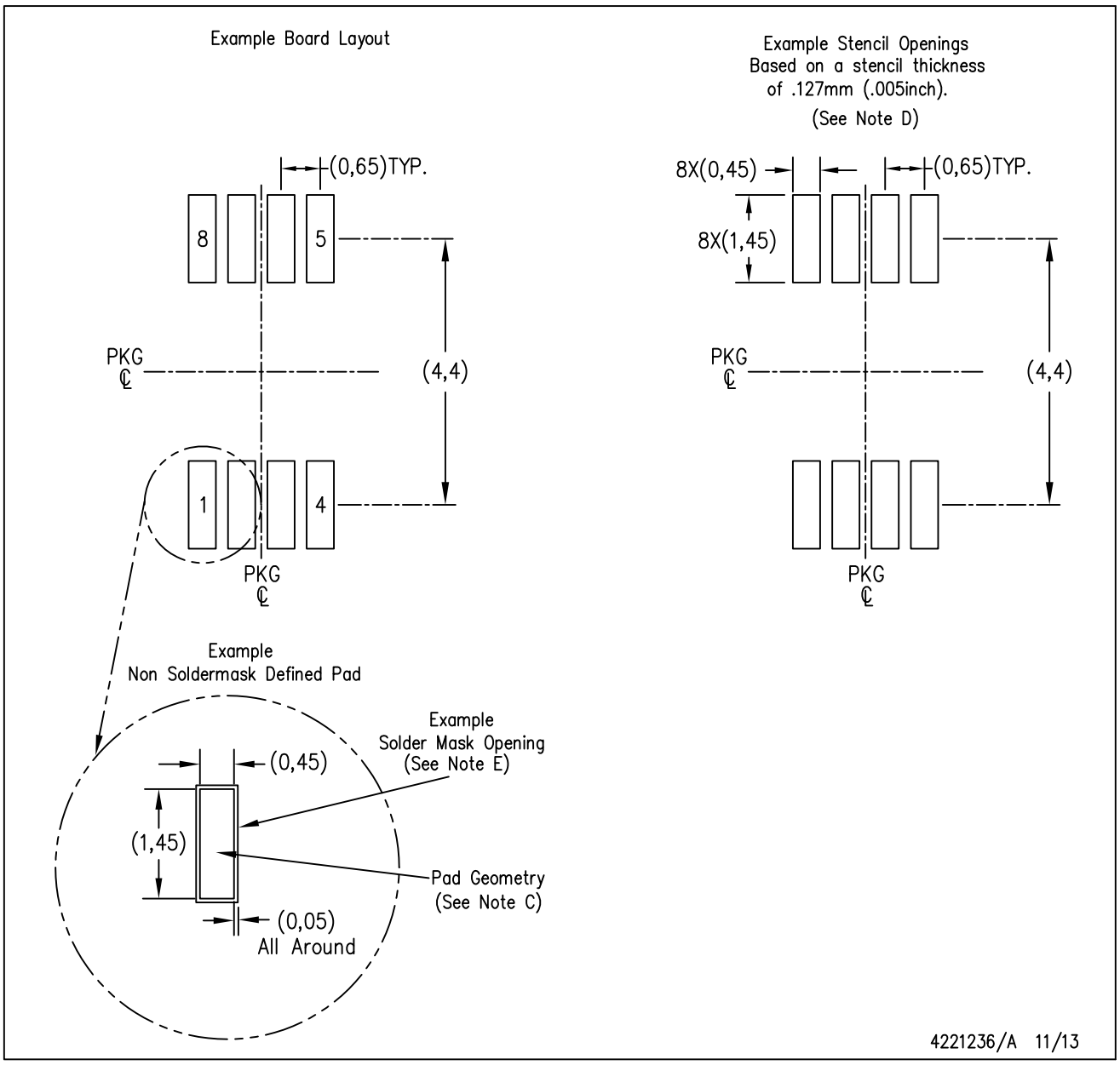
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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