User's Guide
SBOU207–April 2018

THS6301 Evaluation Module

This document provides information about the evaluation module of the amplifier under test. Additionally, this document provides a good example of printed-circuit board (PCB) design for high-speed applications. Remember the following points:

- TI recommends initially reviewing the data sheet of the device under test.
- It is helpful to review the schematic and layout of the THS6301 EVM to determine the design techniques used in the evaluation board.
- Approach the high-speed amplifier PCB design with care. Pay attention to the board parasitic which impacts the overall system performance.

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1 Introduction

The Texas Instruments THS6301 evaluation module (EVM) helps designers evaluate the performance of the THS6301 high-speed, single-port, differential line driver designed for G.fast and legacy xDSL systems available in a 16-pin VQFN package. This document details the THS6301 EVM and is a good starting point for high-speed PCB design involving the THS6301 differential line driver. The document includes a brief description of the module and a list of EVM features, followed by EVM specifications and default EVM configuration, details on connecting and using the EVM, and a discussion of high-speed amplifier PCB design considerations.

1.1 Description

The THS6301 evaluation module (EVM) is used to evaluate the THS6301 device, which is a high-speed, single-port, differential line driver available in a 16-pin VQFN package designed for G.fast and legacy xDSL applications. The EVM is designed to quickly and simply demonstrate the functionality and performance of THS6301 in a fixed gain configuration of 8.5 V/V while driving an equivalent R_{LOAD} = 200 Ω. The EVM is ready to connect to power supplies, signal sources, and test instruments using onboard connectors. The board is set up for differential input and output operation. The EVM requires an external 180° phase-shifted combiner to convert single-ended signals to differential signals for use with standard single-ended 50-Ω laboratory equipment. Two tri-level logic switches on the board facilitate device operation in the various G.fast or DSL modes.

1.2 Evaluation Module Features

The THS6301 high-speed differential line driver EVM features include:

- Configured for single-supply operation only
- Designed for AC-coupled differential 100-Ω input and output connection
- Configured for fixed gain configurations of 8.5 V/V
- Simple interface to the inputs and outputs through SMA connectors
- Two tri-level logic switches (S1 and S2) available to change the device operation in the various G.fast or DSL modes

1.3 THS6301 Operating Conditions

Recommended single-supply voltage of V_{CC} = 12 Vdc (see the device data sheet for minimum and maximum values).

Supply current (I_Q = 37 mA) in G.fast transmit mode with S1 = LO and S2 = HI setting (see the device data sheet for minimum and maximum values).

For complete THS6301 amplifier device specifications, parameter measurement information, and additional application information, see the THS6301 data sheet (SBOS877).

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2 EVM Default Configuration

As delivered, the EVM contains a fully functional example circuit. Provide power supplies, a signal source, and a measuring instrument as s Figure 1 shows. Figure 1 omits some components such as supply bypass capacitors and test points for clarity.

See Figure 2 for the default schematic diagram of the THS6301 EVM.

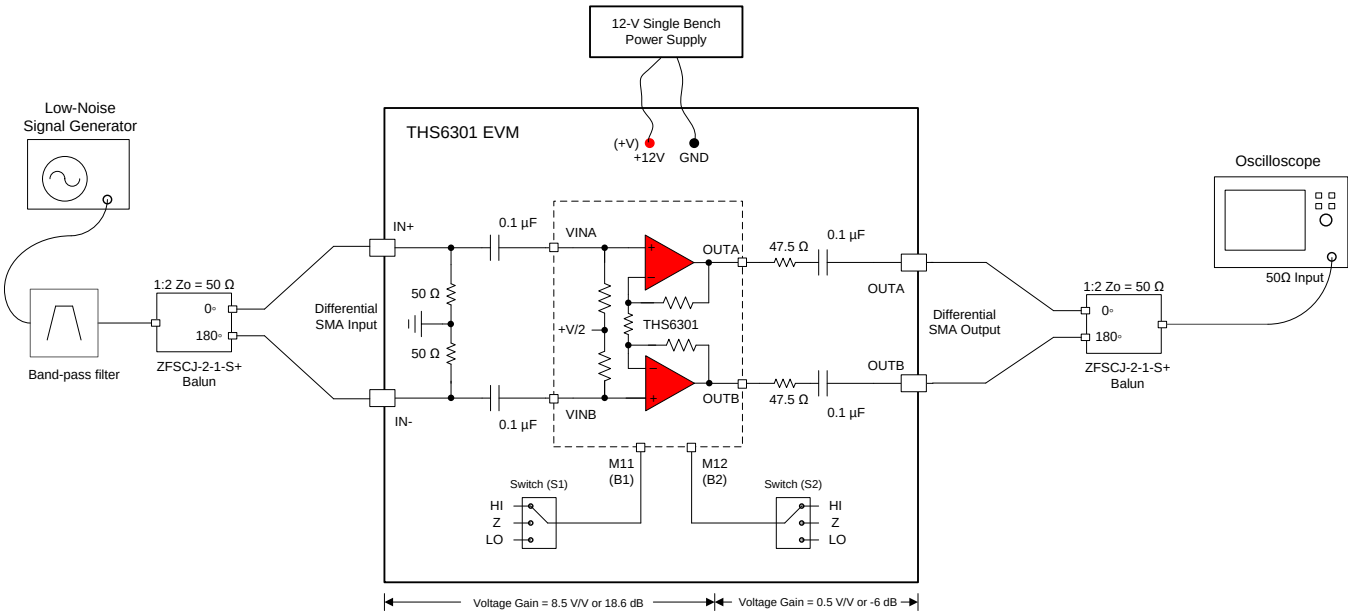


Figure 1. THS6301 EVM Default Configuration Setup Block Diagram

The THS6301 EVM default configuration is a differential input, differential output fixed gain of 8.5 V/V from SMA inputs IN+/- to the THS6301 device output pins as Figure 1 shows. The feedback and gain setting resistors internal to the device set the fixed gain of 8.5 V/V. An external 180° phase-shifted combiner in the input and output is required to convert single-ended signals to differential signals to use with standard single-ended 50-Ω laboratory equipment.

As such, the THS6301 EVM comes with a 50-Ω resistors to GND on the SMA inputs IN+/- for simple interface with differential 100-Ω test equipment. The device inputs are high-impedance and default to the midsupply voltage. On a single 12-V supply, the inputs self bias up to 6V DC voltage. Because the inputs self bias to midsupply, the inputs are AC-coupled with 0.1-µF capacitors to avoid DC current flow from the inputs to the external test equipment, which can result in sub-optimal device operation.

On the EVM, the THS6301 device output is driving an AC-coupled equivalent R_{LOAD} = 200 Ω determined by the output series resistor and the external test equipment as Figure 1 shows. The 47.5-Ω output series resistor interfaces with the external 1:2 balun and results in a voltage loss of approximately 6 dB at the OUTA and OUTB SMA connectors . For high-output signal swings, TI recommends an external 6-dB or 9-dB attenuator at the OUTA and OUTB SMA connectors to protect the measuring instrument from being overdriven by the device output.

The external 1:2 balun exhibits some loss characteristic across frequency provided in the balun datasheet, which attenuates the signal from the signal source or while connecting to the measuring instrument. As a result, the designer must take the voltage loss from the output resistor and the input or output balun into account while measuring the true gain of the THS6301.

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3 Using the THS6301 EVM

This section describes how to connect the THS6301 EVM to the test equipment. TI recommends connecting the EVM as shown in this section to avoid damage to the EVM or the THS6301 installed on the board.

3.1 Required Equipment

The following equipment is required:

- A single DC output power supply (12-V, 100-mA output minimum).
- A DC current meter with resolution to 1 mA and capable of a maximum current which the DC power supply can supply. If available, set the current limit on the DC power supply to 100 mA.

NOTE: Some power supplies incorporate current meters which may be applicable to this test.

- A 50-Ω source impedance signal generator is required. TI recommends using a signal generator that can output at least 100 MHz and a sine wave up to 2 V_{PP}.
- A measuring instrument such as an oscilloscope with a 50-Ω terminated input and 500-MHz minimum bandwidth is recommended. A spectrum analyzer with a 2-GHz input frequency range can be used for linearity tests.
- Two external 1:2 (Z_O = 50 Ω) balun as Figure 1 shows
- External 6-dB or 9-dB attenuator pads as required for high-output signal swings

3.2 Power Supply Setup (see Figure 1)

Use the following procedure for power supply setup:

1. Before connecting the power supply cables to the EVM, set the single DC output power supply to 12 V.
2. Make sure the DC power supply is turned off before proceeding to the next step.
3. Connect the 12-V power supply to the +V of the power supply port on the EVM.
4. Connect the GND on the power supply to the GND port on the EVM.
5. Make sure the DC current meters on the DC output power supply are set to at least 1-mA resolution and 100-mA minimum output current capability.
6. Set the DC power supply to 12 V.
7. Depending on the bias mode for the device set by S1 and S2, the supply current from the EVM should match Table 1.

Table 1. Bias Modes Truth Table

BIAS CONTROL SWITCHES		BIAS MODE DESCRIPTION	TYPICAL QUIESCENT CURRENT (mA)
SWITCH (S1) STATE	SWITCH (S2) STATE		
LO	LO	Receive mode (High power)	16
Z	LO	Receive mode (Low power)	10
HI	LO	G.fast 212 MHz	46
LO	Z	ADSL2+	16
Z	Z	Power down	2
HI	Z	Alternate VDSL (High power)	30
LO	HI	Alternate G.fast 106 MHz	40
Z	HI	VDSL	21
HI	HI	G.fast 106 MHz (Low power)	28

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3.3 Input and Output Test Setup (see Figure 1)

- The THS6301 evaluation board provides the customer flexibility in testing at different input frequencies using external input and output baluns as Figure 1 shows. Figure 1 provides a test balun example.
- For high-output signal swings, TI recommends using external 6-dB or 9-dB attenuator pads at the OUTA and OUTB SMA connectors to protect the measuring instrument from overdrive by the device output.

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4 High-Speed Amplifier PCB Layout Tips

The THS6301 EVM layout (designed for use with high-speed signals) can be used as an example when designing PCBs incorporating the THS6301. Pay careful attention to component selection, grounding, power supply bypassing, and signal path layout. Disregarding these basic design considerations can result in sub-optimal performance of the THS6301 high-speed differential line driver. Select surface-mount capacitors because of the low lead inductance associated with this technology. This minimizes stray inductance and capacitance. Because surface-mount components are physically small, the layout is compact.

A large power supply bypass capacitor with a value of 10 µF at the power input pads help filter switching transients from the laboratory power supply. Power supply bypass capacitors are placed as close to the device power input pins as possible to minimize the return path impedance. This improves high-frequency bypassing and reduces harmonic distortion. The GND side of these capacitors must be close to each other, which minimizes the differential current loops associated with differential output currents. If poor high-frequency performance is observed, replace the 0.1-µF capacitors with microwave capacitors with a self-resonance at the frequency that produces trouble. A proper ground plane on both sides of the PCB must be used with high-speed circuit design. This provides low-inductive ground connections for return current paths. In the area of the amplifier differential input and output pins, remove the ground plane to minimize stray capacitance and reduce ground plane noise coupling into these pins.

In general, keep signal lines as short and straight as possible. TI recommends incorporating microstrip or stripline techniques if signal lines are longer than one inch. These traces must be designed with a characteristic impedance of 50 Ω or 75 Ω as required by the application. Properly terminate this type of signal line with an appropriate resistor.

The PCB used with VQFN thermal pad packages must have features included in the design to remove heat from the package efficiently. At a minimum, there must be an area of solder-tinned copper underneath the thermal pad package. This area is known as the thermal land. The thermal land varies in size depending on which thermal pad is used, the PCB construction, and the amount of heat that must be removed. This thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are shown in *Quad Flatpack No Lead Logic Packages*

Finally, all inputs and outputs must be properly terminated in the layout or in the load instrumentation. Unterminated lines (such as a coaxial cable) can appear as a reactive load to the amplifier. By terminating a transmission line with the characteristic impedance, the load of the amplifier then is purely resistive, and reflections are absorbed at each end of the line. An advantage of using an output termination resistor is that capacitive loads are isolated from the output of the amplifier. This isolation helps minimize the reduction in the phase-margin of the amplifier and improves the amplifier stability, which results in reduced peaking and settling times.

On boards operated from dual power supplies, placing a capacitor directly across the positive and negative power supplies is helpful. This helps the fully differential drive.

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5 EVM Hardware Description

This section describes the EVM hardware and includes the EVM parts list and PCB layout.

5.1 Bill of Materials

Table 2 lists the EVM bill of materials.

Table 2. THS6301 EVM Bill of Materials

Item #	Designator	Qty	Value	Part Number	Manufacturer	Description	Package Reference
1	!PCB1	1		AMPS031	Any	Printed Circuit Board	
2	C1	1	10uF	C1206C106K3RACTU	Kemet	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206_190	1206_190
3	C2, C5, C6, C7, C8	5	0.1uF	C0603C104J3RAC	Kemet	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603
4	C3	1	1000pF	C0402C102J3RACTU	Kemet	CAP, CERM, 1000 pF, 25 V, +/- 5%, X7R, 0402	0402
5	C12	1	100pF	C0402C101J3GACTU	Kemet	CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0402	0402
6	H1, H2, H3, H4	4		NY PMS 440 0025 PH	B&F Fastener Supply	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw
7	H5, H6, H7, H8	4		1902C	Keystone	Standoff, Hex, 0.5"L #4-40 Nylon	Standoff
8	J1	1		1715721	Phoenix Contact	Terminal Block, 5.08 mm, 2x1, TH	2POS Terminal Block
9	J2, J3, J5, J6	4		142-0701-851	Cinch Connectivity	Connector, End launch SMA, 50 ohm, SMT	SMA End Launch
10	LBL1	1		THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch
11	R1, R9	2	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603	0603
12	R2, R8	2	49.9	ERJ-3EKF49R9V	Panasonic	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
13	R3, R6	2	47.5	CRCW060347R5FKEA	Vishay-Dale	RES, 47.5, 1%, 0.1 W, 0603	0603
14	R7	1	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
15	R10	1	75.0k	CRCW060375K0FKEA	Vishay-Dale	RES, 75.0 k, 1%, 0.1 W, 0603	0603
16	R13, R14	2	20.0k	RC0603FR-0720KL	Yageo America	RES, 20.0 k, 1%, 0.1 W, 0603	0603
17	S1, S2	2		AS13AP	NKK Switches	Switch, SPDT, On-Off-On, 0.4 A, 28 VDC, TH	9.8x5.38mm
18	TP1	1		5006	Keystone	Test Point, Compact, Black, TH	Black Compact Testpoint
19	U1	1		THS6301IRSA	Texas Instruments	THS6301IRSA, RSA0016B (VQFN-16)	RSA0016B
20	C4, C9, C10, C11, C13	0	0.1uF	C0603C104J3RAC	Kemet	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603
21	FID1, FID2, FID3, FID4, FID5, FID6	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A
22	J4, J7, J8, J9	0		142-0701-851	Cinch Connectivity	Connector, End launch SMA, 50 ohm, SMT	SMA End Launch
23	J10, J11	0		TSW-102-07-G-S	Samtec	Header, 100mil, 2x1, Gold, TH	2x1 Header
24	R4	0	100	RMCF0402JT100R	Stackpole Electronics Inc	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
25	R5, R15	0	100	CRCW0603100RFKEA	Vishay-Dale	RES, 100, 1%, 0.1 W, 0603	0603
26	R11, R12	0	49.9	CRCW060349R9FKEA	Vishay-Dale	RES, 49.9, 1%, 0.1 W, 0603	0603
27	T1, T2	0		ADT1-1WT+	Minicircuits	RF Transformer, 75 ohm, 0.4 to 800 MHz, SMT	CD542

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5.2 Schematic

Figure 2 illustrates the EVM schematic.

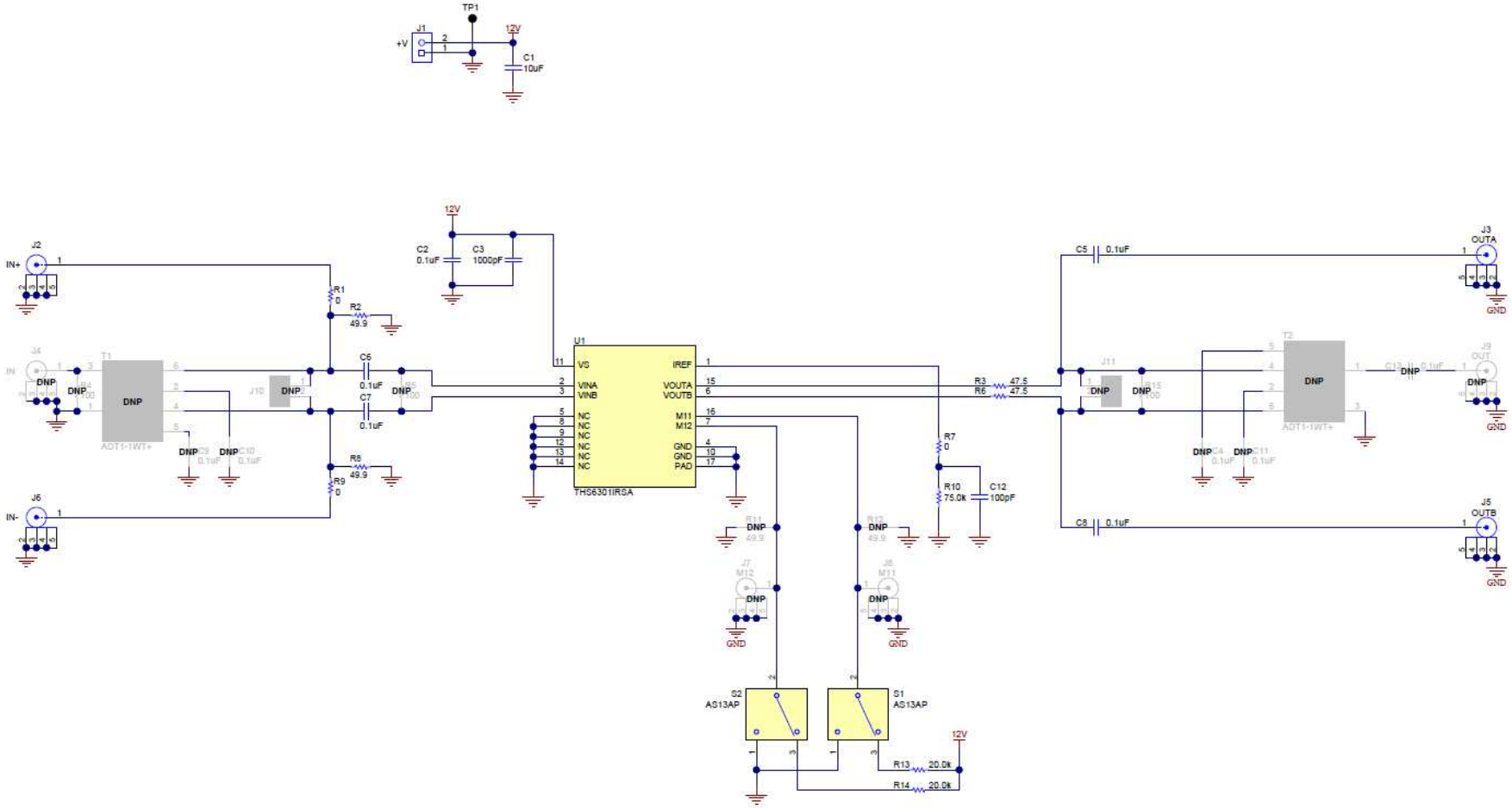


Figure 2. Full Schematic of the THS6301 EVM

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5.3 Circuit Board Layout

Figure 3 through Figure 6 illustrate the EVM PCB layout.

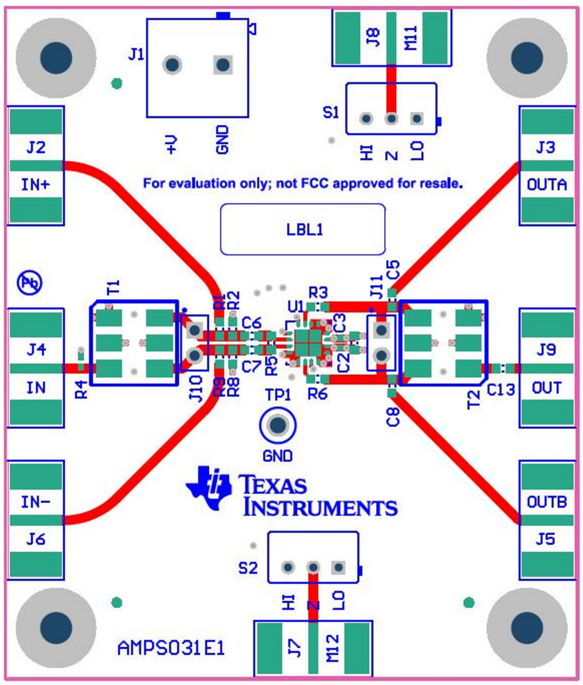


Figure 3. Top Components and Silkscreen Layer

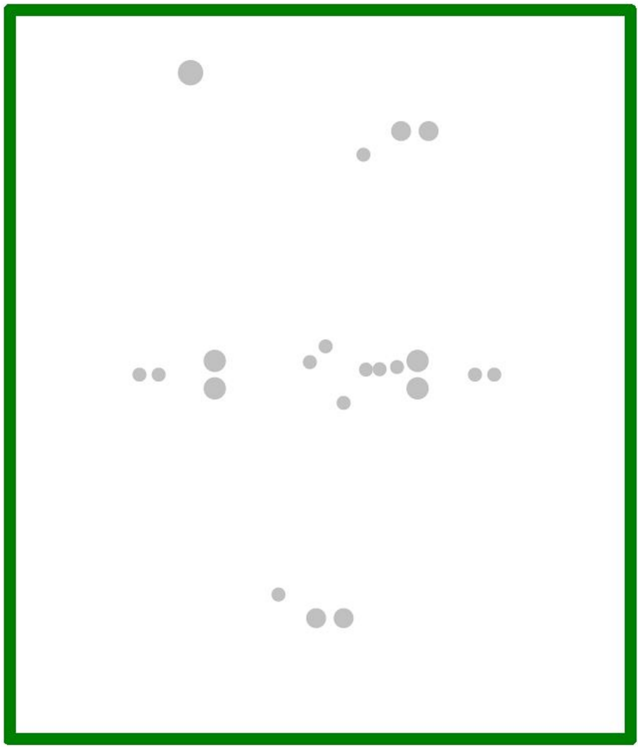


Figure 4. Layer 2 - GND

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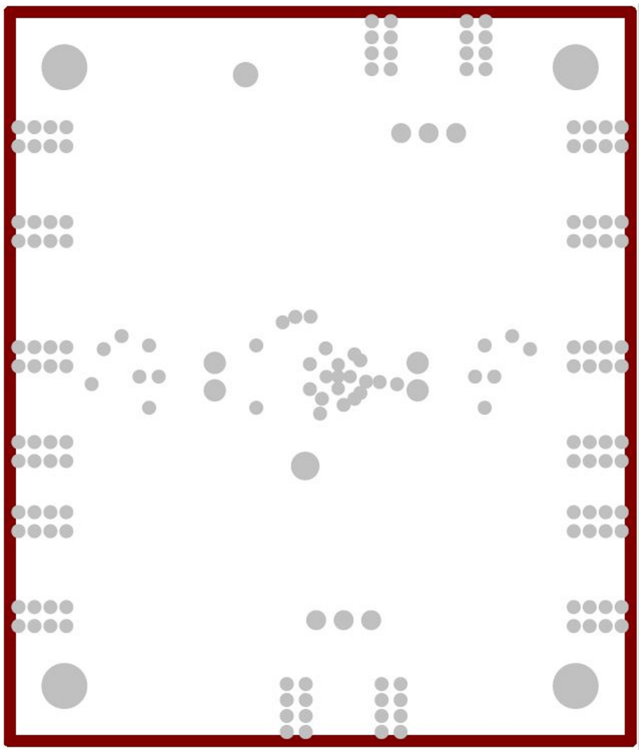


Figure 5. Layer 3 - Power

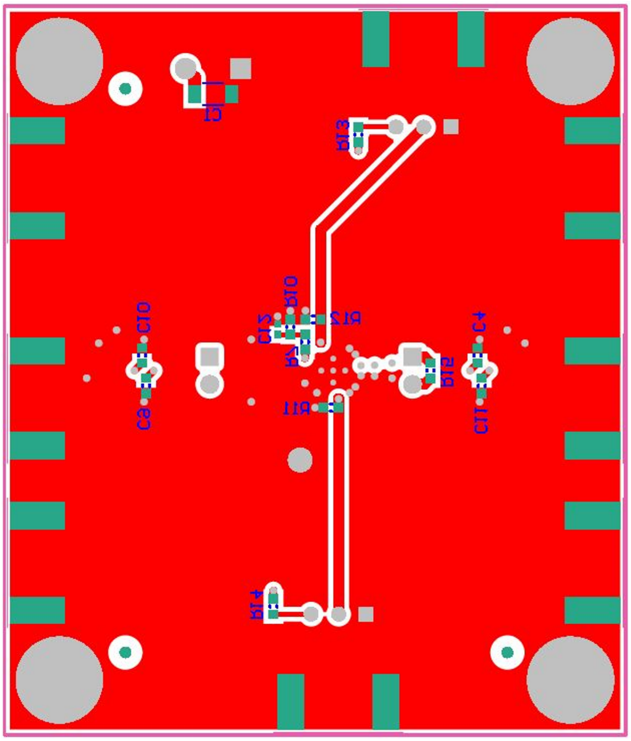


Figure 6. Bottom Components and Silkscreen Layer

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