TEXAS INSTRUMENTS

THS3062EVM

User's Guide

September 2002 *High Performance Linear Products*

SLOU146

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM user's guide. The input supply voltage must not exceed ±15 V for dual supply or 30 V for single supply. The differential input signal must not exceed ±3 V. The output current must not exceed 150 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than xxx°C. The EVM is designed to operate properly with certain components above xxx°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated

Read This First

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1—Introduction and Description
- ❏ Chapter 2—Using The THS3062EVM
- ❏ Chapter 3—THS3062EVM Applications
- ❏ Chapter 4—EVM Hardware Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.



This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

Related Documentation From Texas Instruments

The URL's below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS3062 data sheet (SLOS394)
- Application report (SLOA069), *How (Not) to Decouple High Speed Op Amp Circuits,* http://www-s.ti.com/sc/psheets/sloa069/sloa069.pdf
- Application report (SLMA002), *PowerPAD Thermally Enhanced Package*, http://www-s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report (SLMA004), PowerPAD Made Easy, http://www-s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report (SSYA008), Electrostatic Discharge (ESD), http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf
- High-Speed Amplifier PCB Layout Tips, http://www-s.ti.com/sc/psheets/sloa102/sloa102.pdf

Trademarks

PowerPAD is a trademark of Texas Instruments.

Contents

1 Introduction and Description 1-1
1.1 Evaluation Schematic 1-1

2 Using the THS3062EVM 2-1

3 THS3062EVM Applications 3-1
3.1 Inverting Gain Stage 3-1
3.2 Noninverting Gain Stage 3-2
3.3 Applications for EVM Channel 2 3-2

4 EVM Hardware Description 4-1

Figures

1-1 Schematic of the THS3062EVM 1-3
2-1 THS3062EVM Interconnection Diagram 2-1
3-1 Inverting Gain Stage 3-1
3-2 Noninverting Gain Stage 3-2
4-1 Top Layer 1 (Signals and Silkscreen) for THS3062EVM 4-2
4-2 Internal Plane (Layer 2) Ground Plane 4-2
4-3 Internal Plane (Layer 3) Power Layer 4-3
4-4 Bottom (Layer 4) Ground and Signal 4-3

Tables

4-1 THS3062EVM Bill of Materials 4-1

Chapter 1

Introduction and Description

This chapter provides a description of the THS3062EVM dual high-speed operational amplifier along with a schematic diagram.

1.1 Evaluation Schematic

As delivered, the EVM has a fully functional example circuit, requiring added power supplies, a signal source, and a monitoring instrument. The default schematic diagram is provided in Figure 1-1. The user can change the gain by changing the ratios of the feedback and gain resistors (see the device data sheet for recommended resistor values). The complete EVM schematic—showing all components—is shown in this chapter.

EVM Channel 1:

The default configuration for EVM channel 1 is designed to provide a voltage gain of -1 and a gain of about +2 depending on which input is connected to the signal source. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 1) to the voltage at the input at J2 or J3 respectively.

For optimum frequency response and stability at either -1 or +2 gain, a feedback resistor, R6 (562 Ω), is chosen. R1 is set to the same value to provide a gain in the inverting configuration of -1. To match the signal generator, source impedance R2 was set to 54.9 Ω. This is the closest value when placed in parallel with R3 (562 Ω) that terminates the inverting input to 50 Ω. R4 is set to 953 Ω because when a high impedance instrument is connected to the output connector, J1, the amplifier is loaded at about 1 kΩ.

When EVM channel 1 is used as an inverting amplifier in the default configuration connected to a 50-Ω input device, R4 causes a slight gain error. The total voltage gain is the negative ratio of the feedback resistor, R6, and the gain resistor, R3, times the voltage divider created by R5, R4 and the measurement device input termination resistance. This gain follows the following equation:

$$\frac{V_O}{V_I} = -\frac{R6}{R1}\left(\frac{R4 \parallel 50\ \Omega}{R4 \parallel 50\ \Omega + R5}\right) = -0.475 \quad (1)$$

The noninverting gain of the EVM channel 1 amplifier, when using the default configuration, is affected by the same slight gain error plus the gain error imposed by the inverting input termination resistor, R2. The following equation shows the gain for this situation:

$$\frac{V_O}{V_I} = \left(1 + \frac{R6}{R1 + R2}\right)\left(\frac{R4 \parallel 50\ \Omega}{R4 \parallel 50\ \Omega + R5}\right) = 0.908 \qquad (2)$$

EVM Channel 2:

The default configuration for EVM channel 2 provides for a voltage gain of +1. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 7) to the voltage at the input at J5. For optimum frequency response and stability at a gain of +1 the feedback resistor, R7, of 750 Ω was chosen.

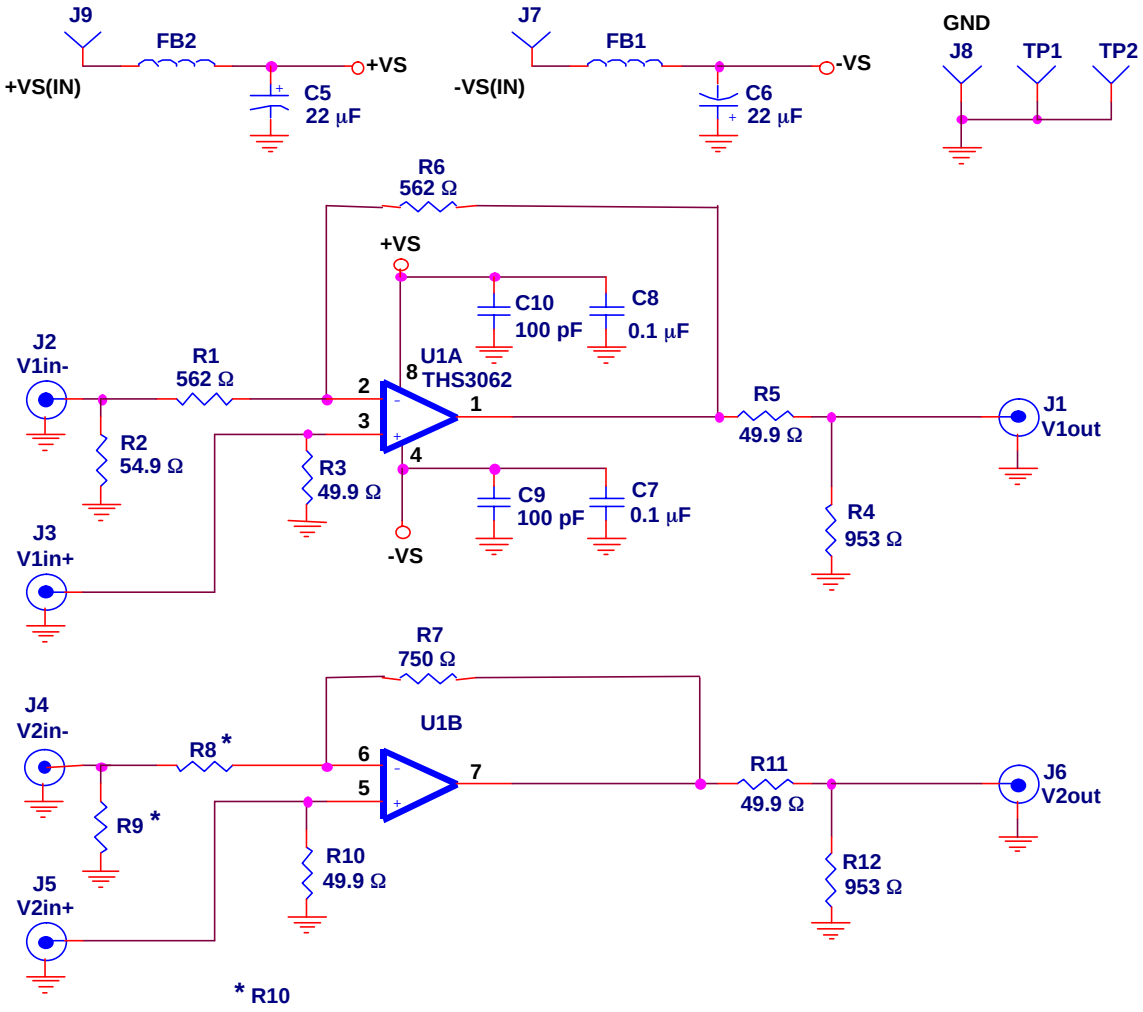
The noninverting gain of the EVM channel 2 amplifier, when using the default configuration, is affected by the same slight gain error caused by R12 as shown in Equation 1 and indicated in the following equation:

$$\frac{V_O}{V_I} = \left(\frac{-R12 \parallel 50\ \Omega}{R12 \parallel 50\ \Omega + R11}\right) = -0.475 \qquad (3)$$

THS3062 dual high-speed operational amplifier EVM features include:

- Wide operating supply voltage range: dual supply ±5 Vdc to dual supply ±15 Vdc operation (see the device data sheet). Single supply operation is obtained by connecting both J6 (GND) and J7 (VS-) to ground.
- Convenient GND test point (TP1).
- Power supply ripple rejection provided by inductors FB1 and FB2 followed by tantalum capacitors C5 and C6.
- Decoupling capacitors, C7and C8, populated with 0.1 µF and capacitors, C9 and C10, populated with 100 pF—design final decoupling in accordance with SLOA069.
- Nominal 50-Ω input impedance for each of the configured inputs, V1in-, V1in+ and V2in+. Termination can be configured according to the application requirement.
- A good example of high-speed amplifier PCB design and layout. Also see High-Speed Amplifier PCB Layout Tips, SLOA102.
- 50-Ω series matching resistors (R5 and R11).
- 953-Ω resistor to ground provide minimum load through 1 kΩ on each amplifier.
- PowerPAD heatsinking capability.

Figure 1-1. Schematic of the THS3062EVM



Chapter 2

Using the THS3062EVM

This chapter shows how to connect the THS3062EVM to test equipment. It is recommended that the user connect the EVM as described in this chapter to avoid damage to the EVM or the THS3062 installed on the board. Figure 2.1 shows how to connect power supplies, a 50-Ω signal source, and a 50-Ω monitoring instrument.

Figure 2-1. THS3062EVM Interconnection Diagram

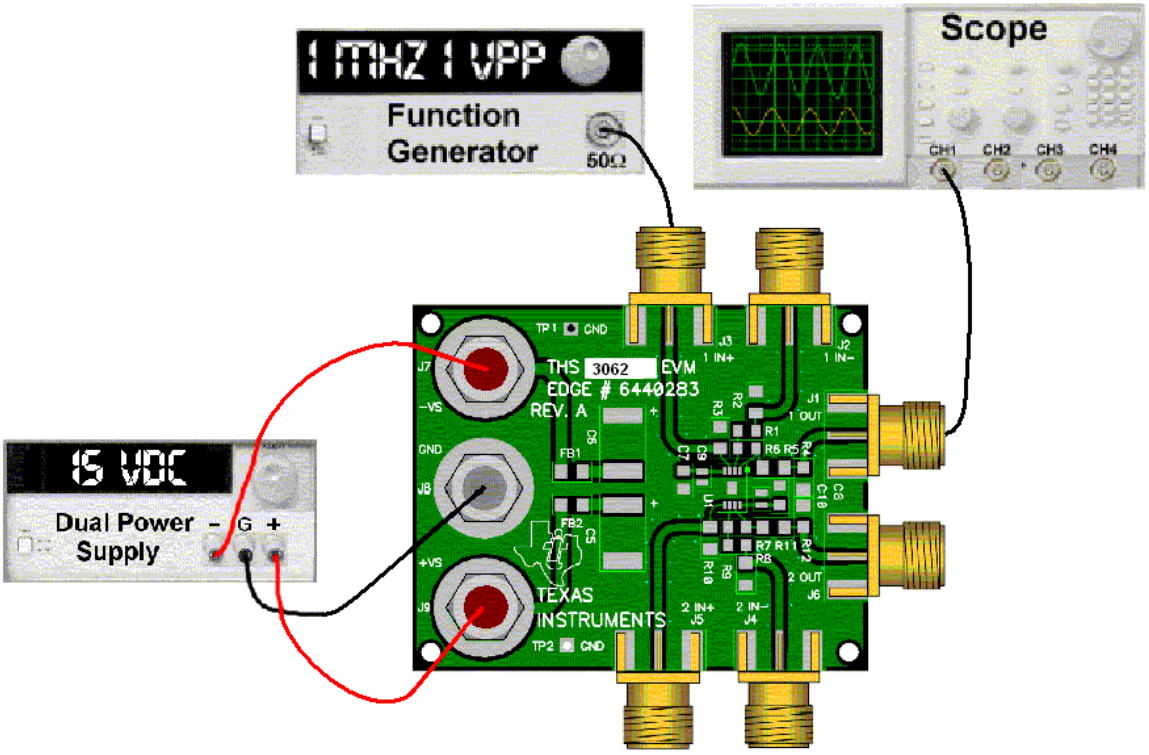


Figure 2-1 shows the connections to measure the output of output 1 while a signal is inserted into EVM channel 1's noninverting input. The signal source can instead be connected to J2 for an inverting signal path. If the oscilloscope input is connected to J6 and the signal source is connected to J5, EVM channel 2 is also configured for a noninverting signal path.

Chapter 3

THS3062EVM Applications

Example applications are presented in this chapter. These applications demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques.

3.1 Inverting Gain Stage

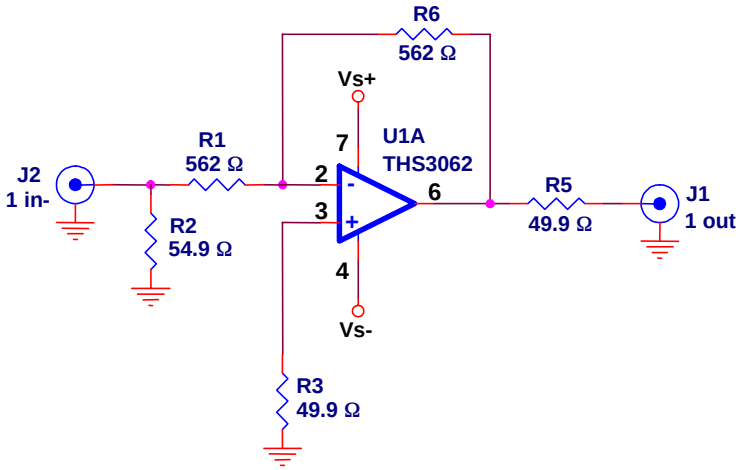
The circuit described in chapter 2 is an inverting gain stage with a voltage divider on the output. Equation 1 indicates the gain when connected to a 50-Ω measurement input device. R4, 953 Ω, was included to provide a 1-k load to the amplifier, the user may remove it as shown in Figure 3-1. When this is done the voltage gain equation from J2 to J1 is simplified as shown in the following equation:

$$\frac{V_O}{V_I} = -\frac{R6}{R1}\left(\frac{50\ \Omega}{50\ \Omega + R5}\right) = -0.5 \qquad (4)$$

R5 is used to match the output impedance of the amplifier to the line being driven and the instrument taking measurements. For short transmission line length, R5 can be replaced with a jumper.

R5 can also be used to isolate the amplifier from extremely large capacitive loads.

Figure 3-1. Inverting Gain Stage

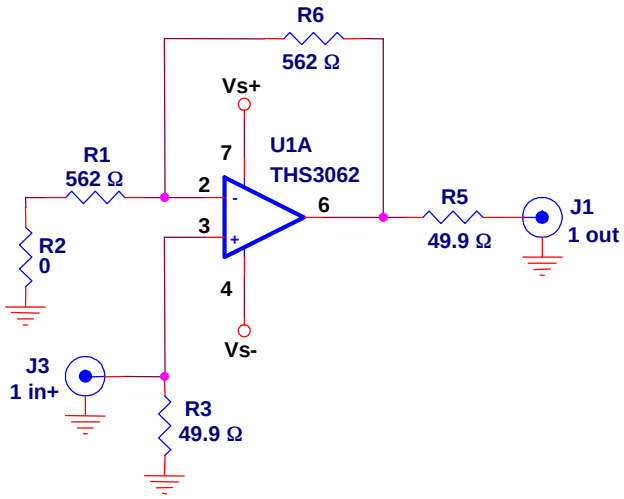


3.2 Noninverting Gain Stage

For a noninverting stage in EVM channel 1, the EVM can be modified to eliminate the gain error imposed by R2 by replacing R2 with a 0-Ω resistor. This is shown in Figure 3-2. R4 has been removed as shown in the inverting gain stage example above. The following equation indicates the voltage gain from J3 to J1:

$$\frac{V_O}{V_I} = \left(1 + \frac{R6}{R1}\right)\left(\frac{50\ \Omega}{50\ \Omega + R5}\right) = 1 \qquad (5)$$

Figure 3-2. Noninverting Gain Stage



This is a common amplifier configuration used to drive a transmission line. The 49.9-Ω resistor in series with the output matches the effective output impedance of the amplifier to the line impedance. In test and measurement instruments the nominal line impedance is assumed to be 50 Ω, for video the nominal line impedance is assumed to be 75 Ω. If testing this device as a video linear driver we recommend changing the value of R5 to 75Ω.

Due to the nature of current feedback high speed amplifiers the gain of the THS3062 can be increased by decreasing the values of R1 and R8 with little change in bandwidth. R6 should be reduced to maintain optimum compensation. Refer to the data sheet for recommended resistor values.

3.3 Applications for EVM Channel 2

Since the board layout of EVM channel 2 is identical to EVM channel 1, the applications above can be applied identically. The only physical difference is that different values have been installed in the default configuration for different EVM channels. In addition, the components are labeled differently for each EVM channel. Refer to complete schematic and board silkscreen to resolve these issues.

Chapter 4

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, component placement diagram, and printed-circuit board layout.

Table 4-1. THS3062EVM Bill of Materials

Item	Description	SMD Size	Reference Designator	PCB QTY	Manufacturer's Part Number	Distributor's Part Number
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi-Key) 240-1010-1-ND
2	Cap, 22 μF, tanatalum, 25 V, 10%	D	C5, C6	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
3	Cap, 0.1 μF, ceramic, X7R, 50 V	0805	C7, C8	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
4	Cap, 100 pF, ceramic, 5%, 150 V	AQ12	C9, C10	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
5	Open	0805	R8	1		
6	Resistor, 750 Ω, 1/8 W, 1%	0805	R7	1	(Phycomp) 9C08052A7500FKHFT	(Garrett) 9C08052A7500FKHFT
7	Resistor, 562 Ω, 1/8 W, 1%	0805	R1, R6	2	(Phycomp) 9C08052A5620FKHFT	(Garrett) 9C08052A5620FKHFT
8	Open	1206	R9	1		
9	Resistor, 54.9 Ω, 1/4W, 1%	1206	R2	1	(Phycomp) 9C12063A54R9FKRFT	(Garrett) 9C12063A54R9FKRFT
10	Resistor, 49.9 , 1/4 W, 1%	1206	R3, R5, R10, R11	1	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
11	Resistor, 953 Ω, 1/8 W, 1%	1206	R4, R12	2	(Phycomp) 9C08052A9530FKHFT	(Garrett) 9C12063A9530FKRFT
12	Jack, banana receptance, 0.25" Dia. Hole		J7, J8, J9		(HH Smith) 101	(Newark) 35F865
13	Test Point, Black		TP1, TP2	2	(Keystone) 5001	(Allied) 839-3601
14	Connector, EDGE, SMA PCB Jack		J1, J2, J3, J4, J5, J6	6	(Johnson) 142-0701-801	(Allied) 528-0238
15	IC, THS3062		U1	1	(TI) THS3062DGN	
16	Printed-circuit board			1	(TI) EDGE #6440283	

Figure 4-1. Top Layer 1 (Signals and Silkscreen) for THS3062EVM

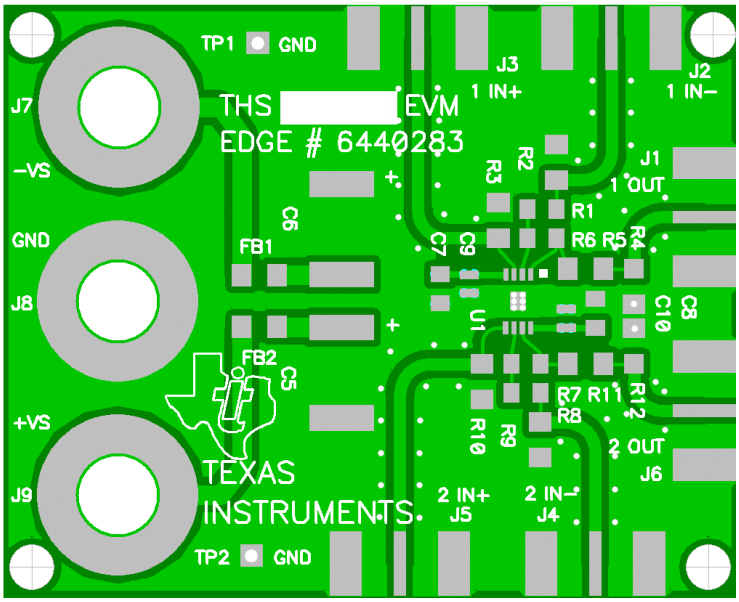


Figure 4-2. Internal Plane (Layer 2) Ground Plane

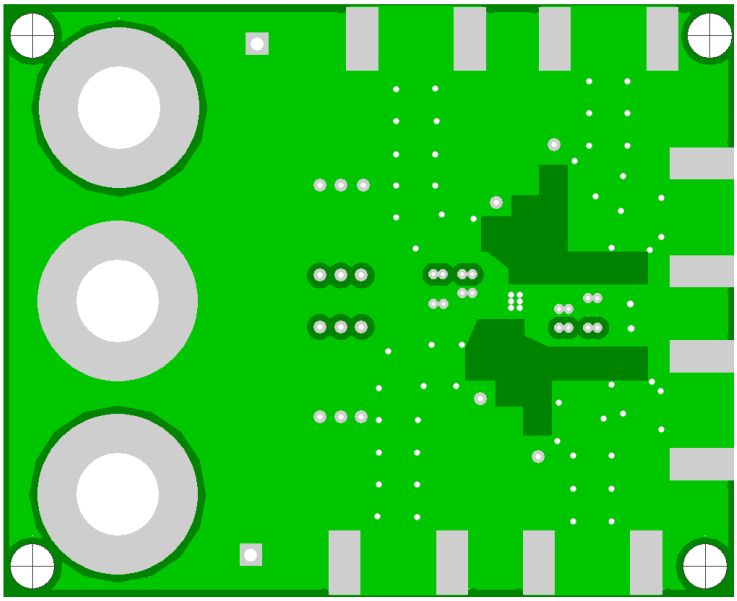


Figure 4-3. Internal Plane (Layer 3) Power Layer

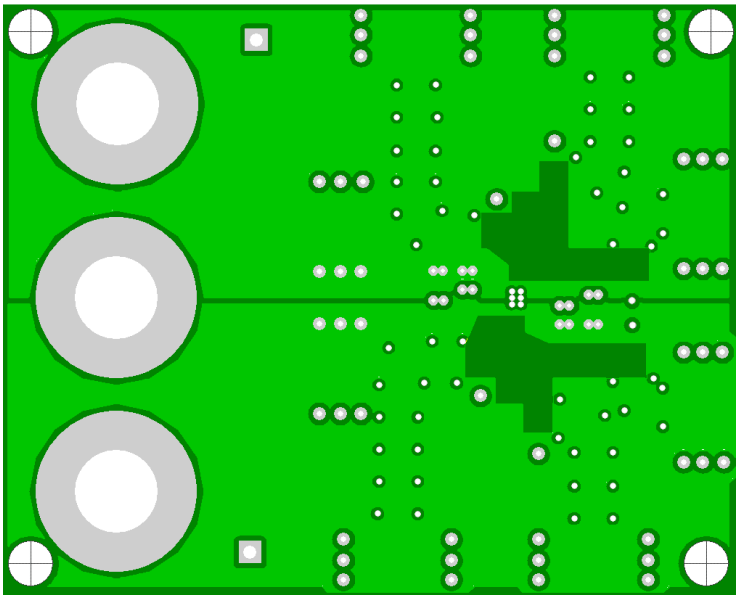


Figure 4-4. Bottom (Layer 4) Ground and Signal

