

THCV231-Q and THCV236-Q

SerDes transmitter and receiver with bi-directional transceiver

General Description

The THCV231-Q and THCV236-Q are designed to support video data transmission between the host and display.

THCV231-Q

One high-speed lane can carry up to 14bits data at a pixel clock frequency from 12MHz to 160MHz.

THCV236-Q

One high-speed lane can carry up to 32bit data and 3bits of synchronizing signals at a pixel clock frequency from 6MHz to 160MHz by converting RGB444 to YCbCr422.

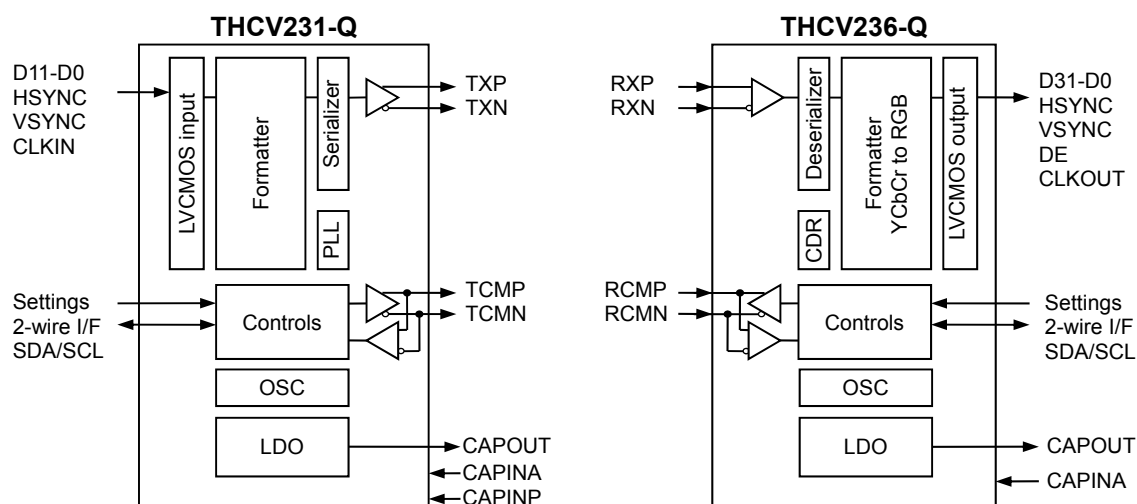
The chipset, which has one high-speed data lane, can transmit video data up to 1080p/60Hz.

The maximum serial data rate is 4.00Gbps/lane.

Features

- Data width selectable
- Wide frequency range
- AC coupling for high-speed lanes
- CDR requires no external frequency reference
- Wide range supply voltage from 1.7V to 3.6V
- Additional spread spectrum on data stream
- 2-wire serial interface bridge function(400kbps)
- Remote side GPIO control and monitoring
- THCV231-Q
 - QFN32 (5mm x 5mm) with exposed pad ground
- THCV236-Q
 - QFN64 (9mm x 9mm) with exposed pad ground
- AEC-Q100 Grade 2 (-40 to 105degC)
- ISO/TS16949 compliant
- EU RoHS compliant

Block Diagram

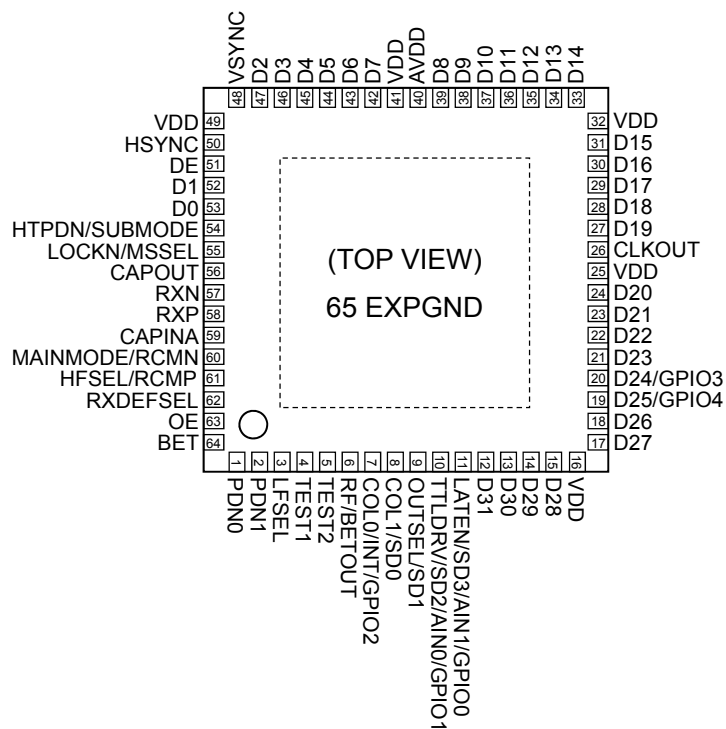
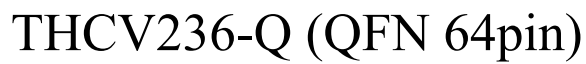


Contents Page

General Description	1
Features	1
Block Diagram	1
Pin Configuration	4
Pin Description	5
Pin Description for THCV231-Q	5
Pin Description for THCV236-Q	6
Functional Overview	10
Functional Description	10
Internal Reference Output/Input Function (CAPOUT, CAPINA, CAPINP)	10
Power Down (PDN1, PDN0, PDN)	11
Pre-emphasis and Drive Select Function (THCV231-Q only)	11
Permanent Clock Output (THCV236-Q only)	11
Spread Spectrum Clock Generator (SSCG)	12
Data Enable	14
Hot-Plug Function	15
Lock Detect Function	15
Field BET Operation	16
Data Width and Frequency Range Select Function	18
Data Mapping	18
2-wire serial I/F Mode	19
2-wire serial I/F Device ID setting	19
2-wire serial I/F Clock Stretching	19
Read/Write access to Sub-Link Master Register	21
Read/Write access to Sub-Link Slave Register	22
Read/Write access to remote side 2-wire serial slave devices connected to Sub-Link Slave Device	24
GPIO	28
Interruption	30
Register Map	31
Absolute Maximum Ratings	40
Recommended Operating Conditions	40
Electrical Specification	40
LVCMOS DC Specification	40
CML DC Specification	41
CML Bi-Directional DC Specification	41

Supply Current	42
Switching Characteristics	42
AC Timing Diagrams and Test Circuits	46
LVCMOS Input, Output Switching Characteristics	46
CML Output Switching Characteristics.....	47
CML Bi-directional Output Test Circuit.....	48
Latency Characteristics	49
Lock and Unlock Sequence	50
2-wire serial I/F Switching Characteristics	51
GPIO Switching Characteristics.....	53
PCB Layout Guideline regarding VDD and AVDD for THCV236-Q	55
Package.....	56
Notices and Requests	58

THCV231-Q (QFN 32pin)



Pin Description

Pin Description for THCV231-Q

Pin Name	Pin No.	Type	Description
TXP	29	CO	High-Speed CML Signal Output (Main-Link)
TXN	30	CO	High-Speed CML Signal Output (Main-Link)
TCMP	27	CB	CML Signal Bidirectional Input/Output (Sub-Link)
TCMN	28	CB	CML Signal Bidirectional Input/Output (Sub-Link)
GPIO4	8	B	<u>GPIO4</u> : General Purpose Input/Output. When GPIO4 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO4 is used as push pull output, no external component is required. <u>LATEN</u> : Latch select input under Field BET (Sub-Link) 0 : Forbidden 1 : Latched result
GPIO3	7	B	<u>GPIO3</u> : General Purpose Input/Output. When GPIO3 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO3 is used as push pull output, no external component is required.
SCL	6	B	SCL input/output for 2-wire serial I/F.
SDA	5	B	SDA input/output for 2-wire serial I/F.
CLKIN	13	I	Clock Input
D11-D0	23,22,20-17,15,14,12-9	I	Pixel Data Input
HSYNC	25	I	HSYNC Input
VSNC	24	I	VSNC Input
RF/BETOUT	4	B	<u>RF</u> : Input Clock Triggering edge select. See Figure 17. 0 : Falling Edge 1 : Rising Edge <u>BETOUT</u> : Field BET Result Output when Field BET mode.
PDN	1	IL	Power Down 0 : Power Down 1 : Normal Operation
TEST2	3	I	Test pin. Must be tied to Ground for normal operation.
TEST1	2	IL	Test pin. Must be tied to Ground for normal operation.
CAPOUT	26	PWR	Decoupling Capacitor Pin, 1.2V output.
CAPINA	31	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
CAPINP	32	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
VDD	16	PWR	1.7-3.6V Digital Power Supply Pin for LVCMOS I/O
AVDD	21	PWR	1.7-3.6V Analog Power Supply Pin for LDO
EXPGND	33	GND	Exposed Pad Ground. Must be tied to the PCB ground plane through an array of vias.

CO : CML Output buffer , CB : CML Bi-directional buffer

I : LVCMOS Input buffer , IL : Low Speed LVCMOS Input buffer , B : LVCMOS Bi-directional buffer

PWR : Power supply , GND : Ground

Pin Description for THCV236-Q

Pin Name	Pin No.	Type	Description
RXP	58	CI	High-Speed CML Signal Input(Main-Link)
RXN	57	CI	High-Speed CML Signal Input(Main-Link)
HFSEL/RCMP	61	CB/I	<u>HFSEL</u> : High Frequency Mode select when PDN1=0. 0 : High Frequency Mode Disable 1 : High Frequency Mode Enable <u>RCMP</u> : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
MAINMODE/RCMN	60	CB/I	<u>MAINMODE</u> : Setting V-by-One[®] HS Mode or Sync Free Mode when PDN1=0 0 : V-by-One[®] HS Mode 1 : Sync Free Mode <u>RCMN</u> : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
HTPDN/SUBMODE	54	BO	<u>HTPDN</u> : Hot Plug Detect Output when PDN1=0. Must be connected to Tx HTPDN with 10kΩ pull-up resistor. <u>SUBMODE</u> : Sub-Link Mode Select when PDN1=1. 0 : 2-wire serial I/F Mode (default No Clock Stretching mode) 1 : Low Speed Data Bridge Mode Forbid setting 1 when connecting with THCV231-Q.
LOCKN/MSEL	55	BO	<u>LOCKN</u> : Lock Detect Output when PDN1=0. Must be connected to Tx LOCKN with 10kΩ pull-up resistor. <u>MSEL</u> : Sub-Link Master/Slave Select when PDN1=1. 0 : Sub-Link Master side(inside 2-wire serial I/F is slave) 1 : Sub-Link Slave side(inside 2-wire serial I/F is master) Sub-Link Master is connected to HOST MPU. Forbid setting 1 when connecting with THCV231-Q.
LATEN/SD3/AIN1/GPIO0	11	B	<u>LATEN</u> : Latch select input under Field BET(Main-Link or Sub-Link). 0 : NOT Latched result 1 : Latched result <u>SD3</u> : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSEL=0), SD3 is output. When Sub-Link is Slave (MSEL=1), SD3 is input. <u>AIN1</u> : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSEL=0. See Table 19. <u>GPIO0</u> : General Purpose Input/Output when SUBMODE=0 and MSEL=1. When GPIO0 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO0 is used as push pull output or input, no external component is required.

TTLDRV/SD2 / AIN0/GPIO1	10	B	<u>TTLDRV</u> : LVCMOS Output Drive Strength Select when PDN1=0. 0 : Weak Drive Strength 1 : Normal Drive Strength <u>SD2</u> : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD2 is input. When Sub-Link is Slave (MSSEL=1), SD2 is output. <u>AIN0</u> : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 19. <u>GPIO1</u> : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO1 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO1 is used as push pull output or input, no external component is required.
OUTSEL/SD1	9	B	<u>OUTSEL</u> : Permanent Clock Output Enable when PDN1=0. 0 : Permanent Clock Output Disable 1 : Permanent Clock Output Enable <u>SD1</u> : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD1 is used as SCL input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD1 is input. When SUBMODE=1 and MSSEL=1, SD1 is output.
COL1/SD0	8	B	<u>COL1</u> : Color Space Converter Enable when PDN1=0 and MAINMODE=0. 0 : Color Space Converter Disable 1 : Color Space Converter Enable Data Width Setting when PDN1=0 and MAINMODE=1. See Table 16. <u>SD0</u> : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD0 is used as SDA input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD0 is input. When SUBMODE=1 and MSSEL=1, SD0 is output.
COL0/INT/ GPIO2	7	B	<u>COL0</u> : Data Width Setting when PDN1=0. See Table 16. <u>INT</u> : Interrupt signal output for Sub-Link when SUBMODE=0 and MSSEL=0. It must be connected with a pull-up resistor to VDD. L : Interrupt occurred H : Steady state <u>GPIO2</u> : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO2 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO2 is used as push pull output or input, no external component is required.
CLKOUT	26	O	Clock Output
D31-D26	12-15,17,18	O	Pixel Data Output

D25/GPIO4	19	B	D25 : Pixel Data Output GPIO4 : General Purpose Input/Output when SUBMODE=0, MSSEL=1 and RXDEFSEL=0. When GPIO4 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO4 is used as push pull output or input, no external component is required.
D24/GPIO3	20	B	D24 : Pixel Data Output GPIO3 : General Purpose Input/Output when SUBMODE=0, MSSEL=1 and RXDEFSEL=0. When GPIO3 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO3 is used as push pull output or input, no external component is required.
D23-D0	21-24,27-31,33-39,42-47,52,53	O	Pixel Data Output
DE	51	O	DE Output
HSYNC	50	O	HSYNC Output
VSYN	48	O	VSYN Output
OE	63	IL	Output Enable 0 : LVCMOS Output Disable (Hi-Z) except for HTPDN, LOCKN when PDN1=0 and except for BETOUT when BET=1 1 : LVCMOS Output Enable
BET	64	IL	Field BET entry 0 : Normal Operation 1 : Field BET Operation
RF/BETOUT	6	B	RF : Output Clock Triggering edge select. See Figure 18. 0 : Falling Edge 1 : Rising Edge BETOUT : Field BET Result Output
RXDEFSEL	62	I	Internal Register Default Setting Select. See Table 36, Table 37 0 : for THCV231-Q 1 : for THCV235-Q
LFSEL	3	I	Low Frequency mode select 0 : Low Frequency mode Disable 1 : Low Frequency mode Enable Forbid setting 1 when connecting with THCV231-Q.
PDN1	2	IL	Sub-Link Power Down 0 : Power Down. Main-Link setting by external pin 1 : Normal Operation. Main-Link Setting by 2-wire serial I/F
PDN0	1	IL	Main-Link Power Down 0 : Power Down 1 : Normal Operation
TEST2	5	I	Test pin. Must be tied to Ground for normal operation.
TEST1	4	IL	Test pin. Must be tied to Ground for normal operation.
CAPOUT	56	PWR	Decoupling Capacitor Pin, 1.2V output.
CAPINA	59	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
VDD	49,41,32,25,16	PWR	1.7-3.6V Digital Power Supply Pin for LVCMOS I/O
AVDD	40	PWR	1.7-3.6V Analog Power Supply Pin for LDO
EXPGND	65	GND	Exposed Pad Ground. Must be tied to the PCB ground plane through an array of vias.

CI : CML Input buffer , CB : CML Bi-directional buffer

I : LVCMOS Input buffer , IL : Low Speed LVCMOS Input buffer , O: LVCMOS Output buffer

B : LVCMOS Bi-directional buffer , BO : Open-Drain LVCMOS Bi-directional buffer

PWR : Power supply , GND : Ground

Table 1. Pin Sharing Description (THCV236-Q)

Sub-Link State →	2-wire serial I/F Mode
Sub-Link Master/Slave →	Master
PDN1	1
HTPDN/SUBMODE	0
LOCKN/MSSEL	0
BET	0
RXDEFSEL	0
RF/BETOUT	RF
	BETOUT(*1)
COL0/INT/GPIO2	INT
COL1/SD0	SD0(SDA)
OUTSEL/SD1	SD1(SCL)
TTLDRV/SD2/AIN0/GPIO1	AIN0
LATEN/SD3/AIN1/GPIO0	AIN1
	LATEN(*2)
D24/GPIO3	GPIO3(*3)
D25/GPIO4	GPIO4(*3)
HTPDN/SUBMODE	SUBMODE
LOCKN/MSSEL	MSSEL
MAINMODE/RCMN	RCMN
HFSEL/RCMP	RCMP

*1 When Field BET mode (Main-Link or Sub-Link), it functions as BETOUT output.

*2 When Field BET mode (Main-Link or Sub-Link), it functions as LATEN input.

*3 Through GPIO input is default on register setting

Functional Overview

With High Speed CML SerDes, proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, the THCV231-Q and THCV236-Q enable transmission of 14bit data through Main-Link by single differential pair cable with minimal external components. In addition, the THCV231-Q and THCV236-Q have Sub-Link which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for Main-Link through the other 1-pair of CML-Line. It does not need any external frequency reference such as a crystal oscillator. The THCV231-Q - THCV236-Q system is able to watch peripheral devices and to control them via 2-wire serial interface or GPIOs. They also can report interrupt events caused by change of GPIO inputs and internal statuses.

Functional Description

Internal Reference Output/Input Function (CAPOUT, CAPINA, CAPINP)

An internal regulator produces the 1.2V (CAPOUT). This 1.2V linear regulator can't supply any other external loads. Bypass CAPOUT to GND with 10uF.

CAPINP (THCV231-Q only) supplies reference voltage for internal PLL, and CAPINA supplies reference voltage for any internal analog circuit. Bypass CAPINP/CAPINA to GND with 0.1uF to remove high frequency noise. CAPOUT, CAPINA and CAPINP must be tied together.

Power supply AVDD is supposed to be stabilized with de-coupling capacitor and series noise filter (for example, ferrite bead).

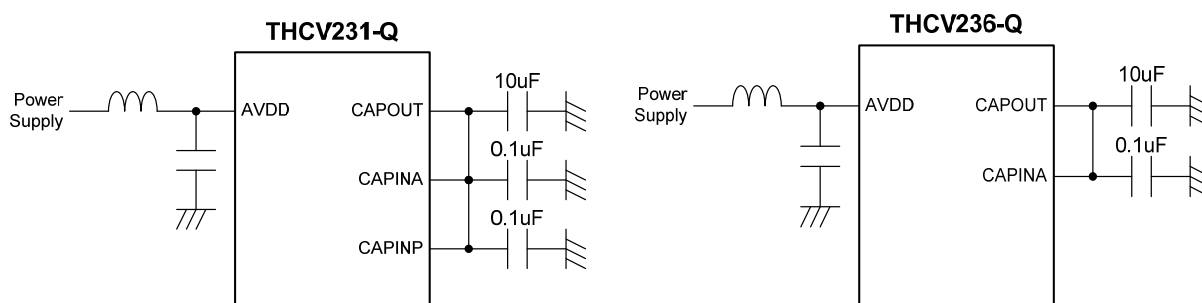


Figure 1. Connection of CAPOUT, CAPINA, CAPINP and Decoupling Capacitor

Power Down (PDN1, PDN0, PDN)

PDN1, PDN0 and PDN turn off internal circuitry of Main-Link and Sub-Link separately.

Table 2. Power Down Setting(THCV231-Q)

PDN	Operation
0	Both Main-Link and Sub-Link power down
1	Both Main-Link and Sub-Link active

Table 3. Power Down Setting(THCV236-Q)

PDN1	PDN0	Operation
0	0	Both Main-Link and Sub-Link power down
0	1	Only Main-Link is active
1	0	Only Sub-Link is active
1	1	Both Main-Link and Sub-Link active

Pre-emphasis and Drive Select Function (THCV231-Q only)

Pre-emphasis can equalize severe signal degradation caused by long-distance or high-speed transmission. PRE register selects the strength of pre-emphasis. CMLDRV register controls CML Main-Link output swing level. See Table 4.

Table 4. Pre-emphasis and Drive Select function table

CMLDRV[1:0] (register)	PRE (register)	Condition	
		Swing Level	Pre-emphasis Level
00	0	400mV diff p-p	0dB
	1		6dB
01	0	600mV diff p-p	0dB
	1		3.5dB
10	*	800mV diff p-p	0dB
11	*	Forbidden	

Permanent Clock Output (THCV236-Q only)

When there is no input from Main-Link, the THCV236-Q will output internal oscillator clock from CLKOUT pin. This function is controlled by OUTSEL pin or OUTSEL_ENABLE register and OUTSEL_SETTING register. See Table 5.

Table 5. Permanent Clock Output function table (PDN1=1)

OUTSEL_ENABLE (register)	OUTSEL_SETTING (register)	Output Clock Frequency(*1)
0	*	-
1	00	80MHz
	01	40MHz(default)
	10	20MHz
	11	10MHz

*1 typical value

Spread Spectrum Clock Generator (SSCG)

The THCV231-Q serial data output and the THCV236-Q parallel data and clock outputs are modulated by programmable SSCG. The THCV231-Q and THCV236-Q SSCG are enabled by only SSEN register. The modulation rate and modulation frequency variation of output spread is controlled through the SSCG control registers on each device. Do not enable spread spectrum for both the THCV231-Q and THCV236-Q at the same time.

Table 6. SSCG enable signal

Mode Entry Signal	Description
SSEN(register)	0:SSCG Disable 1:SSCG Enable

When customer use the mode and frequency range shown in Table 7, register setting is required according to Table 8.

Table 7. Main-Link mode and frequency range requiring register setting

Mode Setting				Freq.Range[MHz] (SSCG Enable)		Register Setting (*2)
MAINMODE	HFSEL	COL1	COL0	min	max	
1	0	0	0	26.6	40	Case1
1	0	0	1	26.6	50	Case1
1	0	1	0	33.3	66.6	Case2
1	1	(*1)	(*1)	50	100	Case3

*1 Don't care

*2 See Table 8

Table 8. SSCG register setting

Step	Register Address(HEX)		Register Value(HEX)				Description
	Sub-Link Master side	Sub-Link Slave side	Case1	Case2	Case3		
					THCV231-Q	THCV236-Q	
1	0x70	0xF0	0x01				Set 1 to PLL_SET_EN
2	0x76	0xF6	0x02		0x02	0x01	Set PLL_SET0
3	0x78	0xF8	0x3C	0x30	0x20		Set PLL_SET1
4	0x7C	0xFC	0x35	0x34	0x24		Set PLL_SET2

Modulation frequency f_{mod} can be determined by HFSEL and LFSEL settings, input clock frequency and FMOD register setting (default value 0xD). Refer to following formula.

$$f_{\text{mod}} = \frac{f_{\text{CLKSSCG}}}{128 \times \text{FMOD}}$$

f_{CLKSSCG} is the frequency listed in Table 9 and Table 10.

Table 9. $f_{CLKSSCG}$ (THCV231-Q)

HFSEL (register)	$f_{CLKSSCG}$
0	$(1/t_{TCIP})/2$
1	$(1/t_{TCIP})/4$

Table 10. $f_{CLKSSCG}$ (THCV236-Q)

HFSEL	LFSEL	$f_{CLKSSCG}$
0	0	$(1/t_{RCP})/2$
1	0	$(1/t_{RCP})/4$
*	1	Forbidden Setting

Up to 0.5 % spread at the 30kHz modulation frequency is stable for most cases. In case of using out of this range, please verify at the actual system.

Data Enable

V-by-One[®] HS mode operation (MAINMODE=0) are shown below. THCV231-Q HSYNC pin input is DE signal. Table 11 and related note shows requirements for DE. Video HSYNC signal may meet DE input requirement. HSYNC output of THCV236-Q under THCV231-Q V-by-One[®] HS mode operation is invalid.

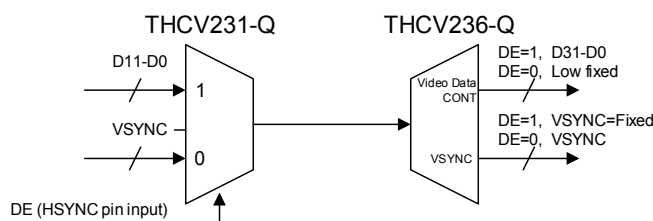


Figure 2. Conceptual Diagram of the Basic Operation of the Chipset in V-by-One[®] HS mode

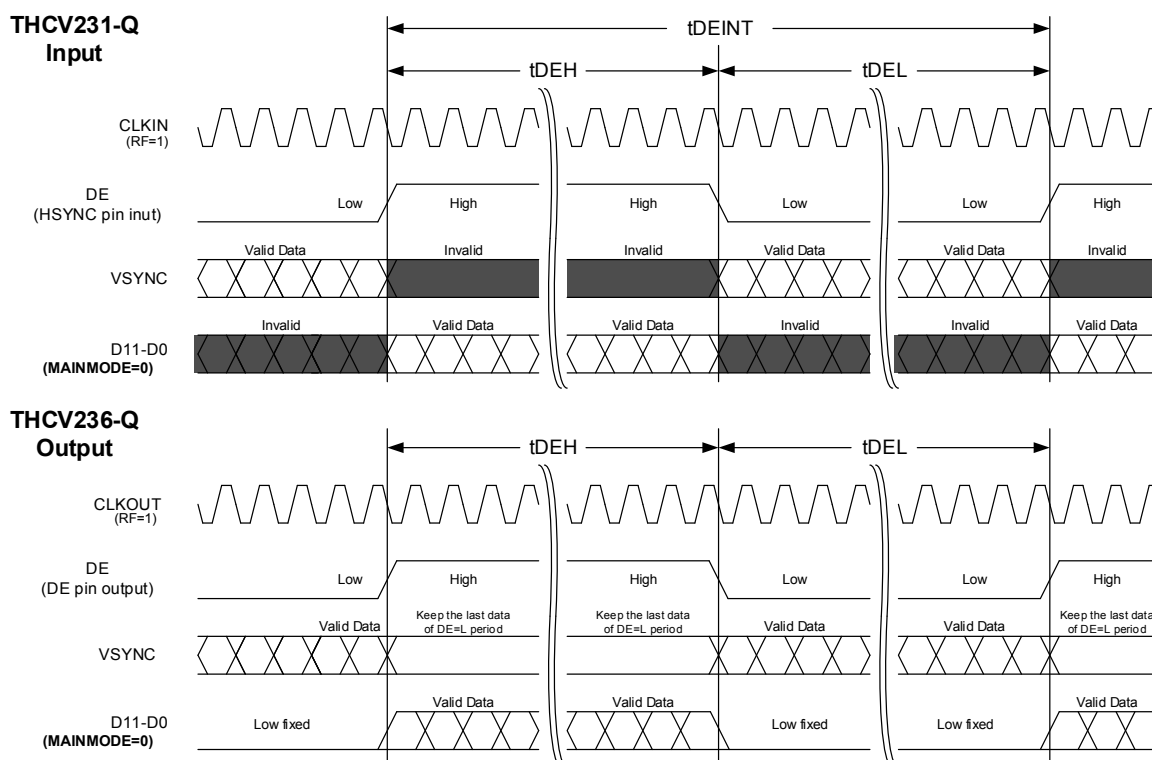


Figure 3. Data and Synchronizing Signals Transmission Timing Diagram in V-by-One[®] HS mode

Table 11. DE Requirement

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tDEH	DE=1 Duration	MAINMODE=0 and HFSEL=0	2×tTCIP	-	-	ns
		MAINMODE=0 and HFSEL=1	4×tTCIP	*Note	-	ns
		MAINMODE=1	Don't care			
tDEL	DE=0 Duration	MAINMODE=0 and HFSEL=0	2×tTCIP	-	-	ns
		MAINMODE=0 and HFSEL=1	4×tTCIP	*Note	-	ns
		MAINMODE=1	Don't care			

*Note: In V-by-One[®] HS Mode (MAINMODE=0) and High Frequency Mode (HFSEL=1), the period between rising edges of DE (tDEINT), high time of DE (tDEH) should always satisfy following equations.

$$tDEH = tTCIP \cdot (2m) \text{ and } tDEINT = tTCIP \cdot (2n), \quad m, n = 2, 3, 4, 5, 6, \dots$$

Hot-Plug Function

HTPDN signal indicates connecting condition between the Transmitter and the Receiver. HTPDN of the transmitter side is high when the Receiver is not active or not connected. Then the Transmitter can enter into the power down mode. HTPDN is set to low by the Receiver when the Receiver is active and connects to the Transmitter, and then the Transmitter must start up and transmit CDR training pattern for link training.

HTPDN is transferred to the Transmitter via Sub-Link line. HOST MPU can confirm HTPDN state by reading Sub-Link Master register (0x00 bit0 HTPDN).

Lock Detect Function

LOCKN indicates whether the receiver CDR PLL is in the lock state or not. LOCKN at the Transmitter input is set to High when the Receiver is not active or at the CDR PLL training state. LOCKN is set to low by the Receiver when CDR lock is done. Then the CDR training mode finishes and the Transmitter shifts to the normal operation.

LOCKN is transferred via Sub-Link line. HOST MPU can confirm LOCKN state by reading Sub-Link Master register (0x00 bit1 LOCKN).

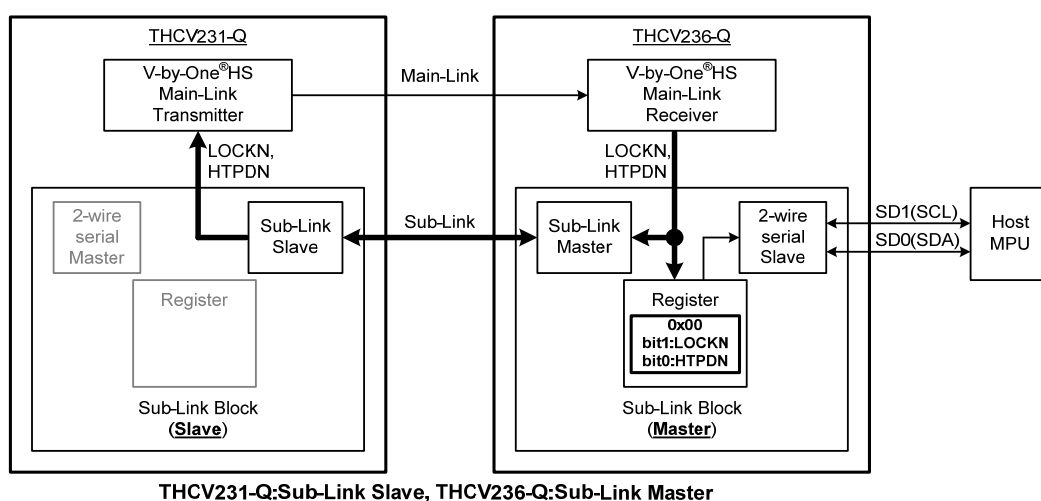


Figure 4. HTPDN, LOCKN transmission route

Field BET Operation

In order to help users to check validity of CML serial line (Main-Link and Sub-Link), the THCV231-Q and THCV236-Q have an operation mode in which they act as a bit error tester (BET). In Main-Link Field BET mode, the THCV231-Q internally generates a test pattern which is then serialized onto the Main-Link CML line. The THCV236-Q also has BET function mode. The THCV236-Q receives the data stream and checks bit errors. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto the CML channel. As for the THCV236-Q, the internal test pattern check circuit gets enabled and reports result on a certain pin named BETOUT. In Sub-Link Field BET mode, Sub-Link Master device internally generates test pattern which is then serialized onto the Sub-Link CML line. Sub-Link Slave device also has BET function mode. Sub-Link Slave device receives the data stream and checks bit errors. Note that Sub-Link Slave device must be set this mode prior to Sub-Link Master device. Pattern check result is output from BETOUT pin of the Sub-Link Slave device. The BETOUT pin goes LOW whenever bit errors occur, or it stays HIGH when there is no bit error.

In Main-Link Field BET mode, user can select two kinds of check result, latched result or NOT latched result by setting LATEN pin input. The latched result is reset by setting LATEN=0. In Sub-Link Field BET mode, only latched result is available. In order to reset the latched result, please once turn off the power and entry Sub-Link Field BET from power on sequence.

GPIO4 pin (THCV231-Q) and LATEN/SD3/AIN1/GPIO0 pin (THCV236-Q) function as LATEN in Field BET mode (Main-Link or Sub-Link).

It is not possible to realize Main-Link Field BET and Sub-Link Field BET at the same time.

Table 12. Main-Link Field BET Operation Settings

THCV231-Q/236-Q Common Setting				THCV236-Q Setting	Condition		
PDN0/PDN1/PDN	SUBMODE	BET	BET_SEL	LATEN	Main-Link	Sub-Link	Output Latch Select
1	0	1 (*1)	0 (*2)	0	Field BET Operation	Normal Operation	NOT Latched Result
				1			Latched Result

*1 THCV231-Q: Register setting (0x53 bit1), THCV236-Q: Pin setting

*2 Register setting (0x53 bit0, Default 0)

Table 13. THCV236-Q Main-Link Field BET Result

BETOUT	Output
L	Bit Error Occurred
H	No Error

Table 14. Sub-Link Field BET Operation Setting

THCV231-Q/THCV236-Q Common Setting		THCV231-Q Setting			THCV236-Q Setting			Condition	
BET	BET_SEL	PDN	GPIO3	GPIO4	PDN1	MSSEL	LATEN	Sub-Link	Output Latch Select
1 (*1)	1 (*2)	1	0	-	1	1	1 (*3)	Field BET Operation (THCV231-Q→THCV236-Q)	Latched Result
			1	1 (*3)		0	-	Field BET Operation (THCV236-Q→THCV231-Q)	

*1 THCV231-Q: Register setting (0x53 bit1), THCV236-Q: Pin setting. Note that BET pin should be 0 at power on sequence.

*2 Register setting (0x53 bit0, Default 0)

*3 Forbidden 0 setting

Table 15. Sub-Link Slave device Sub-Link Field BET Result

BETOUT	Output
L	Bit Error Occurred
H	No Error

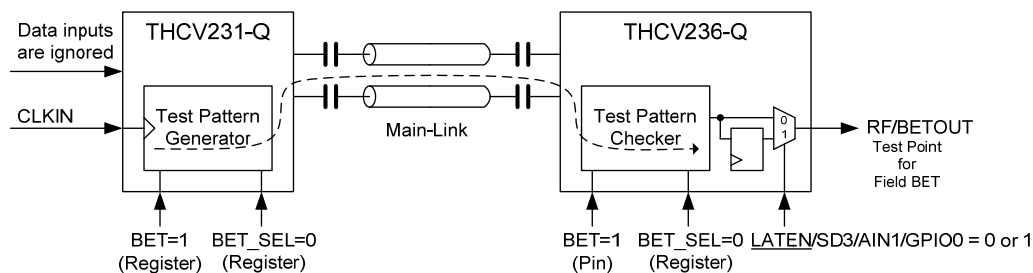


Figure 5. Main-Link Field BET Configuration

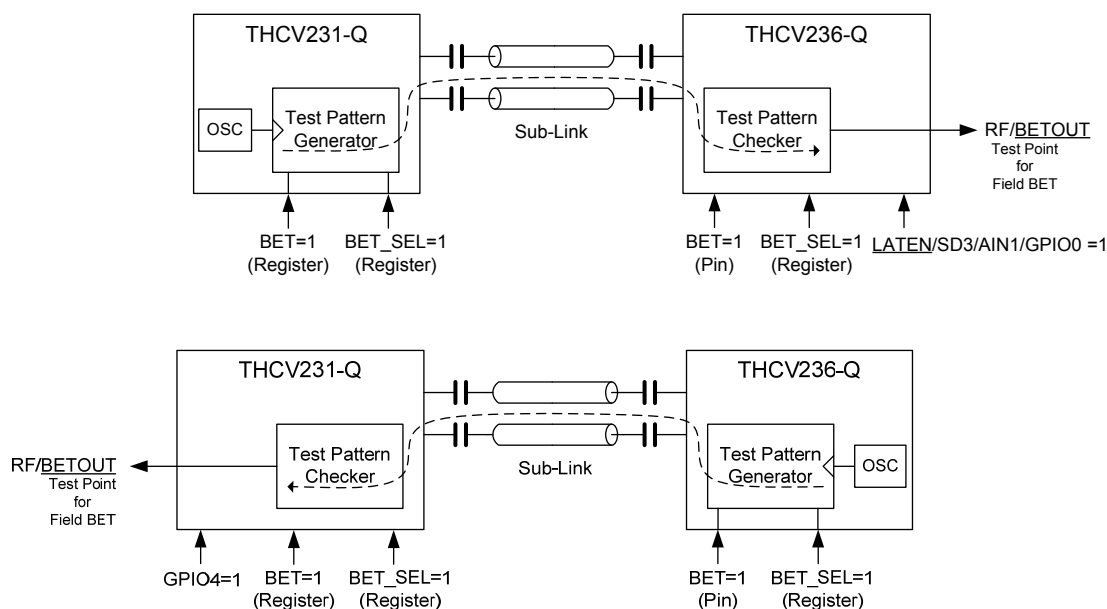


Figure 6. Sub-Link Field BET Configuration

Data Width and Frequency Range Select Function

The THCV231-Q and THCV236-Q support a variety of data width and frequency range. Frequency range is different depending on the mode setting SSCG enable and disable setting. Refer to Table 16 for details.

Table 16. Main-Link Operation Mode Select

Mode Setting				Freq.Range [MHz]				Main-Link CML Bit Rate	Data Width		Comment
				SSCG Disable		SSCG Enable (*1)			Data	Sync	
MAINMODE	HFSEL	COL1	COL0	min	max	min	max				
0	*	1	*	-	-	-	-	-	-	-	Forbidden
0	0	0	0	15	100	26.6	100	x40	12	2	
0	0	0	1	20	133.3	33.3	133.3	x30	12	2	
0	1	0	0	-	-	-	-	-	-	-	Forbidden
0	1	0	1	50	70	50	70	x20	12	2	(*2)
				70	160	70	160				-
1	0	0	0	12	30	26.6	60	x50	14		-
1	0	0	1	15	40	26.6	75	x40	14		-
1	0	1	0	20	75	33.3	100	x30	14		-
1	0	1	1	-	-	-	-	-	-	-	Forbidden
1	1	0	0	-	-	-	-	-	-	-	Forbidden
1	1	0	1	50	70	50	70	x20	14		(*2)
				70	160	70	160				-
1	1	1	0	50	70	50	70	x15	10		(*2)
				70	160	70	160				-
1(*3)	1	1	1	50	70	50	70	x15	8	2	(*2) (*3)
				70	160	70	160				(*3)

*1 Note that register setting is required depending on the mode setting and used frequency range. See Table 7.

*2 Register setting is required. See Table 17.

*3 While Register MAINMODE setting = 1, however, behavior of this exceptional setting is V-by-One® HS Mode whose meaning is MAINMODE = 0.

Table 17. Register setting (HFSEL=1 and Frequency range is from 50MHz to 70MHz)

Step	Register Address(HEX)		Register Value(HEX)		Description
	Sub-Link Master side	Sub-Link Slave side	THCV231-Q	THCV236-Q	
1	0x70	0xF0	0x01		Set 1 to PLL_SET_EN
2	0x76	0xF6	0x02	0x01	Set PLL_SET0
3	0x78	0xF8	0x20		Set PLL_SET1
4	0x7C	0xFC	0x24		Set PLL_SET2

Data Mapping

Table 18. Data Mapping

MAINMODE	0	0	0	1	1	1	1	1	1
HFSEL	0	0	1	0	0	0	1	1	1
COL1	0	0	0	0	0	1	0	1	1
COL0	0	1	1	0	1	0	1	0	1
D0	D0/RAW4	D0/RAW4	D0/RAW4/YC0	D0	D0	D0	D0/RAW4	D0/YC0	D0/RAW0/YC0
D1	D1/RAW5	D1/RAW5	D1/RAW5/YC1	D1	D1	D1	D1/RAW5	D1/YC1	D1/RAW1/YC1
D2	D2/RAW6	D2/RAW6	D2/RAW6/YC2	D2	D2	D2	D2/RAW6	D2/YC2	D2/RAW2/YC2
D3	D3/RAW7	D3/RAW7	D3/RAW7/YC3	D3	D3	D3	D3/RAW7	D3/YC3	D3/RAW3/YC3
D4	D4/RAW8	D4/RAW8	D4/RAW8/YC4	D4	D4	D4	D4/RAW8	D4/YC4	D4/RAW4/YC4
D5	D5/RAW9	D5/RAW9	D5/RAW9/YC5	D5	D5	D5	D5/RAW9	D5/YC5	D5/RAW5/YC5
D6	D6/RAW10	D6/RAW10	D6/RAW10/YC6	D6	D6	D6	D6/RAW10	D6/YC6	D6/RAW6/YC6
D7	D7/RAW11	D7/RAW11	D7/RAW11/YC7	D7	D7	D7	D7/RAW11	D7/YC7	D7/RAW7/YC7
D8	D8/RAW0	D8/RAW0	D8/RAW0	D8	D8	D8	D8/RAW0	-	-
D9	D9/RAW1	D9/RAW1	D9/RAW1	D9	D9	D9	D9/RAW1	-	-
D10	D10/RAW2	D10/RAW2	D10/RAW2	D10	D10	D10	D10/RAW2	-	-
D11	D11/RAW3	D11/RAW3	D11/RAW3	D11	D11	D11	D11/RAW3	-	-
HSYNC	DE*2 (HSYNC*3)	DE*2 (HSYNC*3)	DE*2 (HSYNC*3)	HSYNC*1	HSYNC*1	HSYNC*1	HSYNC*1	HSYNC*1	DE*2 (HSYNC*3)
VSNC	VSNC	VSNC	VSNC	VSNC*1	VSNC*1	VSNC*1	VSNC*1	VSNC*1	VSNC*1

*1 Any signal as well as sync signal can be transmitted when MAINMODE=1.

*2 V-by-One®HS mode operation requires Data Enable (DE) signal rule. Please refer to the related section.

*3 HSYNC signal can be assigned to Data Enable input when V-by-One® HS mode requirements are met.

Sub-Link Mode Setting

2-wire serial I/F Mode

2-wire serial I/F Mode enables register access, using GPIO (General Purpose Input/Output) pin and interrupt function. Sub-Link Master device has 2-wire serial slave block and can be connected to HOST MPU, Sub-Link Slave device has 2-wire serial master block and can be connected to remote side 2-wire serial slave devices.

HOST MPU can access register of Sub-Link Master device, Sub-Link Slave device and remote side 2-wire serial slave devices.

2-wire serial I/F Device ID setting

AIN1 and AIN0 pins determine Device ID setting of the THCV236-Q. Only Sub-Link Master device has AIN1 and AIN0 pin. AIN1 and AIN0 choose one of 4 addresses which give an identification address to the THCV236-Q under 2-wire serial interface bus topology.

Table 19. 2-wire serial I/F Device ID select (Sub-Link Master device Only)

AIN1	AIN0	Device ID
0	0	0x0B
0	1	0x34
1	0	0x77
1	1	0x65

2-wire serial I/F Clock Stretching

In principle, when Sub-Link bridges 2-wire serial interface communication from Sub-Link Master to Sub-Link Slave or remote side 2-wire serial slave devices, time lag occurs between HOST MPU side 2-wire serial access and Sub-Link Slave internal bus access or remote side 2-wire serial access.

2WIRE_MODE (Sub-Link Master side register, 0x0F bit1-0) selects whether 2-wire serial slave of Sub-Link Master perform clock stretching or not.

When 2WIRE_MODE = 00, Sub-Link Master device wait HOST MPU until Sub-Link Slave register access or remote side 2-wire serial slave register access is completed by clock stretching.

When 2WIRE_MODE = 01, Sub-Link Master device informs HOST MPU that Sub-Link Slave register access or remote side 2-wire serial register access has been completed by interruption (INT pin) without clock stretching.

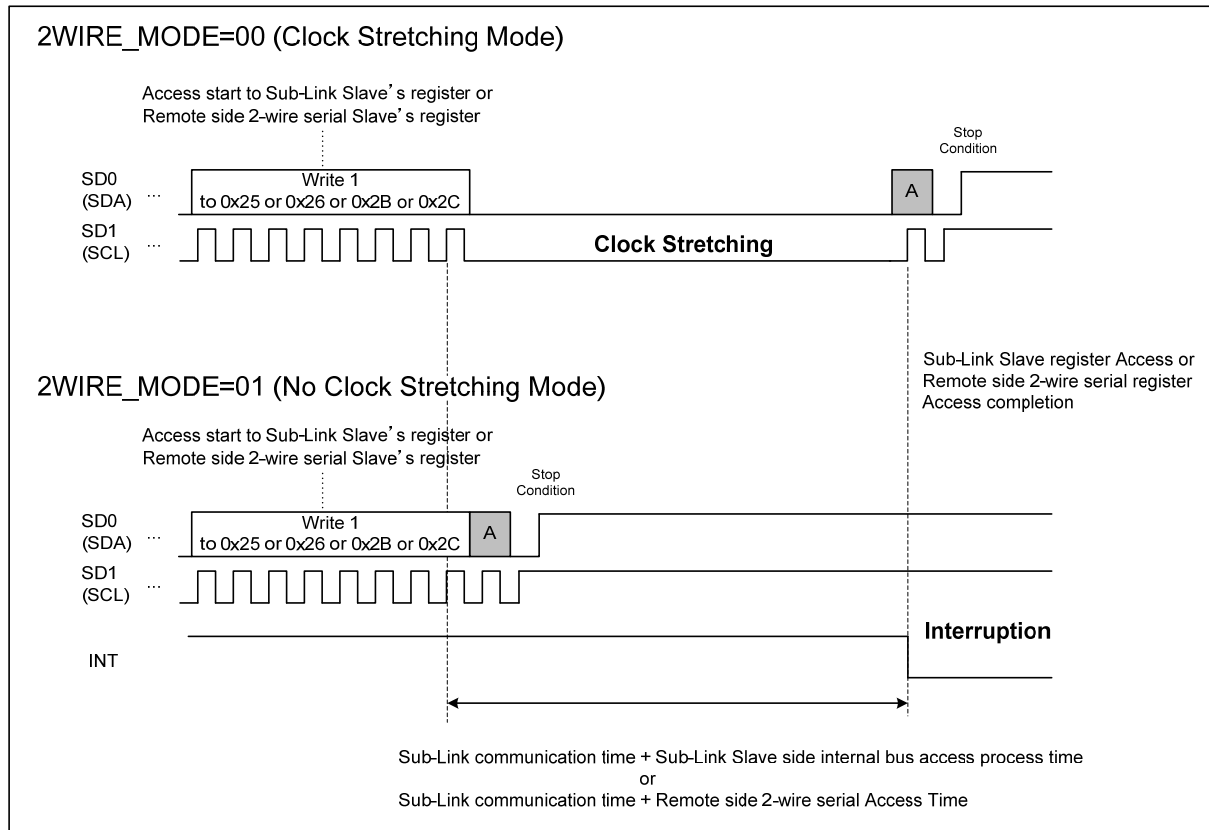


Figure 7. 2WIRE_MODE Operation

Read/Write access to Sub-Link Master Register

HOST MPU can directly access Sub-Link Master's register by 2-wire serial I/F.

Register address of Sub-Link Master is from 0x00 to 0x7F. See **Register Map** for more information.

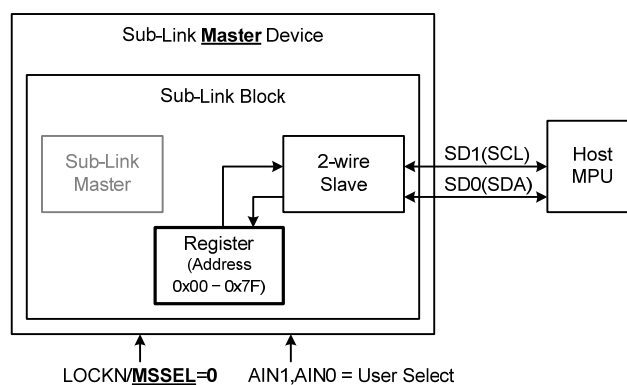


Figure 8. Host to Sub-Link Master Register access configuration

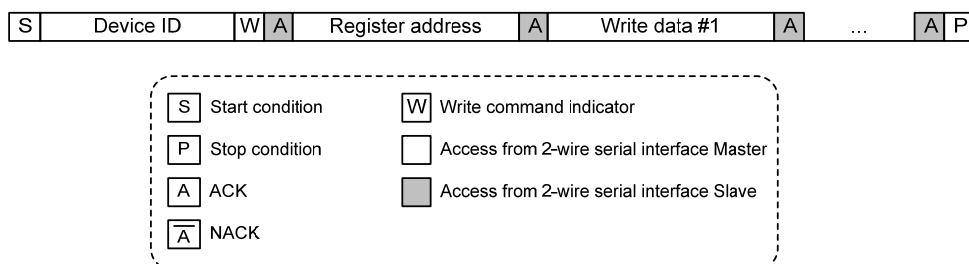


Figure 9. 2-wire serial I/F write to Sub-Link Master register protocol

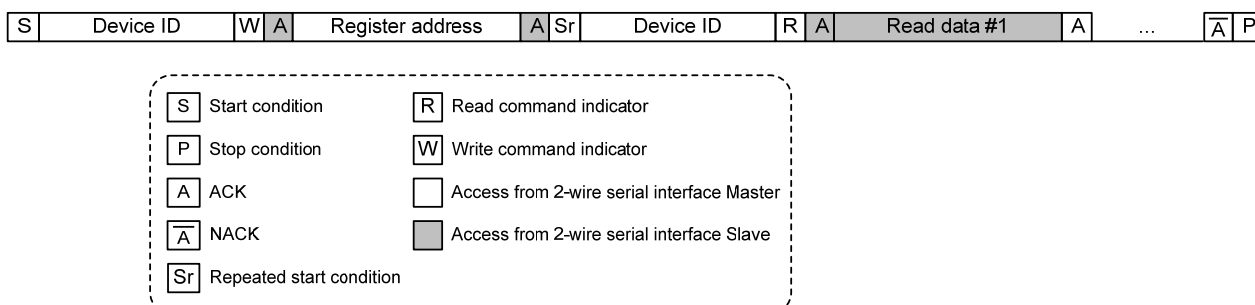


Figure 10. 2-wire serial I/F read to Sub-Link Master register protocol

Read/Write access to Sub-Link Slave Register

HOST MPU can access to Sub-Link Slave's register via Sub-Link Master by Sub-Link Master register settings. Register address of Sub-Link Slave is from 0x80 to 0xFF. See **Register Map** for more information.

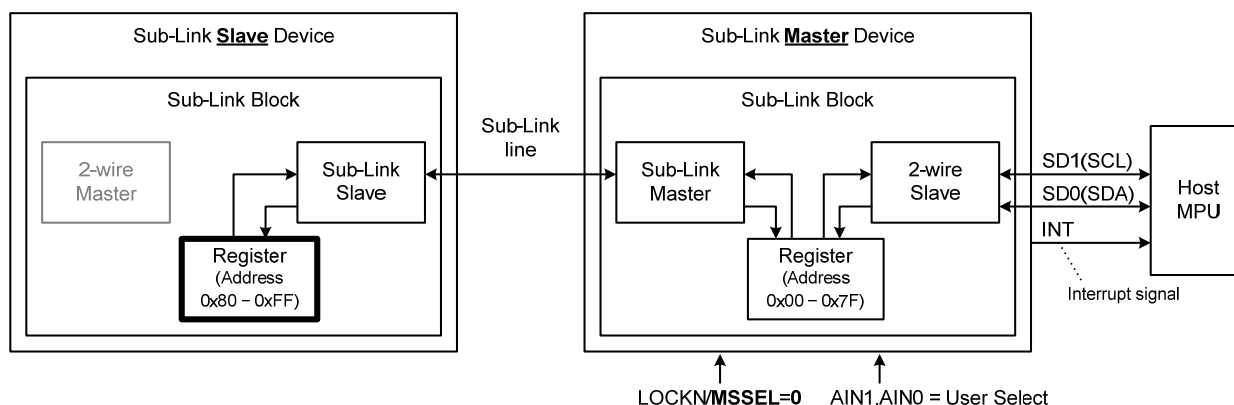


Figure 11. Host MPU to Sub-Link Slave Register access configuration

Table 20. Sub-Link slave register Write Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
2	Set the data for Sub-Link Slave to write (Max 16byte).	W	0x10-0x1F
3	Set Device ID of Sub-Link Master device. (Value corresponding to AIN1 and AIN0 setting. e.g.[AIN1,AIN0]=[0,0] → 7'h0B)	W	0x20
4	Set the byte number written to Sub-Link Slave (Max 16byte). (Byte number = register value + 1)	W	0x21
5	Set the start address of Sub-Link Slave register to write.	W	0x23
6	Write 1 to WR_START_8B. (Start write access to Sub-Link Slave register)	W	0x25 (*1)
7 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed.	-	-
7 (*3)	When write access is completed, 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
8	If write access was normally ended, read value should be "0x1".	R	0x02 bit7

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)

*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

Table 21. Sub-Link slave register Read Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
2	Set Device ID of Sub-Link Master device. (Value corresponding to AIN1 and AIN0 setting. e.g. [AIN1,AIN0]=[0,0] → 7'h0B)	W	0x20
3	Set the byte number read from Sub-Link Slave(Max 16byte). (Byte number = register value + 1)	W	0x22
4	Set the start address of Sub-Link Slave register to read.	W	0x24
5	Write 1 to RD_START_8B. (Start read access to Sub-Link Slave register)	W	0x26 (*1)
6 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x10-0x1F).	-	-
6 (*3)	When read access is completed, read data is stored in Sub-Link Master register (Address 0x10-0x1F) and 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
7	If read access was normally ended, read value should be "0x1".	R	0x02
8	HOST MPU read data stored in Sub-Link Master register.	R	0x10-0x1F

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)

*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

Read/Write access to remote side 2-wire serial slave devices connected to Sub-Link Slave Device

HOST MPU can access to remote side 2-wire serial slave register via Sub-Link Master and Sub-Link Slave by Sub-Link Master register settings. Sub-Link Slave has 2-wire serial master block. Up to 8 devices are connectable to 2-wire serial master of Sub-Link Slave device.

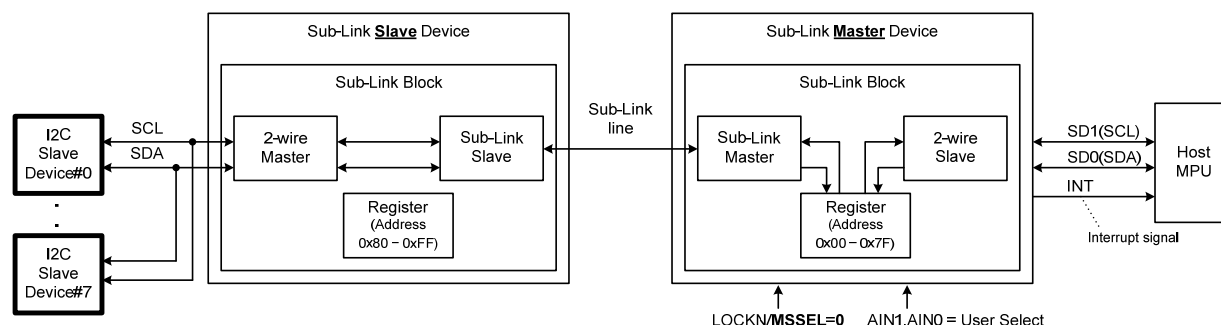


Figure 12. Host to 2-wire serial Slave devices connected to Sub-Link Slave device access configuration

Table 22. Remote side 2-wire serial slave register Write Procedure for 8bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set the data for remote side 2-wire serial slave to write (Max 16byte).	W	0x10-0x1F
4	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B[6:0]), and set 0 to 0x20 bit7.	W	0x20
5	Set the byte number written to remote side 2-wire serial slave (Max 16byte). (Byte number = register value + 1)	W	0x21
6	Set the start address of remote side 2-wire serial slave register to write.	W	0x23
7	Write 1 to WR_START_8B. (Start write access to remote side 2-wire serial slave register)	W	0x25 (*1)
8	2-wire serial slave of Sub-Link Master perform clock stretching until remote side 2-wire serial slave register access is completed. (*2)	-	-
8	When write access is completed, 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L). (*3)	-	-
9	If wire access was normally ended, read value should be "0x1".	R	0x02
10	Repeat from step2 to step9 if needed.	-	-

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)

*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

Table 23. Remote side 2-wire serial slave register Write Procedure for 16bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set the data for remote side 2-wire serial slave to write (Max 16byte).	W	0x10-0x1F
4	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B[6:0]), and set 1 to 0x20 bit7.	W	0x20
5	Set the byte number written to remote side 2-wire serial slave (Max 16byte). (Byte number = register value + 1)	W	0x21
6	Set the low-order bits([7:0]) of start address of remote side 2-wire serial slave register to write.	W	0x27
7	Set the high-order bits([15:8]) of start address of remote side 2-wire serial slave register to write.	W	0x28
8	Write 1 to WR_START_16B. (Start write access to remote side 2-wire serial slave register)	W	0x2B (*1)
9 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until remote side 2-wire serial slave register access is completed.	-	-
9 (*3)	When write access is completed, 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
10	If write access was normally ended, read value should be "0x1".	R	0x02
11	Repeat from step2 to step10 if needed.	-	-

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)

*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

Table 24. Remote side 2-wire serial slave register Read Procedure for 8bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B)(Low-order 7bits), and set 0 to 0x20 bit7.	W	0x20
4	Set the byte number read from remote side 2-wire serial slave(Max 16byte). (Byte number = register value + 1)	W	0x22
5	Set the start address of remote side 2-wire serial slave register to read.	W	0x24
6	Write 1 to RD_START_8B. (Start read access to remote side 2-wire serial slave register)	W	0x26 (*1)
7 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x10-0x1F).	-	-
7 (*3)	When read access is completed, read data is stored in Sub-Link Master register (Address 0x10-0x1F) and 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
8	If read access was normally ended, read value should be "0x1".	R	0x02
9	HOST MPU read data stored in Sub-Link Master register.	R	0x10-0x1F
10	Repeat from step2 to step10 if needed.	-	-

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)

*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

Table 25. Remote side 2-wire serial slave register Read Procedure for 16bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B)(Low-order 7bits), and set 1 to 0x20 bit7.	W	0x20
4	Set the byte number read from remote side 2-wire serial slave(Max 16byte).	W	0x22
5	Set the low-order bits([7:0]) of start address of remote side 2-wire serial slave register to read.	W	0x29
6	Set the high-order bits([15:8]) of start address of remote side 2-wire serial slave register to read.	W	0x2A
7	Write 1 to RD_START_16B. (Start read access to remote side 2-wire serial slave register)	W	0x2C (*1)
8 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x10-0x1F).	-	-
8 (*3)	When read access is completed, read data is stored in Sub-Link Master register (Address 0x10-0x1F) and 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
9	If read access was normally ended, read value should be "0x1".	R	0x02
10	HOST MPU read data stored in Sub-Link Master register.	R	0x10-0x1F
11	Repeat from step2 to step10 if needed.	-	-

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.

*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)

*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

GPIO

The GPIO pin provides up to 2-I/O ports and 2 types of GPIO are available (“Through GPIO” and “Programmable GPIO”). All GPIO pins of THCV236-Q have another function if being set. See Table 27. GPIO type is selected by GPIO_TYPE register (0x40(Sub-Link Master), 0xC0(Sub-Link Slave)). Programmable GPIO is available by all GPIO pins. Through GPIO is available by only GPIO4 and GPIO3 pin. See Through GPIO section and Programmable GPIO section about detail of respective GPIO type.

Table 26. GPIO Type

GPIO#	GPIO Type	
	Through GPIO	Programmable GPIO
GPIO4	Available	Available
GPIO3		

Table 27. GPIO setting of THCV236-Q

Pin Name	Function
	Sub-Link Master RXDEFSEL=0
D25/GPIO4	GPIO4
D24/GPIO3	GPIO3
COL0/INT/GPIO2	INT
TTLDRV/SD2/AIN0/GPIO1	AIN0
LATEN/SD3/AIN1/GPIO0	AIN1

Through GPIO

Input to GPIO4 and GPIO3 of Sub-Link Master device is output from GPIO4 and GPIO3 of Sub-Link Slave device respectively. Note that these GPIO signals can’t be transferred from Sub-Link Slave device to Sub-Link Master device. It’s possible to confirm GPIO4 and GPIO3 input value to Sub-Link Master by register read (0x41 GPIO_n_INPUT_MONITOR (n=4,3)). Each GPIO output signal goes to Low when Sub-Link communication fails. Sub-Link communication status can be observed by register read (0x82 bit2 COMERR_INT).

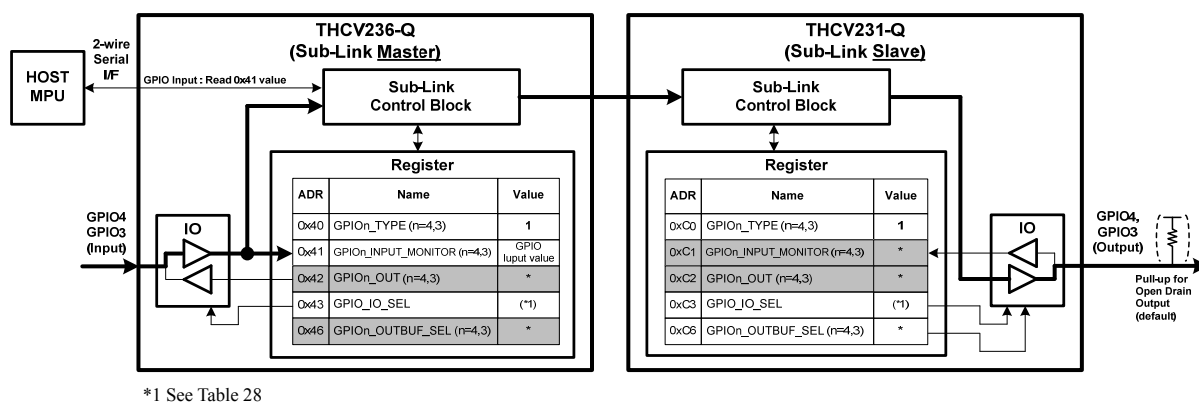


Figure 13. Through GPIO

Table 28. THCV231-Q, THCV236-Q(RXDEFSEL=0) Through GPIO register setting

Device	Sub-Link Master/Slave	GPIO Input/Output Number		GPIO4 , GPIO3 Input/Output Configuration (I:Input, O:Output)		Register Settings			
		Input	Output	GPIO4	GPIO3	GPIO Type		GPIO IO Direction	
						Address (HEX)	Value (BIN)	Address (HEX)	Value (BIN)
THCV231-Q	Slave	0	2	O	O	0xC0	XXX11XXX	0xC3	XXX00XXX
THCV236-Q	Master	2	0	I	I	0x40	XXX11XXX	0x43	XXX11XXX

Programmable GPIO

Settings input/output and reading/writing are controlled by register settings in the Sub-Link Master. HOST MPU commands register setting in the Sub-Link Master.

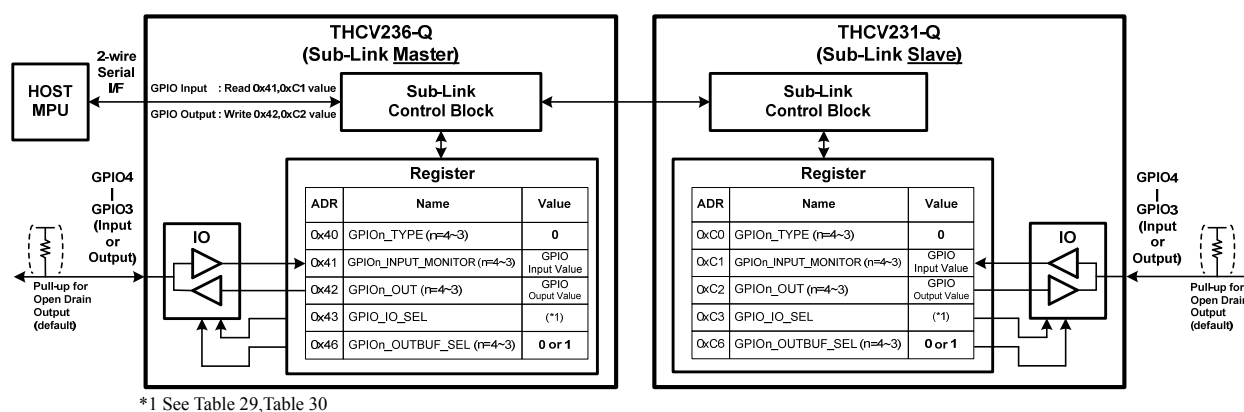


Figure 14. Programmable GPIO

Register settings are required according to the number of GPIO used by customer. See Table 29 and Table 30. When the number of GPIO used by customer is less than the value listed in Table 29 and Table 30, choose any setting which includes that.

Table 29. THCV231-Q Programmable GPIO register setting

Sub-Link Master/Slave	GPIO Input/Output Number		GPIO4 - GPIO3 Input/Output Configuration (I:Input, O:Output)		Register Settings			
	Input	Output	GPIO4	GPIO3	GPIO Type		GPIO IO Direction	
					Address (HEX)	Value (BIN)	Address (HEX)	Value (BIN)
Slave	2	0	I	I	0xC0	XXX00000	0xC3	XXX11XXX
	1	1	I	O				XXX10XXX
	0	2	O	O				XXX00XXX

Table 30. THCV236-Q Programmable GPIO register setting (RXDEFSEL=0)

Sub-Link Master/Slave	GPIO Input/Output Number		GPIO4 - GPIO0 Input/Output Configuration (I:Input, O:Output, -:Unavailable)					Register Settings			
	Input	Output	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	GPIO Type		GPIO IO Direction	
								Address (HEX)	Value (BIN)	Address (HEX)	Value (BIN)
Master	2	0	I	I	-	-	-	0x40	XXX00XXX	0x43	XXX11XXX
	1	1	I	O	-	-	-				XXX10XXX
	0	2	O	O	-	-	-				XXX00XXX

Interruption

INT pin outputs interrupt event indicator on Sub-Link Master side of the system. The INT signal is active low.

Being set by 2-wire serial interface, the THCV231-Q and THCV236-Q can monitor any changes of GPIO input pins, Sub-Link communication statuses and internal statuses as an interrupt. About the way to make interruption occur and the way to clear the interruption, see Table 32(Address 0x02, 0x03) and Table 33(Address 0x82, 0x83).

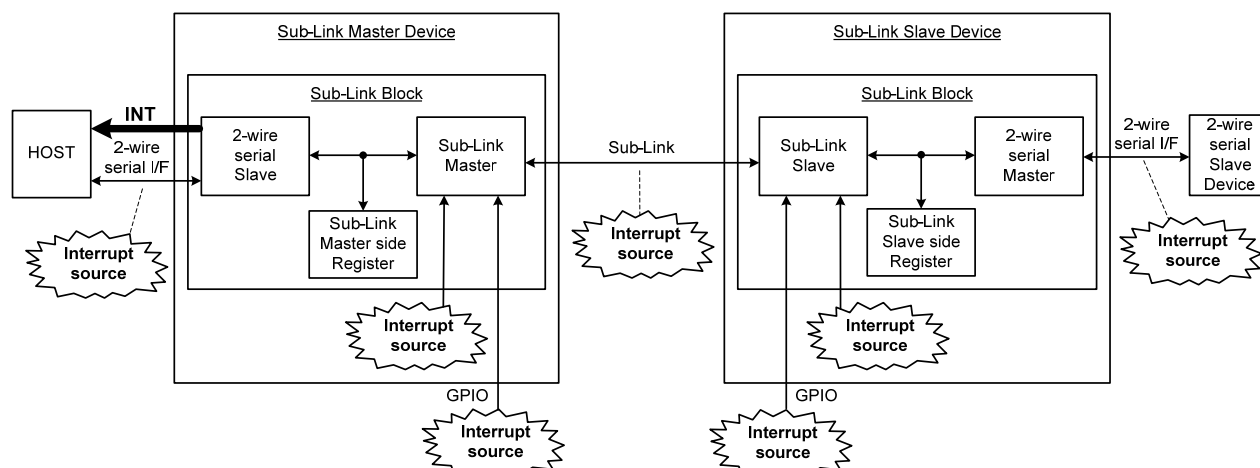


Figure 15. 2-wire serial I/F Interrupt to HOST access configuration

Table 31. Interrupt output

INT	State
L	Interrupt occurred
H	Steady state

Register Map

HOST MPU can set various operating conditions of the THCV231-Q and THCV236-Q through internal registers.

Sub-Link Master (2-wire serial slave) is connected to external HOST MPU (2-wire serial master).

Sub-Link Slave (2-wire serial master) is connected to external 2-wire serial slave devices.

Sub-Link Master device has address 0x00-0x7F, Sub-Link Slave device has address 0x80-0xFF. See Figure 16.

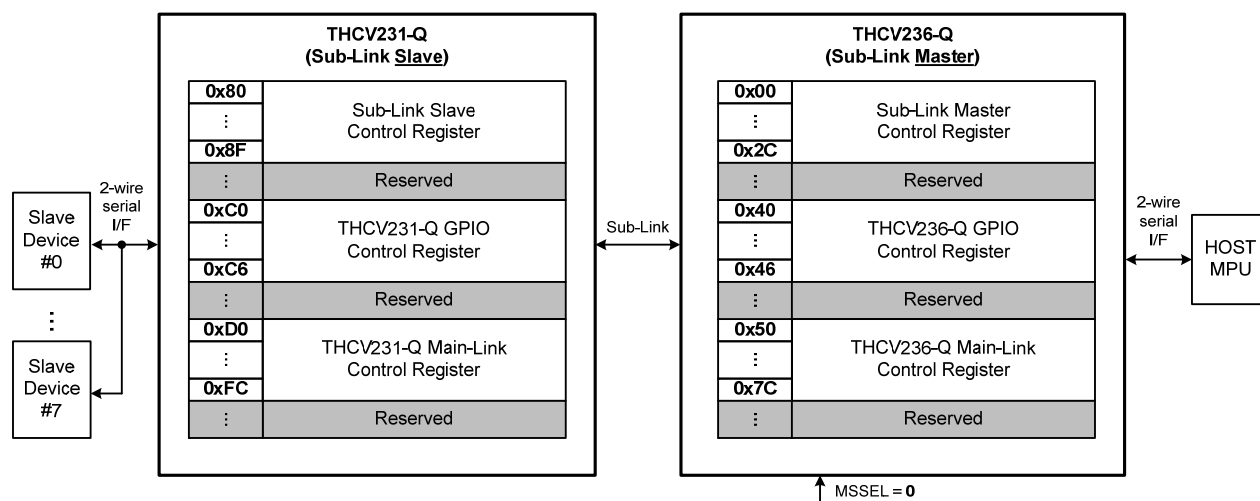


Figure 16. Sub-Link Master/Slave device Register Address configuration

Table 32. Sub-Link Master Control Register

Address (Hex)	Bit#	R/W	Default (Hex)	Register Name	Description	Note
0x00	7:3	R	0x00	Reserved		-
	2	R	0	INT	Interrupt condition 0: Steady state 1: Interrupt occurred(INT output =L)	-
	1	R	1	LOCKN	V-by-One®HS lock status 0: Locked (LOCKN=L) 1: Unlocked	-
	0	R	1	HTPDN	V-by-One®HS plug status 0: Connected (HTPDN=L) 1: Not connected or Rx inactive	-
0x01	7:1	R	0x00	Reserved		-
	0	RW	0	SFTRST	Sub-Link soft reset Write 1: Sub-Link reset Automatically cleared into 0 after reset action. 0 is always read.	-
0x02	7	RW	0	2WIRE_ACS_END_INT	Cause of interrupt access completion to register of Sub-Link Slave or Remote side 2-wire serial Slave device 0: Access incomplete 1: Access complete Any write action: clear this bit into 0	(*1)
	6	RW	0	LOCKN_INT	Cause of interrupt LOCKN 0: No change on lock status ever 1: Lock status has once changed Any write action: clear this bit into 0	
	5	RW	0	HTPDN_INT	Cause of interrupt HTPDN 0: No change on plug status ever 1: Plug status has once changed Any write action: clear this bit into 0	
	4	R	0	SLAVESIDE_INT	Cause of interrupt Sub-Link Slave side 0: No interrupt at Sub-Link Slave ever 1: Interrupted at Sub-Link Slave once This bit is cleared when cause of interrupt register at Sub-Link Slave (0x82) is cleared.	
	3	R	0	GPIO_INT	Cause of interrupt Sub-Link Master GPIO 0: No change in Master GPIO inputs ever 1: Master GPIO inputs have once changed. This bit is cleared when GPIO _n _INPUT_MONITOR (n=4~0) register (0x41) is read.	
	2	RW	0	COMERR_INT	Cause of interrupt Sub-Link communication Error 0: No communication error on Sub-Link ever 1: Communication error on Sub-Link once happened Any write action: clear this bit into 0	
	1	RW	0	2WIRE_TIMEOUT_INT	Cause of interrupt 2-wire serial time out 0: 2-wire serial access in time ever 1: 2-wire serial access has once had time out Any write action: clear this bit into 0	
	0	RW	0	SLINK_TIMEOUT_INT	Cause of interrupt Sub-Link time out 0: Sub-Link access in time ever 1: Sub-Link has once had time out Any write action: clear this bit into 0	
0x03	7	R	(*2)	2WIRE_ACS_END_INT_ENABLE	0: "2WIRE_ACS_END_INT" is blocked to take interrupt action 1: "2WIRE_ACS_END_INT" is allowed to take action on INT output	-
	6	RW	0	LOCKN_INT_ENABLE	0: "LOCKN_INT" is blocked to take interrupt action 1: "LOCKN_INT" is allowed to take action on INT output	-
	5	RW	0	HTPDN_INT_ENABLE	0: "HTPDN_INT" is blocked to take interrupt action 1: "HTPDN_INT" is allowed to take action on INT output	-
	4	RW	0	SLAVESIDE_INT_ENABLE	0: "SLAVESIDE_INT" is blocked to take interrupt action 1: "SLAVESIDE_INT" is allowed to take action on INT output	-
	3	RW	0	GPIO_INT_ENABLE	0: "GPIO_INT" is blocked to take interrupt action 1: "GPIO_INT" is allowed to take action on INT output	-
	2	RW	0	COMERR_INT_ENABLE	0: "COMERR_INT" is blocked to take interrupt action 1: "COMERR_INT" is allowed to take action on INT output	-
	1	RW	0	2WIRE_TIMEOUT_INT_ENABLE	0: "2WIRE_TIMEOUT_INT" is blocked to take interrupt action 1: "2WIRE_TIMEOUT_INT" is allowed to take action on INT output	-
	0	RW	0	SLINK_TIMEOUT_INT_ENABLE	0: "SLINK_TIMEOUT_INT" is blocked to take interrupt action 1: "SLINK_TIMEOUT_INT" is allowed to take action on INT output	-

*1 These registers are always active independent of Interrupt permission register.

*2 When No clock stretching mode, the value is 1 fixed, otherwise 0 fixed

Address (Hex)	Bit#	R/W	Default (Hex)	Register Name	Description	Note
0x04	7	RW	0	2WIRE_DEV_ADDR_0_ENABLE	0: Value in "2WIRE_DEV_ADDR_0" is inactive 1: Value in "2WIRE_DEV_ADDR_0" is active	(*3)
	6:0	RW	0x00	2WIRE_DEV_ADDR_0	Remote side 2-wire serial Slave Device Address #0	
0x05	7	RW	0	2WIRE_DEV_ADDR_1_ENABLE	0: Value in "2WIRE_DEV_ADDR_1" is inactive 1: Value in "2WIRE_DEV_ADDR_1" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_1	Remote side 2-wire serial Slave Device Address #1	
0x06	7	RW	0	2WIRE_DEV_ADDR_2_ENABLE	0: Value in "2WIRE_DEV_ADDR_2" is inactive 1: Value in "2WIRE_DEV_ADDR_2" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_2	Remote side 2-wire serial Slave Device Address #2	
0x07	7	RW	0	2WIRE_DEV_ADDR_3_ENABLE	0: Value in "2WIRE_DEV_ADDR_3" is inactive 1: Value in "2WIRE_DEV_ADDR_3" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_3	Remote side 2-wire serial Slave Device Address #3	
0x08	7	RW	0	2WIRE_DEV_ADDR_4_ENABLE	0: Value in "2WIRE_DEV_ADDR_4" is inactive 1: Value in "2WIRE_DEV_ADDR_4" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_4	Remote side 2-wire serial Slave Device Address #4	
0x09	7	RW	0	2WIRE_DEV_ADDR_5_ENABLE	0: Value in "2WIRE_DEV_ADDR_5" is inactive 1: Value in "2WIRE_DEV_ADDR_5" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_5	Remote side 2-wire serial Slave Device Address #5	
0x0A	7	RW	0	2WIRE_DEV_ADDR_6_ENABLE	0: Value in "2WIRE_DEV_ADDR_6" is inactive 1: Value in "2WIRE_DEV_ADDR_6" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_6	Remote side 2-wire serial Slave Device Address #6	
0x0B	7	RW	0	2WIRE_DEV_ADDR_7_ENABLE	0: Value in "2WIRE_DEV_ADDR_7" is inactive 1: Value in "2WIRE_DEV_ADDR_7" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_7	Remote side 2-wire serial Slave Device Address #7	
0x0C	7:0	RW	0x00	Reserved		-
0x0D	7:0	R	0x00	Reserved		-
0x0E	7:2	R	0x00	Reserved		-
	1:0	RW	0x0	Reserved. Must be 0		-
0x0F	7:2	R	0x00	Reserved		-
	1:0	RW	0x1	2WIRE_MODE	00: clock stretching mode 01: No clock stretching mode 10: Reserved (Forbidden) 11: Reserved (Forbidden)	-
0x10	7:0	RW	0x00	2WIRE_DATA0	2-wire serial I/F Write/Read Data #0	-
0x11	7:0	RW	0x00	2WIRE_DATA1	2-wire serial I/F Write/Read Data #1	-
0x12	7:0	RW	0x00	2WIRE_DATA2	2-wire serial I/F Write/Read Data #2	-
0x13	7:0	RW	0x00	2WIRE_DATA3	2-wire serial I/F Write/Read Data #3	-
0x14	7:0	RW	0x00	2WIRE_DATA4	2-wire serial I/F Write/Read Data #4	-
0x15	7:0	RW	0x00	2WIRE_DATA5	2-wire serial I/F Write/Read Data #5	-
0x16	7:0	RW	0x00	2WIRE_DATA6	2-wire serial I/F Write/Read Data #6	-
0x17	7:0	RW	0x00	2WIRE_DATA7	2-wire serial I/F Write/Read Data #7	-
0x18	7:0	RW	0x00	2WIRE_DATA8	2-wire serial I/F Write/Read Data #8	-
0x19	7:0	RW	0x00	2WIRE_DATA9	2-wire serial I/F Write/Read Data #9	-
0x1A	7:0	RW	0x00	2WIRE_DATA10	2-wire serial I/F Write/Read Data #10	-
0x1B	7:0	RW	0x00	2WIRE_DATA11	2-wire serial I/F Write/Read Data #11	-
0x1C	7:0	RW	0x00	2WIRE_DATA12	2-wire serial I/F Write/Read Data #12	-
0x1D	7:0	RW	0x00	2WIRE_DATA13	2-wire serial I/F Write/Read Data #13	-
0x1E	7:0	RW	0x00	2WIRE_DATA14	2-wire serial I/F Write/Read Data #14	-
0x1F	7:0	RW	0x00	2WIRE_DATA15	2-wire serial I/F Write/Read Data #15	-
0x20	7	RW	0	2WIRE_ADR_SEL	Remote side 2-wire Slave device's Register Address bit width select 0: 8bit Register Address 1: 16bit Register Address	-
	6:0	RW	0x00	2WIRE_TARGET_DEV_ADR	2-wire serial I/F Access Target Device Address setting	-
0x21	7:4	R	0x0	Reserved		-
	3:0	RW	0x0	WR_REQ_BYTE	2-wire serial I/F Write Request Byte Number for both 8bit and 16bit Register Address device. Byte Number = register value + 1 (e.g. 0x2 for 3byte burst)	-
0x22	7:4	R	0x0	Reserved		-
	3:0	RW	0x0	RD_REQ_BYTE	2-wire serial I/F Read Request Byte Number for both 8bit and 16bit Register Address device. Byte Number = register value + 1 (e.g. 0x2 for 3byte burst)	-
0x23	7:0	RW	0x00	WR_START_ADR_8B	2-wire serial I/F Write Start Register Address for 8bit Register Address device	-
0x24	7:0	RW	0x00	RD_START_ADR_8B	2-wire serial I/F Read Start Register Address for 8bit Register Address device	-
0x25	7:1	R	0x00	Reserved		-
	0	RW	0	WR_START_8B	2-wire serial I/F Write Access Start Trigger for 8bit Register Address device	-
0x26	7:1	R	0x00	Reserved		-
	0	RW	0	RD_START_8B	2-wire serial I/F Read Access Start Trigger for 8bit Register Address device	-
0x27	7:0	RW	0x00	WR_START_ADR_16B_0	2-wire serial I/F Write Start Register Address(Low-order bits = [7:0]) for 16bit Register Address device	-
0x28	7:0	RW	0x00	WR_START_ADR_16B_1	2-wire serial I/F Write Start Register Address(High-order bits = [15:8]) for 16bit Register Address device	-
0x29	7:0	RW	0x00	RD_START_ADR_16B_0	2-wire serial I/F Read Start Register Address(Low-order bits = [7:0]) for 16bit Register Address device	-
0x2A	7:0	RW	0x00	RD_START_ADR_16B_1	2-wire serial I/F Read Start Register Address(High-order bits = [15:8]) for 16bit Register Address device	-
0x2B	7:1	R	0x00	Reserved		-
	0	RW	0	WT_START_16B	2-wire serial I/F Write Access Start Trigger for 16bit Register Address device	-
0x2C	7:1	R	0x00	Reserved		-
	0	RW	0	RD_START_16B	2-wire serial I/F Read Access Start Trigger for 16bit Register Address device	-
0x2D-0x3F	7:0	R	0x00	Reserved		-

*3 Assignment of 2-wire serial slave device address connected to Sub-Link Slave outside

Table 33. Sub-Link Slave Control Register

Address (Hex)	Bit#	R/W	Default (Hex)	Name	Description	Note
0x80	7:0	R	0x00	Reserved		-
	7:1	R	0x00	Reserved		-
0x81	0	RW	0	2WIRE_RST	2-wire serial I/F reset Write 1: 16 pulse SCL signal is sent to 2-wire serial slave device connected to Sub-Link Slave. This bit is a remedy against SDA=L, 2-wire serial stuck condition. Automatically cleared into 0 after reset action. 0 is always read.	-
0x82	7:6	R	0x0	Reserved		-
	5	RW	0	2WIRE_RST_END_INT	Cause of interrupt 2-wire serial reset done 0: Normal operation 1: 2-wire serial reset signal has all finished Any write action: clear this bit into 0	-
	4	RW	0	2WIRE_NACK_INT	Cause of interrupt 2-wire serial Slave NACK 0: No NACK from remote side 2-wire serial slave ever 1: NACK from remote side 2-wire serial slave once come Any write action: clear this bit into 0	-
	3	R	0	GPIO_INT	Cause of interrupt Sub-Link Slave GPIO 0: No change in Slave GPIO inputs ever 1: Slave GPIO inputs have once changed. This bit is cleared when GPIO _n _INPUT_MONITOR (n=4,3) register (0xC1) is read.	-
	2	RW	0	COMERR_INT	Cause of interrupt Sub-Link communication Error 0: No communication error on Sub-Link ever 1: Communication error on Sub-Link once happened Any write action: clear this bit into 0	-
	1	RW	0	2WIRE_TIMEOUT_INT	Cause of interrupt 2-wire serial time out 0: 2-wire serial access in time ever 1: 2-wire serial access has once had time out Any write action: clear this bit into 0	-
	0	RW	0	SLINK_TIMEOUT_INT	Cause of interrupt Sub-Link time out: Sub-Link access in time ever 1: Sub-Link has once had time out Any write action: clear this bit into 0	-
0x83	7:6	R	0x0	Reserved		-
	5	RW	0	2WIRE_RST_ENABLED_INT_ENABLE	0: "2WIRE_RST_END_INT" is blocked to be reported to Master Side. 1: "2WIRE_RST_END_INT" is allowed to be reported to Master Side.	(*1)
	4	RW	0	2WIRE_NACK_INT_ENABLE	0: "2WIRE_NACK_INT" is blocked to be reported to Master Side. 1: "2WIRE_NACK_INT" is allowed to be reported to Master Side.	
	3	RW	0	GPIO_INT_ENABLE	0: "GPIO_INT" is blocked to be reported to Master Side. 1: "GPIO_INT" is allowed to be reported to Master Side.	
	2	RW	0	COMERR_INT_ENABLE	0: "COMERR_INT" is blocked to be reported to Master Side. 1: "COMERR_INT" is allowed to be reported to Master Side.	
	1	RW	0	2WIRE_TIMEOUT_INT_ENABLE	0: "2WIRE_TIMEOUT_INT" is blocked to be reported to Master Side. 1: "2WIRE_TIMEOUT_INT" is allowed to be reported to Master Side.	
	0	RW	0	SLINK_TIMEOUT_INT_ENABLE	0: "SLINK_TIMEOUT_INT" is blocked to be reported to Master Side. 1: "SLINK_TIMEOUT_INT" is allowed to be reported to Master Side.	
0x84-0x8B	7:0	R	0x00	Reserved		-
0x8C	7	R	0	Reserved		-
	6:0	RW	0x2D	SCL_W_H	SCL High width [t_{HIGH}] setting. Output SCL High width is defined as below. $((SCL_W_H + 1) * 8 + 8) * t_{OSC}$	-
0x8D	7	R	0	Reserved		-
	6:0	RW	0x37	SCL_W_L	SCL Low width [t_{LOW}] setting. Output SCL Low width is defined as below. $((SCL_W_L + 1) * 8 + 8) * t_{OSC}$	-
0x8E	7:2	R	0x00	Reserved		-
	1:0	RW	0x0	Reserved. Must be 0		-
0x8F	7:2	R	0x00	Reserved		-
	1:0	RW	0x1	Reserved		-
0x90-0xBF	7:0	R	0x00	Reserved		-

*1 Interrupt signal from Sub-Link Slave is reported to Sub-Link Master as Cause of interrupt Sub-Link Slave Side (0x02 bit4 SLAVESIDE_INT).

Table 34. THCV231-Q GPIO Control Register Map

Address (Hex) Sub-Link Slave	Bit#	R/W	Default t (Hex)	Name	Description	Note
0xC0	7:5	R	0x0		Reserved	-
	4	RW	1	GPIO4_TYPE	GPIO4 type select 0: Programmable GPIO 1: Through GPIO	-
	3	RW	1	GPIO3_TYPE	GPIO3 type select 0: Programmable GPIO 1: Through GPIO	-
	2:0	R	0x0		Reserved	-
0xC1	7:5	R	0x0		Reserved	-
	4	R	0	GPIO4_INPUT_MONITOR	GPIO4 input value	(*1)
	3	R	0	GPIO3_INPUT_MONITOR	GPIO3 input value	
	2:0	R	0x0		Reserved	-
0xC2	7:5	R	0x0		Reserved	-
	4	RW	0	GPIO4_OUT	GPIO4 output value setting	(*2)
	3	RW	0	GPIO3_OUT	GPIO3 output value setting	
	2:0	RW	0x0		Reserved	-
0xC3	7:5	R	0x0		Reserved	-
	4:3	RW	0x0	GPIO_IO_SEL	GPIO input/output direction setting See Table 28, Table 29 and Table 30	-
	2:0	RW	0x7		Reserved	-
	7:5	R	0x0		Reserved	-
0xC4	4	RW	1	GPIO4_FILT_ENABLE	GPIO4 input filter enable 0: Disable 1: Enable	(*3)
	3	RW	1	GPIO3_FILT_ENABLE	GPIO3 input filter enable 0: Disable 1: Enable	
	2:0	RW	0x7		Reserved	-
	7:5	R	0x0		Reserved	-
0xC5	7:5	R	0x0		Reserved	-
	4	RW	1	GPIO4_INT_ENABLE	GPIO4 interrupt enable 0: Disable 1: Enable	(*4)
	3	RW	1	GPIO3_INT_ENABLE	GPIO3 interrupt enable 0: Disable 1: Enable	
	2:0	RW	0x7		Reserved	-
0xC6	7:5	R	0x0		Reserved	-
	4	RW	0	GPIO4_OUTBUF_SEL	GPIO4 output buffer select 0: GPIO4 is open-drain output 1: GPIO4 is push pull output	-
	3	RW	0	GPIO3_OUTBUF_SEL	GPIO3 output buffer select 0: GPIO3 is open-drain output 1: GPIO3 is push pull output	-
	2:0	RW	0x0		Reserved	-
0xC7-0xCF	7:0	R	0x00		Reserved	-

*1 Active only when GPIO is set as input port.

*2 Active only when GPIO type is set as "Programmable GPIO" and set as output port.

*3 Filter eliminates input glitch shorter than $t_{osc}/2$.

*4 GPIO input transition is counted as GPIO_INT(0x82 bit3).

Table 35. THCV231-Q Main-Link Control Register Map

Address (Hex) Sub-Link Slave	Bit#	R/W	Default (Hex)	Name	Description	Note
0xD0	7	RW	1	MAINMODE	MAINMODE setting 0: Forbidden 1: Sync Free Mode	-
	6	RW	1	HFSEL	HFSEL setting 0: High Frequency Mode Disable 1: High Frequency Mode Enable	-
	5	RW	0	COL1	COL1 setting Data Width Setting. See Table 16.	-
	4	RW	1	COL0	COL0 setting Data Width Setting. See Table 16.	-
	3	RW	0	PRE	PRE setting 0: Pre-Emphasis Disable 1: Pre-Emphasis Enable	(*1)
	2:1	RW	0x2	CMLDRV	CMLDRV setting 00: 400mV diff p-p 01: 600mV diff p-p 10: 800mV diff p-p 11: Reserved (Forbidden)	
	0	RW	0	Reserved		-
0xD1	7:6	R	0x0	Reserved		-
	5	RW	0	SSEN	SSEN setting 0: SSCG Disable 1: SSCG Enable	(*2)
	4:0	RW	0x05	SPREAD	SSCG modulation depth setting Spread depth = $\pm$ SPREAD x 0.1% (Center Spread)	
0xD2	7:4	R	0x0	Reserved		-
	3:0	RW	0xD	FMOD	SSCG Modulation Frequency Setting	-
0xD3	7:2	R	0x00	Reserved		-
	1	RW	0	BET	Field BET Mode Enable setting 0: Normal Mode 1: Field BET Operation	-
	0	RW	0	BET_SEL	Main-Link / Sub-Link Field BET Mode select 0: Main-Link Field BET Mode 1: Sub-Link Field BET Mode	-
0xD4	7	R	0	Reserved		-
	6:0	RW	0x3E	Reserved. Must be default setting.		-
0xD5-0xEC	7:0	RW	0x00	Reserved		-
0xED	7:3	R	0x00	Reserved		-
	2:0	RW	0x1	Reserved		-
0xEE	7:1	R	0x00	Reserved		-
	0	RW	1	Reserved. Must be 1		-
0xEF	7:0	R	0x00	Reserved		-
0xF0	7:2	R	0x00	Reserved		-
	1	RW	0	Reserved. Must be 0		-
	0	RW	0	PLL_SET_EN	SSCG PLL setting register Enable 1: Enable 0: Disable	-
0xF1-0xF5	7:0	R	0x00	Reserved		-
0xF6	7:6	R	0x0	Reserved		-
	5:0	RW	0xFF	PLL_SET0	SSCG PLL setting	(*3)
0xF7	7:4	R	0x0	Reserved		-
	3:0	RW	0x0	Reserved. Must be default setting.		-
0xF8	7:0	RW	0xFF	PLL_SET1	SSCG PLL setting	(*3)
0xF9-0xFB	7:0	RW	0x00	Reserved. Must be default setting.		-
0xFC	7:6	R	0x0	Reserved		-
	5:0	RW	0xFF	PLL_SET2	SSCG PLL setting	(*3)
0xFD-0xFF	7:0	RW	0xFF	Reserved. Must be default setting.		-

*1 See Table 4

*2 SSEN=1 and SPREAD=0 setting is forbidden

*3 See Table 8, Table 17

Table 36. THCV236-Q GPIO Control Register Map

Address (Hex) Sub-Link Master	Bit#	R/W	Default (Hex)	Name	Description	Note
0x40	7:5	R	0x0		Reserved	-
	4	RW	1	GPIO4_TYPE	GPIO4 type select 0: Programmable GPIO 1: Through GPIO	-
	3	RW	1	GPIO3_TYPE	GPIO3 type select 0: Programmable GPIO 1: Through GPIO	-
	2	R	0	GPIO2_TYPE	GPIO2 type select 0: Programmable GPIO 0 Fix	-
	1	R	0	GPIO1_TYPE	GPIO1 type select 0: Programmable GPIO 0 Fix	-
	0	R	0	GPIO0_TYPE	GPIO0 type select 0: Programmable GPIO 0 Fix	-
0x41	7:5	R	0x0		Reserved	-
	4	R	0	GPIO4_INPUT_MONITOR	GPIO4 input value	(*1)
	3	R	0	GPIO3_INPUT_MONITOR	GPIO3 input value	
	2	R	0	GPIO2_INPUT_MONITOR	GPIO2 input value	
	1	R	0	GPIO1_INPUT_MONITOR	GPIO1 input value	
	0	R	0	GPIO0_INPUT_MONITOR	GPIO0 input value	
0x42	7:5	R	0x0		Reserved	-
	4	RW	0	GPIO4_OUT	GPIO4 output value setting	(*2)
	3	RW	0	GPIO3_OUT	GPIO3 output value setting	
	2	RW	0	GPIO2_OUT	GPIO2 output value setting	
	1	RW	0	GPIO1_OUT	GPIO1 output value setting	
	0	RW	0	GPIO0_OUT	GPIO0 output value setting	
0x43	7:5	R	0x0		Reserved	-
	4	RW	(*3)	GPIO_IO_SEL	GPIO input/output direction setting See Table 28, Table 29 and Table 30	-
	3	RW	(*3)			
	2:0	RW	0x7			
0x44	7:5	R	0x0		Reserved	-
	4	RW	1	GPIO4_FILTER_ENABLE	GPIO4 input filter enable 0: Disable 1: Enable	(*4)
	3	RW	1	GPIO3_FILTER_ENABLE	GPIO3 input filter enable 0: Disable 1: Enable	
	2	RW	1	GPIO2_FILTER_ENABLE	GPIO2 input filter enable 0: Disable 1: Enable	
	1	RW	1	GPIO1_FILTER_ENABLE	GPIO1 input filter enable 0: Disable 1: Enable	
	0	RW	1	GPIO0_FILTER_ENABLE	GPIO0 input filter enable 0: Disable 1: Enable	
0x45	7:5	R	0x0		Reserved	-
	4	RW	1	GPIO4_INT_ENABLE	GPIO4 interrupt enable 0: Disable 1: Enable	(*5)
	3	RW	1	GPIO3_INT_ENABLE	GPIO3 interrupt enable 0: Disable 1: Enable	
	2	RW	1	GPIO2_INT_ENABLE	GPIO2 interrupt enable 0: Disable 1: Enable	
	1	RW	1	GPIO1_INT_ENABLE	GPIO1 interrupt enable 0: Disable 1: Enable	
	0	RW	1	GPIO0_INT_ENABLE	GPIO0 interrupt enable 0: Disable 1: Enable	

*1 Active only when GPIO is set as input port.

*2 Active only when GPIO type is set as "Programmable GPIO" and set as output port.

*3 Default value depends on RXDEFSEL setting when Power on sequence. RXDEFSEL=1 → default value is 0, RXDEFSEL=0 → default value is 1.

*4 Filter eliminates input glitch shorter than $t_{osc}/2$.

*5 GPIO input transition is counted as GPIO_INT(0x02 bit3).

Address (Hex) Sub-Link Master	Bit#	R/W	Default (Hex)	Name	Description	Note
0x46	7:5	R	0x0		Reserved	-
	4	RW	0	GPIO4_OUTBUF_SEL	GPIO4 output buffer select 0: GPIO4 is open-drain output 1: GPIO4 is push pull output	-
	3	RW	0	GPIO3_OUTBUF_SEL	GPIO3 output buffer select 0: GPIO3 is open-drain output 1: GPIO3 is push pull output	-
	2	RW	0	GPIO2_OUTBUF_SEL	GPIO2 output buffer select 0: GPIO2 is open-drain output 1: GPIO2 is push pull output	-
	1	RW	0	GPIO1_OUTBUF_SEL	GPIO1 output buffer select 0: GPIO1 is open-drain output 1: GPIO1 is push pull output	-
	0	RW	0	GPIO0_OUTBUF_SEL	GPIO0 output buffer select 0: GPIO0 is open-drain output 1: GPIO0 is push pull output	-
0x47 -0x4F	7:0	R	0x00		Reserved	-

Table 37. THCV236-Q Main-Link Control Register Map

Address (Hex)	Bit#	R/W	Default (Hex)	Name	Description	Note
0x50	7	RW	(*1)	MAINMODE	MAINMODE setting 0: V-by-One® HS Mode 1: Sync Free Mode	-
	6	RW	(*1)	HFSEL	HFSEL setting 0: High Frequency Mode Disable 1: High Frequency Mode Enable	-
	5	RW	0	COL1	COL1 setting when MAINMODE =0 0: Color Space Converter Disable 1: Color Space Converter Enable when MAINMODE =1 Data Width Setting. See Table 16.	-
	4	RW	(*1)	COL0	COL0 setting Data Width Setting. See Table 16.	-
	3	RW	0	Reserved		-
	2:1	RW	0x0	Reserved		-
	0	RW	0	TTLDRV	TTLDRV setting 0: Weak Drive Strength 1: Normal Drive Strength	-
0x51	7:6	R	0x0	Reserved		-
	5	RW	0	SSEN	SSEN setting 0: SSCG Disable 1: SSCG Enable	(*2)
	4:0	RW	0x05	SPREAD	SSCG modulation depth setting Spread depth = $\pm \text{SPREAD} \times 0.1\%$ (Center Spread)	
0x52	7:4	R	0x0	Reserved		-
	3:0	RW	0xD	FMOD	SSCG Modulation Frequency Setting	-
0x53	7:2	R	0x00	Reserved		-
	1	RW	0	Reserved		-
	0	RW	0	BET_SEL	Main-Link / Sub-Link Field BET Mode select 0: Main-Link Field BET Mode 1: Sub-Link Field BET Mode	-
	7	R	0	Reserved		-
0x54	6:0	RW	0x3E	Reserved. Must be default setting.		-
	7:0	RW	0x0	Reserved		-
0x55 -0x6C	7:0	RW	0x0	Reserved		-
0x6D	7:3	R	0x00	Reserved		-
	2	RW	0	OUTSEL_ENABLE	Permanent Clock Output Enable setting 0: Permanent Clock Output Disable 1: Permanent Clock Output Enable	-
	1:0	RW	0x1	OUTSEL_SETTING	Permanent Clock Frequency setting 00: 80MHz (Clock Period : t_{OSC}) 01: 40MHz (Clock Period : $t_{OSC}/2$) 10: 20MHz (Clock Period : $t_{OSC}/4$) 11: 10MHz (Clock Period : $t_{OSC}/8$)	(*3)
0x6E	7:1	R	0x00	Reserved		-
	0	RW	1	Reserved. Must be 1		-
0x6F	7:0	R	0x00	Reserved		-
0x70	7:2	R	0x00	Reserved		-
	1	RW	0	Reserved. Must be 0		-
	0	RW	0	PLL_SET_EN	SSCG PLL setting register Enable 1: Enable 0: Disable	-
0x71 -0x75	7:0	R	0x00	Reserved		-
0x76	7:6	R	0x0	Reserved		-
	5:0	RW	0x00	PLL_SET0	SSCG PLL setting	(*4)
0x77	7:4	R	0x0	Reserved		-
	3:0	RW	0x0	Reserved. Must be default setting.		-
0x78	7:0	RW	0xFF	PLL_SET1	SSCG PLL setting	(*4)
0x79 -0x7B	7:0	R	0x00	Reserved. Must be default setting.		-
0x7C	7:6	R	0x0	Reserved		-
	5:0	RW	0xFF	PLL_SET2	SSCG PLL setting	(*4)
0x7D -0x7F	7:0	R	0xFF	Reserved. Must be default setting.		-

*1 Default value depends on RXDEFSEL setting when Power on sequence. RXDEFSEL=1 → default value is 0, RXDEFSEL=0 → default value is 1.

*2 SSEN=1 and SPREAD=0 setting is forbidden

*3 Described value is typical value. It has variation in the range from min spec value to max spec value of t_{OSC} .

*4 See Table 8, Table 17

Absolute Maximum Ratings

Table 38. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage(VDD,AVDD)	-0.3	-	4.0	V
LVC MOS Input Voltage	-0.3	-	VDD+0.3	V
LVC MOS Output Voltage	-0.3	-	VDD+0.3	V
LVC MOS Bi-directional buffer Input Voltage	-0.3	-	VDD+0.3	V
LVC MOS Bi-directional buffer Output Voltage	-0.3	-	VDD+0.3	V
Open-Drain Output Voltage	-0.3	-	4.0	V
CML Receiver Input Voltage	-0.3	-	CAPINA+0.3	V
CML Transmitter Output Voltage	-0.3	-	CAPINA+0.3	V
CML Bi-directional buffer Input Voltage	-0.3	-	VDD+0.3	V
CML Bi-directional buffer Output Voltage	-0.3	-	VDD+0.3	V
Output Current	-50	-	50	mA
Storage temperature	-55	-	125	°C
Junction temperature	-	-	125	°C
Reflow Peak Temperature/Time	-	-	260/10	°C/sec
Maximum Power Dissipation THCV231-Q@+25°C	-	-	3.2	W
Maximum Power Dissipation THCV236-Q@+25°C	-	-	4.0	W

Recommended Operating Conditions

Table 39. Recommended Operating Condition

Parameter	Min	Typ	Max	Unit
Supply Voltage(VDD,AVDD)	1.7	-	3.6	V
Operating Temperature	-40	-	105	°C

Electrical Specification

LVC MOS DC Specification

Table 40. LVC MOS DC Specification

Symbol	Parameter	Pin Type	Condition	Min	Typ	Max	Unit
VIH	High Level Input Voltage	I	VDD=1.7-2.0V	0.65×VDD	-	VDD	V
			VDD=2.0-3.0V	0.70×VDD	-	VDD	V
			VDD=3.0-3.6V	2.0	-	VDD	V
		IL,B	VDD=1.7-3.6V	0.70×VDD	-	VDD	V
VIL	Low Level Input Voltage	I	VDD=1.7-2.0V	0	-	0.35×VDD	V
			VDD=2.0-3.0V	0	-	0.30×VDD	V
			VDD=3.0-3.6V	0	-	0.8	V
		IL,B	VDD=1.7-3.6V	0	-	0.30×VDD	V
VOH	High Level Output Voltage	O,B	VDD=1.7-3.6V IOH=-4mA	VDD-0.45	-	VDD	V
VOL	Low Level Output Voltage	O,B	VDD=1.7-3.6V IOL=4mA	0	-	0.45	V
		BO	VDD=1.7-3.6V IOL=2mA	0	-	0.2	V
IIH	Input Leak Current High	I,IL	VIN=VDD	-	-	10	uA
IIL	Input Leak Current Low	I,IL	VIN=0V	-10	-	-	uA
IOZH	Output Leak Current High in Hi-Z State	O,B,BO	VIN=VDD	-	-	10	uA
IOZL	Output Leak Current Low in Hi-Z State	O,B,BO	VIN=0V	-10	-	10	uA

CML DC Specification

Table 41. CML DC Specification(THCV231-Q)

Symbol	Parameter	Condition(*1)	Min	Typ	Max	Unit
VTOD	CML Differential Output Voltage	CMLDRV[1:0]=00	133	200	267	mV
		CMLDRV[1:0]=01	200	300	400	mV
		CMLDRV[1:0]=10	300	400	500	mV
PRE	CML Pre-emphasis Level	PRE=0	-	0	-	%
		PRE=1,CMLDRV[1:0]=00	-	100	-	%
		PRE=1,CMLDRV[1:0]=01	-	50	-	%
VTOC	CML Common Mode Output Voltage	PRE=0	CAPINA-VTOD			mV
		PRE=1,CMLDRV[1:0]=00	CAPINA-2×VTOD			mV
		PRE=1,CMLDRV[1:0]=01	CAPINA-1.5×VTOD			mV
ITOH	CML Output Leak Current High	PDN=0,TXP/N=CAPINA	-30	-	30	uA
ITOS	CML Output Short Current	PDN=0,TXP/N=0V	-80	-	-	mA

*1 PRE and CMLDRV[1:0] are registers.

Table 42. CML DC Specification(THCV236-Q)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input Low Threshold	-	-50	-	-	mV
IRIH	CML Input Leak Current High	PDN0=0,RXP/N=CAPINA	-10	-	10	uA
IRIL	CML Input Leak Current Low	PDN0=0,RXP/N=0V	-10	-	10	uA
IRRIH	CML Input Current High	RXP/N=CAPINA	-	-	2	mA
IRRIL	CML Input Current Low	RXP/N=0V	-6	-	-	mA
RRIN	CML Differential Input Resistance	-	80	100	120	Ω

CML Bi-Directional DC Specification

Table 43. CML Bi-Directional DC Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBTH	Bi-Directional Buffer Differential Input High Threshold	-	-	-	150	mV
VBTL	Bi-Directional Buffer Differential Input Low Threshold	-	-150	-	-	mV
IBIH	Bi-Directional Buffer Output Leak Current High	xCMP/N=VDD(x=T,R)	-10	-	10	uA
IBIL	Bi-Directional Buffer Output Leak Current Low	xCMP/N=0V(x=T,R)	-10	-	10	uA
RTERM	Bi-Directional Buffer Termination Resistance	Transmitter State	37.5	50	62.5	Ω
		Receiver State	150	200	250	Ω
VBOD	Bi-Directional Buffer Differential Output Voltage	RDIFF=400Ω	300	-	660	mV
VBOC	Bi-Directional Buffer Common Output Voltage	-	-	VDD-0.3	-	V
IBOZ	Bi-Directional Buffer TRI-STATE Current	PDN=0(THCV231-Q) PDN1=0(THCV236-Q)	-10	-	10	uA

Supply Current

Table 44. Supply Current(THCV231-Q)

Symbol	Parameter	Condition(*1)	Min	Typ	Max	Unit
ITCCW	Transmitter Supply Current	PDN=1, HFSEL=1	-	-	115	mA
ITCCS	Transmitter Power Down Supply Current	PDN = 0 All Inputs = Fixed 0 or 1 Typical value is under 25 °C	-	2.5	20	mA

*1 HFSEL is a register.

Table 45. Supply Current(THCV236-Q)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IRCCW	Receiver Supply Current	Cload=8pF, PDN0=1,PDN1=1,HFSEL=1	-	-	220	mA
IRCCS	Receiver Power Down Supply Current	PDN0 = 0 and PDN1 =0 All Inputs = Fixed 0 or 1 Typical value is under 25 °C	-	2.5	20	mA

Switching Characteristics

Table 46. Switching Characteristics (THCV231-Q)

Symbol	Parameter	Condition(*1)	Min	Typ	Max	Unit
tTRF	CML Output Rise and Fall Time (20%-80%)	-	50	-	150	ps
tTCIP	CLKIN Period	See Table 16	1000/Freq.Range[MHz]			ns
tTCH	CLKIN High Time	-	0.35×tTCIP	0.5×tTCIP	0.65×tTCIP	ns
tTCL	CLKIN Low Time	-	0.35×tTCIP	0.5×tTCIP	0.65×tTCIP	ns
tTS	Data Input Setup to CLKIN	-	2.0	-	-	ns
tTH	Data Input Hold to CLKIN	-	1.0	-	-	ns
tTPD	Power On to PDN High Delay	-	0	-	-	ns
tTCD	Input Clock to Output Data Delay	MAINMODE=1, HFSEL=0	56×tTCIP	-	65×tTCIP	ns
		MAINMODE=1, HFSEL=1	109×tTCIP	-	132×tTCIP	ns
tTPLL0	PDN High to CML Output Delay	-	-	-	10	ms
tTPLL1	PDN Low to CML Output High Fix Delay	-	-	-	20	ns
tTNP0	LOCKN High to Training Pattern Output Delay	-	-	-	10	ms
tTNP1	LOCKN Low to Data Pattern Output Delay	-	-	-	10	ms

*1 MAINMODE and HFSEL are registers.

Table 47. Switching Characteristics (THCV236-Q)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tRBIT	Unit Interval	-	250	-	1666	ps
tRCP	CLKOUT Period	See Table 16	1000/Freq.Range[MHz]			ns
tRCH	CLKOUT High Time	-	-	tRCP/2	-	ns
tRCL	CLKOUT Low Time	-	-	tRCP/2	-	ns
tDOUT	Data Output Period	-	-	tRCP	-	ns
tRPD	Power On to PDN0 High Delay	-	0	-	-	ns
tRDC	Input Data to Output Clock Delay	MAINMODE=1,HFSEL=0	61×tRCP	-	70×tRCP	ns
		MAINMODE=1,HFSEL=1	116×tRCP	-	140×tRCP	ns
tRHPD0	PDN0 High to HTPDN Low Delay	-	-	-	10	ms
tRHPD1	PDN0 Low to HTPDN High Delay	-	-	-	50	us
tRPLL0	Training Pattern Input to LOCKN Low Delay	-	-	-	10	ms
tRPLL1	PDN0 Low to LOCKN High Delay	-	-	-	10	us
tRLCK0	LOCKN Low to Data Output Delay	-	-	-	5	ms
tRLCK1	LOCKN High to Data Output Stop Delay	-	-	-	10	us
tROSC0	PDN0 High to Permanent Clock output Delay	OUTSEL=1	-	-	5	ms
tROSC1	LOCKN Low to Permanent Clock output Low Delay	OUTSEL=1	-	-	1	ms
tROSC2	LOCKN High to Permanent Clock output Delay	OUTSEL=1	-	-	10	us
tRS	Data Output Setup to CLKOUT	-	0.45×tRCP-0.65	-	-	ns
tRH	Data Output Hold to CLKOUT	-	0.45×tRCP-0.65	-	-	ns
tTLH	Clock, Data Output Low to High Transition Time	Clock , TTLDRV=0	-	-	2.0	ns
		Data , TTLDRV=0	-	-	3.5	ns
		Clock , TTLDRV=1	-	-	0.8	ns
		Data , TTLDRV=1	-	-	1.9	ns
tTHL	Clock, Data Output High to Low Transition Time	Clock , TTLDRV=0	-	-	2.4	ns
		Data , TTLDRV=0	-	-	4.4	ns
		Clock , TTLDRV=1	-	-	1.0	ns
		Data , TTLDRV=1	-	-	2.2	ns

Table 48. CML Bi-Directional Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tBUI	Bi-Directional Buffer Unit Interval	-	80	100	120	ns
tBRF	Bi-Directional Buffer Rise and Fall Time(20%-80%)	-	150	-	1000	ps
tBPJTX	Bi-Directional Buffer Transmitter Period Jitter Accuracy (peak to peak)	-	-	-	1	ns
tBPJRX	Bi-Directional Buffer Receiver Period Jitter Tolerance (peak to peak)	-	8	-	-	ns

Table 49. 2-wire serial slave AC Timing (Sub-Link Master device)

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL clock frequency	-	-	400	kHz
t _{HD;STA}	Hold time (repeated) START condition	0.6	-	-	us
t _{LOW}	LOW period of the SCL clock	1.3	-	-	us
t _{HIGH}	HIGH period of the SCL clock	0.6	-	-	us
t _{HD;DAT}	Data hold time: output	-	9×t _{osc}	-	us
	Data hold time: input	20	-	-	ns
t _{SU;DAT}	Data setup time: output	500	-	-	ns
	Data setup time: input	100	-	-	ns
t _r	Rise time of both SDA and SCL signals	-	-	300(*1)	ns
t _f	Fall time of both SDA and SCL signals (pull-up resistor:2.5kΩ,bus capacitance:400pF)	-	-	300	ns
t _{SU;STO}	Setup time for STOP condition	0.6	-	-	ns
t _{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
t _{SP}	Pulse width of spikes which must be suppressed by the input filter	-	-	50	ns
t _{PDS}	Required wait time from PDN1 high to START condition	2	-	-	ms

*1 Please adjust Pull-up resistor and bus capacitance to meet the spec value.

Table 50. 2-wire serial master AC Timing (Sub-Link Slave device)

Symbol	Parameter	Min	Typ	Max	Unit
t _{osc}	Cycle of internal oscillator clock	10.417	12.5	15.625	ns
t _{HD;STA}	Hold time (repeated) START condition	-	(SCL_W_H × 8 – 3) × t _{osc}	-	us
t _{LOW}	LOW period of the SCL clock	-	((SCL_W_L + 1) × 8 + 8) × t _{osc}	-	us
t _{HIGH}	HIGH period of the SCL clock	-	((SCL_W_H + 1) × 8 + 8) × t _{osc}	-	us
t _{HD;DAT}	Data hold time: output	-	9×t _{osc}	-	us
	Data hold time: input	20	-	-	ns
t _{SU;DAT}	Data setup time: output	31×t _{osc}	-	-	ns
	Data setup time: input	100	-	-	ns
t _r	Rise time of both SDA and SCL signals	-	-	300(*1)	ns
t _f	Fall time of both SDA and SCL signals (pull-up resistor:2.5kΩ, bus capacitance:400pF)	-	-	300	ns
t _{SU;STO}	Setup time for STOP condition	-	386×t _{osc}	-	ns
t _{BUF}	Bus free time between a STOP and START condition	4.7	-	-	us

*1 Please adjust Pull-up resistor and bus capacitance to meet the spec value.

Table 51. 2-wire serial interface transaction wait time

Symbol	Parameter	Min	Typ	Max	Unit
t _{WSSR}	Write access completion time to Sub-Link Slave register	-	-	110	us
t _{RSSR}	Read access completion time to Sub-Link Slave register	-	-	90	us
t _{WRS}	Write start to Remote side Start Condition generating time	-	-	65	us
t _{RPW}	Remote side Stop Condition generating to Write access completion time	-	-	300	us
t _{RRS}	Read start to Remote side Start Condition generating time	-	-	65	us
t _{RPR}	Remote side Stop Condition generating to Read access completion time	-	-	300	us
t _{SSEP}	Sub-Link Slave External processing time	Depending on characteristics of 2-wire serial slave devices connected to Sub-Link Slave			us

Table 52. Sub-Link control switching characteristics (2-wire serial I/F Mode)

Symbol	Parameter	Min	Typ	Max	Unit
t _{PVM}	Programmable GPIO output at Sub-Link Master data valid	-	-	0	us
t _{PVS}	Programmable GPIO output at Sub-Link Slave data valid	-	-	110	us
t _{TGPIO}	Through GPIO delay	-	-	280	us
t _{IVM}	Sub-Link Master interrupt valid	-	-	90	us
t _{IRM}	Sub-Link Master interrupt reset delay	-	-	0	us
t _{IVS}	Sub-Link Slave interrupt valid	-	-	300	us
t _{IRS}	Sub-Link Slave interrupt reset delay	2WIRE_MODE=00	-	300	us
		2WIRE_MODE=01	-	0	us
t _{PS}	Programmable GPIO input data setup	10000×(1/f _{SCL})	-	-	us
t _{PH}	Programmable GPIO input data hold	0	-	-	us

AC Timing Diagrams and Test Circuits

LVC MOS Input, Output Switching Characteristics

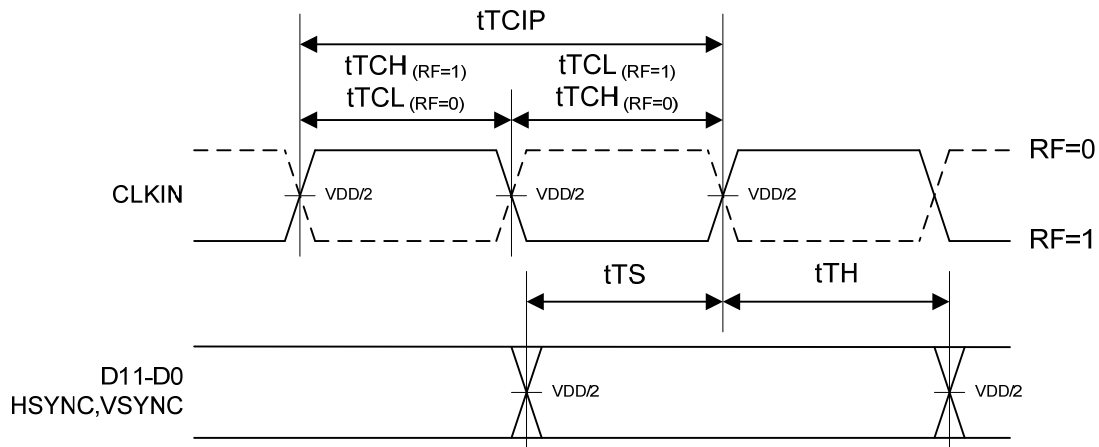


Figure 17. LVC MOS Input Switching Timing Diagrams

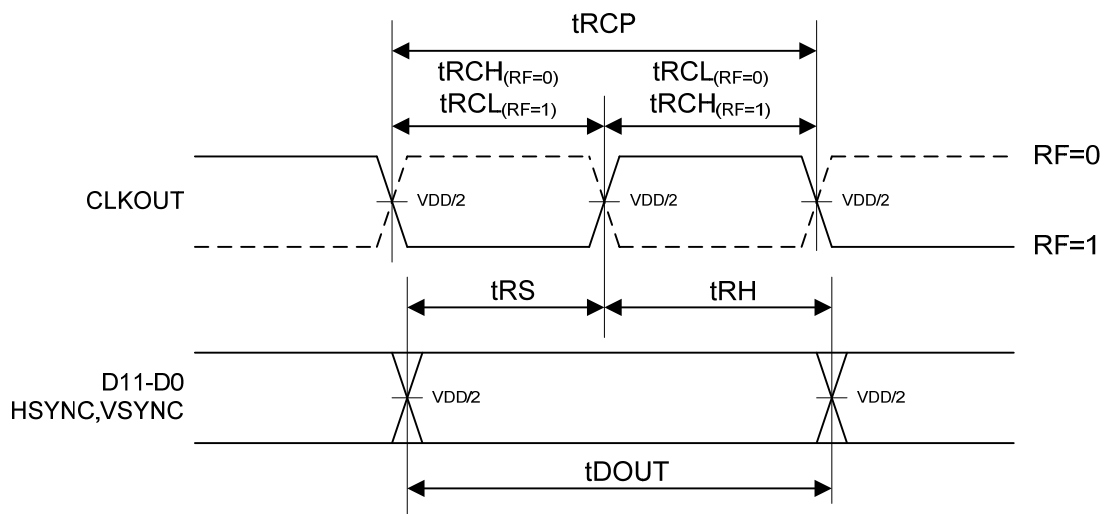
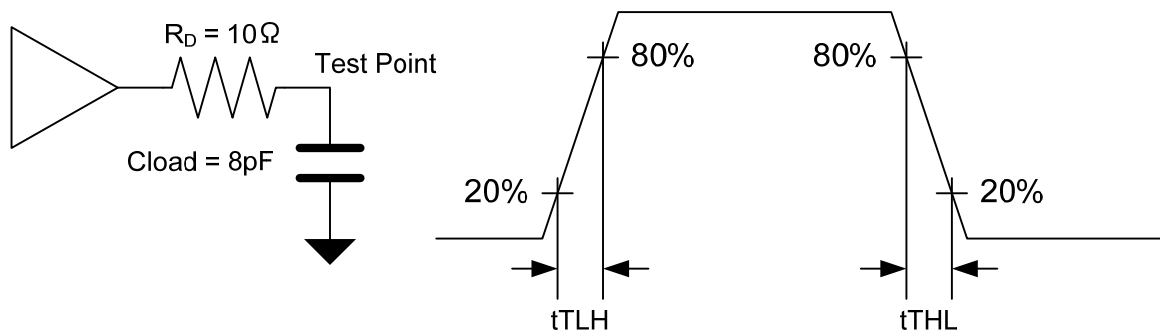


Figure 18. LVC MOS Output Switching Timing Diagrams

CML Output Switching Characteristics

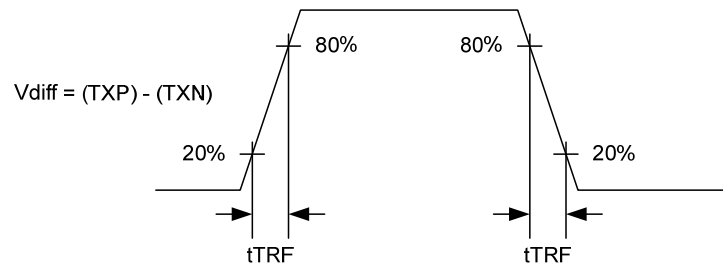
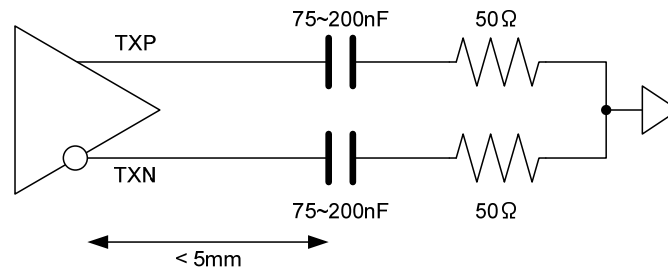


Figure 19. CML Output Switching Characteristics

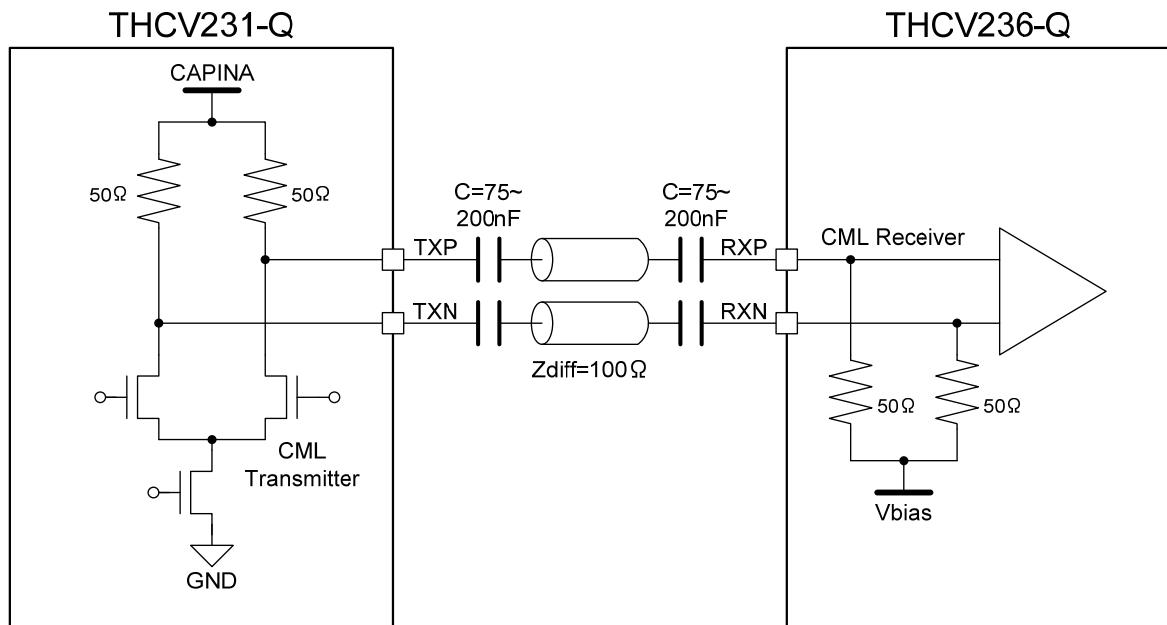


Figure 20. CML Buffer Equivalent Circuit

CML Bi-directional Output Test Circuit

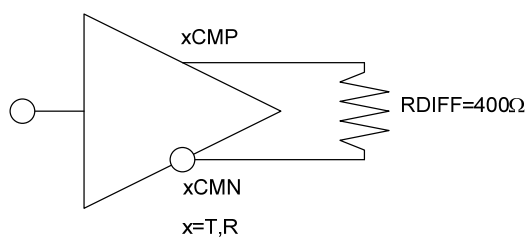


Figure 21. Bi-directional CML VBOD/VBOC Test Circuit

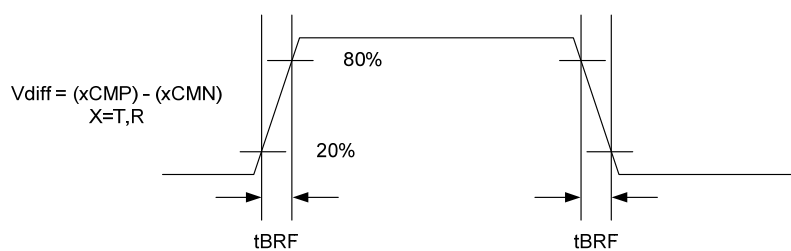
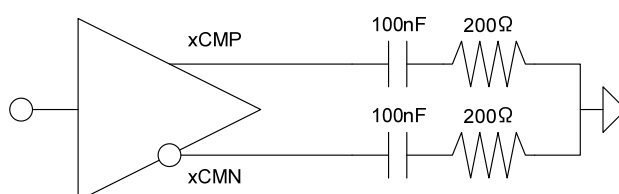


Figure 22. Bi-directional CML Switching Timing Diagram and Test Circuit

Latency Characteristics

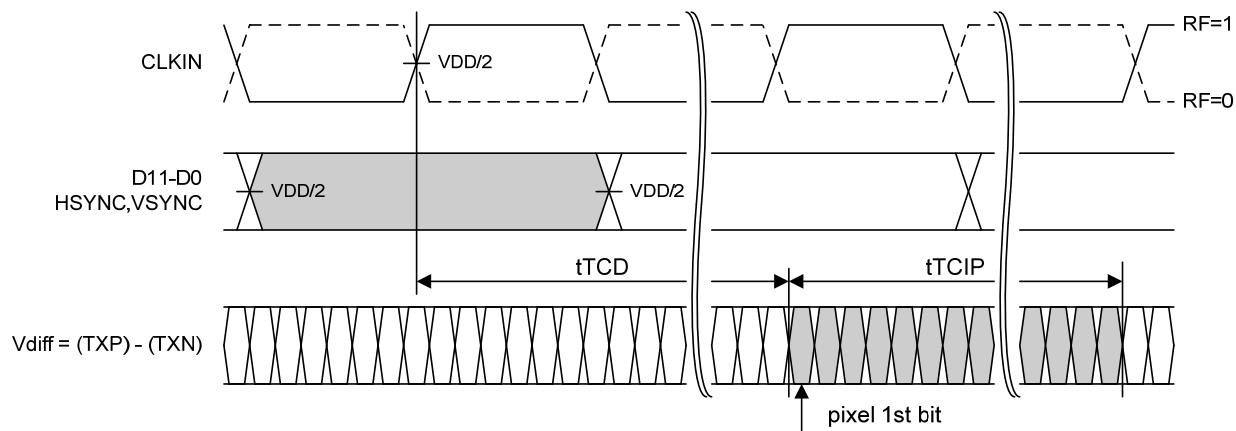


Figure 23. THCV231-Q Latency

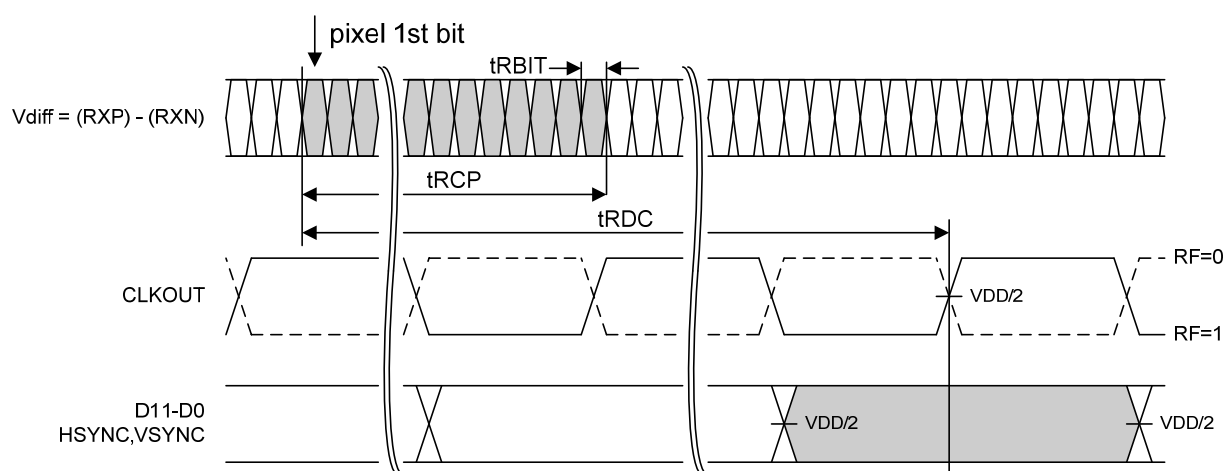


Figure 24. THCV236-Q Latency

Lock and Unlock Sequence

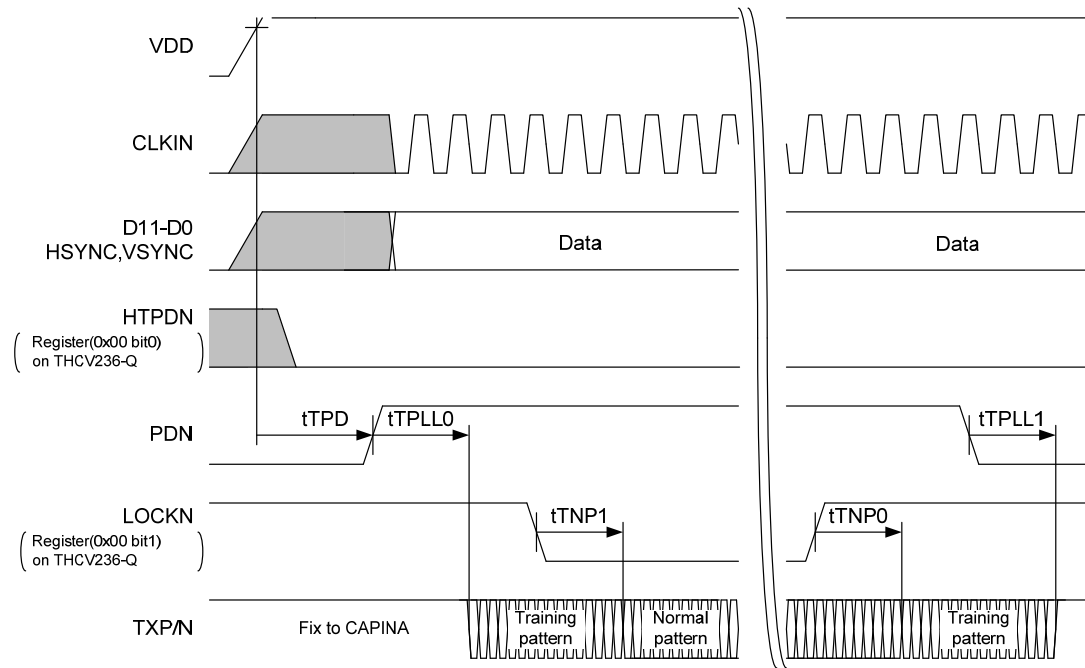
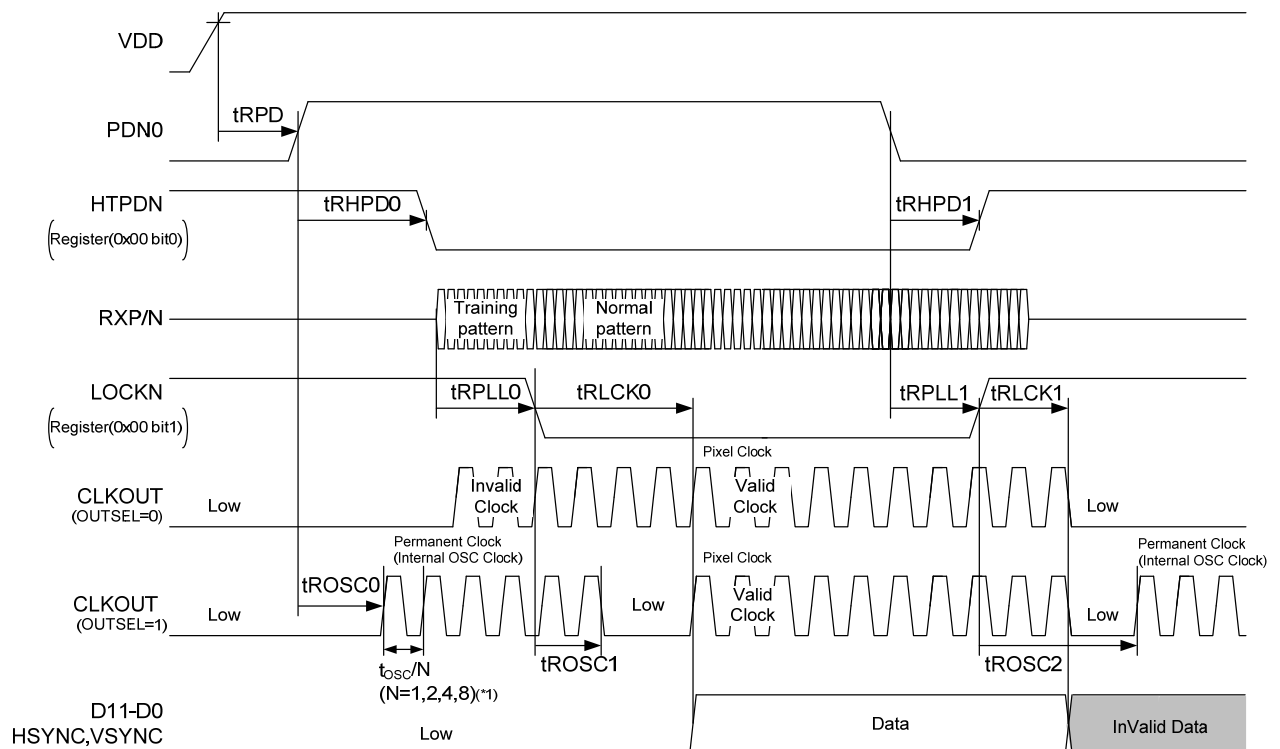


Figure 25. THCV231-Q Lock/Unlock Sequence



*1 N depends on setting of OUTSEL_SETTING register (0x6D bit1,0). See Register Map (Table 36)

Figure 26. THCV236-Q Lock/Unlock Sequence

2-wire serial I/F Switching Characteristics

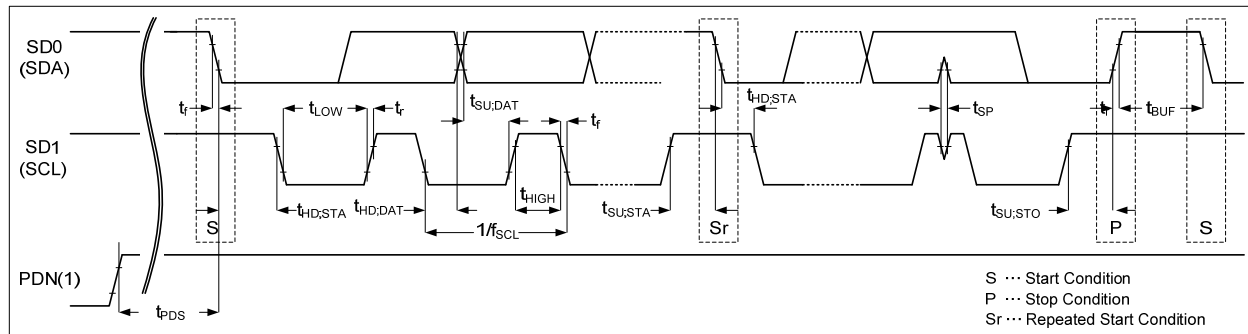


Figure 27. 2-wire serial interface Timing Diagram

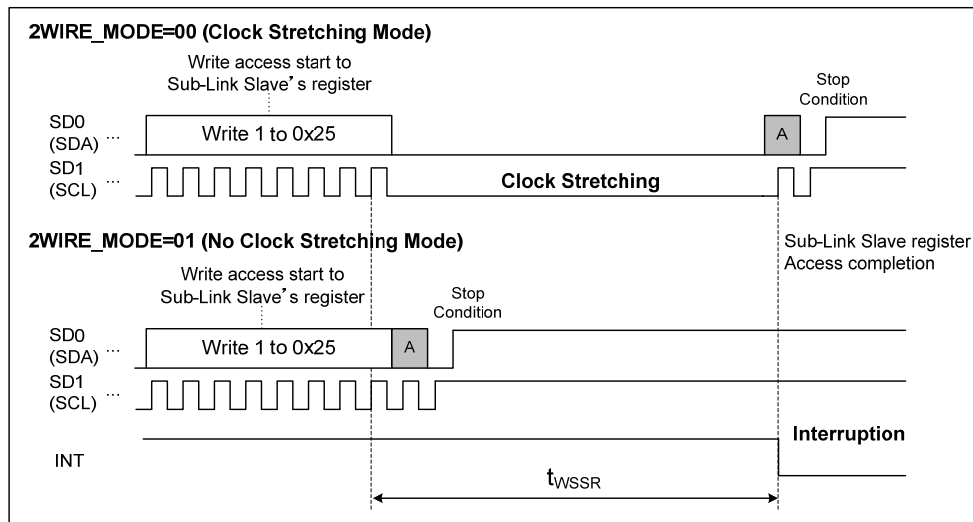


Figure 28. Write access completion time to Sub-Link Slave register

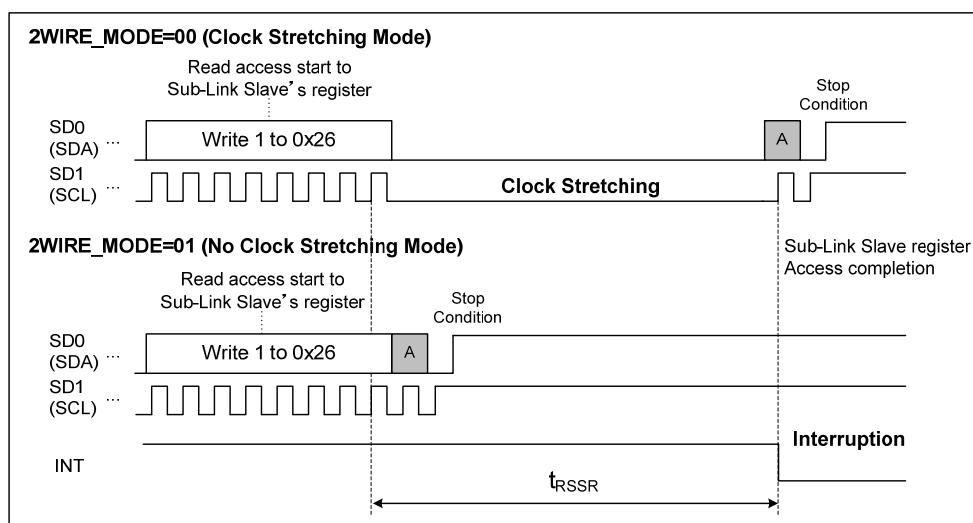


Figure 29. Read access completion time to Sub-Link Slave register

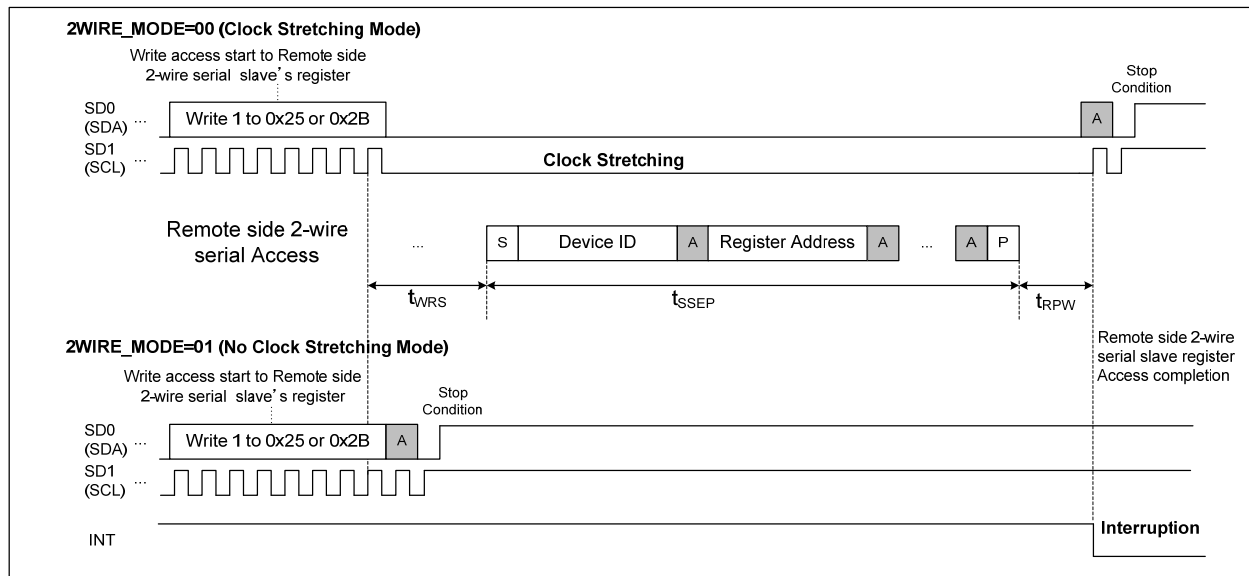


Figure 30. Write access completion time to Remote side 2-wire serial slave register

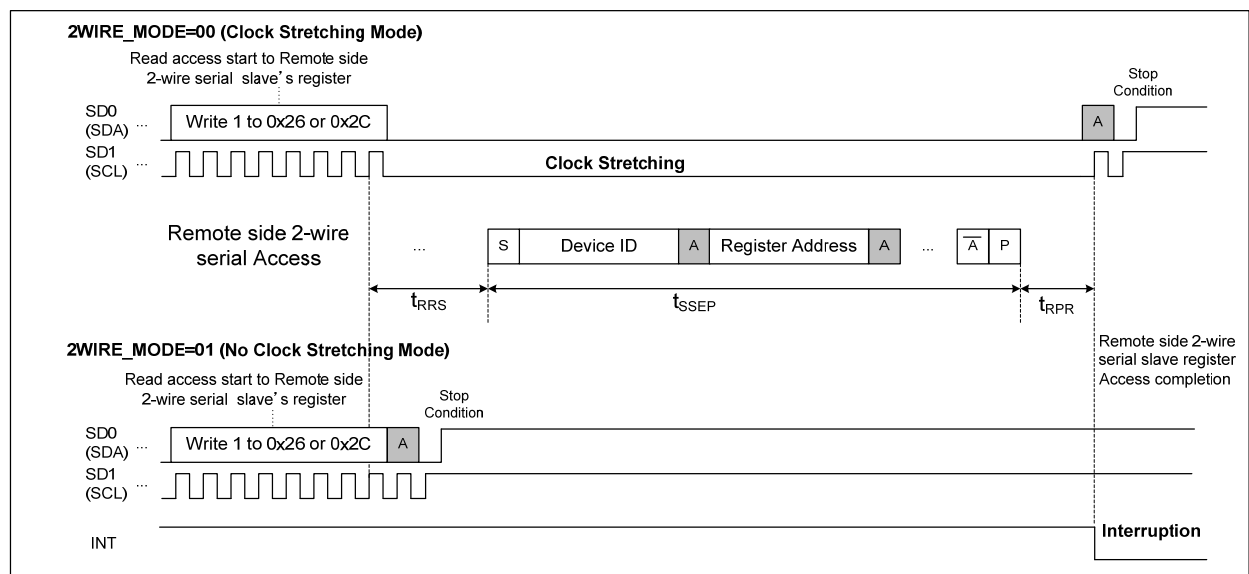
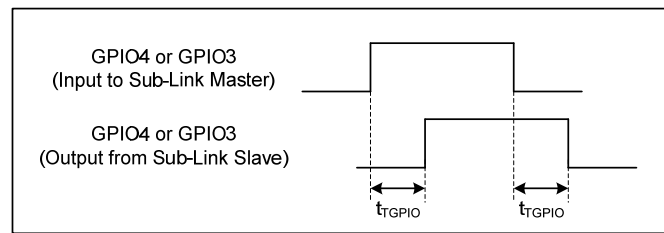
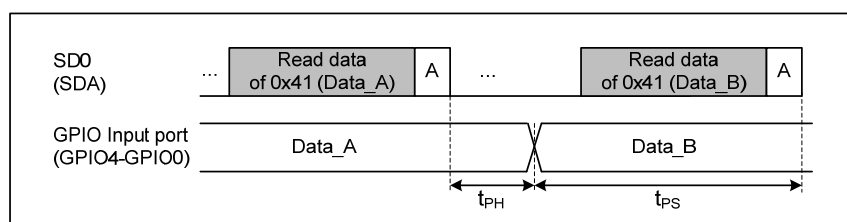
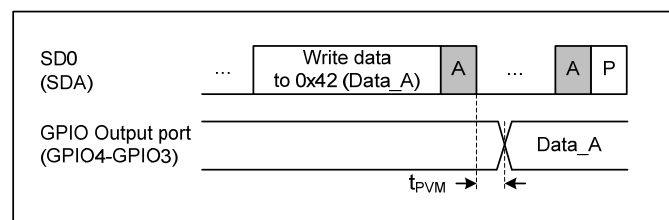
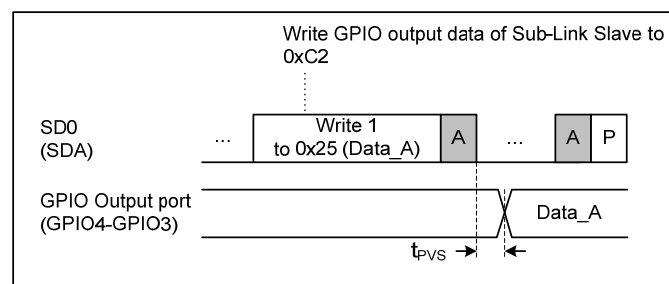


Figure 31. Read access completion time to Remote side 2-wire serial slave register

GPIO Switching Characteristics

**Figure 32. Through GPIO delay****Figure 33. Programmable GPIO input timing at Sub-Link Master side****Figure 34. Programmable GPIO output timing at Sub-Link Master side****Figure 35. Programmable GPIO output timing at Sub-Link Slave side**

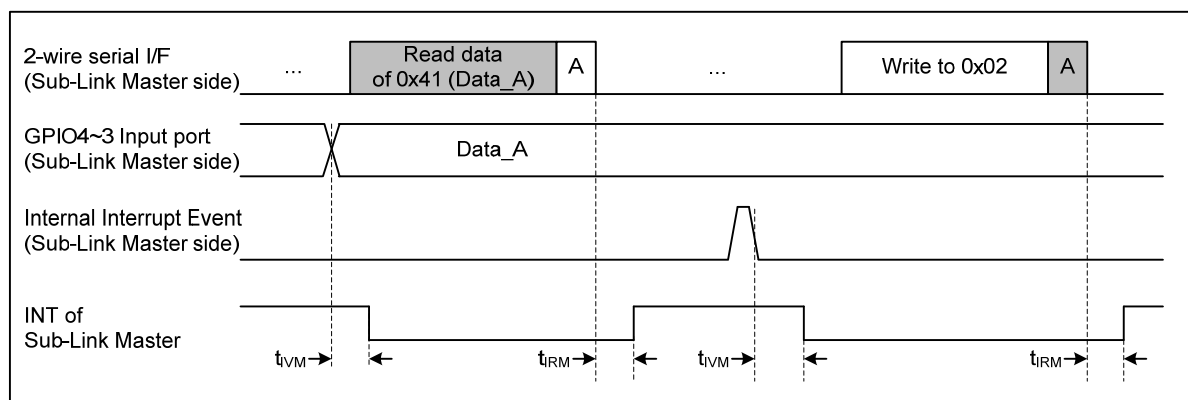


Figure 36. GPIO input and other interrupt event timing at Sub-Link Master side

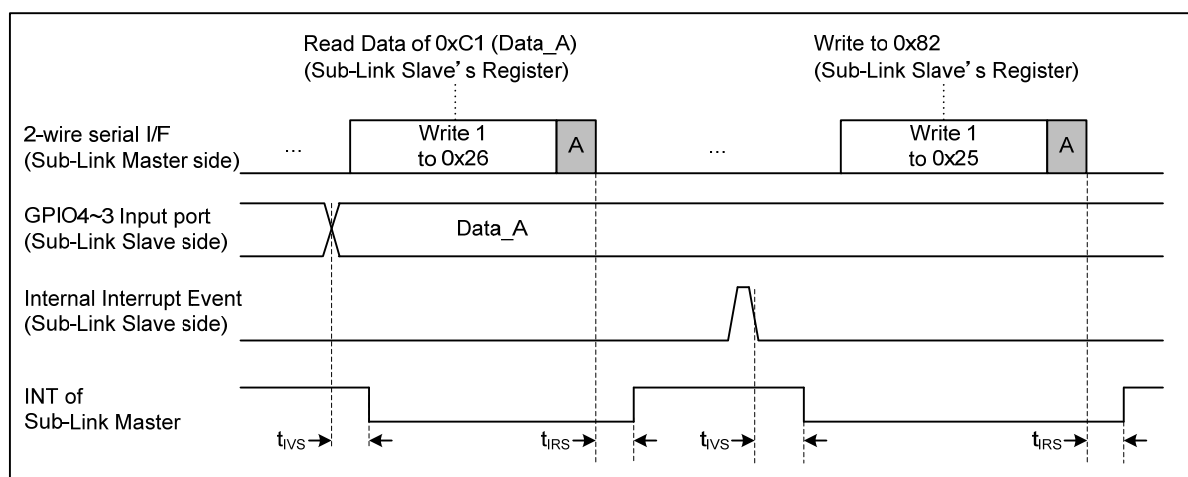


Figure 37. GPIO input and other interrupt event timing at Sub-Link Slave side (Clock Stretching Mode)

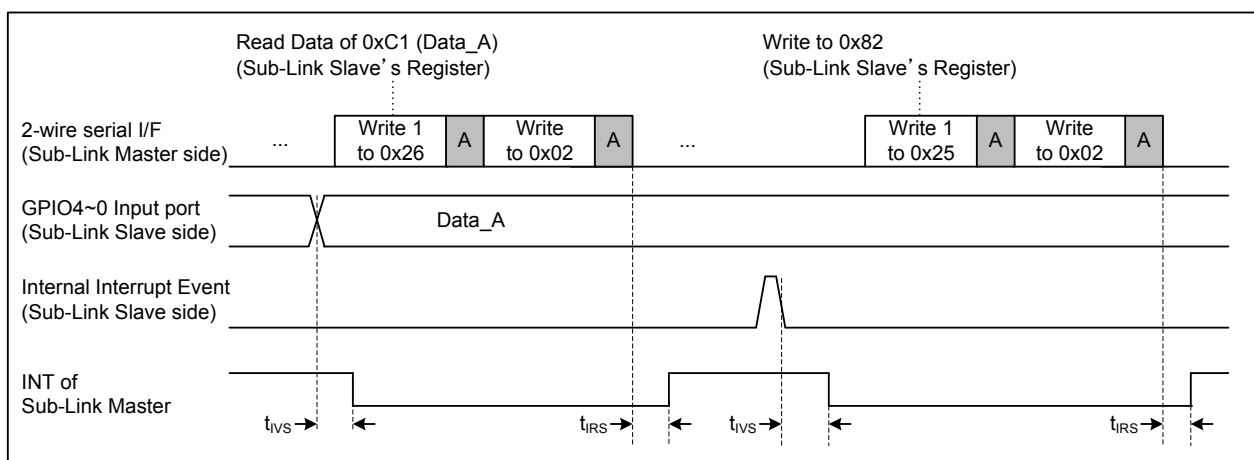
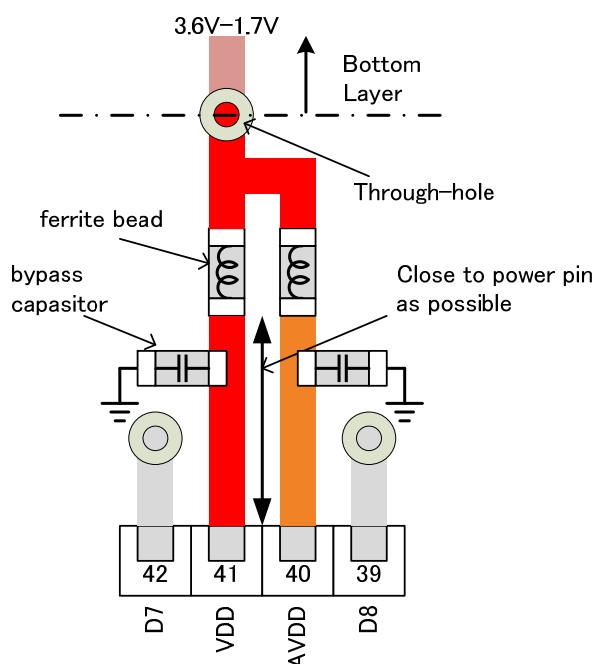


Figure 38. GPIO input and other interrupt event timing at Sub-Link Slave side (No-Clock Stretching Mode)

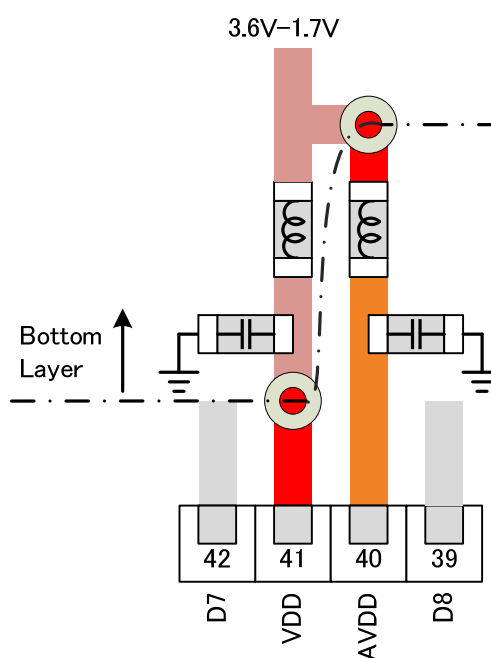
PCB Layout Guideline regarding VDD and AVDD for THCV236-Q

When power is supplied from reverse side layer to AVDD, please place ferrite bead between through-hole and AVDD/VDD pins (Good Example1, 2). If it is needed to set ferrite beads on reverse side, please set GND-through-hole between AVDD and VDD, and separate the distance as possible (Example). Don't set through-holes next to each other between ferrite beads and AVDD/VDD pins (Bad Example).

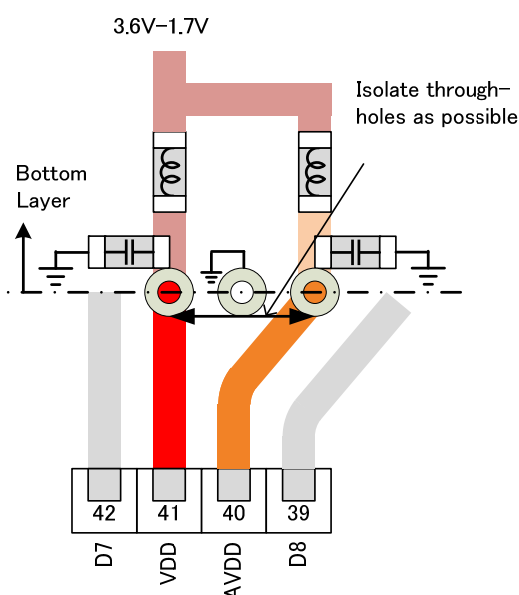
Good Example 1



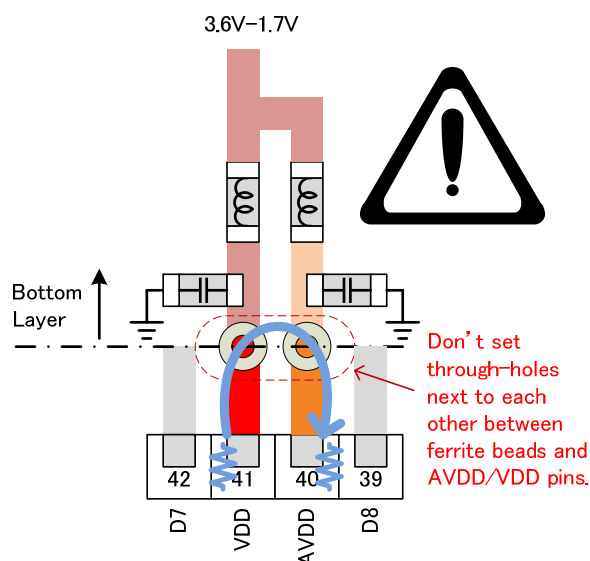
Good Example 2



Example



Bad Example



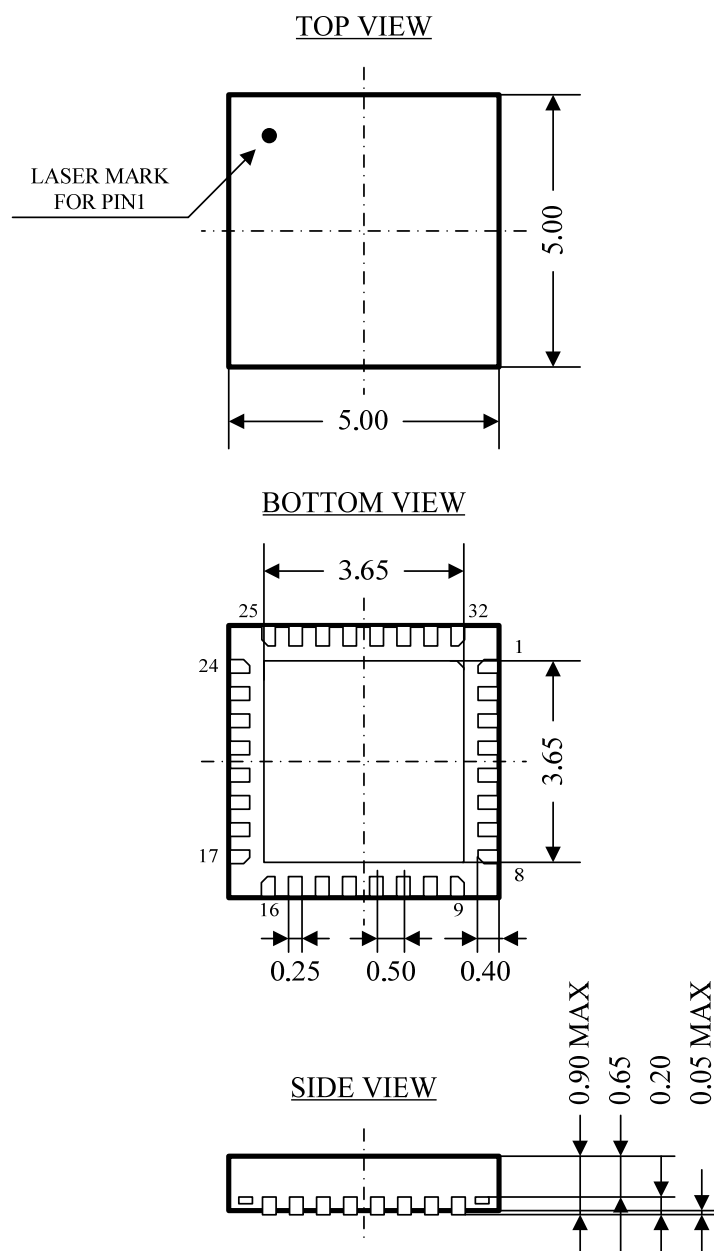
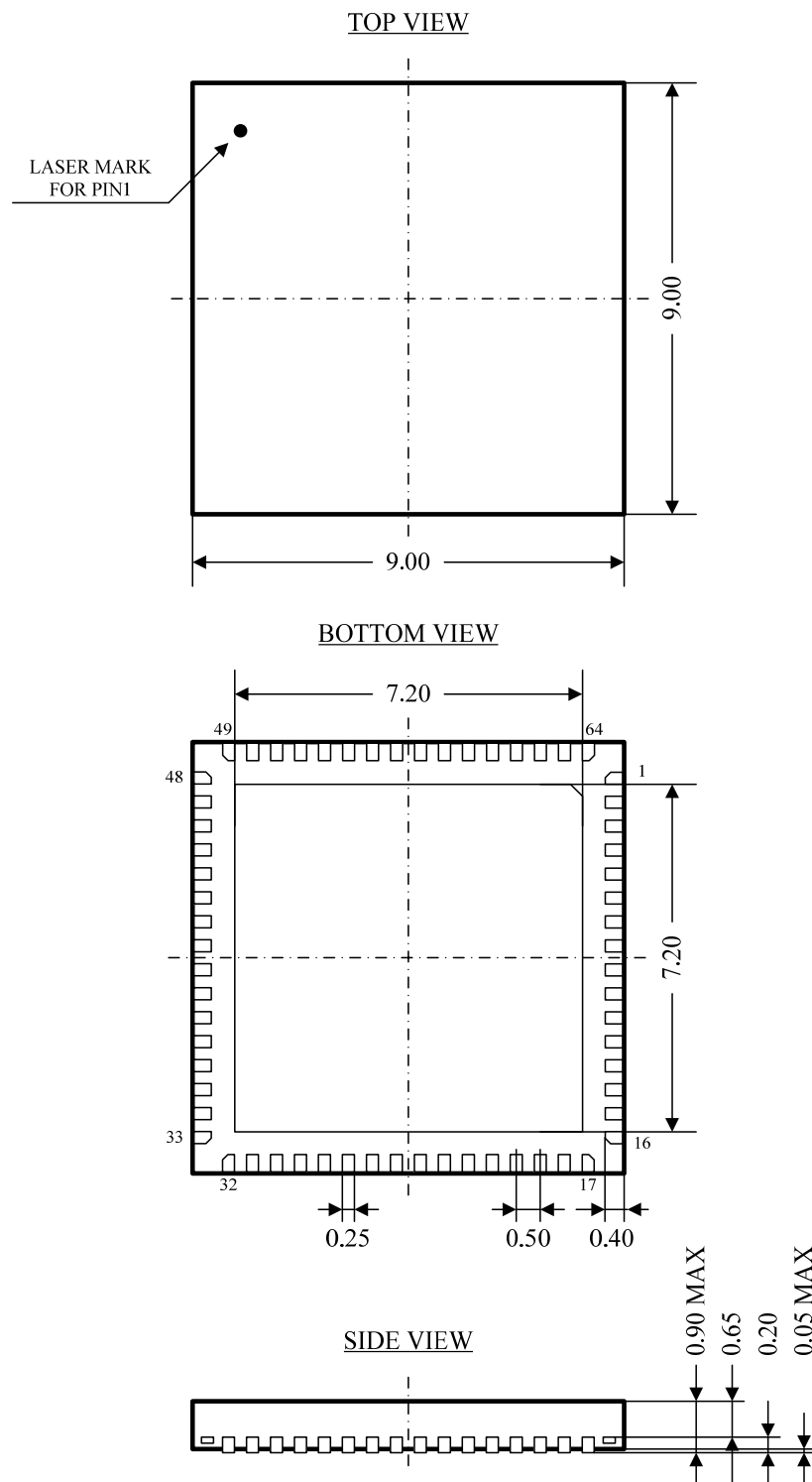


Figure 39.32-pin QFN package physical dimension



Unit : mm

Figure 40. 64-pin QFN package physical dimension

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copyright, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. Product Application
 - 5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
 - 5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of ISO/TS16949 ("the Specified Product") in this data sheet. THine Electronics, Inc. ("THine") accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
 - 5.3 THine accepts liability for demands and specifications of the Specified Product only to the extent that the user and THine have been previously and explicitly agreed to each other.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation/proof.
8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.
9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

THine Electronics, Inc.

sales@thine.co.jp

<http://www.thine.co.jp>