THCV235 and THCV236

SerDes transmitter and receiver with bi-directional transceiver

General Description

The THCV235 and THCV236 are designed to support video data transmission between the host and display.

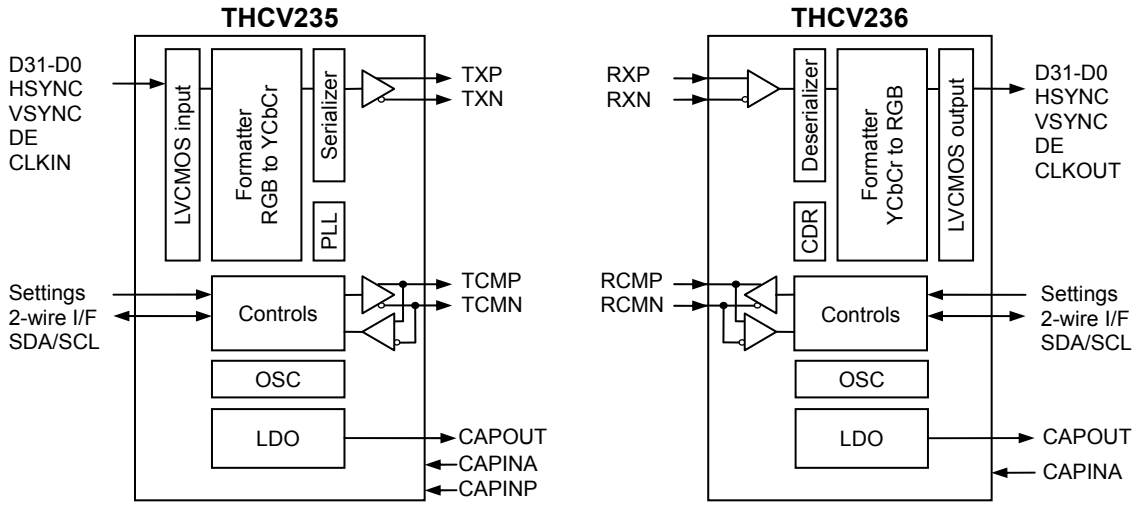
One high-speed lane can carry up to 32bit data and 3bits of synchronizing signals at a pixel clock frequency from 6MHz to 160MHz by converting RGB444 to YCbCr422.

The chipset, which has one high-speed data lane, can transmit video data up to 1080p/60Hz.
The maximum serial data rate is 4.00Gbps/lane.

Features

- Color depth selectable:24/32bit
- RGB ⇔YCbCr422 color space conversion function
- Wide frequency range
- AC coupling for high-speed lanes
- CDR requires no external frequency reference
- Wide range supply voltage from 1.7V to 3.6V
- Additional spread spectrum on data stream
- 2-wire serial interface bridge function(400kbps)
- Remote side GPIO control and monitoring
- Low speed data bridge function
- QFN64(9mm x 9mm) with exposed pad ground
- V-by-One® HS standard version1.4 compliant
- EU RoHS compliant

Block Diagram



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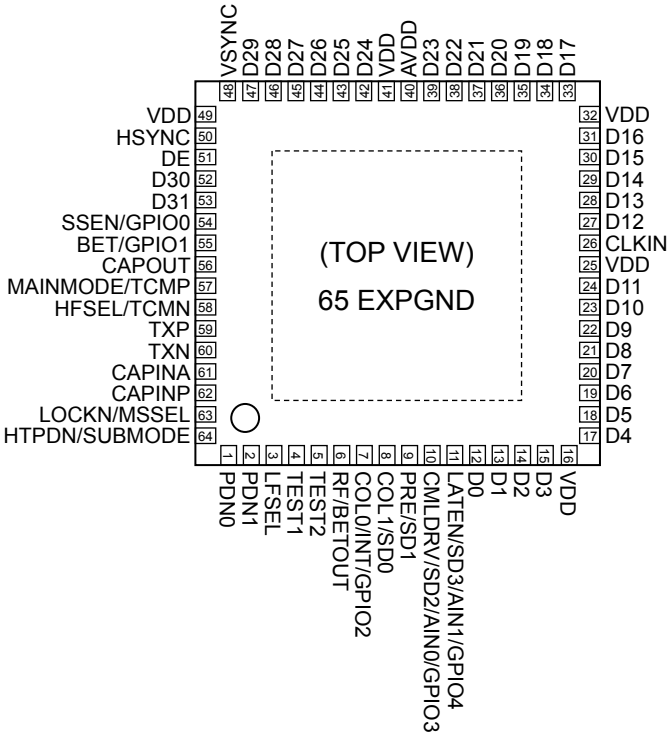
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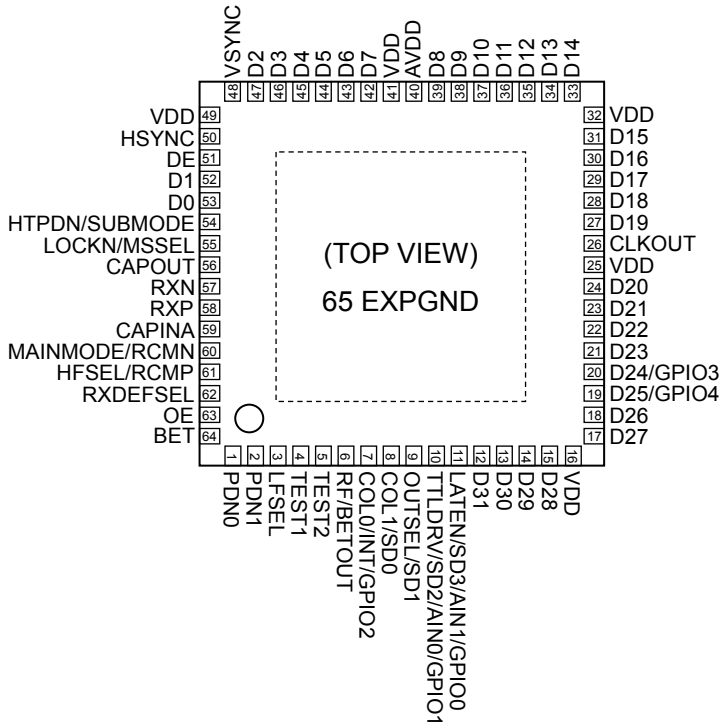
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Pin Configuration

THCV235 (QFN 64pin)



THCV236 (QFN 64pin)



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Pin Description

Pin Description for THCV235

Pin Name	Pin No.	Type	Description
TXP	59	CO	High-Speed CML Signal Output(Main-Link)
TXN	60	CO	High-Speed CML Signal Output(Main-Link)
MAINMODE/ TCMP	57	I/CB	MAINMODE : Setting V-by-One® HS Mode or Sync Free Mode when PDN1=0. See page12. 0 : V-by-One® HS Mode 1 : Sync Free Mode TCMP : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
HFSEL/TCMN	58	I/CB	HFSEL : High Frequency mode select when PDN1=0. 0 : High Frequency mode Disable 1 : High Frequency mode Enable TCMN : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
HTPDN/ SUBMODE	64	IL	HTPDN : Hot Plug Detect Input when PDN1=0. SUBMODE : Sub-Link Mode Select when PDN1=1. 0: 2-wire serial interface(I/F) Mode(default No Clock Stretching mode) 1: Low Speed Data Bridge Mode Forbid the different setting between THCV235 and THCV236.
LOCKN/MSSEL	63	IL	LOCKN : Lock Detect Input when PDN1=0. MSSEL : Sub-Link Master/Slave Select when PDN1=1. 0 : Sub-Link Master side(inside 2-wire serial I/F is slave) 1 : Sub-Link Slave side(inside 2-wire serial I/F is master) Sub-Link Master is connected to HOST MPU. Forbid the same setting between THCV235 and THCV236.
LATEN/SD3/AIN1/ GPIO4	11	B	LATEN : Latch select input under Field BET(Main-Link or Sub-Link). 0 : NOT Latched result 1 : Latched result SD3 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD3 is output. When Sub-Link is Slave (MSSEL=1), SD3 is input. AIN1 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO4 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO4 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO4 is used as push pull output or input, no external component is required.

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CMLDRV/SD2/ AIN0/GPIO3	10	B	CMLDRV : High-Speed CML Output Drive Strength Select when PDN1=0. 0 : Weak Drive Strength (600mV diff p-p) 1 : Normal Drive Strength (800mV diff p-p) SD2 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD2 is input. When Sub-Link is Slave (MSSEL=1), SD2 is output. AIN0 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO3 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO3 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO3 is used as push pull output or input, no external component is required.
PRE/SD1	9	B	PRE : Pre-Emphasis Level Select Input when PDN1=0. 0 : Pre-Emphasis Disable 1 : Pre-Emphasis Enable (when CMLDRV=1. See Table 4) SD1 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD1 is used as SCL input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD1 is input. When SUBMODE=1 and MSSEL=1, SD1 is output.
COL1/SD0	8	B	COL1 : Color Space Converter Enable when PDN1=0 and MAINMODE=0. 0 : Color Space Converter Disable 1 : Color Space Converter Enable Data Width Setting when PDN1=0 and MAINMODE=1. See Table 20. SD0 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD0 is used as SDA input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD0 is input. When SUBMODE=1 and MSSEL=1, SD0 is output.
COL0/INT/GPIO2	7	B	COL0 : Data Width Setting when PDN1=0. See Table 20. INT : Interrupt signal output for Sub-Link when SUBMODE=0 and MSSEL=0. It must be connected with a pull-up resistor to VDD. L : Interrupt occurred H : Steady state GPIO2 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO2 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO2 is used as push pull output or input, no external component is required.

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BET/GPIO1	55	BO	BET : Field BET entry when PDN1=0 or Sub-Link is active and Low Speed Data Bridge Mode(PDN1=1, SUBMODE=1). 0 : Normal Operation 1 : Field BET Operation GPIO1 : General Purpose Input/Output when SUBMODE=0. GPIO1 has Open-Drain Output buffer, it must be connected with a pull-up resistor to VDD.
SSEN/GPIO0	54	BO	SSEN : Spread Spectrum Clock Generator(SSCG) Enable when PDN1=0 or Sub-Link is active and Low Speed Data Bridge Mode(PDN1=1, SUBMODE=1). 0 : SSCG Disable 1 : SSCG Enable GPIO0 : General Purpose Input/Output when SUBMODE=0. GPIO0 has Open-Drain Output buffer, it must be connected with a pull-up resistor to VDD.
CLKIN	26	I	Clock Input
D31-D0	53,52,47-42, 39-33,31-27, 24-17,15-12	I	Pixel Data Input
DE	51	I	DE Input
HSYNC	50	I	HSYNC Input
VSYNC	48	I	VSYNC Input
RF/BETOUT	6	B	RF : Input Clock Triggering edge select. See Figure 19. 0 : Falling Edge 1 : Rising Edge BETOUT : Field BET Result Output when Field BET mode
LFSEL	3	I	Low Frequency mode select 0 : Low Frequency mode Disable 1 : Low Frequency mode Enable
PDN1	2	IL	Sub-Link Power Down 0 : Power Down. Main-Link setting by external pin 1 : Normal Operation. Main-Link Setting by 2-wire serial I/F
PDN0	1	IL	Main-Link Power Down 0 : Power Down 1 : Normal Operation
TEST2	5	I	Test pin. Must be tied to Ground for normal operation.
TEST1	4	IL	Test pin. Must be tied to Ground for normal operation.
CAPOUT	56	PWR	Decoupling Capacitor Pin, 1.2V output.
CAPINA	61	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
CAPINP	62	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
VDD	49,41,32,25,16	PWR	1.7-3.6V Digital Power Supply Pin for LVCMOS I/O
AVDD	40	PWR	1.7-3.6V Analog Power Supply Pin for LDO
EXPGND	65	GND	Exposed Pad Ground. Must be tied to the PCB ground plane through an array of vias.

CO : CML Output buffer , CB : CML Bi-directional buffer
I : LVCMOS Input buffer , IL : Low Speed LVCMOS Input buffer
B : LVCMOS Bi-directional buffer , BO : Open-Drain LVCMOS Bi-directional buffer
PWR : Power supply , GND : Ground

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Table 1. Pin Sharing Description (THCV235)

Sub-Link State →	Sub-Link Power Down	Low Speed Data Bridge Mode		2-wire serial I/F Mode	
Sub-Link Master/Slave →	-	Master	Slave	Master	Slave
PDN1	**0**	**1**	**1**	**1**	**1**
HTPDN/SUBMODE	*	**1**	**1**	**0**	**0**
LOCKN/MSSEL	*	**0**	**1**	**0**	**1**
BET/GPIO1	**0**	**0**	**0**	*	*
RF/BETOUT	RF				
	BETOUT(*2)				
COL0/INT/GPIO2	COL0	COL0	COL0	INT	GPIO2(*4)
COL1/SD0	COL1	SD0(input)	SD0(output)(*6)	SD0(SDA)	SD0(SDA)
PRE/SD1	PRE	SD1(input)	SD1(output)(*6)	SD1(SCL)	SD1(SCL)
CMLDRV/SD2/AIN0/GPIO3	CMLDRV	SD2(input)	SD2(output)(*6)	AIN0	GPIO3(*5)
LATEN/SD3/AIN1/GPIO4	-(*1)	SD3(output)(*6)	SD3(input)	AIN1	GPIO4(*5)
	LATEN(*3)				
SSEN/GPIO0	SSEN	SSEN	SSEN	GPIO0(*4)	GPIO0(*4)
BET/GPIO1	BET	BET	BET	GPIO1(*4)	GPIO1(*4)
MAINMODE/TCMP	MAINMODE	TCMP			
HFSEL/TCMN	HFSEL	TCMN			
LOCKN/MSSEL	LOCKN	MSSEL			
HTPDN/SUBMODE	HTPDN	SUBMODE			

*1 There is no function. LVCMOS IO has input state. Must be fixed at 0 or 1 input.
*2 When Field BET mode (Main-Link or Sub-Link), it functions as BETOUT output.
*3 When Field BET mode (Main-Link or Sub-Link), it functions as LATEN input.
*4 Programmable GPIO input is default on register setting.
*5 Through GPIO open-drain output is default on register setting.
*6 Low Speed Data Bridge Mode output is LVCMOS push pull buffer.

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Pin Description for THCV236

Pin Name	Pin No.	Type	Description
RXP	58	CI	High-Speed CML Signal Input(Main-Link)
RXN	57	CI	High-Speed CML Signal Input(Main-Link)
HFSEL/RCMP	61	CB/I	HFSEL : High Frequency Mode select when PDN1=0. 0 : High Frequency Mode Disable 1 : High Frequency Mode Enable RCMP : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
MAINMODE/ RCMN	60	CB/I	MAINMODE : Setting V-by-One® HS Mode or Sync Free Mode when PDN1=0 0 : V-by-One® HS Mode 1 : Sync Free Mode RCMN : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
HTPDN/ SUBMODE	54	BO	HTPDN : Hot Plug Detect Output when PDN1=0. Must be connected to Tx HTPDN with 10kΩ pull-up resistor. SUBMODE : Sub-Link Mode Select when PDN1=1. 0 : 2-wire serial I/F Mode (default No Clock Stretching mode) 1 : Low Speed Data Bridge Mode Forbid the different setting between THCV235 and THCV236.
LOCKN/ MSSEL	55	BO	LOCKN : Lock Detect Output when PDN1=0. Must be connected to Tx LOCKN with 10kΩ pull-up resistor. MSSEL : Sub-Link Master/Slave Select when PDN1=1. 0 : Sub-Link Master side(inside 2-wire serial I/F is slave) 1 : Sub-Link Slave side(inside 2-wire serial I/F is master) Sub-Link Master is connected to HOST MPU. Forbid the same setting between THCV235 and THCV236.
LATEN/SD3/ AIN1/GPIO0	11	B	LATEN : Latch select input under Field BET(Main-Link or Sub-Link). 0 : NOT Latched result 1 : Latched result SD3 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD3 is output. When Sub-Link is Slave (MSSEL=1), SD3 is input. AIN1 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO0 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO0 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO0 is used as push pull output or input, no external component is required.

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TTLDRV/SD2/ AIN0/GPIO1	10	B	TTLDRV : TTL Output Drive Strength Select when PDN1=0. 0 : Weak Drive Strength 1 : Normal Drive Strength SD2 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD2 is input. When Sub-Link is Slave (MSSEL=1), SD2 is output. AIN0 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO1 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO1 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO1 is used as push pull output or input, no external component is required.
OUTSEL/SD1	9	B	OUTSEL : Permanent Clock Output Enable when PDN1=0. 0 : Permanent Clock Output Disable 1 : Permanent Clock Output Enable SD1 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD1 is used as SCL input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD1 is input. When SUBMODE=1 and MSSEL=1, SD1 is output.
COL1/SD0	8	B	COL1 : Color Space Converter Enable when PDN1=0 and MAINMODE=0. 0 : Color Space Converter Disable 1 : Color Space Converter Enable Data Width Setting when PDN1=0 and MAINMODE=1. See Table 20. SD0 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD0 is used as SDA input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD0 is input. When SUBMODE=1 and MSSEL=1, SD0 is output.
COL0/INT/ GPIO2	7	B	COL0 : Data Width Setting when PDN1=0. See Table 20. INT : Interrupt signal output for Sub-Link when SUBMODE=0 and Sub-Link Master. It must be connected with a pull-up resistor to VDD. L : Interrupt occurred H : Steady state GPIO2 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO2 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO2 is used as push pull output or input, no external component is required.
CLKOUT	26	O	Clock Output
D31-D26	12-15,17,18	O	Pixel Data Output

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D25/GPIO4	19	B	D25 : Pixel Data Output GPIO4 : General Purpose Input/Output when SUBMODE=0, MSSEL=0 and RXDEFSEL=0. When GPIO4 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO4 is used as push pull output or input, no external component is required.
D24/GPIO3	20	B	D24 : Pixel Data Output GPIO3 : General Purpose Input/Output when SUBMODE=0, MSSEL=0 and RXDEFSEL=0. When GPIO3 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO3 is used as push pull output or input, no external component is required.
D23-D0	21-24,27-31,33-39, 42-47,52,53	O	Pixel Data Output
DE	51	O	DE Output
HSYNC	50	O	HSYNC Output
VSYNC	48	O	VSYNC Output
OE	63	IL	Output Enable 0 : LVCMOS Output Disable (Hi-Z) except for HTPDN, LOCKN when PDN1=0 and except for BETOUT when BET=1. 1 : LVCMOS Output Enable
BET	64	IL	Field BET entry 0 : Normal Operation 1 : Field BET Operation
RF/BETOUT	6	B	RF : Output Clock Triggering edge select. See Figure 20. 0 : Falling Edge 1 : Rising Edge BETOUT : Field BET Result Output
RXDEFSEL	62	I	Internal Register Default Setting Select. See Table 44, Table 45 0 : for THCV231 1 : for THCV235
LFSEL	3	I	Low Frequency mode select 0 : Low Frequency mode Disable 1 : Low Frequency mode Enable
PDN1	2	IL	Sub-Link Power Down 0 : Power Down. Main-Link setting by external pin 1 : Normal Operation. Main-Link Setting by 2-wire serial I/F
PDN0	1	IL	Main-Link Power Down 0 : Power Down 1 : Normal Operation
TEST2	5	I	Test pin. Must be tied to Ground for normal operation.
TEST1	4	IL	Test pin. Must be tied to Ground for normal operation.
CAPOUT	56	PWR	Decoupling Capacitor Pin, 1.2V output.
CAPINA	59	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
VDD	49,41,32,25,16	PWR	1.7-3.6V Digital Power Supply Pin for LVCMOS I/O
AVDD	40	PWR	1.7-3.6V Analog Power Supply Pin for LDO
EXPGND	65	GND	Exposed Pad Ground. Must be tied to the PCB ground plane through an array of vias.

CI : CML Input buffer , CB : CML Bi-directional buffer
I : LVCMOS Input buffer , IL : Low Speed LVCMOS Input buffer , O: LVCMOS Output buffer
B : LVCMOS Bi-directional buffer , BO : Open-Drain LVCMOS Bi-directional buffer
PWR : Power supply , GND : Ground

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Table 2. Pin Sharing Description (THCV236)

Sub-Link State →	Sub-Link Power Down	Low Speed Data Bridge Mode		2-wire serial I/F Mode		
Sub-Link Master/Slave →	-	Master	Slave	Master 1	Master 2	Slave
PDN1	**0**	**1**	**1**	**1**	**1**	**1**
HTPDN/SUBMODE	*	**1**	**1**	**0**	**0**	**0**
LOCKN/MSSEL	*	**0**	**1**	**0**	**0**	**1**
BET	**0**	**0**	**0**	**0**	**0**	**0**
RXDEFSEL	*	*	*	**1**	**0**	*
RF/BETOUT	RF					
	BETOUT(*2)					
COL0/INT/GPIO2	COL0	COL0	COL0	INT	INT	GPIO2(*4)
COL1/SD0	COL1	SD0(input)	SD0(output)(*6)	SD0(SDA)	SD0(SDA)	SD0(SDA)
OUTSEL/SD1	OUTSEL	SD1(input)	SD1(output)(*6)	SD1(SCL)	SD1(SCL)	SD1(SCL)
TTLDRV/SD2/AIN0/GPIO1	TTLDRV	SD2(input)	SD2(output)(*6)	AIN0	AIN0	GPIO1(*4)
LATEN/SD3/AIN1/GPIO0	-(*1)	SD3(output)(*6)	SD3(input)	AIN1	AIN1	GPIO0(*4)
	LATEN(*3)					
D24/GPIO3	D24	D24	D24	D24	GPIO3(*5)	D24
D25/GPIO4	D25	D25	D25	D25	GPIO4(*5)	D25
HTPDN/SUBMODE	HTPDN	SUBMODE				
LOCKN/MSSEL	LOCKN	MSSEL				
MAINMODE/RCMN	MAINMODE	RCMN				
HFSEL/RCMP	HFSEL	RCMP				

*1 There is no function. LVCMOS IO has input state. Must be fixed at 0 or 1 input.
*2 When Field BET mode (Main-Link or Sub-Link), it functions as BETOUT output.
*3 When Field BET mode (Main-Link or Sub-Link), it functions as LATEN input.
*4 Programmable GPIO input is default on register setting.
*5 Through GPIO input is default on register setting.
*6 Low Speed Data Bridge Mode output is LVCMOS push pull buffer.

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Functional Overview

With High Speed CML SerDes, proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, the THCV235 and THCV236 enable transmission of 24/30bit video data, 2bits of user defined data, synchronizing signals HSYNC,VSYNC and DE(Data Enable) as well as any data (up to 35 bit) through Main-Link by single differential pair cable with minimal external components. In addition, the THCV235 and THCV236 have Sub-Link which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for Main-Link through the other 1-pair of CML-Line. It does not need any external frequency reference, such as a crystal oscillator. The THCV235 - THCV236 system is able to watch and control peripheral devices via 2-wire serial interface or GPIOs. They also can report interrupt events caused by change of GPIO inputs and internal statuses.

Functional Description

Internal Reference Output/Input Function (CAPOUT, CAPINA, CAPINP)

An internal regulator produces the 1.2V (CAPOUT). This 1.2V linear regulator can't supply any other external loads. Bypass CAPOUT to GND with 10uF.

CAPINP (THCV235 only) supplies reference voltage for internal PLL, and CAPINA supplies reference voltage for any internal analog circuit. Bypass CAPINP/CAPINA to GND with 0.1uF to remove high frequency noise. CAPOUT, CAPINA and CAPINP must be tied together.

Power supply AVDD is supposed to be stabilized with de-coupling capacitor and series noise filter (for example, ferrite bead).

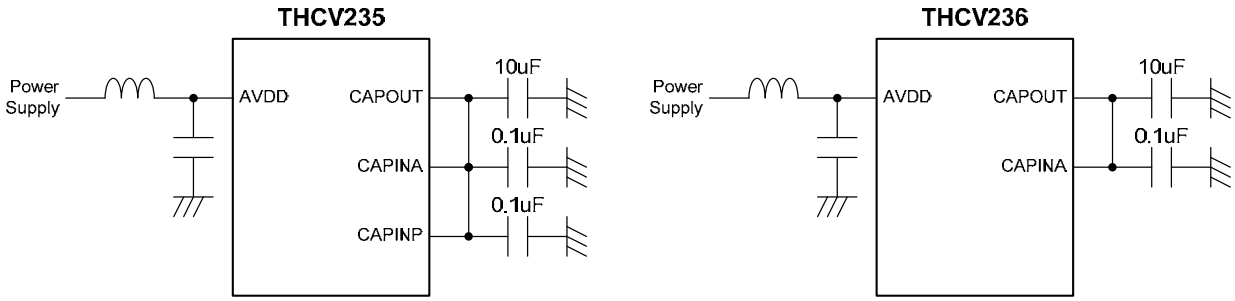


Figure 1. Connection of CAPOUT, CAPINA, CAPINP and Decoupling Capacitor

Power Down (PDN1, PDN0)

PDN1 and PDN0 turn off internal circuitry of Main-Link and Sub-Link separately.

Table 3. Power Down Setting

PDN1	PDN0	Operation
0	0	Both Main-Link and Sub-Link power down
0	1	Only Main-Link is active
1	0	Only Sub-Link is active
1	1	Both Main-Link and Sub-Link active

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Main-Link Mode Setting

Two modes of Main-Link operation are available. Mode select is done by MAINMODE pin (when PDN1=0) or MAINMODE register (when PDN1=1).

V-by-One® HS Mode (MAINMODE=0)

V-by-One® HS Mode is compliant with V-by-One® HS standard Version1.4. (See Figure 3 and Table 14)

Sync Free Mode (MAINMODE=1)

Incoming data can be transmitted by Sync Free Mode without DE requirement. (See Table 14)

Color Space Conversion

The THCV235 converts RGB444 to YCbCr422 and the THCV236 converts back to RGB. This function can only be used in V-by-One® HS mode and enabled by COL1=1 setting. COL1 is external pin (when PDN1=0) or internal register (when PDN1=1). Color space conversion coefficients are compliant with ITU-R BT.709-5.

Pre-emphasis and Drive Select Function (THCV235 only)

Pre-emphasis can equalize severe signal degradation caused by long-distance or high-speed transmission. PRE pin or PRE register selects the strength of pre-emphasis. CMLDRV pin or CMLDRV register controls CML Main-Link output swing level. See Table 4 and Table 5.

Table 4. Pre-emphasis and Drive Select function table (PDN1=0)

CMLDRV (pin)	PRE (pin)	Condition	
		Swing Level	Pre-emphasis Level
0	0	600mV diff p-p	0dB
	1		3.5dB
1	*	800mV diff p-p	0dB

Table 5. Pre-emphasis and Drive Select function table (PDN1=1)

CMLDRV[1:0] (register)	PRE (register)	Condition	
		Swing Level	Pre-emphasis Level
00	0	400mV diff p-p	0dB
	1		6dB
01	0	600mV diff p-p	0dB
	1		3.5dB
10	*	800mV diff p-p	0dB
11	*	Forbidden	

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Permanent Clock Output (THCV236 only)

When there is no input from Main-Link, the THCV236 will output internal oscillator clock from CLKOUT pin. This function is controlled by OUTSEL pin or OUTSEL_ENABLE register and OUTSEL_SETTING register. See Table 6 and Table 7.

Table 6. Permanent Clock Output function table (PDN1=0)

OUTSEL (pin)	Output Clock Frequency(*1)
0	-
1	40MHz

*1 typical value

Table 7. Permanent Clock Output function table (PDN1=1)

OUTSEL_ ENABLE (register)	OUTSEL_ SETTING (register)	Output Clock Frequency(*1)
0	*	-
1	00	80MHz
	01	40MHz(default)
	10	20MHz
	11	10MHz

*1 typical value

Spread Spectrum Clock Generator (SSCG)

The THCV235 serial data output and the THCV236 parallel data and clock outputs are modulated by programmable SSCG. The THCV235 SSCG is enabled by SSEN pin or SSEN register. The THCV236 SSCG is enabled by only SSEN register. The modulation rate and modulation frequency variation of output spread is controlled through the SSCG control registers on each device. Do not enable spread spectrum for both the THCV235 and THCV236 at the same time.

Table 8. SSCG enable signal (THCV235)

PDN1	SUBMODE	Mode Entry Signal	Description
0	* (Function as HTPDN)	SSEN (pin)	0:SSCG Disable 1:SSCG Enable
1	0	SSEN (register)	
	1	SSEN (pin)	

Table 9. SSCG enable signal (THCV236)

PDN1	SUBMODE	Mode Entry Signal	Description
*	*	SSEN(register)	0:SSCG Disable 1:SSCG Enable

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When customer use the mode and frequency range shown in Table 10, register setting is required according to Table 11.

Table 10. Main-Link mode and frequency range requiring register setting

Mode Setting					Freq.Range[MHz] (SSCG Enable)		Register Setting (*2)
MAINMODE	HFSEL	LFSEL	COL1	COL0	min	max	
0	0	0	(*1)	0	26.6	50	Case1
0	0	0	(*1)	1	33.3	66.6	Case2
0	1	0	(*1)	(*1)	50	100	Case3
1	0	0	0	0	26.6	40	Case1
1	0	0	0	1	26.6	50	Case1
1	0	0	1	0	33.3	66.6	Case2
1	1	0	(*1)	(*1)	50	100	Case3

*1 Don't care
*2 See Table 11

Table 11. SSCG register setting

Step	Register Address(HEX)		Register Value(HEX)				Description
	Sub-Link Master side	Sub-Link Slave side	Case1	Case2	Case3		
					THCV235	THCV236	
1	0x70	0xF0	0x01				Set 1 to PLL_SET_EN
2	0x76	0xF6	0x02		0x02	0x01	Set PLL_SET0
3	0x78	0xF8	0x3C	0x30	0x20		Set PLL_SET1
4	0x7C	0xFC	0x35	0x34	0x24		Set PLL_SET2

Modulation frequency f_{mod} can be determined by HFSEL and LFSEL settings, input clock frequency and FMOD register setting (default value 0xD). Refer to following formula.

$$f_{\mathrm{mod}} = \frac{f_{CLKSSCG}}{128 \times FMOD}$$

$f_{CLKSSCG}$ is the frequency listed in Table 12 and Table 13.

Table 12. $f_{CLKSSCG}$ (THCV235)

HFSEL	LFSEL	$f_{CLKSSCG}$
0	0	(1/tTCIP)/2
0	1	1/tTCIP
1	0	(1/tTCIP)/4
1	1	Forbidden Setting

Table 13. $f_{CLKSSCG}$ (THCV236)

HFSEL	LFSEL	$f_{CLKSSCG}$
0	0	(1/tRCP)/2
0	1	1/tRCP
1	0	(1/tRCP)/4
1	1	Forbidden Setting

Up to 0.5 % spread at the 30kHz modulation frequency is stable for most cases. In case of using out of this range, please verify at the actual system.

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Data Enable

Figure 2 is the conceptual diagram of the V-by-One® HS mode operation (MAINMODE=0) of the chipset.

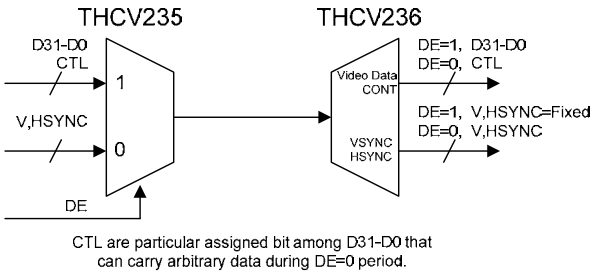
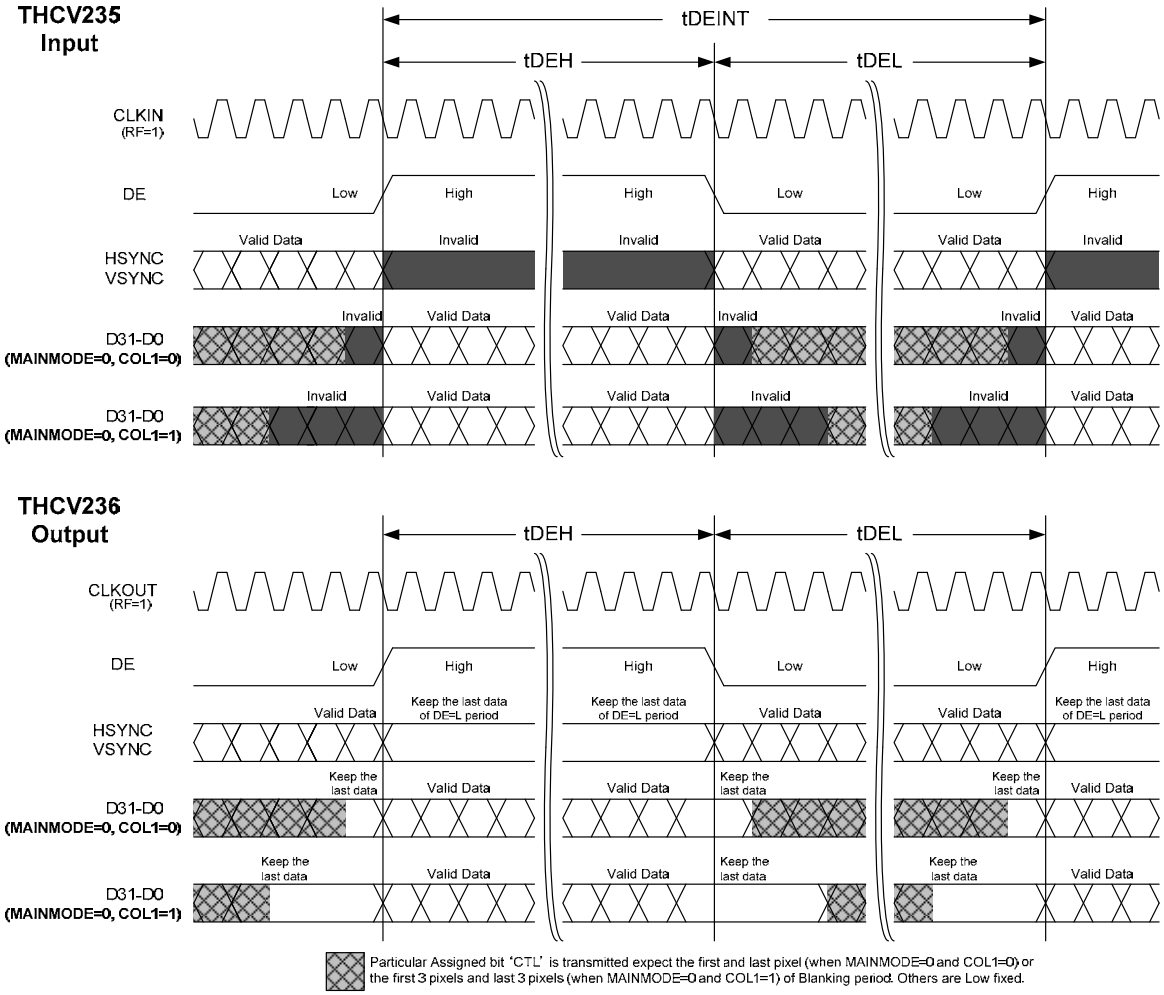


Figure 2. Conceptual Diagram of the Basic Operation of the Chipset in V-by-One® HS mode

There are some requirements for DE. Figure 3 shows the timing diagram of it.



Note: In V-by-One® HS Mode (MAINMODE=0) and High Frequency Mode (HFSEL=1), the period between rising edges of DE (tDEINT), high time of DE (tDEH) should always satisfy following equations.

$$tDEH = tTCIP*(2m)$$
$$tDEINT = tTCIP*(2n)$$
$$m,n=2,3,4,5,6\ldots\ldots$$

Figure 3. Data and Synchronizing Signals Transmission Timing Diagram in V-by-One® HS mode

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Table 14. DE Requirement

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tDEH	DE=1 Duration	MAINMODE=0 HFSEL=0	2×tTCIP	-	-	ns
		MAINMODE=0 HFSEL=1	4×tTCIP	-	-	ns
		MAINMODE=1	Don't care			
tDEL	DE=0 Duration	MAINMODE=0 HFSEL=0	2×tTCIP	-	-	ns
		MAINMODE=0 HFSEL=1	4×tTCIP	-	-	ns
		MAINMODE=1	Don't care			

Hot-Plug Function

HTPDN signal indicates connecting condition between the Transmitter and the Receiver. HTPDN of the transmitter side is high when the Receiver is not active or not connected. Then Transmitter can enter into the power down mode. HTPDN is set to low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training.

When PDN1 = 0 (Sub-Link Power Down), HTPDN is transferred to Transmitter by HTPDN pin.
HTPDN is open-drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

HTPDN connection between the Transmitter and the Receiver can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken as low.

When PDN1 = 1 (Sub-Link Active), HTPDN is transferred to Transmitter via Sub-Link line.
HTPDN/SUBMODE pin functions as Sub-Link mode select (SUBMODE). HOST MPU can confirm HTPDN state by reading Sub-Link Master register (0x00 bit0 HTPDN).

Lock Detect Function

LOCKN indicates whether the receiver CDR PLL is in the lock state or not. LOCKN at the Transmitter input is set to High by pull-up resistor when Receiver is not active or at the CDR PLL training state. LOCKN is set to low by the Receiver when CDR lock is done. Then the CDR training mode finishes and Transmitter shifts to the normal operation.

When PDN1 = 0 (Sub-Link Power Down), LOCKN is transferred to Transmitter by LOCKN pin. LOCKN is open-drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

When HTPDN is included in an application, the LOCKN signal should only be considered when the HTPDN is pulled low by the Receiver.

When PDN1 = 1 (Sub-Link Active), LOCKN is transferred via Sub-Link line. LOCKN/MSSEL pin functions as Sub-Link Master/Slave select (MSSEL). HOST MPU can confirm LOCKN state by reading Sub-Link Master register (0x00 bit1 LOCKN).

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Table 15. HTPDN,LOCKN transmission route setting

PDN1	HTPDN,LOCKN
0	HTPDN, LOCKN are transmitted via external DC signal.
1	HTPDN, LOCKN are transmitted via Sub-Link.

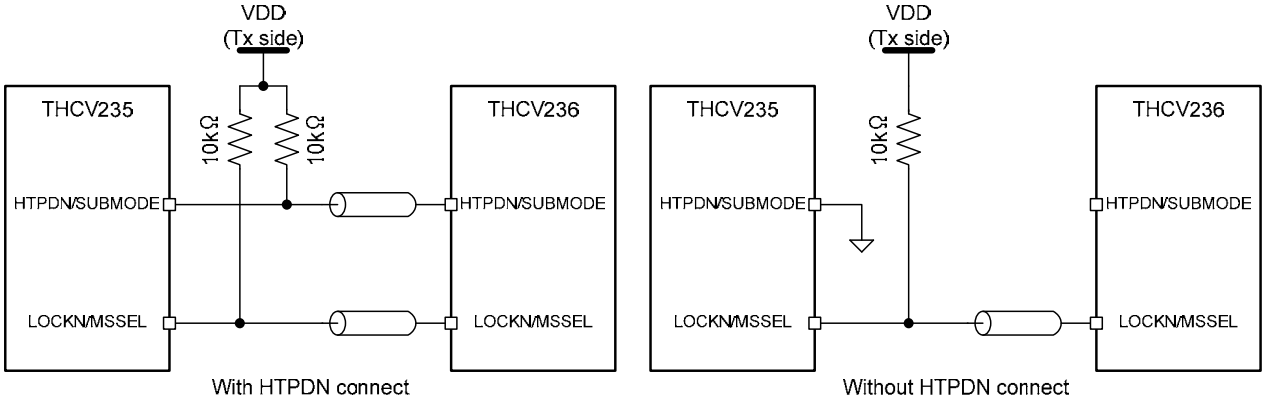


Figure 4. Hot-plug and Lock Detect Scheme when PDN1=0

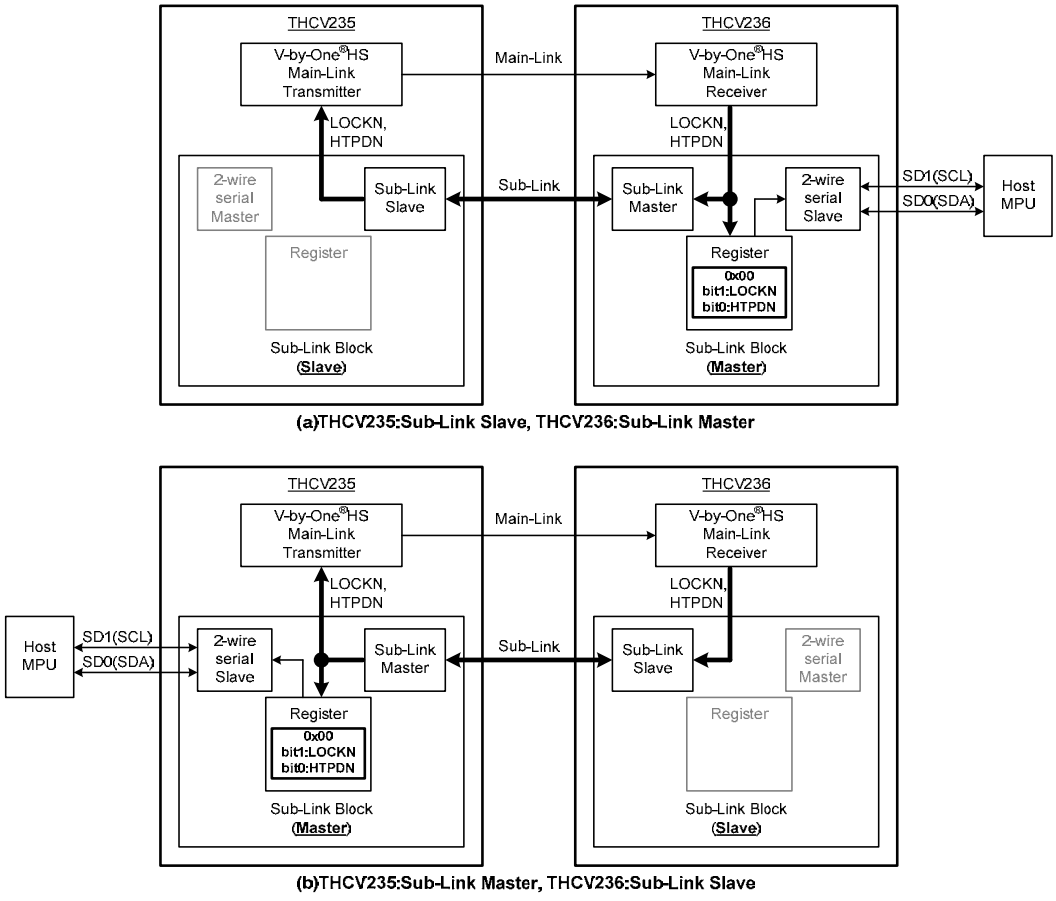


Figure 5. HTPDN,LOCKN transmission route when PDN1=1

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Field BET Operation

In order to help users to check validity of CML serial line (Main-Link and Sub-Link), the THCV235 and THCV236 have an operation mode in which they act as a bit error tester (BET). In Main-Link Field BET mode, the THCV235 internally generates test pattern which is then serialized onto the Main-Link CML line. The THCV236 also has BET function mode. The THCV236 receives the data stream and checks bit errors. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto the CML channel. As for the THCV236, the internal test pattern check circuit gets enabled and reports result on a certain pin named BETOUT. In Sub-Link Field BET mode, Sub-Link Master device internally generates test pattern which is then serialized onto the Sub-Link CML line. Sub-Link Slave device also has BET function mode. Sub-Link Slave device receives the data stream and checks bit errors. Note that Sub-Link Slave device must be set this mode prior to Sub-Link Master device. Pattern check result is output from BETOUT pin of the Sub-Link Slave device. The BETOUT pin goes LOW whenever bit errors occur, or it stays HIGH when there is no bit error.

In Main-Link Field BET mode, user can select two kinds of check result, latched result or NOT latched result by setting LATEN pin input. The latched result is reset by setting LATEN=0. In Sub-Link Field BET mode, only latched result is available. In order to reset the latched result, please once turn off the power and entry Sub-Link Field BET from power on sequence.

LATEN/SD3/AIN1/GPIO4 pin (THCV235) and LATEN/SD3/AIN1/GPIO0 pin (THCV236) function as LATEN in Field BET mode (Main-Link or Sub-Link).

It is not possible to realize Main-Link Field BET and Sub-Link Field BET at the same time.

Table 16. Main-Link Field BET Operation Settings

THCV235/236 Common Setting					THCV236 Setting	Condition		
PDN0	PDN1	SUBMODE	BET	BET_SEL	LATEN	Main-Link	Sub-Link	Output Latch Select
1	0	-	1 (*1)	0 (*3)	0	Field BET Operation	Power Down	NOT Latched Result
					1			Latched Result
	1	1	1 (*1)	0 (*3)	0		Normal Operation	NOT Latched Result
					1			Latched Result
		0	1 (*2)	0 (*4)	0			NOT Latched Result
					1			Latched Result

*1 Pin setting
*2 THCV235: Register setting (0x53 bit1), THCV236: Pin setting
*3 When PDN0=1, PDN1=0 and BET=1 or PDN0=1, PDN1=1, SUBMODE=1 and BET=1, BET_SEL is set to 0 automatically.
*4 Register setting (0x53 bit0, Default 0)

Table 17. THCV236 Main-Link Field BET Result

BETOUT	Output
L	Bit Error Occurred
H	No Error

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Table 18. Sub-Link Field BET Operation Setting

THCV235/THCV236 Common Setting					THCV235 Setting		THCV236 Setting		Condition		
PDN0	PDN1	SUBMODE	BET	BET_SEL	MSSEL	LATEN	MSSEL	LATEN	Main-Link	Sub-Link	Output Latch Select
0	1	1	1 (*1)	1 (*3)	0	-	1	1 (*5)	Power Down	Field BET Operation	Latched Result
					1	1 (*5)	0	-			
		0	1 (*2)	1 (*4)	0	-	1	1 (*5)			
					1	1 (*5)	0	-			

*1 Pin setting. Note that BET pin should be 0 at power on sequence.
*2 THCV235: Register setting (0x53 bit1), THCV236: Pin setting. Note that BET pin should be 0 at power on sequence.
*3 When PDN0=0, PDN1=1, SUBMODE=1 and BET=1, BET_SEL is set to 1 automatically.
*4 Register setting (0x53 bit0, Default 0)
*5 Forbidden 0 setting

Table 19. Sub-Link Slave device Sub-Link Field BET Result

BETOUT	Output
L	Bit Error Occurred
H	No Error

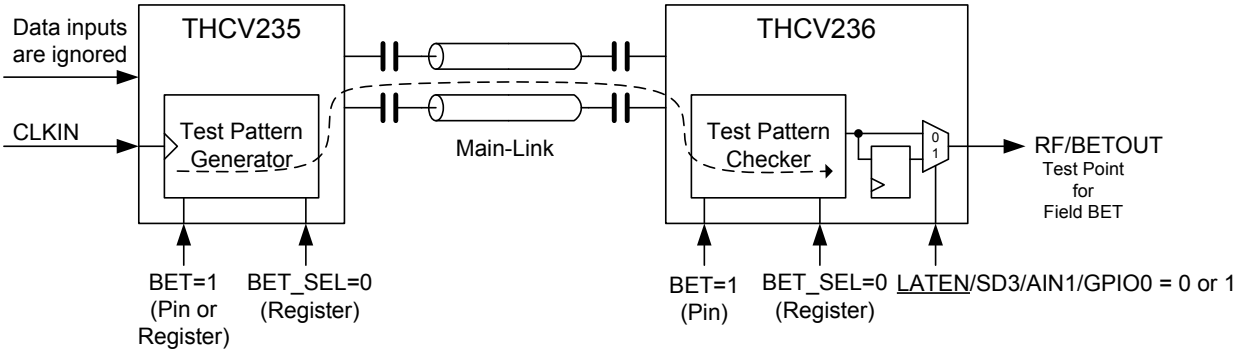


Figure 6. Main-Link Field BET Configuration

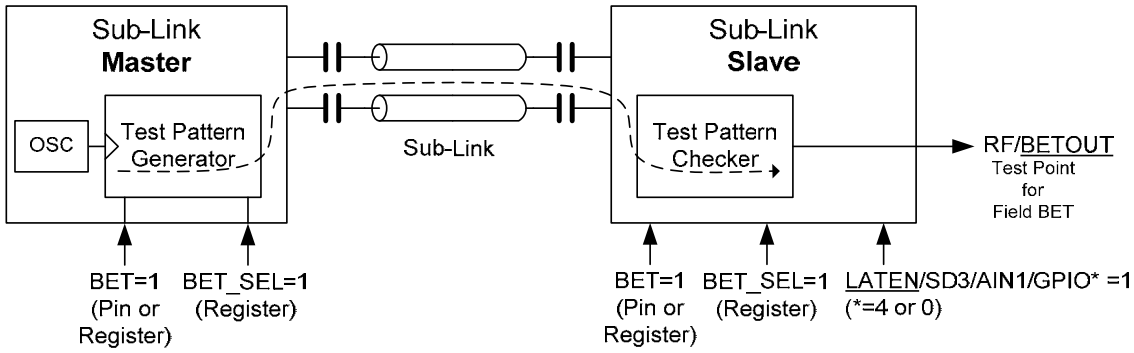


Figure 7. Sub-Link Field BET Configuration

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Data Width and Frequency Range Select Function

The THCV235 and THCV236 support a variety of data width and frequency range. Frequency range is different depending on the mode setting and SSCG enable and disable setting. Refer to Table 20 and Table 21 for details.

Table 20. Main-Link Operation Mode Select (PDN1=1 and SUBMODE=0)

Mode Setting					Freq.Range [MHz]				Main-Link CML Bit Rate	Data Width		Comment
					SSCG Disable		SSCG Enable (*1)					
MAIN MODE	HFSEL	LFSEL	COL1	COL0	min	max	min	max		Data	Sync	
0	0	0	0	0	15	100	26.6	100	x40	32	3	-
0	0	0	0	1	20	133.3	33.3	133.3	x30	24	3	-
0	0	0	1	0	15	100	26.6	100	x40	32	3	Color Space Conversion
0	0	0	1	1	20	133.3	33.3	133.3	x30	24	3	Color Space Conversion
0	0	1	0	0	7.5	15	16.4	32.5	x80	32	3	-
0	0	1	0	1	10	20	19.2	38	x60	24	3	-
0	0	1	1	0	7.5	15	16.4	32.5	x80	32	3	Color Space Conversion
0	0	1	1	1	10	20	19.2	38	x60	24	3	Color Space Conversion
0	1	0	0	0	50	70	50	70	x25	20	3	(*2)
					70	160	70	160				-
0	1	0	0	1	50	70	50	70	x20	16	3	(*2)
					70	160	70	160				-
0	1	0	1	0	50	70	50	70	x25	30	3	Color Space Conversion. (*2)
					70	160	70	160				Color Space Conversion
0	1	0	1	1	50	70	50	70	x20	24	3	Color Space Conversion. (*2)
					70	160	70	160				Color Space Conversion
0	1	1	*	*	-	-	-	-	-	-		Forbidden
1	0	0	0	0	12	80	26.6	80	x50	35		-
1	0	0	0	1	15	100	26.6	100	x40	30		-
1	0	0	1	0	20	133.3	33.3	133.3	x30	22		-
1	0	0	1	1	-	-	-	-	-	-		Forbidden
1	0	1	0	0	6	12	16.4	32.6	x100	35		-
1	0	1	0	1	7.5	15	16.4	32.6	x80	30		-
1	0	1	1	0	10	20	19	38	x60	22		-
1	0	1	1	1	-	-	-	-	-	-		Forbidden
1	1	0	0	0	50	70	50	70	x25	19		(*2)
					70	160	70	160				-
1	1	0	0	1	50	70	50	70	x20	15		(*2)
					70	160	70	160				-
1	1	0	1	0	50	70	50	70	x15	11		(*2)
					70	160	70	160				-
1	1	0	1	1	-	-	-	-	-	-		Forbidden
1	1	1	*	*	-	-	-	-	-	-		Forbidden

*1 Note that register setting is required depending on the mode setting and used frequency range. See Table 10.
*2 Register setting is required. See Table 21.

Table 21. Register setting (HFSEL=1 and Frequency range is from 50MHz to 70MHz)

Step	Register Address(HEX)		Register Value(HEX)		Description
	Sub-Link Master side	Sub-Link Slave side	THCV235	THCV236	
1	0x70	0xF0	0x01		Set 1 to PLL_SET_EN
2	0x76	0xF6	0x02	0x01	Set PLL_SET0
3	0x78	0xF8	0x20		Set PLL_SET1
4	0x7C	0xFC	0x24		Set PLL_SET2

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Table 22. Main-Link Operation Mode Select (PDN1=0 or PDN1=1 and SUBMODE=1)

Mode Setting					Freq.Range [MHz]				Main-Link CML Bit Rate	Data Width		Comment
					SSCG Disable		SSCG Enable (THCV235 Only)					
MAIN MODE	HFSEL	LFSEL	COL1	COL0	min	max	min	max		Data	Sync	
0	0	0	0	0	15	100	50	100	x40	32	3	-
0	0	0	0	1	20	133.3	66.6	133.3	x30	24	3	-
0	0	0	1	0	15	100	50	100	x40	32	3	Color Space Conversion
0	0	0	1	1	20	133.3	66.6	133.3	x30	24	3	Color Space Conversion
0	0	1	0	0	7.5	15	16.4	32.5	x80	32	3	-
0	0	1	0	1	10	20	19.2	38	x60	24	3	-
0	0	1	1	0	7.5	15	16.4	32.5	x80	32	3	Color Space Conversion
0	0	1	1	1	10	20	19.2	38	x60	24	3	Color Space Conversion
0	1	0	0	0	70	160	100	160	x25	20	3	-
0	1	0	0	1	70	160	100	160	x20	16	3	-
0	1	0	1	0	70	160	100	160	x25	30	3	Color Space Conversion
0	1	0	1	1	70	160	100	160	x20	24	3	Color Space Conversion
0	1	1	*	*	-	-	-	-	-	-		Forbidden
1	0	0	0	0	12	80	40	80	x50	35		-
1	0	0	0	1	15	100	50	100	x40	30		-
1	0	0	1	0	20	133.3	66.6	133.3	x30	22		-
1	0	0	1	1	-	-	-	-	-	-		Forbidden
1	0	1	0	0	6	12	16.4	32.5	x100	35		-
1	0	1	0	1	7.5	15	16.4	32.5	x80	30		-
1	0	1	1	0	10	20	19.2	38	x60	22		-
1	0	1	1	1	-	-	-	-	-	-		Forbidden
1	1	0	0	0	70	160	100	160	x25	19		-
1	1	0	0	1	70	160	100	160	x20	15		-
1	1	0	1	0	70	160	100	160	x15	11		-
1	1	0	1	1	-	-	-	-	-	-		Forbidden
1	1	1	*	*	-	-	-	-	-	-		Forbidden

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Data Mapping

Table 23. V-by-One® HS Mode Data Mapping

MAINMODE	0	0	0	0	0	0	0	0	0	0	0	0
HFSEL	0	0	0	0	0	0	0	0	1	1	1	1
LFSEL	0	0	0	0	1	1	1	1	0	0	0	0
COL1	0	0	1	1	0	0	1	1	0	0	1	1
COL0	0	1	0	1	0	1	0	1	0	1	0	1
D0	R2	R0	R2	R0	R2	R0	R2	R0	Cb/Cr2	Cb/Cr0	R2	R0
D1	R3	R1	R3	R1	R3	R1	R3	R1	Cb/Cr3	Cb/Cr1	R3	R1
D2	R4	R2	R4	R2	R4	R2	R4	R2	Cb/Cr4	Cb/Cr2	R4	R2
D3	R5	R3	R5	R3	R5	R3	R5	R3	Cb/Cr5	Cb/Cr3	R5	R3
D4	R6	R4	R6	R4	R6	R4	R6	R4	Cb/Cr6	Cb/Cr4	R6	R4
D5	R7	R5	R7	R5	R7	R5	R7	R5	Cb/Cr7	Cb/Cr5	R7	R5
D6	R8	R6	R8	R6	R8	R6	R8	R6	Cb/Cr8	Cb/Cr6	R8	R6
D7	R9	R7	R9	R7	R9	R7	R9	R7	Cb/Cr9	Cb/Cr7	R9	R7
D8	G2	G0	G2	G0	G2	G0	G2	G0	Y2	Y0	G2	G0
D9	G3	G1	G3	G1	G3	G1	G3	G1	Y3	Y1	G3	G1
D10	G4	G2	G4	G2	G4	G2	G4	G2	Y4	Y2	G4	G2
D11	G5	G3	G5	G3	G5	G3	G5	G3	Y5	Y3	G5	G3
D12	G6	G4	G6	G4	G6	G4	G6	G4	Y6	Y4	G6	G4
D13	G7	G5	G7	G5	G7	G5	G7	G5	Y7	Y5	G7	G5
D14	G8	G6	G8	G6	G8	G6	G8	G6	Y8	Y6	G8	G6
D15	G9	G7	G9	G7	G9	G7	G9	G7	Y9	Y7	G9	G7
D16	B2(*1)	B0(*1)	B2(*1)	B0(*1)	B2(*1)	B0(*1)	B2(*1)	B0(*1)	-	-	B2	B0
D17	B3(*1)	B1(*1)	B3(*1)	B1(*1)	B3(*1)	B1(*1)	B3(*1)	B1(*1)	-	-	B3	B1
D18	B4(*1)	B2(*1)	B4(*1)	B2(*1)	B4(*1)	B2(*1)	B4(*1)	B2(*1)	-	-	B4	B2
D19	B5(*1)	B3(*1)	B5(*1)	B3(*1)	B5(*1)	B3(*1)	B5(*1)	B3(*1)	-	-	B5	B3
D20	B6(*1)	B4(*1)	B6(*1)	B4(*1)	B6(*1)	B4(*1)	B6(*1)	B4(*1)	-	-	B6	B4
D21	B7(*1)	B5(*1)	B7(*1)	B5(*1)	B7(*1)	B5(*1)	B7(*1)	B5(*1)	-	-	B7	B5
D22	B8(*1)	B6(*1)	B8(*1)	B6(*1)	B8(*1)	B6(*1)	B8(*1)	B6(*1)	-	-	B8	B6
D23	B9(*1)	B7(*1)	B9(*1)	B7(*1)	B9(*1)	B7(*1)	B9(*1)	B7(*1)	-	-	B9	B7
D24	CONT1 (*1,*2)	-	CONT1 (*1,*2)	-	CONT1 (*1,*2)	-	CONT1 (*1,*2)	-	-	-	-	-
D25	CONT2 (*1,*2)	-	CONT2 (*1,*2)	-	CONT2 (*1,*2)	-	CONT2 (*1,*2)	-	-	-	-	-
D26	B0(*1)	-	B0(*1)	-	B0(*1)	-	B0(*1)	-	-	-	B0	-
D27	B1(*1)	-	B1(*1)	-	B1(*1)	-	B1(*1)	-	-	-	B1	-
D28	G0(*1)	-	G0(*1)	-	G0(*1)	-	G0(*1)	-	Y0(*1)	-	G0(*1)	-
D29	G1(*1)	-	G1(*1)	-	G1(*1)	-	G1(*1)	-	Y1(*1)	-	G1(*1)	-
D30	R0(*1)	-	R0(*1)	-	R0(*1)	-	R0(*1)	-	Cb/Cr0(*1)	-	R0(*1)	-
D31	R1(*1)	-	R1(*1)	-	R1(*1)	-	R1(*1)	-	Cb/Cr1(*1)	-	R1(*1)	-
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

*1 CTL bits, which are carried during DE=0 except the first pixel and the last pixel (when COL1=0) or the first 3pixels and the last 3pixels (when COL1=1).
*2 User defined data inputs (THCV235) and outputs (THCV236).

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Table 24. Sync Free Mode Data Mapping

MAINMODE	1	1	1	1	1	1	1	1	1	1	1	1
HFSEL	0	0	0	0	0	0	0	0	1	1	1	1
LFSEL	0	0	0	0	1	1	1	1	0	0	0	0
COL1	0	0	1	1	0	0	1	1	0	0	1	1
COL0	0	1	0	1	0	1	0	1	0	1	0	1
D0	D0	D0	D0	-	D0	D0	D0	-	D0/C0	D0/RAW4	D0/YC0	-
D1	D1	D1	D1	-	D1	D1	D1	-	D1/C1	D1/RAW5	D1/YC1	-
D2	D2	D2	D2	-	D2	D2	D2	-	D2/C2	D2/RAW6	D2/YC2	-
D3	D3	D3	D3	-	D3	D3	D3	-	D3/C3	D3/RAW7	D3/YC3	-
D4	D4	D4	D4	-	D4	D4	D4	-	D4/C4	D4/RAW8	D4/YC4	-
D5	D5	D5	D5	-	D5	D5	D5	-	D5/C5	D5/RAW9	D5/YC5	-
D6	D6	D6	D6	-	D6	D6	D6	-	D6/C6	D6/RAW10	D6/YC6	-
D7	D7	D7	D7	-	D7	D7	D7	-	D7/C7	D7/RAW11	D7/YC7	-
D8	D8	D8	D8	-	D8	D8	D8	-	D8/Y0	D8/RAW0	-	-
D9	D9	D9	D9	-	D9	D9	D9	-	D9/Y1	D9/RAW1	-	-
D10	D10	D10	D10	-	D10	D10	D10	-	D10/Y2	D10/RAW2	-	-
D11	D11	D11	D11	-	D11	D11	D11	-	D11/Y3	D11/RAW3	-	-
D12	D12	D12	D12	-	D12	D12	D12	-	D12/Y4	-	-	-
D13	D13	D13	D13	-	D13	D13	D13	-	D13/Y5	-	-	-
D14	D14	D14	D14	-	D14	D14	D14	-	D14/Y6	-	-	-
D15	D15	D15	D15	-	D15	D15	D15	-	D15/Y7	-	-	-
D16	D16	D16	D16	-	D16	D16	D16	-	-	-	-	-
D17	D17	D17	D17	-	D17	D17	D17	-	-	-	-	-
D18	D18	D18	D18	-	D18	D18	D18	-	-	-	-	-
D19	D19	D19	-	-	D19	D19	-	-	-	-	-	-
D20	D20	D20	-	-	D20	D20	-	-	-	-	-	-
D21	D21	D21	-	-	D21	D21	-	-	-	-	-	-
D22	D22	D22	-	-	D22	D22	-	-	-	-	-	-
D23	D23	D23	-	-	D23	D23	-	-	-	-	-	-
D24	D24	D24	-	-	D24	D24	-	-	-	-	-	-
D25	D25	D25	-	-	D25	D25	-	-	-	-	-	-
D26	D26	D26	-	-	D26	D26	-	-	-	-	-	-
D27	D27	-	-	-	D27	-	-	-	-	-	-	-
D28	D28	-	-	-	D28	-	-	-	-	-	-	-
D29	D29	-	-	-	D29	-	-	-	-	-	-	-
D30	D30	-	-	-	D30	-	-	-	-	-	-	-
D31	D31	-	-	-	D31	-	-	-	-	-	-	-
HSYNC(*1)	HSYNC	HSYNC	HSYNC	-	HSYNC	HSYNC	HSYNC	-	HSYNC	HSYNC	HSYNC	-
VSYNC(*1)	VSYNC	VSYNC	VSYNC	-	VSYNC	VSYNC	VSYNC	-	VSYNC	VSYNC	VSYNC	-
DE(*1)	DE	DE	DE	-	DE	DE	DE	-	DE/FIELD	DE	DE	-

*1 Any signal as well as sync signal can be transmitted.

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Sub-Link Mode Setting

PDN1=1 setting makes Sub-Link active and two modes of Sub-Link operation are available. Sub-Link operation mode is select by SUBMODE pin.

When SUBMODE=0, Sub-Link is 2-wire serial I/F Mode.

When SUBMODE=1, Sub-Link is Low Speed Data Bridge Mode.

SUBMODE must be same setting at the THCV235 and THCV236.Bi-directional communication is done between Sub-Link Master device and Sub-Link Slave device in both modes. MSSEL pin selects Master/Slave side of Sub-Link and 2-wire serial interface in the devices. MSSEL must be different setting at the THCV235 and THCV236. See Table 25 about Sub-Link operation mode settings.

Table 25. Sub-Link operation mode, Master/Slave Setting

SUBMODE	MSSEL	Operation Mode	Sub-Link Master/Slave
0	0	2-wire serial I/F	Sub-Link Master (2-wire serial Slave)
	1		Sub-Link Slave (2-wire serial Master)
1	0	Low Speed Data Bridge	Sub-Link Master
	1		Sub-Link Slave

2-wire serial I/F Mode

2-wire serial I/F Mode enables register access, using GPIO (General Purpose Input/Output) pin and interrupt function. Sub-Link Master device has 2-wire serial slave block and can be connected to HOST MPU, Sub-Link Slave device has 2-wire serial master block and can be connected to remote side 2-wire serial slave devices.

HOST MPU can access register of Sub-Link Master device, Sub-Link Slave device and remote side 2-wire serial slave devices.

2-wire serial I/F Device ID setting

AIN1 and AIN0 pins determine Device ID setting of the THCV235 and THCV236. Only Sub-Link Master device has AIN1 and AIN0 pin. AIN1 and AIN0 choose one of 4 addresses which give an identification address to the THCV235 and THCV236 under 2-wire serial interface bus topology.

Table 26. 2-wire serial I/F Device ID select (Sub-Link Master device Only)

AIN1	AIN0	Device ID
0	0	0x0B
0	1	0x34
1	0	0x77
1	1	0x65

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2-wire serial I/F Clock Stretching

In principle, when Sub-Link bridges 2-wire serial interface communication from Sub-Link Master to Sub-Link Slave or remote side 2-wire serial slave devices, time lag occurs between HOST MPU side 2-wire serial access and Sub-Link Slave internal bus access or remote side 2-wire serial access.

2WIRE_MODE (Sub-Link Master side register, 0x0F bit1-0) selects whether 2-wire serial slave of Sub-Link Master perform clock stretching.

When 2WIRE_MODE = 00, Sub-Link Master device wait HOST MPU until Sub-Link Slave register access or remote side 2-wire serial slave register access is completed by clock stretching.

When 2WIRE_MODE = 01, Sub-Link Master device informs HOST MPU that Sub-Link Slave register access or remote side 2-wire serial register access has been completed by interruption (INT pin) without clock stretching.

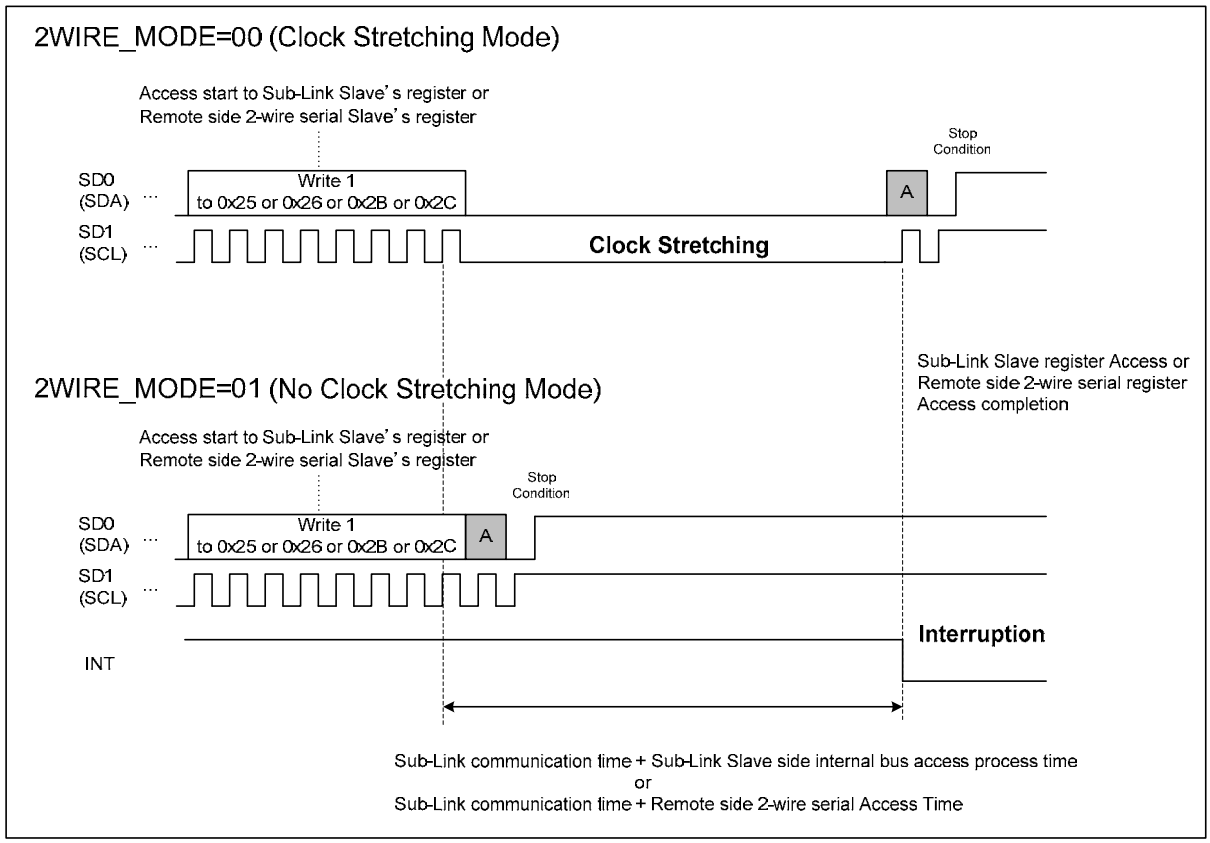


Figure 8. 2WIRE_MODE Operation

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Read/Write access to Sub-Link Master Register

HOST MPU can directly access Sub-Link Master's register by 2-wire serial I/F. Register address of Sub-Link Master is from 0x00 to 0x7F. See **Register Map** for more information.

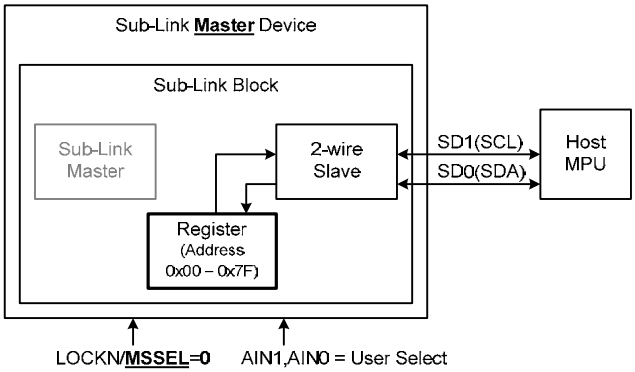


Figure 9. Host to Sub-Link Master Register access configuration

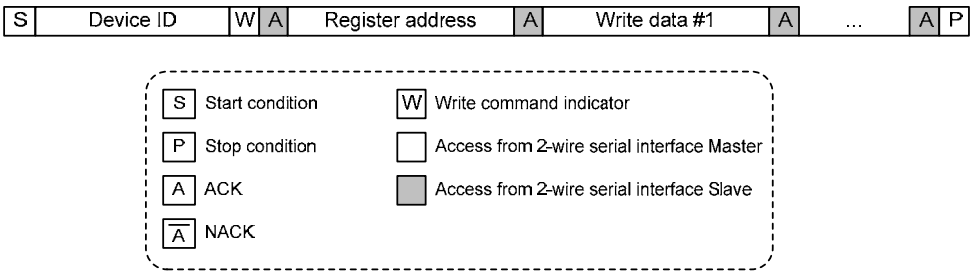


Figure 10. 2-wire serial I/F write to Sub-Link Master register protocol

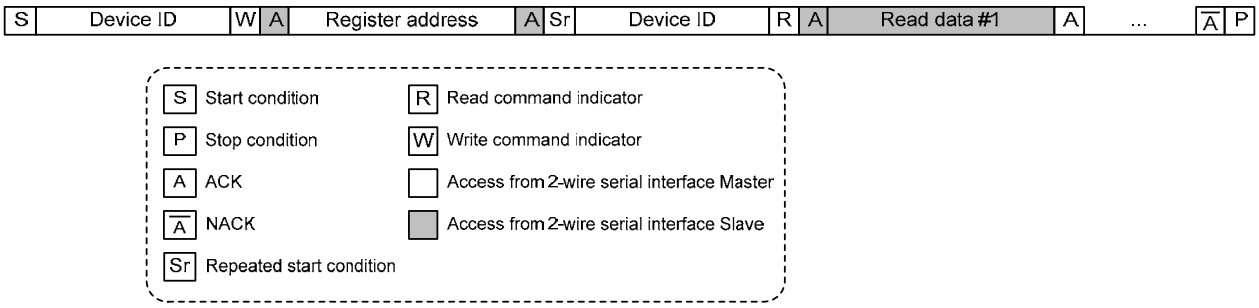


Figure 11. 2-wire serial I/F read to Sub-Link Master register protocol

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Read/Write access to Sub-Link Slave Register

HOST MPU can access to Sub-Link Slave's register via Sub-Link Master by Sub-Link Master register settings. Register address of Sub-Link Slave is from 0x80 to 0xFF. See **Register Map** for more information.

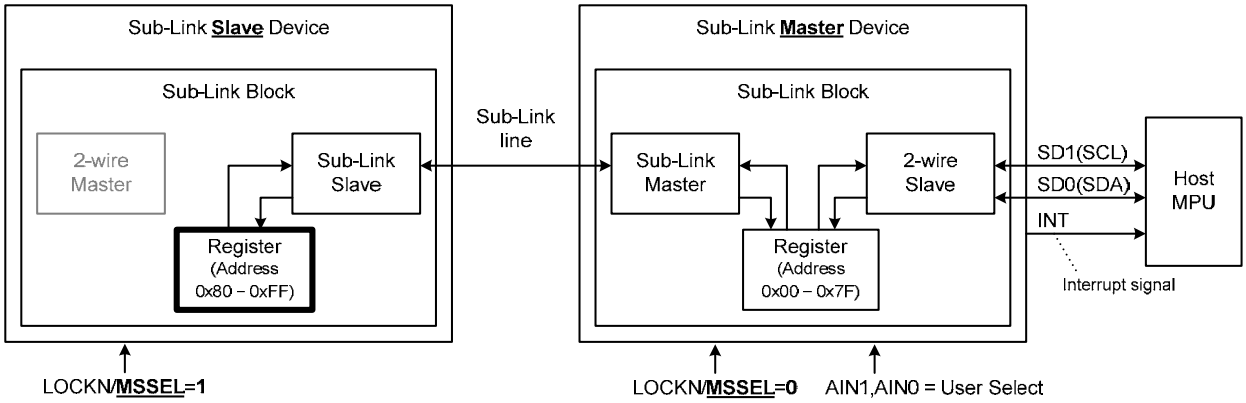


Figure 12. Host MPU to Sub-Link Slave Register access configuration

Table 27. Sub-Link slave register Write Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
2	Set the data for Sub-Link Slave to write (Max 16byte).	W	0x10-0x1F
3	Set Device ID of Sub-Link Master device. (Value corresponding to AIN1 and AIN0 setting. e.g.[AIN1,AIN0]=[0,0] → 7'h0B)	W	0x20
4	Set the byte number written to Sub-Link Slave (Max 16byte) (Byte number = register value + 1)	W	0x21
5	Set the start address of Sub-Link Slave register to write.	W	0x23
6	Write 1 to WR_START_8B. (Start write access to Sub-Link Slave register)	W	0x25 (*1)
7 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed.	-	-
7 (*3)	When write access is completed, 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
8	If write access was normally ended, read value should be "0x1".	R	0x02 bit7

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.
*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)
*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

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Table 28. Sub-Link slave register Read Procedure

Step	Description	R/W	Address
1	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
2	Set Device ID of Sub-Link Master device. (Value corresponding to AIN1 and AIN0 setting. e.g.[AIN1,AIN0]=[0,0] → 7'h0B)	W	0x20
3	Set the byte number read from Sub-Link Slave(Max 16byte). (Byte number = register value + 1)	W	0x22
4	Set the start address of Sub-Link Slave register to read.	W	0x24
5	Write 1 to RD_START_8B. (Start read access to Sub-Link Slave register)	W	0x26 (*1)
6 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x10-0x1F).	-	-
6 (*3)	When read access is completed, read data is stored in Sub-Link Master register (Address 0x10-0x1F) and 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
7	If read access was normally ended, read value should be "0x1".	R	0x02
8	HOST MPU read data stored in Sub-Link Master register.	R	0x10-0x1F

*1 It's Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.
*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)
*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

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Read/Write access to remote side 2-wire serial slave devices connected to Sub-Link Slave Device

HOST MPU can access to remote side 2-wire serial slave register via Sub-Link Master and Sub-Link Slave by Sub-Link Master register settings. Sub-Link Slave has 2-wire serial master block. Up to 8 devices are connectable to 2-wire serial master of Sub-Link Slave device.

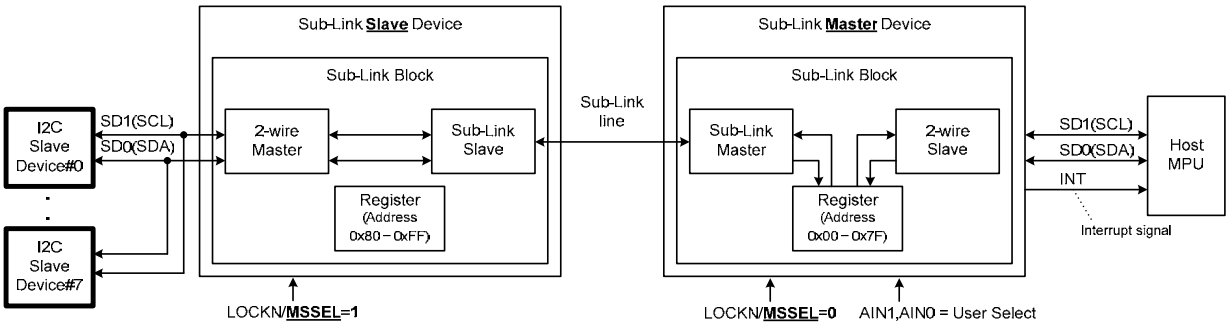


Figure 13. Host to 2-wire serial Slave devices connected to Sub-Link Slave device access configuration

Table 29. Remote side 2-wire serial slave register Write Procedure for 8bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set the data for remote side 2-wire serial slave to write (Max 16byte).	W	0x10-0x1F
4	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B[6:0]), and set 0 to 0x20 bit7.	W	0x20
5	Set the byte number written to remote side 2-wire serial slave (Max 16byte). (Byte number = register value + 1)	W	0x21
6	Set the start address of remote side 2-wire serial slave register to write.	W	0x23
7	Write 1 to WR_START_8B. (Start write access to remote side 2-wire serial slave register)	W	0x25 (*1)
8 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until remote side 2-wire serial slave register access is completed.	-	-
8 (*3)	When write access is completed, 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
9	If wire access was normally ended, read value should be “0x1”.	R	0x02
10	Repeat from step2 to step9 if needed.	-	-

*1 It’s Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.
*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)
*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

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Table 30. Remote side 2-wire serial slave register Write Procedure for 16bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set the data for remote side 2-wire serial slave to write (Max 16byte).	W	0x10-0x1F
4	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B[6:0]), and set 1 to 0x20 bit7.	W	0x20
5	Set the byte number written to remote side 2-wire serial slave (Max 16byte). (Byte number = register value + 1)	W	0x21
6	Set the low-order bits([7:0]) of start address of remote side 2-wire serial slave register to write.	W	0x27
7	Set the high-order bits([15:8]) of start address of remote side 2-wire serial slave register to write.	W	0x28
8	Write 1 to WR_START_16B. (Start write access to remote side 2-wire serial slave register)	W	0x2B (*1)
9 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until remote side 2-wire serial slave register access is completed.	-	-
9 (*3)	When write access is completed, 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
10	If write access was normally ended, read value should be “0x1”.	R	0x02
11	Repeat from step2 to step10 if needed.	-	-

*1 It’s Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.
*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)
*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

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Table 31. Remote side 2-wire serial slave register Read Procedure for 8bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B[6:0]), and set 0 to 0x20 bit7.	W	0x20
4	Set the byte number read from remote side 2-wire serial slave(Max 16byte). (Byte number = register value + 1)	W	0x22
5	Set the start address of remote side 2-wire serial slave register to read.	W	0x24
6	Write 1 to RD_START_8B. (Start read access to remote side 2-wire serial slave register)	W	0x26 (*1)
7 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x10-0x1F).	-	-
7 (*3)	When read access is completed, read data is stored in Sub-Link Master register (Address 0x10-0x1F) and 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
8	If read access was normally ended, read value should be “0x1”.	R	0x02
9	HOST MPU read data stored in Sub-Link Master register.	R	0x10-0x1F
10	Repeat from step2 to step10 if needed.	-	-

*1 It’s Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.
*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)
*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

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Table 32. Remote side 2-wire serial slave register Read Procedure for 16bit register address

Step	Description	R/W	Address
1	Set slave address of remote side 2-wire serial slave device (Low-order 7bits), and enable this address (High-order 1bit).	W	0x04-0x0B
2	Write 1 or 0 and clear(auto clear) access status register (2WIRE_ACS_END_INT).	W	0x02 bit7
3	Set slave address of access target 2-wire serial slave (choose the value set in 0x04-0x0B[6:0]), and set 1 to 0x20 bit7.	W	0x20
4	Set the byte number read from remote side 2-wire serial slave(Max 16byte).	W	0x22
5	Set the low-order bits([7:0]) of start address of remote side 2-wire serial slave register to read.	W	0x29
6	Set the high-order bits([15:8]) of start address of remote side 2-wire serial slave register to read.	W	0x2A
7	Write 1 to RD_START_16B. (Start read access to remote side 2-wire serial slave register)	W	0x2C (*1)
8 (*2)	2-wire serial slave of Sub-Link Master perform clock stretching until Sub-Link Slave register access is completed. When read access is completed, SCL is released and read data is stored in Sub-Link Master register (Address 0x10-0x1F).	-	-
8 (*3)	When read access is completed, read data is stored in Sub-Link Master register (Address 0x10-0x1F) and 2WIRE_ACS_END_INT register value become 1 and interrupt occurs (INT=H → L).	-	-
9	If read access was normally ended, read value should be “0x1”.	R	0x02
10	HOST MPU read data stored in Sub-Link Master register.	R	0x10-0x1F
11	Repeat from step2 to step10 if needed.	-	-

*1 It’s Prohibit that HOST MPU start access to Sub-Link Slave or remote 2-wire serial slave before the previous access to Sub-Link Slave or remote side 2-wire serial slave is completed.
*2 When 2WIRE_MODE = 00 (Clock Stretching Mode)
*3 When 2WIRE_MODE = 01 (No Clock Stretching Mode)

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GPIO

The GPIO pin provides up to 5-I/O ports (THCV235) or 3-I/O ports (THCV236) and 2 types of GPIO are available (“Through GPIO” and “Programmable GPIO”). The number of available GPIO pin depends on Sub-Link operation mode settings (See Table 34 and Table 35). All GPIO pins have another function if being set (See 0, Table 2). GPIO type is selected by GPIO_TYPE register (0x40(Sub-Link Master), 0xC0(Sub-Link Slave)). Programmable GPIO is available by all GPIO pins. Through GPIO is available by only GPIO4 and GPIO3 pin. See Through GPIO section and Programmable GPIO section about detail of respective GPIO type.

Table 33. GPIO Type

GPIO#	GPIO Type	
	Through GPIO	Programmable GPIO
GPIO4	Available	Available
GPIO3		
GPIO2	Unavailable	
GPIO1		
GPIO0		

Table 34. GPIO setting of THCV235

Pin Name	Function	
	Sub-Link Master	Sub-Link Slave
LATEN/SD3/AIN1/GPIO4	AIN1	GPIO4
CMLDRV/SD2/AIN0/GPIO3	AIN0	GPIO3
COL0/INT/GPIO2	INT	GPIO2
BET/GPIO1	GPIO1	GPIO1
SSEN/GPIO0	GPIO0	GPIO0

Table 35. GPIO setting of THCV236

Pin Name	Function		
	Sub-Link Master		Sub-Link Slave
	RXDEFSEL=0	RXDEFSEL=1	
D25/GPIO4	GPIO4	D25	D25
D24/GPIO3	GPIO3	D24	D24
COL0/INT/GPIO2	INT	INT	GPIO2
TTLDRV/SD2/AIN0/GPIO1	AIN0	AIN0	GPIO1
LATEN/SD3/AIN1/GPIO0	AIN1	AIN1	GPIO0

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Through GPIO

Input to GPIO4 and GPIO3 of Sub-Link Master device is output from GPIO4 and GPIO3 of Sub-Link Slave device respectively. Note that these GPIO signals can't be transferred from Sub-Link Slave device to Sub-Link Master device and Through GPIO function is available only when THCV235 is Sub-Link Slave and THCV236 is Sub-Link Master and RXDEFSEL=0. Register settings are required. See Table 36.

It's possible to confirm GPIO4 and GPIO3 input value to Sub-Link Master by register read (0x41 GPIO_INPUT_MONITOR). Each GPIO output signal goes to Low when Sub-Link communication fails. Sub-Link communication status can be observed by register read (0x82 bit2 COMERR_INT).

When the THCV236 is Sub-Link Master and RXDEFSEL=1 (THCV236 has no GPIO4 and GPIO3 input pin as Through GPIO), Through GPIO outputs of THCV235 (Sub-Link Slave) keep low.

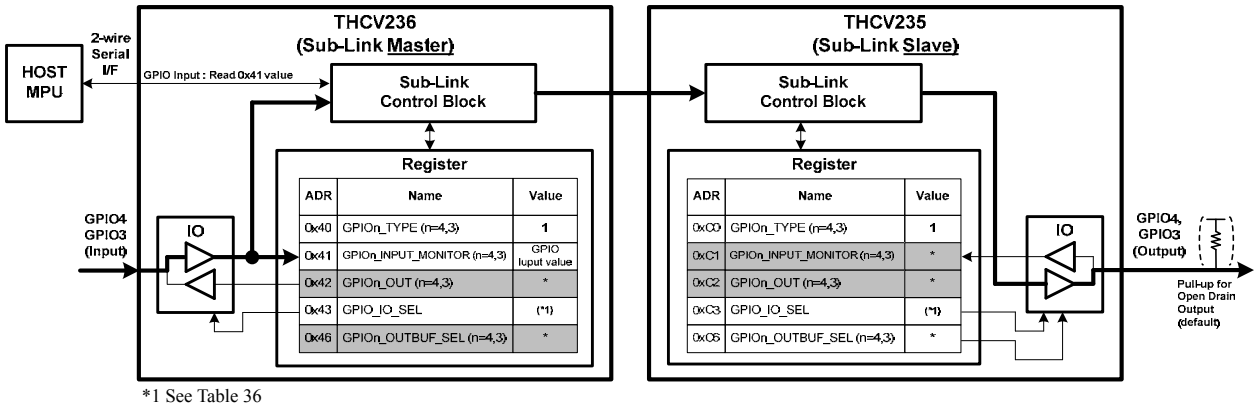


Figure 14. Through GPIO (Only GPIO4 and GPIO3)

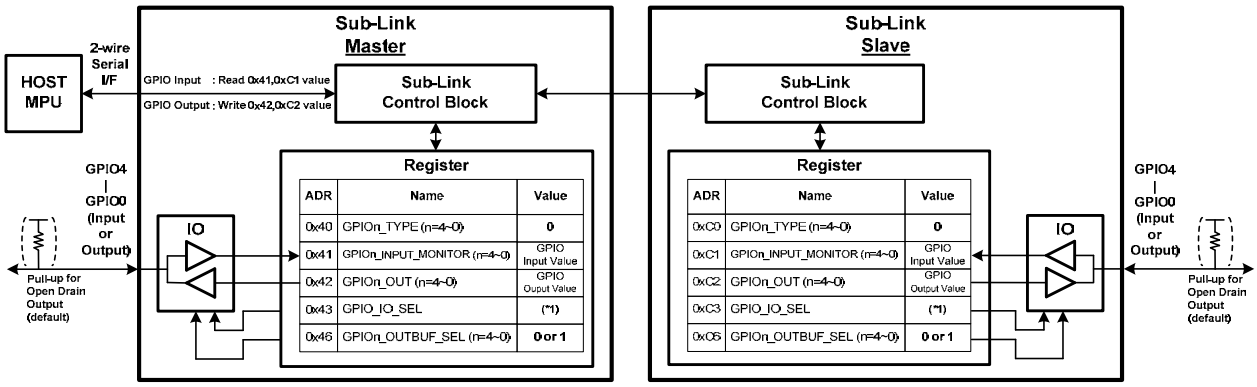
Table 36. THCV235, THCV236(RXDEFSEL=0) Through GPIO register setting

Device	Sub-Link Master/Slave	GPIO Input/Output Number		GPIO4 , GPIO3 Input/Output Configuration (I:Input, O:Output)		Register Settings			
						GPIO Type		GPIO IO Direction	
		Input	Output	GPIO4	GPIO3	Address (HEX)	Value (BIN)	Address (HEX)	Value (BIN)
THCV235	Slave	0	2	O	O	0xC0	XXX11XXX	0xC3	XXX00XXX
THCV236	Master	2	0	I	I	0x40	XXX11XXX	0x43	XXX11XXX

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Programmable GPIO

Settings input/output and reading/writing are controlled by register settings in the Sub-Link Master. HOST MPU commands register setting in the Sub-Link Master.



*1 See Table 37, Table 38

Figure 15. Programmable GPIO

Register settings are required according to the number of GPIO used by customer. See Table 37 and Table 38. When the number of GPIO used by customer is less than the value listed in Table 37 and Table 38, choose any setting which includes that.

Table 37. THCV235 Programmable GPIO register setting

Sub-Link Master/Slave	GPIO Input/Output Number		GPIO4 - GPIO0 Input/Output Configuration (I:Input, O:Output, -:Unavailable)					Register Settings			
								GPIO Type		GPIO IO Direction	
	Input	Output	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	Address (HEX)	Value (BIN)	Address (HEX)	Value (BIN)
Master	2	0	-	-	-	I	I	0x40	XXXXXX00	0x43	XXXXXX11
	1	1	-	-	-	I	O				XXXXXX10
	0	2	-	-	-	O	O				XXXXXX00
Slave	5	0	I	I	I	I	I	0xC0	XXX00000	0xC3	XXX11111
	4	1	I	I	I	I	O				XXX11110
	3	2	I	I	I	O	O				XXX11100
	2	3	I	I	O	O	O				XXX11000
	1	4	I	O	O	O	O				XXX10000
	0	5	O	O	O	O	O				XXX00000

Table 38. THCV236 Programmable GPIO register setting

Sub-Link Master/Slave	GPIO Input/Output Number		GPIO4 – GPIO0 Input/Output Configuration (I:Input, O:Output, -:Unavailable)					Register Settings			
								GPIO Type		GPIO IO Direction	
	Input	Output	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	Address (HEX)	Value (BIN)	Address (HEX)	Value (BIN)
Master	2	0	I	I	-	-	-	0x40	XXX00XXX	0x43	XXX11XXX
	1	1	I	O	-	-	-				XXX10XXX
	0	2	O	O	-	-	-				XXX00XXX
Slave	3	0	-	-	I	I	I	0xC0	XXXXX000	0xC3	XXXXX111
	2	1	-	-	I	O	I				XXXXX101
	1	2	-	-	O	I	O				XXXXX010
	0	3	-	-	O	O	O				XXXXX000

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Interruption

INT pin outputs interrupt event indicator on Sub-Link Master side of the system. The INT signal is active low. Being set by 2-wire serial interface, the THCV235 and THCV236 can monitor any changes of GPIO input pins, Sub-Link communication statuses and internal statuses as an interrupt. About the way to make interruption occur and the way to clear the interruption, see Table 40 (Address 0x02, 0x03) and Table 41 (Address 0x82, 0x83).

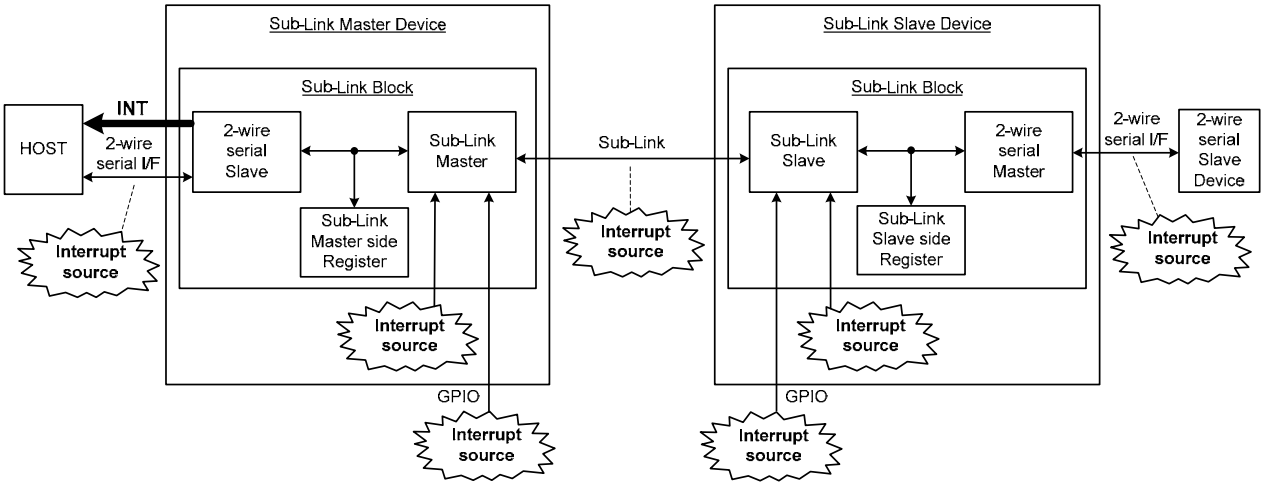


Figure 16. 2-wire serial I/F Interrupt to HOST access configuration

Table 39. Interrupt output

INT	State
L	Interrupt occurred
H	Steady state

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Low Speed Data Bridge Mode

Low speed data input to SD2, SD1 and SD0 of Sub-Link Master device is output respectively from SD2, SD1 and SD0 of Sub-Link Slave device by LVCMOS push pull output buffer. Low speed data input to SD3 of Sub-Link Slave device is output from SD3 of Sub-Link Master device by LVCMOS push pull output buffer.

At Low Speed Data Bridge Mode, access to register of the THCV235 and THCV236 is unable.

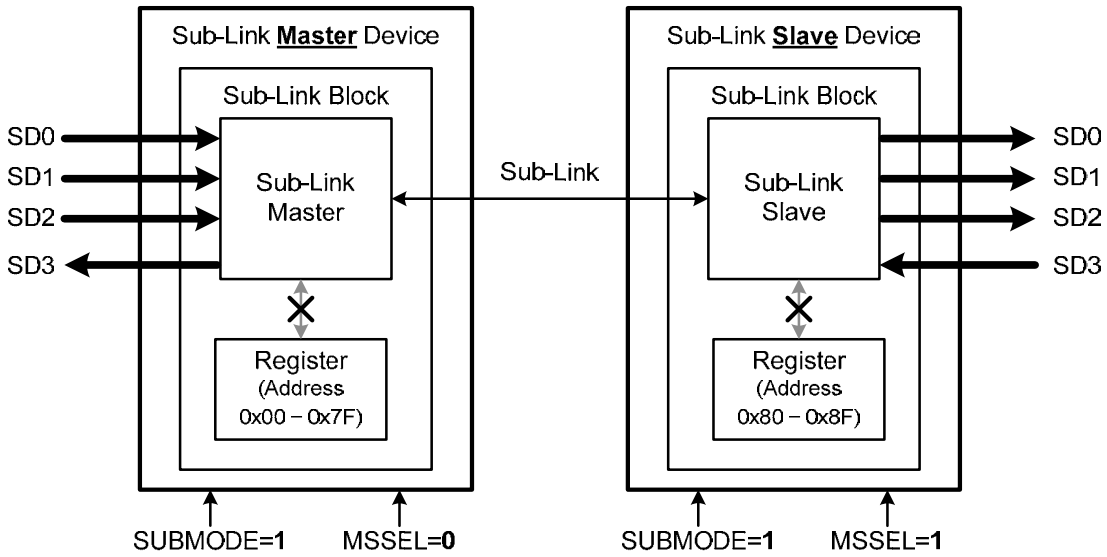


Figure 17. Low Speed Data Bridge Mode configuration

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Register Map

HOST MPU can set various operating conditions of the THCV235 and THCV236 through internal registers. The THCV235 and THCV236 have two types of register address map depending upon Sub-Link configuration.

Sub-Link Master (2-wire serial slave) is connected to external HOST MPU (2-wire serial master).

Sub-Link Slave (2-wire serial master) is connected to external 2-wire serial slave devices.

Sub-Link Master device has address 0x00-0x7F, Sub-Link Slave device has address 0x80-0xFF. See Figure 18.

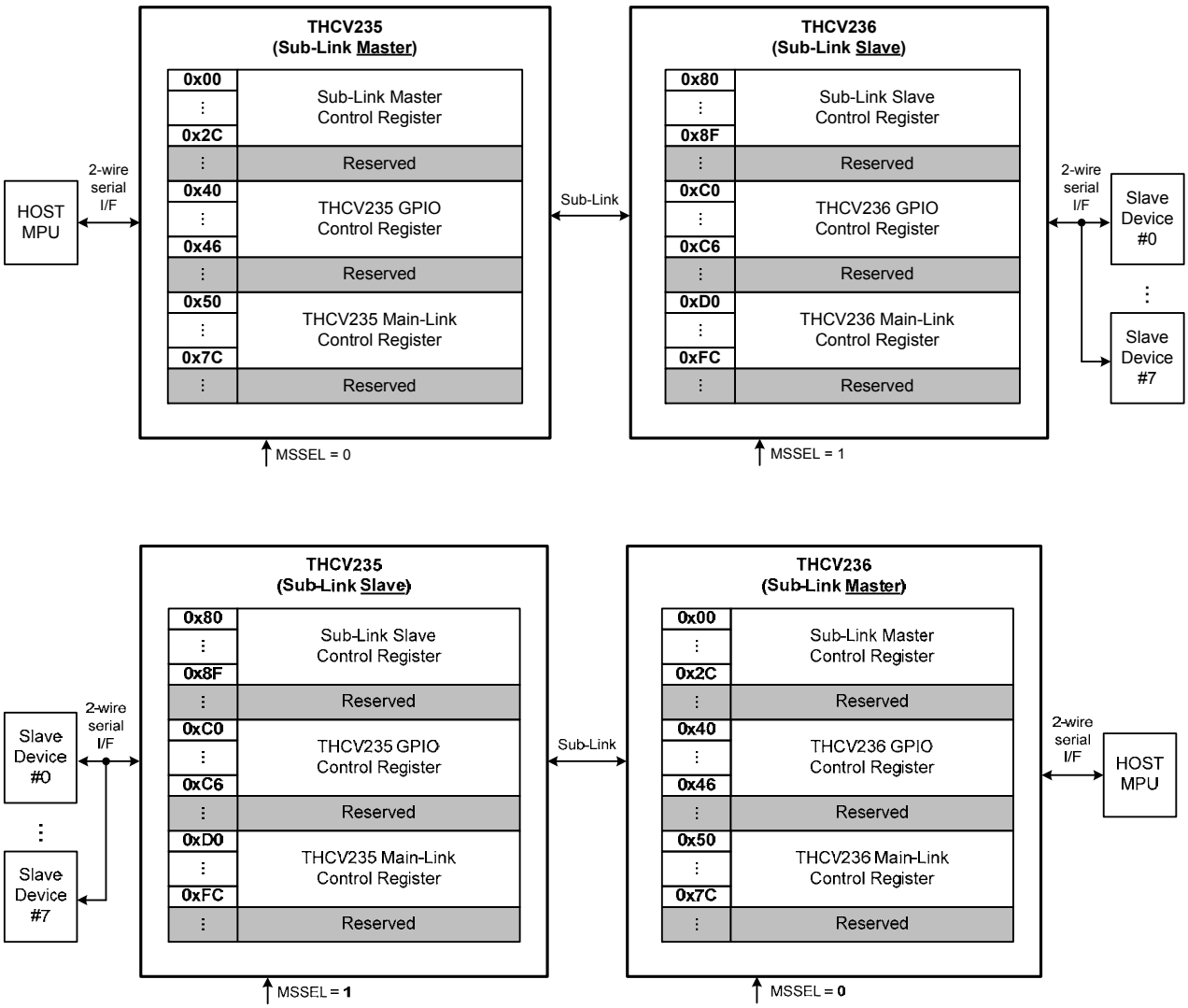


Figure 18. Sub-Link Master/Slave device Register Address configuration

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Table 40. Sub-Link Master Control Register

Address (Hex)	Bit#	R/W	Default (Hex)	Register Name	Description	Note
0x00	7:3	R	0x00	Reserved		-
	2	R	0	INT	Interrupt condition 0: Steady state 1: Interrupt occurred(INT output =L)	-
	1	R	1	LOCKN	V-by-One® HS lock status 0: Locked (LOCKN=L) 1: Unlocked	-
	0	R	1	HTPDN	V-by-One® HS plug status 0: Connected (HTPDN=L) 1: Not connected or Rx inactive	-
0x01	7:1	R	0x00	Reserved		-
	0	RW	0	SFTRST	Sub-Link soft reset Write 1: Sub-Link reset Automatically cleared into 0 after reset action. 0 is always read.	-
0x02	7	RW	0	2WIRE_ACS_END_INT	Cause of interrupt access completion to register of Sub-Link Slave or Remote side 2-wire serial Slave device 0: Access incomplete 1: Access complete Any write action: clear this bit into 0	
	6	RW	0	LOCKN_INT	Cause of interrupt LOCKN 0: No change on lock status ever 1: Lock status has once changed Any write action: clear this bit into 0	
	5	RW	0	HTPDN_INT	Cause of interrupt HTPDN 0: No change on plug status ever 1: Plug status has once changed Any write action: clear this bit into 0	
	4	R	0	SLAVESIDE_INT	Cause of interrupt Sub-Link Slave side 0: No interrupt at Sub-Link Slave ever 1: Interrupted at Sub-Link Slave once This bit is cleared when cause of interrupt register at Sub-Link Slave (0x82) is cleared.	(*1)
	3	R	0	GPIO_INT	Cause of interrupt Sub-Link Master GPIO 0: No change in Master GPIO inputs ever 1: Master GPIO inputs have once changed. This bit is cleared when GPIOn_INPUT_MONITOR (n=4~0) register (0x41) is read.	
	2	RW	0	COMERR_INT	Cause of interrupt Sub-Link communication Error 0: No communication error on Sub-Link ever 1: Communication error on Sub-Link once happened Any write action: clear this bit into 0	
	1	RW	0	2WIRE_TIMEOUT_INT	Cause of interrupt 2-wire serial time out 0: 2-wire serial access in time ever 1: 2-wire serial access has once had time out Any write action: clear this bit into 0	
	0	RW	0	SLINK_TIMEOUT_INT	Cause of interrupt Sub-Link time out 0: Sub-Link access in time ever 1: Sub-Link has once had time out Any write action: clear this bit into 0	
0x03	7	R	(*2)	2WIRE_ACS_END_INT_ENABLE	0: "2WIRE_ACS_END_INT" is blocked to take interrupt action 1: "2WIRE_ACS_END_INT" is allowed to take action on INT output	-
	6	RW	0	LOCKN_INT_ENABLE	0: "LOCKN_INT" is blocked to take interrupt action 1: "LOCKN_INT" is allowed to take action on INT output	-
	5	RW	0	HTPDN_INT_ENABLE	0: "HTPDN_INT" is blocked to take interrupt action 1: "HTPDN_INT" is allowed to take action on INT output	-
	4	RW	0	SLAVESIDE_INT_ENABLE	0: "SLAVESIDE_INT" is blocked to take interrupt action 1: "SLAVESIDE_INT" is allowed to take action on INT output	-
	3	RW	0	GPIO_INT_ENABLE	0: "GPIO_INT" is blocked to take interrupt action 1: "GPIO_INT" is allowed to take action on INT output	-
	2	RW	0	COMERR_INT_ENABLE	0: "COMERR_INT" is blocked to take interrupt action 1: "COMERR_INT" is allowed to take action on INT output	-
	1	RW	0	2WIRE_TIMEOUT_INT_ENABLE	0: "2WIRE_TIMEOUT_INT" is blocked to take interrupt action 1: "2WIRE_TIMEOUT_INT" is allowed to take action on INT output	-
	0	RW	0	SLINK_TIMEOUT_INT_ENABLE	0: "SLINK_TIMEOUT_INT" is blocked to take interrupt action 1: "SLINK_TIMEOUT_INT" is allowed to take action on INT output	-

*1 These registers are always active independent of Interrupt permission register.

*2 When No clock stretching mode, the value is 1 fixed, otherwise 0 fixed.

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Table 40. Sub-Link Master Control Register (continued)

Address (Hex)	Bit#	R/W	Default (Hex)	Register Name	Description	Note
0x04	7	RW	0	2WIRE_DEV_ADDR_0_ENABLE	0: Value in "2WIRE_DEV_ADDR_0" is inactive 1: Value in "2WIRE_DEV_ADDR_0" is active	(*3)
	6:0	RW	0x00	2WIRE_DEV_ADDR_0	Remote side 2-wire serial Slave Device Address #0	
0x05	7	RW	0	2WIRE_DEV_ADDR_1_ENABLE	0: Value in "2WIRE_DEV_ADDR_1" is inactive 1: Value in "2WIRE_DEV_ADDR_1" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_1	Remote side 2-wire serial Slave Device Address #1	
0x06	7	RW	0	2WIRE_DEV_ADDR_2_ENABLE	0: Value in "2WIRE_DEV_ADDR_2" is inactive 1: Value in "2WIRE_DEV_ADDR_2" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_2	Remote side 2-wire serial Slave Device Address #2	
0x07	7	RW	0	2WIRE_DEV_ADDR_3_ENABLE	0: Value in "2WIRE_DEV_ADDR_3" is inactive 1: Value in "2WIRE_DEV_ADDR_3" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_3	Remote side 2-wire serial Slave Device Address #3	
0x08	7	RW	0	2WIRE_DEV_ADDR_4_ENABLE	0: Value in "2WIRE_DEV_ADDR_4" is inactive 1: Value in "2WIRE_DEV_ADDR_4" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_4	Remote side 2-wire serial Slave Device Address #4	
0x09	7	RW	0	2WIRE_DEV_ADDR_5_ENABLE	0: Value in "2WIRE_DEV_ADDR_5" is inactive 1: Value in "2WIRE_DEV_ADDR_5" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_5	Remote side 2-wire serial Slave Device Address #5	
0x0A	7	RW	0	2WIRE_DEV_ADDR_6_ENABLE	0: Value in "2WIRE_DEV_ADDR_6" is inactive 1: Value in "2WIRE_DEV_ADDR_6" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_6	Remote side 2-wire serial Slave Device Address #6	
0x0B	7	RW	0	2WIRE_DEV_ADDR_7_ENABLE	0: Value in "2WIRE_DEV_ADDR_7" is inactive 1: Value in "2WIRE_DEV_ADDR_7" is active	
	6:0	RW	0x00	2WIRE_DEV_ADDR_7	Remote side 2-wire serial Slave Device Address #7	
0x0C	7:0	RW	0x00	Reserved		-
0x0D	7:0	R	0x00	Reserved		-
0x0E	7:2	R	0x00	Reserved		-
	1:0	RW	0x0	Reserved. Must be 0		-
0x0F	7:2	R	0x00	Reserved		-
	1:0	RW	0x1	2WIRE_MODE	00: clock stretching mode 01: No clock stretching mode 10: Reserved (Forbidden) 11: Reserved (Forbidden)	-
0x10	7:0	RW	0x00	2WIRE_DATA0	2-wire serial I/F Write/Read Data #0	-
0x11	7:0	RW	0x00	2WIRE_DATA1	2-wire serial I/F Write/Read Data #1	-
0x12	7:0	RW	0x00	2WIRE_DATA2	2-wire serial I/F Write/Read Data #2	-
0x13	7:0	RW	0x00	2WIRE_DATA3	2-wire serial I/F Write/Read Data #3	-
0x14	7:0	RW	0x00	2WIRE_DATA4	2-wire serial I/F Write/Read Data #4	-
0x15	7:0	RW	0x00	2WIRE_DATA5	2-wire serial I/F Write/Read Data #5	-
0x16	7:0	RW	0x00	2WIRE_DATA6	2-wire serial I/F Write/Read Data #6	-
0x17	7:0	RW	0x00	2WIRE_DATA7	2-wire serial I/F Write/Read Data #7	-
0x18	7:0	RW	0x00	2WIRE_DATA8	2-wire serial I/F Write/Read Data #8	-
0x19	7:0	RW	0x00	2WIRE_DATA9	2-wire serial I/F Write/Read Data #9	-
0x1A	7:0	RW	0x00	2WIRE_DATA10	2-wire serial I/F Write/Read Data #10	-
0x1B	7:0	RW	0x00	2WIRE_DATA11	2-wire serial I/F Write/Read Data #11	-
0x1C	7:0	RW	0x00	2WIRE_DATA12	2-wire serial I/F Write/Read Data #12	-
0x1D	7:0	RW	0x00	2WIRE_DATA13	2-wire serial I/F Write/Read Data #13	-
0x1E	7:0	RW	0x00	2WIRE_DATA14	2-wire serial I/F Write/Read Data #14	-
0x1F	7:0	RW	0x00	2WIRE_DATA15	2-wire serial I/F Write/Read Data #15	-
0x20	7	RW	0	2WIRE_ADR_SEL	Remote side 2-wire Slave device's Register Address bit width select 0: 8bit Register Address 1: 16bit Register Address	-
	6:0	RW	0x00	2WIRE_TARGET_DEV_ADR	2-wire serial I/F Access Target Device Address setting	-
0x21	7:4	R	0x0	Reserved		-
	3:0	RW	0x0	WR_REQ_BYTE	2-wire serial I/F Write Request Byte Number for both 8bit and 16bit Register Address device. Byte Number = register value + 1 (e.g. 0x2 for 3byte burst)	-
0x22	7:4	R	0x0	Reserved		-
	3:0	RW	0x0	RD_REQ_BYTE	2-wire serial I/F Read Request Byte Number for both 8bit and 16bit Register Address device. Byte Number = register value + 1 (e.g. 0x2 for 3byte burst)	-
0x23	7:0	RW	0x00	WR_START_ADR_8B	2-wire serial I/F Write Start Register Address for 8bit Register Address device	-
0x24	7:0	RW	0x00	RD_START_ADR_8B	2-wire serial I/F Read Start Register Address for 8bit Register Address device	-
0x25	7:1	R	0x00	Reserved		-
	0	RW	0	WR_START_8B	2-wire serial I/F Write Access Start Trigger for 8bit Register Address device	-
0x26	7:1	R	0x00	Reserved		-
	0	RW	0	RD_START_8B	2-wire serial I/F Read Access Start Trigger for 8bit Register Address device	-
0x27	7:0	RW	0x00	WR_START_ADR_16B_0	2-wire serial I/F Write Start Register Address(Low-order bits = [7:0]) for 16bit Register Address device	-
0x28	7:0	RW	0x00	WR_START_ADR_16B_1	2-wire serial I/F Write Start Register Address(High-order bits = [15:8]) for 16bit Register Address device	-
0x29	7:0	RW	0x00	RD_START_ADR_16B_0	2-wire serial I/F Read Start Register Address(Low-order bits = [7:0]) for 16bit Register Address device	-
0x2A	7:0	RW	0x00	RD_START_ADR_16B_1	2-wire serial I/F Read Start Register Address(High-order bits = [15:8]) for 16bit Register Address device	-
0x2B	7:1	R	0x00	Reserved		-
	0	RW	0	WT_START_16B	2-wire serial I/F Write Access Start Trigger for 16bit Register Address device	-
0x2C	7:1	R	0x00	Reserved		-
	0	RW	0	RD_START_16B	2-wire serial I/F Read Access Start Trigger for 16bit Register Address device	-
0x2D-0x3F	7:0	R	0x00	Reserved		-

*3 Assignment of 2-wire serial slave device address connected to Sub-Link Slave outside

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Table 41. Sub-Link Slave Control Register

Address (Hex)	Bit#	R/W	Default (Hex)	Name	Description	Note
0x80	7:0	R	0x00	Reserved		-
0x81	7:1	R	0x00	Reserved		-
	0	RW	0	2WIRE_RST	2-wire serial I/F reset Write 1: 16 pulse SCL signal is sent to 2-wire serial slave device connected to Sub-Link Slave. This bit is a remedy against SDA=L, 2-wire serial stuck condition. Automatically cleared into 0 after reset action.0 is always read.	-
0x82	7:6	R	0x0	Reserved		-
	5	RW	0	2WIRE_RST_END_INT	Cause of interrupt 2-wire serial reset done 0: Normal operation 1: 2-wire serial reset signal has all finished Any write action: clear this bit into 0	-
	4	RW	0	2WIRE_NACK_INT	Cause of interrupt 2-wire serial Slave NACK 0: No NACK from remote side 2-wire serial slave ever 1: NACK from remote side 2-wire serial slave once come Any write action: clear this bit into 0	-
	3	R	0	GPIO_INT	Cause of interrupt Sub-Link Slave GPIO 0: No change in Slave GPIO inputs ever 1: Slave GPIO inputs have once changed. This bit is cleared when GPIOn_INPUT_MONITOR (n=4~0) register (0xC1) is read.	-
	2	RW	0	COMERR_INT	Cause of interrupt Sub-Link communication Error 0: No communication error on Sub-Link ever 1: Communication error on Sub-Link once happened Any write action: clear this bit into 0	-
	1	RW	0	2WIRE_TIMEOUT_INT	Cause of interrupt 2-wire serial time out 0: 2-wire serial access in time ever 1: 2-wire serial access has once had time out Any write action: clear this bit into 0	-
	0	RW	0	SLINK_TIMEOUT_INT	Cause of interrupt Sub-Link time out0: Sub-Link access in time ever 1: Sub-Link has once had time out Any write action: clear this bit into 0	-
0x83	7:6	R	0x0	Reserved		-
	5	RW	0	2WIRE_RST_ENABLED_INT_ENABLE	0: "2WIRE_RST_END_INT" is blocked to be reported to Master Side. 1: "2WIRE_RST_END_INT" is allowed to be reported to Master Side.	(*1)
	4	RW	0	2WIRE_NACK_INT_ENABLE	0: "2WIRE_NACK_INT" is blocked to be reported to Master Side. 1: "2WIRE_NACK_INT" is allowed to be reported to Master Side.	
	3	RW	0	GPIO_INT_ENABLE	0: "GPIO_INT" is blocked to be reported to Master Side. 1: "GPIO_INT" is allowed to be reported to Master Side.	
	2	RW	0	COMERR_INT_ENABLE	0: "COMERR_INT" is blocked to be reported to Master Side. 1: "COMERR_INT" is allowed to be reported to Master Side.	
	1	RW	0	2WIRE_TIMEOUT_INT_ENABLE	0: "2WIRE_TIMEOUT_INT" is blocked to be reported to Master Side. 1: "2WIRE_TIMEOUT_INT" is allowed to be reported to Master Side.	
	0	RW	0	SLINK_TIMEOUT_INT_ENABLE	0: "SLINK_TIMEOUT_INT" is blocked to be reported to Master Side. 1: "SLINK_TIMEOUT_INT" is allowed to be reported to Master Side.	
0x84 -0x8B	7:0	R	0x00	Reserved		-
0x8C	7	R	0	Reserved		-
	6:0	RW	0x2D	SCL_W_H	SCL High width [t_{HIGH}] setting. Output SCL High width is defined as below. ((SCL_W_H + 1) * 8 + 8) * t_{OSC}	-
0x8D	7	R	0	Reserved		-
	6:0	RW	0x37	SCL_W_L	SCL Low width [t_{LOW}] setting. Output SCL Low width is defined as below. ((SCL_W_L + 1) * 8 + 8) * t_{OSC}	-
0x8E	7:2	R	0x00	Reserved		-
	1:0	RW	0x0	Reserved. Must be 0		-
0x8F	7:2	R	0x00	Reserved		-
	1:0	RW	0x1	Reserved		-
0x90 -0xBF	7:0	R	0x00	Reserved		-

*1 Interrupt signal from Sub-Link Slave is reported to Sub-Link Master as Cause of interrupt Sub-Link Slave Side (0x02 bit4 SLAVESIDE_INT).

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Table 42. THCV235 GPIO Control Register Map

Address (Hex)		Bit#	R/W	Default (Hex)	Name	Description	Note
Sub-Link Master	Sub-Link Slave						
0x40	0xC0	7:5	R	0x0	Reserved		-
		4	RW	1	GPIO4_TYPE	GPIO4 type select 0: Programmable GPIO 1: Through GPIO	-
		3	RW	1	GPIO3_TYPE	GPIO3 type select 0: Programmable GPIO 1: Through GPIO	-
		2	R	0	GPIO2_TYPE	GPIO2 type select 0: Programmable GPIO 0 Fix	-
		1	R	0	GPIO1_TYPE	GPIO1 type select 0: Programmable GPIO 0 Fix	-
		0	R	0	GPIO0_TYPE	GPIO0 type select 0: Programmable GPIO 0 Fix	-
0x41	0xC1	7:5	R	0x0	Reserved		-
		4	R	0	GPIO4_INPUT_MONITOR	GPIO4 input value	(*1)
		3	R	0	GPIO3_INPUT_MONITOR	GPIO3 input value	
		2	R	0	GPIO2_INPUT_MONITOR	GPIO2 input value	
		1	R	0	GPIO1_INPUT_MONITOR	GPIO1 input value	
		0	R	0	GPIO0_INPUT_MONITOR	GPIO0 input value	
0x42	0xC2	7:5	R	0x0	Reserved		
		4	RW	0	GPIO4_OUT	GPIO4 output value setting	(*2)
		3	RW	0	GPIO3_OUT	GPIO3 output value setting	
		2	RW	0	GPIO2_OUT	GPIO2 output value setting	
		1	RW	0	GPIO1_OUT	GPIO1 output value setting	
		0	RW	0	GPIO0_OUT	GPIO0 output value setting	
0x43	0xC3	7:5	R	0x0	Reserved		-
		4:0	RW	0x07	GPIO_IO_SEL	GPIO input/output direction setting See Table 36, Table 37 and Table 38	-
0x44	0xC4	7:5	R	0x0	Reserved		-
		4	RW	1	GPIO4_FILT_ENABLE	GPIO4 input filter enable 0: Disable 1: Enable	(*3)
		3	RW	1	GPIO3_FILT_ENABLE	GPIO3 input filter enable 0: Disable 1: Enable	
		2	RW	1	GPIO2_FILT_ENABLE	GPIO2 input filter enable 0: Disable 1: Enable	
		1	RW	1	GPIO1_FILT_ENABLE	GPIO1 input filter enable 0: Disable 1: Enable	
		0	RW	1	GPIO0_FILT_ENABLE	GPIO0 input filter enable 0: Disable 1: Enable	

*1 Active only when GPIO is set as input port.
*2 Active only when GPIO type is set as "Programmable GPIO" and set as output port.
*3 Filter eliminates input glitch shorter than $t_{OSC}/2$.

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Table 42. THCV235 GPIO Control Register Map (continued)

Address (Hex)		Bit#	R/W	Default (Hex)	Name	Description	Note
Sub-Link Master	Sub-Link Slave						
0x45	0xC5	7:5	R	0x0	Reserved		-
		4	RW	1	GPIO4_INT_ENABLE	GPIO4 interrupt enable 0: Disable 1: Enable	
		3	RW	1	GPIO3_INT_ENABLE	GPIO3 interrupt enable 0: Disable 1: Enable	
		2	RW	1	GPIO2_INT_ENABLE	GPIO2 interrupt enable 0: Disable 1: Enable	(*4)
		1	RW	1	GPIO1_INT_ENABLE	GPIO1 interrupt enable 0: Disable 1: Enable	
		0	RW	1	GPIO0_INT_ENABLE	GPIO0 interrupt enable 0: Disable 1: Enable	
0x46	0xC6	7:5	R	0x0	Reserved		-
		4	RW	0	GPIO4_OUTBUF_SEL	GPIO4 output buffer select 0: GPIO4 is open-drain output 1: GPIO4 is push pull output	-
		3	RW	0	GPIO3_OUTBUF_SEL	GPIO3 output buffer select 0: GPIO3 is open-drain output 1: GPIO3 is push pull output	-
		2	RW	0	GPIO2_OUTBUF_SEL	GPIO2 output buffer select 0: GPIO2 is open-drain output 1: GPIO2 is push pull output	-
		1	RW	0	GPIO1_OUTBUF_SEL	GPIO1 has only open-drain output buffer. Must be 0 setting 0: GPIO1 is open-drain output	-
		0	RW	0	GPIO0_OUTBUF_SEL	GPIO0 has only open-drain output buffer. Must be 0 setting 0: GPIO0 is open-drain output	-
0x47 -0x4F	0xC7 -0xCF	7:0	R	0x00	Reserved		-

*4 GPIO input transition is counted as GPIO_INT(0x02 or 0x82 bit3).

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Table 43. THCV235 Main-Link Control Register Map

Address (Hex)		Bit#	R/W	Default (Hex)	Name	Description	Note
Sub-Link Master	Sub-Link Slave						
0x50	0xD0	7	RW	0	MAINMODE	MAINMODE setting 0: V-by-One® HS Mode 1: Sync Free Mode	-
		6	RW	0	HFSEL	HFSEL setting 0: High Frequency Mode Disable 1: High Frequency Mode Enable	-
		5	RW	0	COL1	COL1 setting when MAINMODE =0 0: Color Space Converter Disable 1: Color Space Converter Enable when MAINMODE =1 Data Width Setting. See Table 20.	-
		4	RW	0	COL0	COL0 setting Data Width Setting. See Table 20.	-
		3	RW	0	PRE	PRE setting 0: Pre-Emphasis Disable 1: Pre-Emphasis Enable	(*1)
		2:1	RW	0x2	CMLDRV	CMLDRV setting 00: 400mV diff p-p 01: 600mV diff p-p 10: 800mV diff p-p 11: Reserved (Forbidden)	
		0	RW	0	Reserved		-
0x51	0xD1	7:6	R	0x0	Reserved		-
		5	RW	0	SSEN	SSEN setting 0: SSCG Disable 1: SSCG Enable	(*2)
		4:0	RW	0x05	SPREAD	SSCG modulation depth setting Spread depth = ±SPREAD x 0.1% (Center Spread)	
0x52	0xD2	7:4	R	0x0	Reserved		-
		3:0	RW	0xD	FMOD	SSCG Modulation Frequency setting	-
0x53	0xD3	7:2	R	0x00	Reserved		-
		1	RW	0	BET	Field BET Mode Enable setting 0: Normal Mode 1: Field BET Operation	-
		0	RW	0	BET_SEL	Main-Link / Sub-Link Field BET Mode select 0: Main-Link Field BET Mode 1: Sub-Link Field BET Mode	-
0x54	0xD4	7	R	0	Reserved		-
		6:0	RW	0x3E	Reserved. Must be default setting.		-
0x55 -0x6C	0xD5 -0xEC	7:0	RW	0x00	Reserved		-
0x6D	0xED	7:3	R	0x00	Reserved		-
		2:0	RW	0x1	Reserved		-
0x6E	0xEE	7:1	R	0x00	Reserved		-
		0	RW	1	Reserved. Must be 1		-
0x6F	0xEF	7:0	R	0x00	Reserved		-
0x70	0xF0	7:2	R	0x00	Reserved		-
		1	RW	0	Reserved. Must be 0		-
		0	RW	0	PLL_SET_EN	SSCG PLL setting register Enable 1: Enable 0: Disable	-
0x71 -0x75	0xF1 -0xF5	7:0	R	0x00	Reserved		-
0x76	0xF6	7:6	R	0x0	Reserved		-
		5:0	RW	0xXX	PLL_SET0	SSCG PLL setting	(*3)
0x77	0xF7	7:4	R	0x0	Reserved		-
		3:0	RW	0x0	Reserved. Must be default setting.		-
0x78	0xF8	7:0	RW	0xXX	PLL_SET1	SSCG PLL setting	(*3)
0x79 -0x7B	0xF9 -0xFB	7:0	RW	0x00	Reserved. Must be default setting.		-
0x7C	0xFC	7:6	R	0x0	Reserved.		-
		5:0	RW	0xXX	PLL_SET2	SSCG PLL setting	(*3)
0x7D -0x7F	0xFD -0xFF	7:0	RW	0xXX	Reserved. Must be default setting.		-

*1 See Table 4 and Table 5
*2 SSEN=1 and SPREAD=0 setting is forbidden
*3 See Table 11, Table 21

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Table 44. THCV236 GPIO Control Register Map

Address (Hex)		Bit#	R/W	Default (Hex)	Name	Description	Note
Sub-Link Master	Sub-Link Slave						
0x40	0xC0	7:5	R	0x0	Reserved		-
		4	RW	1	GPIO4_TYPE	GPIO4 type select 0: Programmable GPIO 1: Through GPIO	-
		3	RW	1	GPIO3_TYPE	GPIO3 type select 0: Programmable GPIO 1: Through GPIO	-
		2	R	0	GPIO2_TYPE	GPIO2 type select 0: Programmable GPIO 0 Fix	-
		1	R	0	GPIO1_TYPE	GPIO1 type select 0: Programmable GPIO 0 Fix	-
		0	R	0	GPIO0_TYPE	GPIO0 type select 0: Programmable GPIO 0 Fix	-
0x41	0xC1	7:5	R	0x0	Reserved		-
		4	R	0	GPIO4_INPUT_MONITOR	GPIO4 input value	(*1)
		3	R	0	GPIO3_INPUT_MONITOR	GPIO3 input value	
		2	R	0	GPIO0_INPUT_MONITOR(*2)	GPIO0 input value	
		1	R	0	GPIO1_INPUT_MONITOR	GPIO1 input value	
		0	R	0	GPIO2_INPUT_MONITOR(*2)	GPIO2 input value	
0x42	0xC2	7:5	R	0x0	Reserved		-
		4	RW	0	GPIO4_OUT	GPIO4 output value setting	(*3)
		3	RW	0	GPIO3_OUT	GPIO3 output value setting	
		2	RW	0	GPIO2_OUT	GPIO2 output value setting	
		1	RW	0	GPIO1_OUT	GPIO1 output value setting	
		0	RW	0	GPIO0_OUT	GPIO0 output value setting	
0x43	0xC3	7:5	R	0x0	Reserved		-
		4	RW	(*4)	GPIO_IO_SEL	GPIO input/output direction setting See Table 36, Table 37, and Table 38	-
		3	RW	(*4)			
		2:0	RW	0x7			
0x44	0xC4	7:5	R	0x0	Reserved		-
		4	RW	1	GPIO4_FILT_ENABLE	GPIO4 input filter enable 0: Disable 1: Enable	(*5)
		3	RW	1	GPIO3_FILT_ENABLE	GPIO3 input filter enable 0: Disable 1: Enable	
		2	RW	1	GPIO0_FILT_ENABLE(*6)	GPIO0 input filter enable 0: Disable 1: Enable	
		1	RW	1	GPIO1_FILT_ENABLE	GPIO1 input filter enable 0: Disable 1: Enable	
		0	RW	1	GPIO2_FILT_ENABLE(*6)	GPIO2 input filter enable 0: Disable 1: Enable	

*1 Active only when GPIO is set as input port.
*2 Note that GPIO2_INPUT_MONITOR corresponds to Bit#"0", GPIO0_INPUT_MONITOR corresponds to Bit#"2".
*3 Active only when GPIO type is set as "Programmable GPIO" and set as output port.
*4 Default value depends on RXDEFSEL setting when Power on sequence. RXDEFSEL=1 → default value is 0, RXDEFSEL=0 → default value is 1.
*5 Filter eliminates input glitch shorter than $t_{OSC}/2$.
*6 Note that GPIO2_FILT_ENABLE corresponds to Bit#"0", GPIO0_FILT_ENABLE corresponds to Bit#"2".

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Table 44. THCV236 GPIO Control Register Map (continued)

Address (Hex)		Bit#	R/W	Default (Hex)	Name	Description	Note
Sub-Link Master	Sub-Link Slave						
0x45	0xC5	7:5	R	0x0	Reserved		-
		4	RW	1	GPIO4_INT_ENABLE	GPIO4 interrupt enable 0: Disable 1: Enable	
		3	RW	1	GPIO3_INT_ENABLE	GPIO3 interrupt enable 0: Disable 1: Enable	
		2	RW	1	GPIO0_INT_ENABLE(*8)	GPIO0 interrupt enable 0: Disable 1: Enable	(*7)
		1	RW	1	GPIO1_INT_ENABLE	GPIO1 interrupt enable 0: Disable 1: Enable	
		0	RW	1	GPIO2_INT_ENABLE(*8)	GPIO2 interrupt enable 0: Disable 1: Enable	
0x46	0xC6	7:5	R	0x0	Reserved		-
		4	RW	0	GPIO4_OUTBUF_SEL	GPIO4 output buffer select 0: GPIO4 is open-drain output 1: GPIO4 is push pull output	-
		3	RW	0	GPIO3_OUTBUF_SEL	GPIO3 output buffer select 0: GPIO3 is open-drain output 1: GPIO3 is push pull output	-
		2	RW	0	GPIO2_OUTBUF_SEL	GPIO2 output buffer select 0: GPIO2 is open-drain output 1: GPIO2 is push pull output	-
		1	RW	0	GPIO1_OUTBUF_SEL	GPIO1 output buffer select 0: GPIO1 is open-drain output 1: GPIO1 is push pull output	-
		0	RW	0	GPIO0_OUTBUF_SEL	GPIO0 output buffer select 0: GPIO0 is open-drain output 1: GPIO0 is push pull output	-
0x47 -0x4F	0xC7 -0xCF	7:0	R	0x00	Reserved		-

*7 GPIO input transition is counted as GPIO_INT(0x02 or 0x82 bit3).
*8 Note that GPIO2_INT_ENABLE corresponds to Bit#"0", GPIO0_INT_ENABLE corresponds to Bit#"2".

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Table 45. THCV236 Main-Link Control Register Map

Address (Hex)		Bit#	R/W	Default (Hex)	Name	Description	Note
Sub-Link Master	Sub-Link Slave						
0x50	0xD0	7	RW	(*1)	MAINMODE	MAINMODE setting 0: V-by-One® HS Mode 1: Sync Free Mode	-
		6	RW	(*1)	HFSEL	HFSEL setting 0: High Frequency Mode Disable 1: High Frequency Mode Enable	-
		5	RW	0	COL1	COL1 setting when MAINMODE =0 0: Color Space Converter Disable 1: Color Space Converter Enable when MAINMODE =1 Data Width Setting. See Table 20.	-
		4	RW	(*1)	COL0	COL0 setting Data Width Setting. See Table 20.	-
		3	RW	0	Reserved		-
		2:1	RW	0x0	Reserved		-
		0	RW	0	TTLDRV	TTLDRV setting 0: Weak Drive Strength 1: Normal Drive Strength	-
0x51	0xD1	7:6	R	0x0	Reserved		-
		5	RW	0	SSEN	SSEN setting 0: SSCG Disable 1: SSCG Enable	(*2)
		4:0	RW	0x05	SPREAD	SSCG modulation depth setting Spread depth = ±SPREAD x 0.1% (Center Spread)	
0x52	0xD2	7:4	R	0x0	Reserved		-
		3:0	RW	0xD	FMOD	SSCG Modulation Frequency setting	-
0x53	0xD3	7:2	R	0x00	Reserved		-
		1	RW	0	Reserved		-
		0	RW	0	BET_SEL	Main-Link / Sub-Link Field BET Mode select 0: Main-Link Field BET Mode 1: Sub-Link Field BET Mode	-
0x54	0xD4	7	R	0	Reserved		-
		6:0	RW	0x3E	Reserved. Must be default setting.		-
0x55 -0x6C	0xD5 -0xEC	7:0	RW	0x00	Reserved		-
0x6D	0xED	7:3	R	0x00	Reserved		-
		2	RW	0	OUTSEL_ENABLE	Permanent Clock Output Enable setting 0: Permanent Clock Output Disable 1: Permanent Clock Output Enable	-
		1:0	RW	0x1	OUTSEL_SETTING	Permanent Clock Frequency setting 00: 80MHz (Clock Period : t_{OSC}) 01: 40MHz (Clock Period : t_{OSC}/2) 10: 20MHz (Clock Period : t_{OSC}/4) 11: 10MHz (Clock Period : t_{OSC}/8)	(*3)
0x6E	0xEE	7:1	R	0x00	Reserved		-
		0	RW	1	Reserved. Must be 1		-
0x6F	0xEF	7:0	R	0x00	Reserved		-
0x70	0xF0	7:2	R	0x00	Reserved		-
		1	RW	0	Reserved. Must be 0		-
		0	RW	0	PLL_SET_EN	SSCG PLL setting register Enable 1: Enable 0: Disable	-
0x71 -0x75	0xF1 -0xF5	7:0	R	0x00	Reserved		-
0x76	0xF6	7:6	R	0x0	Reserved		-
		5:0	RW	0xXX	PLL_SET0	SSCG PLL setting	(*4)
0x77	0xF7	7:4	R	0x0	Reserved		-
		3:0	RW	0x0	Reserved. Must be default setting.		-
0x78	0xF8	7:0	RW	0xXX	PLL_SET1	SSCG PLL setting	(*4)
0x79 -0x7B	0xF9 -0xFB	7:0	RW	0x00	Reserved. Must be default setting.		-
0x7C	0xFC	7:6	R	0x0	Reserved.		-
		5:0	RW	0xXX	PLL_SET2	SSCG PLL setting	(*4)
0x7D -0x7F	0xFD -0xFF	7:0	RW	0xXX	Reserved. Must be default setting.		-

*1 Default value depends on RXDEFSEL setting when Power on sequence. RXDEFSEL=1 → default value is 0, RXDEFSEL=0 → default value is 1.
*2 SSEN=1 and SPREAD=0 setting is forbidden.
*3 Described value is typical value. It has variation in the range from min spec value to max spec value of t_{OSC}.
*4 See Table 11, Table 21.

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Absolute Maximum Ratings

Table 46. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage(VDD,AVDD)	-0.3	-	4.0	V
LVCMOS Input Voltage	-0.3	-	VDD+0.3	V
LVCMOS Output Voltage	-0.3	-	VDD+0.3	V
LVCMOS Bi-directional buffer Input Voltage	-0.3	-	VDD+0.3	V
LVCMOS Bi-directional buffer Output Voltage	-0.3	-	VDD+0.3	V
Open-Drain Output Voltage	-0.3	-	4.0	V
CML Receiver Input Voltage	-0.3	-	CAPINA+0.3	V
CML Transmitter Output Voltage	-0.3	-	CAPINA+0.3	V
CML Bi-directional buffer Input Voltage	-0.3	-	VDD+0.3	V
CML Bi-directional buffer Output Voltage	-0.3	-	VDD+0.3	V
Output Current	-50	-	50	mA
Storage temperature	-55	-	125	°C
Junction temperature	-	-	125	°C
Reflow Peak Temperature/Time	-	-	260/10	°C/sec
Maximum Power Dissipation @+25°C	-	-	2.5	W

Recommended Operating Conditions

Table 47. Recommended Operating Condition

Parameter	Min	Typ	Max	Unit
Supply Voltage(VDD,AVDD)	1.7	-	3.6	V
Operating Temperature	-40	-	105	°C

Electrical Specification

LVCMOS DC Specification

Table 48. LVCMOS DC Specification

Symbol	Parameter	Pin Type	Condition	Min	Typ	Max	Unit
VIH	High Level Input Voltage	I	VDD=1.7-2.0V	0.65×VDD	-	VDD	V
			VDD=2.0-3.0V	0.70×VDD	-	VDD	V
			VDD=3.0-3.6V	2.0	-	VDD	V
		IL,B	VDD=1.7-3.6V	0.70×VDD	-	VDD	V
VIL	Low Level Input Voltage	I	VDD=1.7-2.0V	0	-	0.35×VDD	V
			VDD=2.0-3.0V	0	-	0.30×VDD	V
			VDD=3.0-3.6V	0	-	0.8	V
		IL,B	VDD=1.7-3.6V	0	-	0.30×VDD	V
VOH	High Level Output Voltage	O,B	VDD=1.7-3.6V IOH=-4mA	VDD-0.45	-	VDD	V
VOL	Low Level Output Voltage	O,B	VDD=1.7-3.6V IOL=4mA	0	-	0.45	V
		BO	VDD=1.7-3.6V IOL=2mA	0	-	0.2	V
IIH	Input Leak Current High	I,IL	VIN=VDD	-	-	10	uA
IIL	Input Leak Current Low	I,IL	VIN=0V	-10	-	-	uA
IOZH	Output Leak Current High in Hi-Z State	O,B,BO	VIN=VDD	-	-	10	uA
IOZL	Output Leak Current Low in Hi-Z State	O,B,BO	VIN=0V	-10	-	10	uA

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CML DC Specification

Table 49. CML DC Specification(THCV235)

Symbol	Parameter	Condition(*1)	Min	Typ	Max	Unit
VTOD	CML Differential Output Voltage	PDN1=0,CMLDRV=0	200	300	400	mV
		PDN1=0,CMLDRV=1	300	400	500	mV
		PDN1=1,CMLDRV[1:0]=00	133	200	267	mV
		PDN1=1,CMLDRV[1:0]=01	200	300	400	mV
		PDN1=1,CMLDRV[1:0]=10	300	400	500	mV
PRE	CML Pre-emphasis Level	PRE=0	-	0	-	%
		PDN1=0,PRE=1,CMLDRV=0	-	50	-	%
		PDN1=1,PRE=1,CMLDRV[1:0]=00	-	100	-	%
		PDN1=1,PRE=1,CMLDRV[1:0]=01	-	50	-	%
VTOC	CML Common Mode Output Voltage	PRE=0	CAPINA-VTOD			mV
		PDN1=0,PRE=1,CMLDRV=0	CAPINA-1.5×VTOD			mV
		PDN1=1,PRE=1,CMLDRV[1:0]=00	CAPINA-2×VTOD			mV
		PDN1=1,PRE=1,CMLDRV[1:0]=01	CAPINA-1.5×VTOD			mV
ITOH	CML Output Leak Current High	PDN0=0,TXP/N=CAPINA	-30	-	30	uA
ITOS	CML Output Short Current	PDN0=0,TXP/N=0V	-80	-	-	mA

*1 When PDN1=0, PRE and CMLDRV are external pins. When PDN1=1, PRE and CMLDRV[1:0] are registers.

Table 50. CML DC Specification(THCV236)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input High Threshold	-	-50	-	-	mV
IRIH	CML Input Leak Current High	PDN0=0,RXP/N=CAPINA	-10	-	10	uA
IRIL	CML Input Leak Current Low	PDN0=0,RXP/N=0V	-10	-	10	uA
IRRIH	CML Input Current High	RXP/N=CAPINA	-	-	2	mA
IRRIL	CML Input Current Low	RXP/N=0V	-6	-	-	mA
RRIN	CML Differential Input Resistance	-	80	100	120	Ω

CML Bi-Directional DC Specification

Table 51. CML Bi-Directional DC Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBTH	Bi-Directional Buffer Differential Input High Threshold	-	-	-	150	mV
VBTL	Bi-Directional Buffer Differential Input Low Threshold	-	-150	-	-	mV
IBIH	Bi-Directional Buffer Output Leak Current High	xCMP/N=VDD(x=T,R)	-10	-	10	uA
IBIL	Bi-Directional Buffer Output Leak Current Low	xCMP/N=0V(x=T,R)	-10	-	10	uA
RTERM	Bi-Directional Buffer Termination Resistance	Transmitter State	37.5	50	62.5	Ω
		Receiver State	150	200	250	Ω
VBOD	Bi-Directional Buffer Differential Output Voltage	RDIFF=400Ω	300	-	660	mV
VBOC	Bi-Directional Buffer Common Output Voltage	-	-	VDD-0.3	-	V
IBOZ	Bi-Directional Buffer TRI-STATE Current	PDN1=0	-10	-	10	uA

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Supply Current

Table 52. Supply Current(THCV235)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ITCCW	Transmitter Supply Current	PDN0=1,PDN1=1, HFSEL=1	-	-	160	mA
ITCCS	Transmitter Power Down Supply Current	PDN0=0 and PDN1=0 All Inputs = Fixed 0 or 1 Typical value is under 25°C	-	2.5	20	mA

Table 53. Supply Current(THCV236)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IRCCW	Receiver Supply Current	Cload=8pF, PDN0=1,PDN1=1,HFSEL=1	-	-	220	mA
IRCCS	Receiver Power Down Supply Current	PDN0=0 and PDN1=0 All Inputs = Fixed 0 or 1 Typical value is under 25°C	-	2.5	20	mA

Switching Characteristics

Table 54. Switching Characteristics (THCV235)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tTRF	CML Output Rise and Fall Time (20%-80%)	-	50	-	150	ps
tTCIP	CLKIN Period	See Table 20	1000/Freq.Range[MHz]			ns
tTCH	CLKIN High Time	-	0.35×tTCIP	0.5×tTCIP	0.65×tTCIP	ns
tTCL	CLKIN Low Time	-	0.35×tTCIP	0.5×tTCIP	0.65×tTCIP	ns
tTS	Data Input Setup to CLKIN	-	2.0	-	-	ns
tTH	Data Input Hold to CLKIN	-	1.0	-	-	ns
tTPD	Power On to PDN0 High Delay	-	0	-	-	ns
tTCD	Input Clock to Output Data Delay	MAINMODE=0, HFSEL=0,COL1=0	55×tTCIP	-	62×tTCIP	ns
		MAINMODE=0, HFSEL=0,COL1=1	76×tTCIP	-	83×tTCIP	ns
		MAINMODE=0, HFSEL=1,COL1=0	107×tTCIP	-	124×tTCIP	ns
		MAINMODE=0, HFSEL=1,COL1=1	128×tTCIP	-	145×tTCIP	ns
		MAINMODE=1, HFSEL=0	56×tTCIP	-	65×tTCIP	ns
		MAINMODE=1, HFSEL=1	109×tTCIP	-	132×tTCIP	ns
tTPLL0	PDN0 High to CML Output Delay	-	-	-	10	ms
tTPLL1	PDN0 Low to CML Output High Fix Delay	-	-	-	20	ns
tTNP0	LOCKN High to Training Pattern Output Delay	-	-	-	10	ms
tTNP1	LOCKN Low to Data Pattern Output Delay	-	-	-	10	ms

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Table 55. Switching Characteristics (THCV236)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tRBIT	Unit Interval	-	250	-	1666	ps
tRCP	CLKOUT Period	See Table 20	1000/Freq.Range[MHz]			ns
tRCH	CLKOUT High Time	-	-	tRCP/2	-	ns
tRCL	CLKOUT Low Time	-	-	tRCP/2	-	ns
tDOUT	Data Output Period	-	-	tRCP	-	ns
tRPD	Power On to PDN0 High Delay	-	0	-	-	ns
tRDC	Input Data to Output Clock Delay	MAINMODE=0,HFSEL=0,COL1=0	60×tRCP	-	67×tRCP	ns
		MAINMODE=0,HFSEL=0,COL1=1	81×tRCP	-	88×tRCP	ns
		MAINMODE=0,HFSEL=1,COL1=0	114×tRCP	-	132×tRCP	ns
		MAINMODE=0,HFSEL=1,COL1=1	135×tRCP	-	153×tRCP	ns
		MAINMODE=1,HFSEL=0	61×tRCP	-	70×tRCP	ns
		MAINMODE=1,HFSEL=1	116×tRCP	-	140×tRCP	ns
tRHPD0	PDN0 High to HTPDN Low Delay	-	-	-	10	ms
tRHPD1	PDN0 Low to HTPDN High Delay	-	-	-	50	us
tRPLL0	Training Pattern Input to LOCKN Low Delay	-	-	-	10	ms
tRPLL1	PDN0 Low to LOCKN High Delay	-	-	-	10	us
tRLCK0	LOCKN Low to Data Output Delay	-	-	-	5	ms
tRLCK1	LOCKN High to Data Output Stop Delay	-	-	-	10	us
tROSC0	PDN0 High to Permanent Clock output Delay	OUTSEL=1	-	-	5	ms
tROSC1	LOCKN Low to Permanent Clock output Low Delay	OUTSEL=1	-	-	1	ms
tROSC2	LOCKN High to Permanent Clock output Delay	OUTSEL=1	-	-	10	us
tRS	Data Output Setup to CLKOUT	-	0.45×tRCP-0.65	-	-	ns
tRH	Data Output Hold to CLKOUT	-	0.45×tRCP-0.65	-	-	ns
tTLH	Clock, Data Output Low to High Transition Time	Clock , TTLDRV=0	-	-	2.0	ns
		Data , TTLDRV=0	-	-	3.5	ns
		Clock , TTLDRV=1	-	-	0.8	ns
		Data , TTLDRV=1	-	-	1.9	ns
tTHL	Clock, Data Output High to Low Transition Time	Clock , TTLDRV=0	-	-	2.4	ns
		Data , TTLDRV=0	-	-	4.4	ns
		Clock , TTLDRV=1	-	-	1.0	ns
		Data , TTLDRV=1	-	-	2.2	ns

Table 56. CML Bi-Directional Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tBUI	Bi-Directional Buffer Unit Interval	-	80	100	120	ns
tBRF	Bi-Directional Buffer Rise and Fall Time(20%-80%)	-	150	-	1000	ps
tBPJTX	Bi-Directional Buffer Transmitter Period Jitter Accuracy (peak to peak)	-	-	-	1	ns
tBPJRX	Bi-Directional Buffer Receiver Period Jitter Tolerance (peak to peak)	-	8	-	-	ns

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Table 57. 2-wire serial slave AC Timing (Sub-Link Master device)

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	-	-	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	0.6	-	-	us
t_{LOW}	LOW period of the SCL clock	1.3	-	-	us
t_{HIGH}	HIGH period of the SCL clock	0.6	-	-	us
$t_{HD;DAT}$	Data hold time: output	-	$9\times t_{OSC}$	-	us
	Data hold time: input	20	-	-	ns
$t_{SU;DAT}$	Data setup time: output	500	-	-	ns
	Data setup time: input	100	-	-	ns
t_r	Rise time of both SDA and SCL signals	-	-	300(*1)	ns
t_f	Fall time of both SDA and SCL signals (pull-up resistor:2.5kΩ,bus capacitance:400pF)	-	-	300	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6	-	-	ns
t_{BUF}	Bus free time between a STOP and START condition	1.3	-	-	us
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	-	-	50	ns
t_{PDS}	Required wait time from PDN1 high to START condition	2	-	-	ms

*1 Please adjust Pull-up resistor and bus capacitance to meet the spec value.

Table 58. 2-wire serial master AC Timing (Sub-Link Slave device)

Symbol	Parameter	Min	Typ	Max	Unit
t_{OSC}	Cycle of internal oscillator clock	10.417	12.5	15.625	ns
$t_{HD;STA}$	Hold time (repeated) START condition	-	$(SCL_W_H \times 8 - 3) \times t_{OSC}$	-	us
t_{LOW}	LOW period of the SCL clock	-	$((SCL_W_L + 1) \times 8 + 8) \times t_{OSC}$	-	us
t_{HIGH}	HIGH period of the SCL clock	-	$((SCL_W_H + 1) \times 8 + 8) \times t_{OSC}$	-	us
$t_{HD;DAT}$	Data hold time: output	-	$9\times t_{OSC}$	-	us
	Data hold time: input	20	-	-	ns
$t_{SU;DAT}$	Data setup time: output	$31\times t_{OSC}$	-	-	ns
	Data setup time: input	100	-	-	ns
t_r	Rise time of both SDA and SCL signals	-	-	300(*1)	ns
t_f	Fall time of both SDA and SCL signals (pull-up resistor:2.5kΩ,bus capacitance:400pF)	-	-	300	ns
$t_{SU;STO}$	Setup time for STOP condition	-	$386\times t_{OSC}$	-	ns
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	-	us

*1 Please adjust Pull-up resistor and bus capacitance to meet the spec value.

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Table 59. 2-wire serial interface transaction wait time

Symbol	Parameter	Min	Typ	Max	Unit
t_{WSSR}	Write access completion time to Sub-Link Slave register	-	-	110	us
t_{RSSR}	Read access completion time to Sub-Link Slave register	-	-	90	us
t_{WRS}	Write start to Remote side Start Condition generating time	-	-	65	us
t_{RPW}	Remote side Stop Condition generating to Write access completion time	-	-	300	us
t_{RRS}	Read start to Remote side Start Condition generating time	-	-	65	us
t_{RPR}	Remote side Stop Condition generating to Read access completion time	-	-	300	us
t_{SSEP}	Sub-Link Slave External processing time	Depending on characteristics of 2-wire serial slave devices connected to Sub-Link Slave			us

Table 60. Sub-Link control switching characteristics (2-wire serial I/F Mode)

Symbol	Parameter		Min	Typ	Max	Unit
t_{PVM}	Programmable GPIO output at Sub-Link Master data valid		-	-	0	us
t_{PVS}	Programmable GPIO output at Sub-Link Slave data valid		-	-	110	us
t_{TGPIO}	Through GPIO delay		-	-	280	us
t_{IVM}	Sub-Link Master interrupt valid		-	-	90	us
t_{IRM}	Sub-Link Master interrupt reset delay		-	-	0	us
t_{IVS}	Sub-Link Slave interrupt valid		-	-	300	us
t_{IRS}	Sub-Link Slave interrupt reset delay	2WIRE_MODE=00	-	-	300	us
		2WIRE_MODE=01	-	-	0	
t_{PS}	Programmable GPIO input data setup		$10000\times(1/f_{SCL})$	-	-	us
t_{PH}	Programmable GPIO input data hold		0	-	-	us

Table 61. Sub-Link control switching characteristics (Low Speed Data Bridge Mode)

Symbol	Parameter	Min	Typ	Max	Unit
t_{LSD}	Low Speed Data input to output delay	-	-	20	us
f_{LSSR}	Low Speed Data input sampling rate	70	-	-	kHz

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AC Timing Diagrams and Test Circuits

LVCMOS Input, Output Switching Characteristics

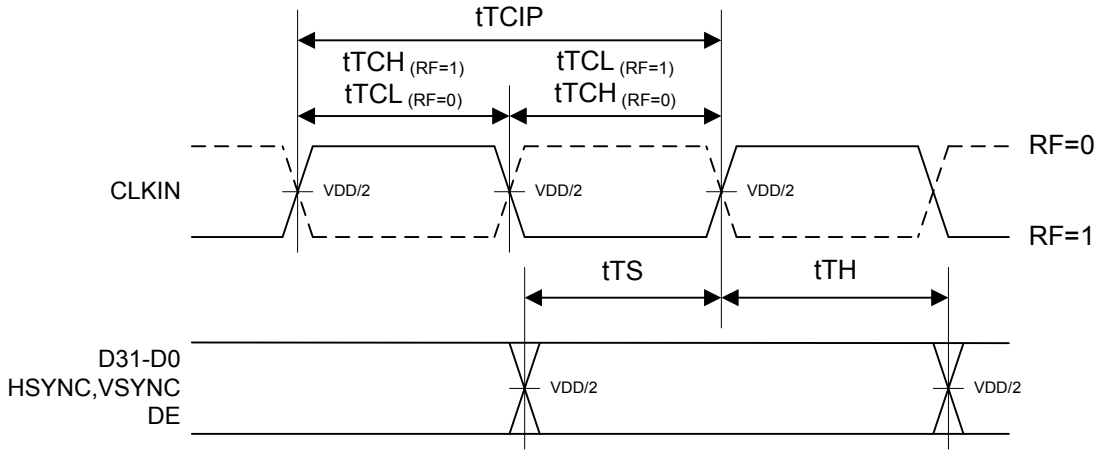


Figure 19. LVCMOS Input Switching Timing Diagrams

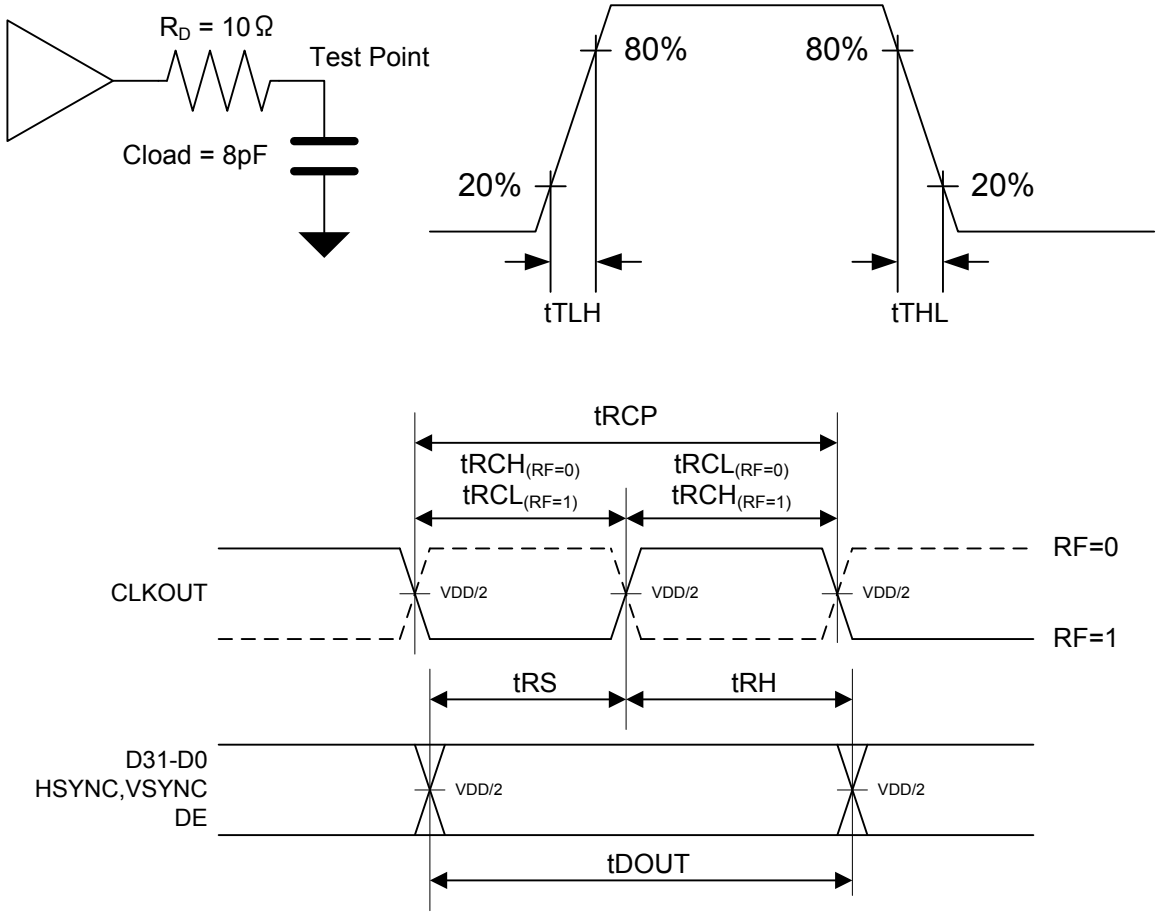


Figure 20. LVCMOS Output Switching Timing Diagrams

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CML Output Switching Characteristics

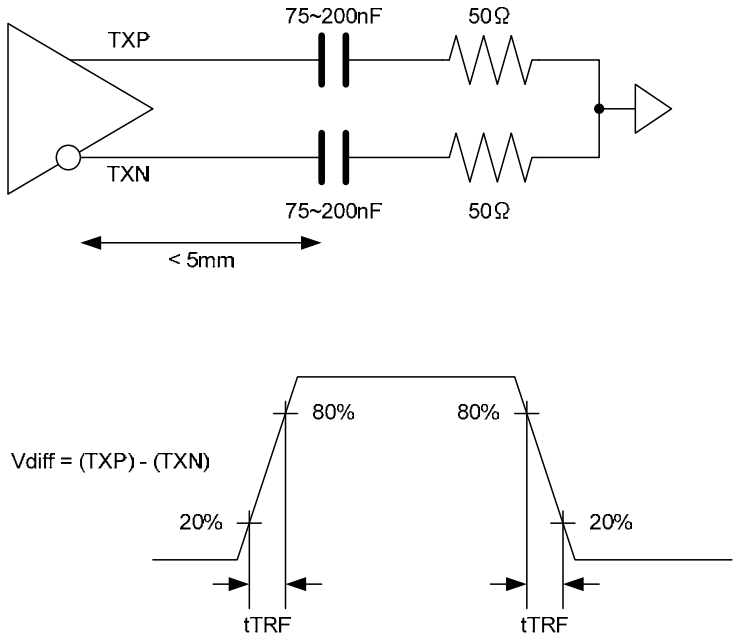


Figure 21. CML Output Switching Characteristics

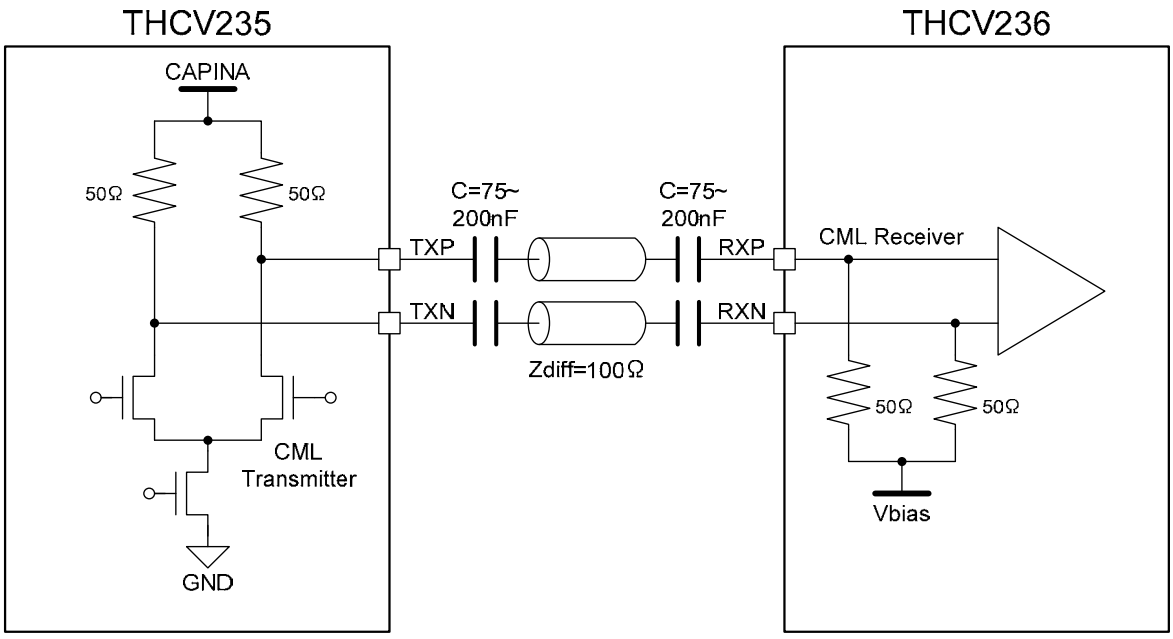


Figure 22. CML Buffer Equivalent Circuit

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CML Bi-directional Output Test Circuit

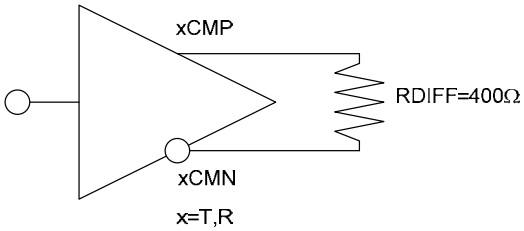


Figure 23. Bi-directional CML VBOD/VBOC Test Circuit

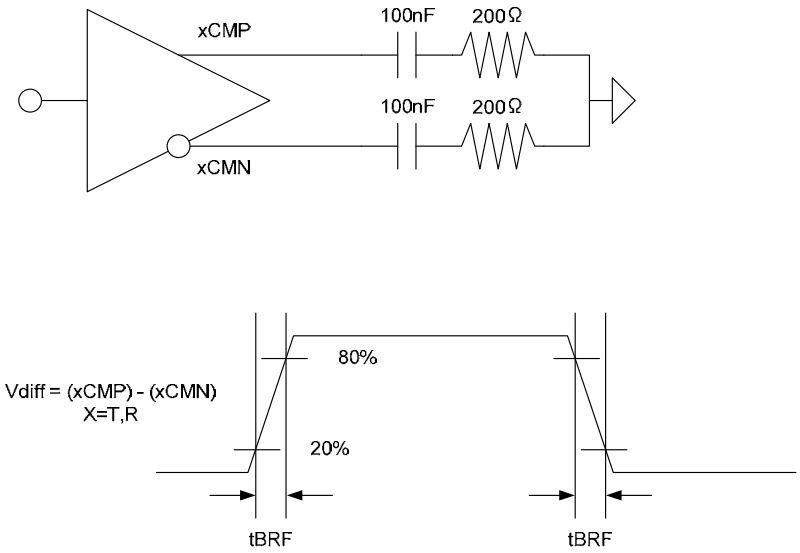


Figure 24. Bi-directional CML Switching Timing Diagram and Test Circuit

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Latency Characteristics

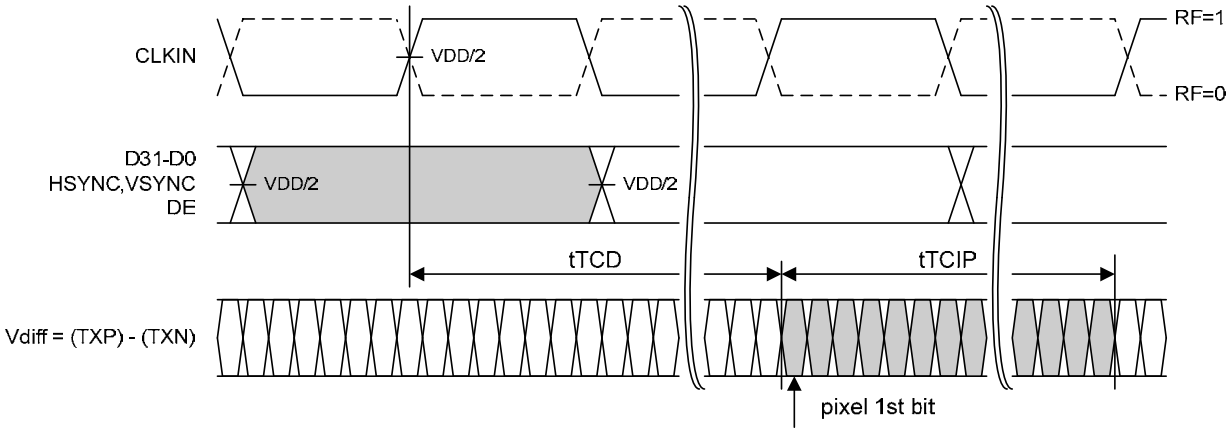


Figure 25. THCV235 Latency

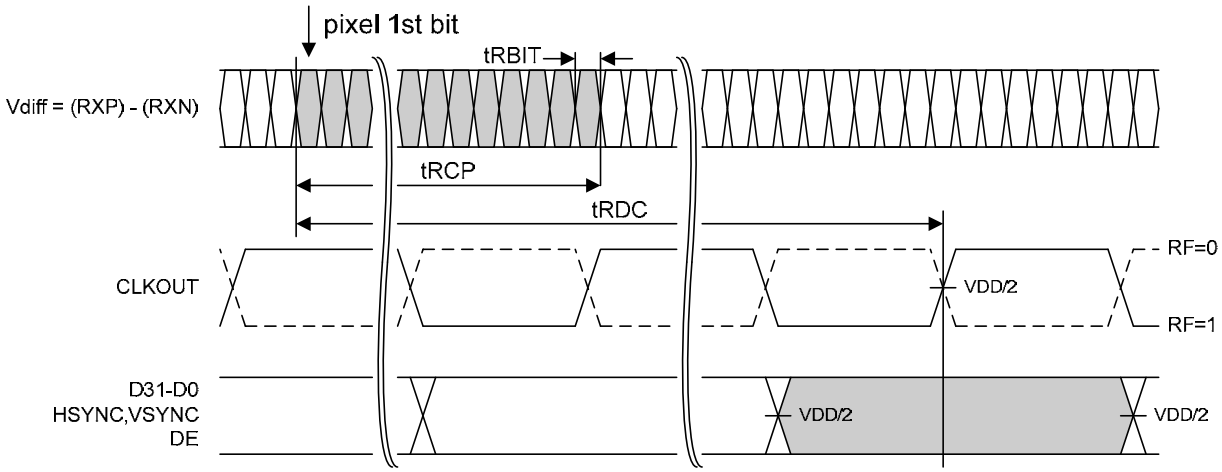


Figure 26. THCV236 Latency

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Lock and Unlock Sequence

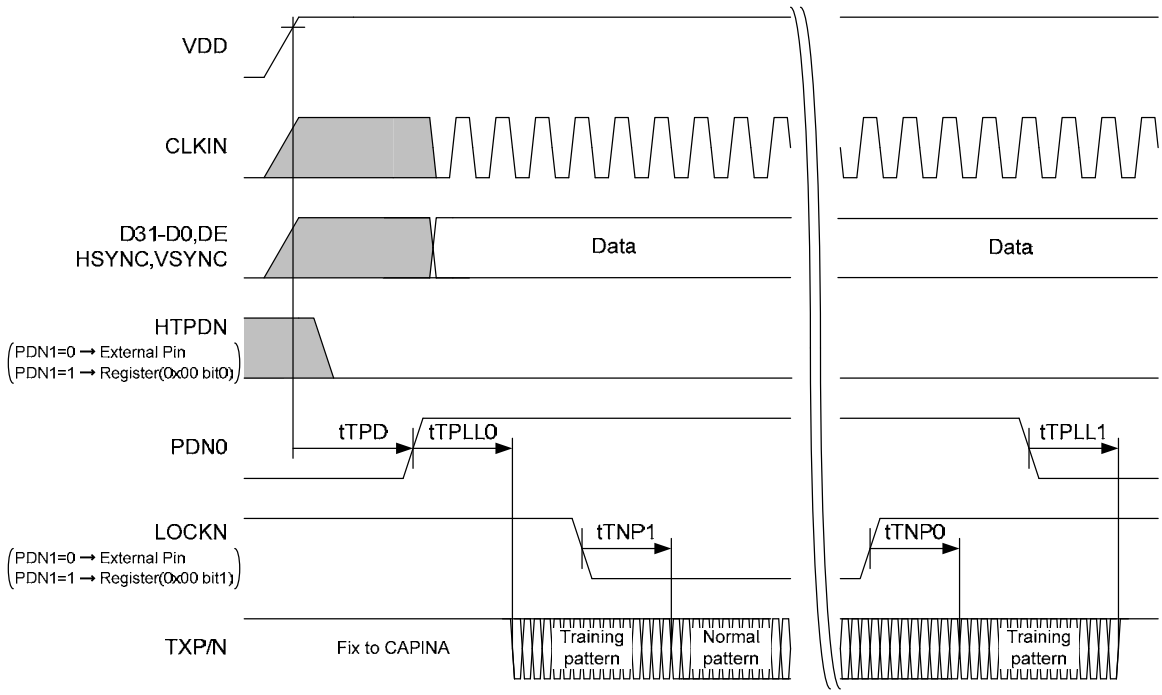
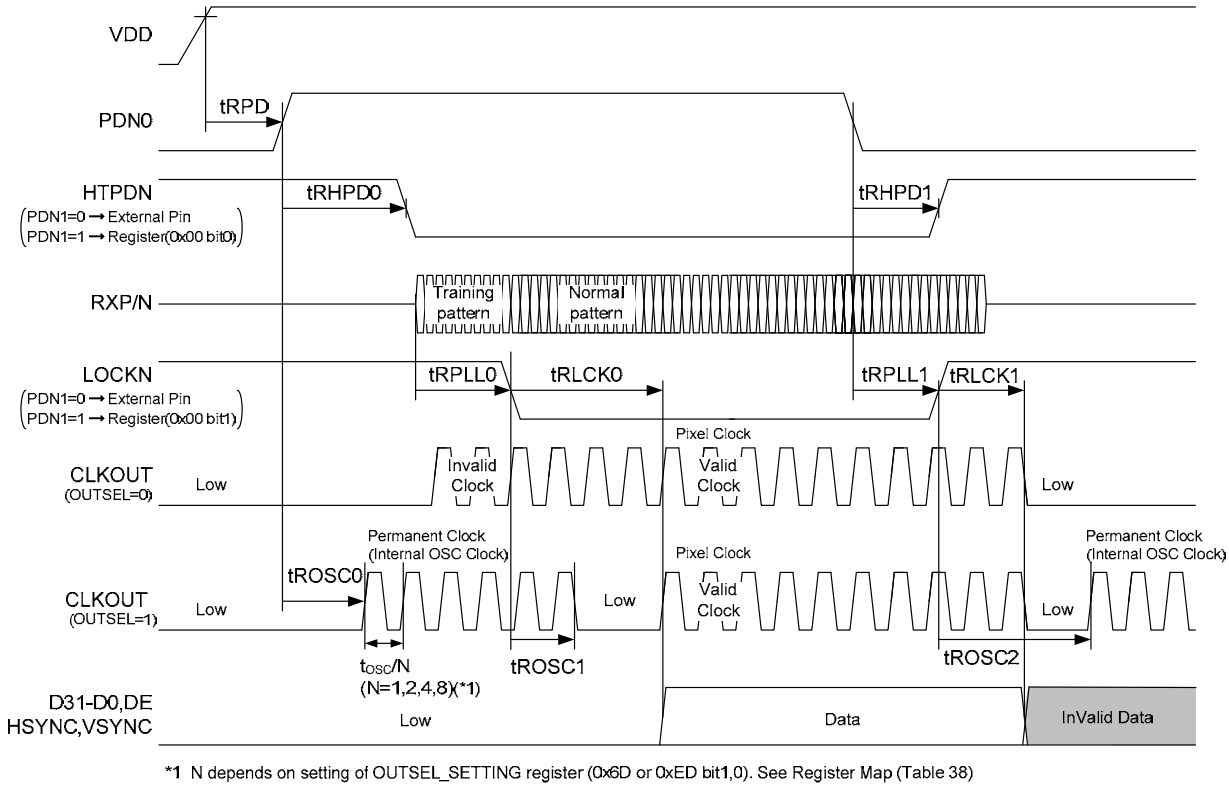


Figure 27. THCV235 Lock/Unlock Sequence



*1 N depends on setting of OUTSEL_SETTING register (0x6D or 0xED bit1,0). See Register Map (Table 38)

Figure 28. THCV236 Lock/Unlock Sequence

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2-wire serial I/F Switching Characteristics

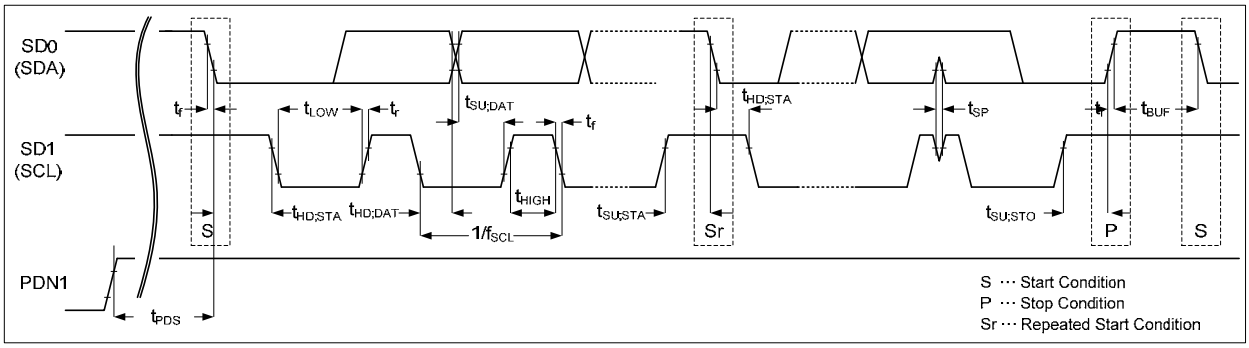


Figure 29. 2-wire serial interface Timing Diagram

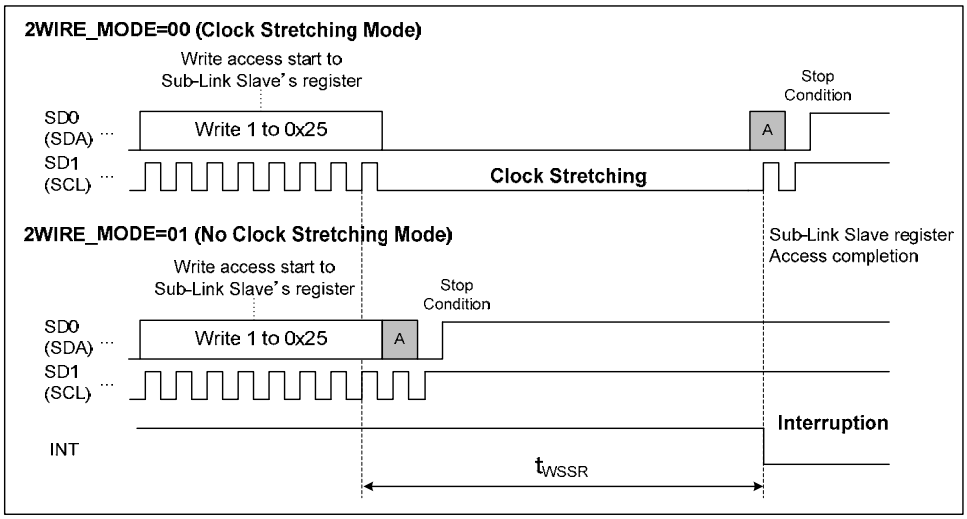


Figure 30. Write access completion time to Sub-Link Slave register

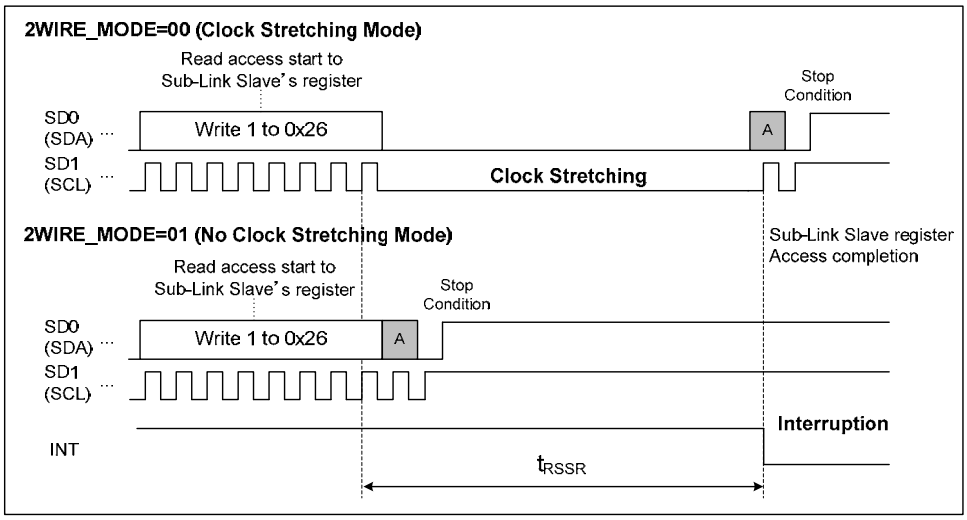


Figure 31. Read access completion time to Sub-Link Slave register

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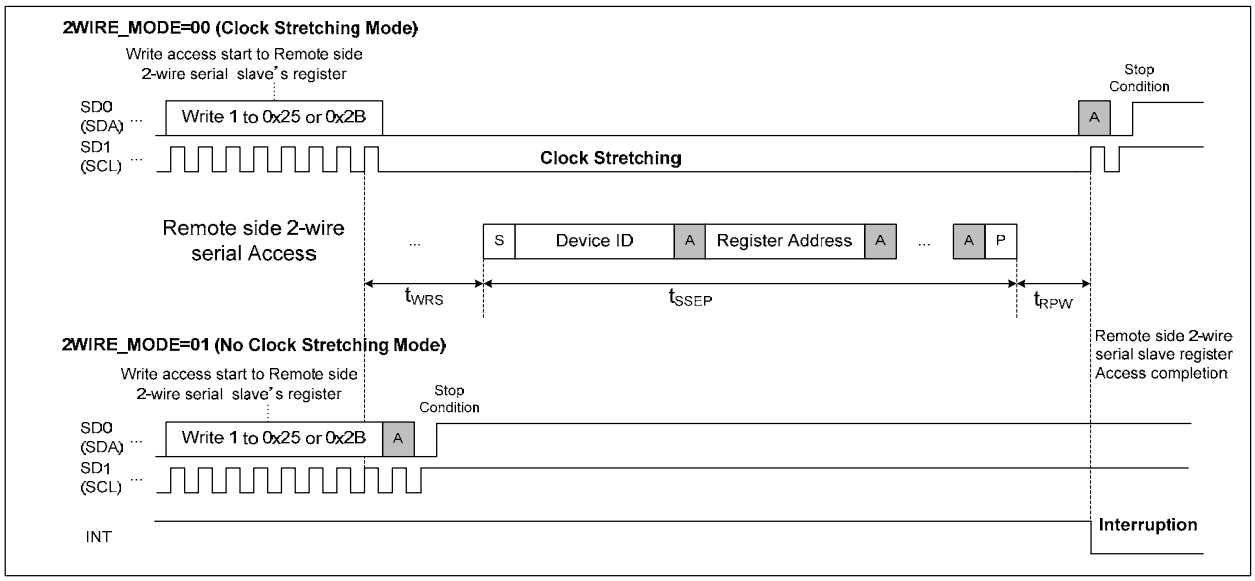


Figure 32. Write access completion time to Remote side 2-wire serial slave register

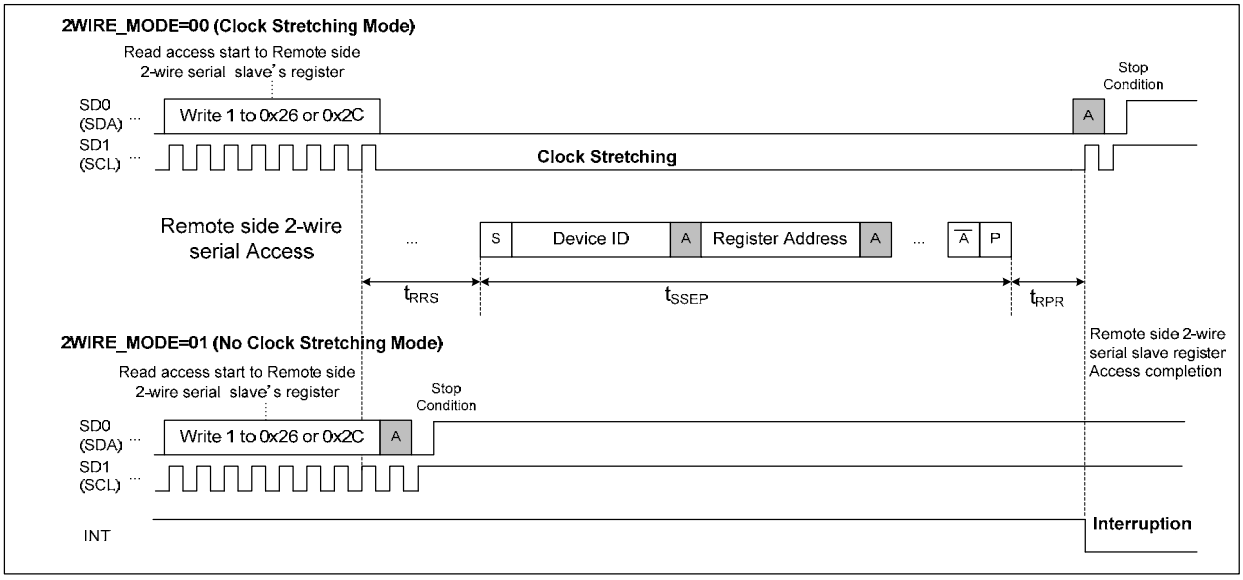


Figure 33. Read access completion time to Remote side 2-wire serial slave register

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GPIO Switching Characteristics

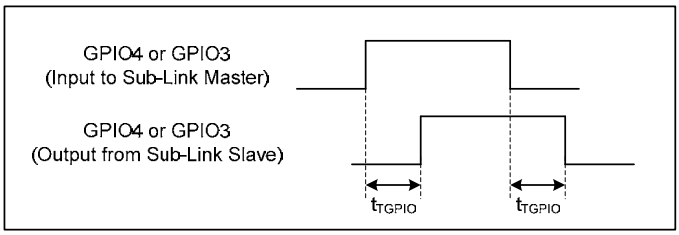


Figure 34. Through GPIO delay

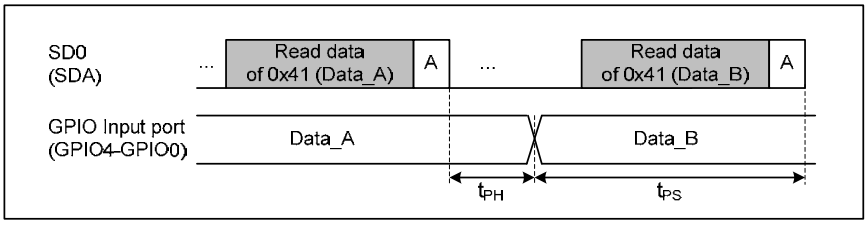


Figure 35. Programmable GPIO input timing at Sub-Link Master side

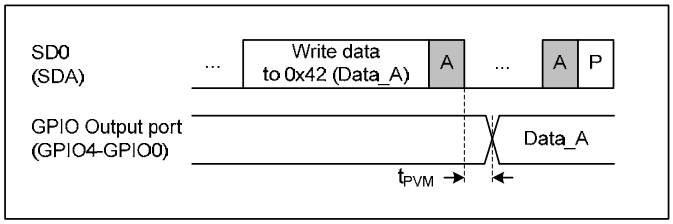


Figure 36. Programmable GPIO output timing at Sub-Link Master side

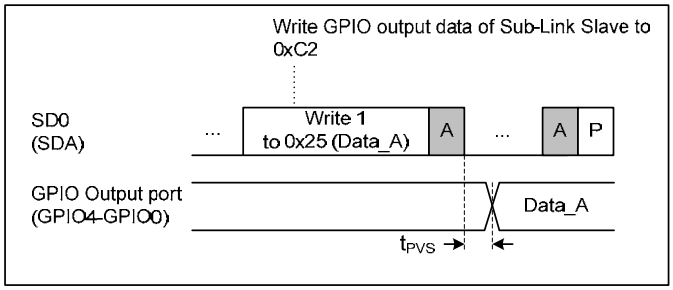


Figure 37. Programmable GPIO output timing at Sub-Link Slave side

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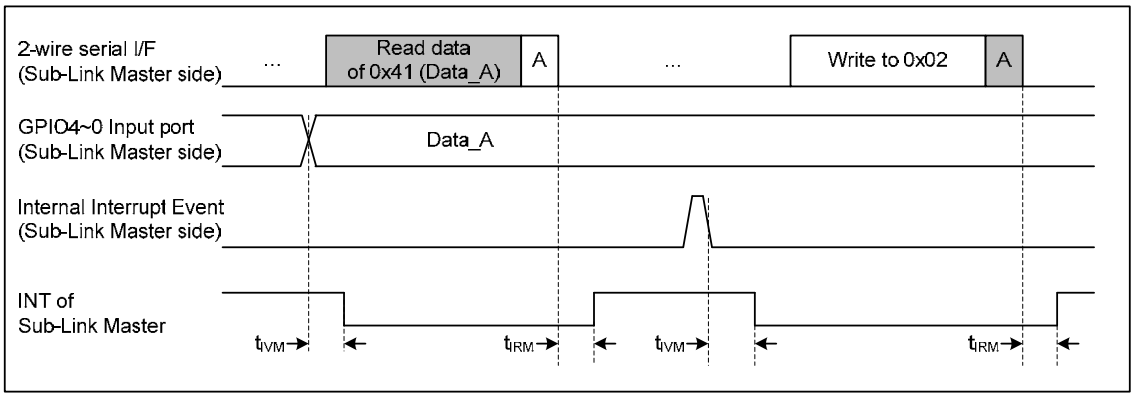


Figure 38. GPIO input and other interrupt event timing at Sub-Link Master side

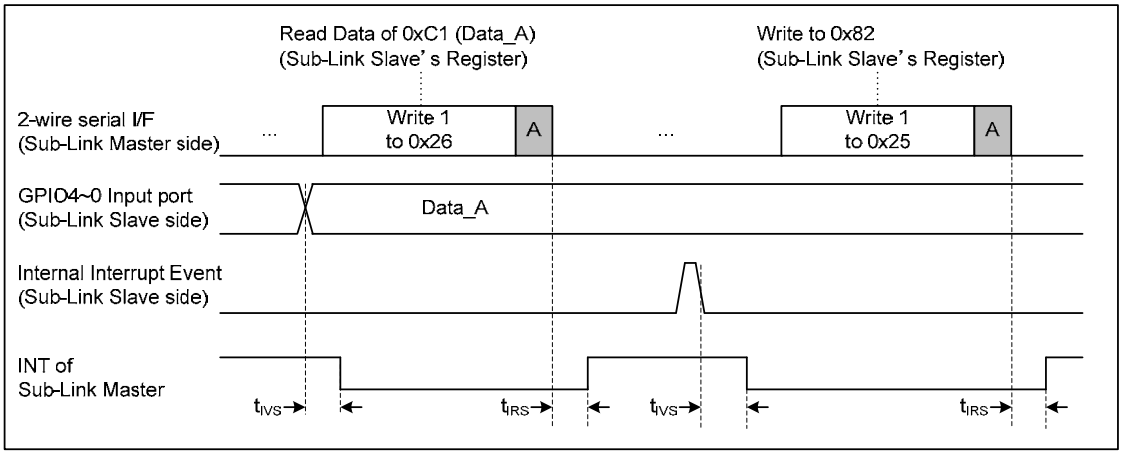


Figure 39. GPIO input and other interrupt event timing at Sub-Link Slave side (Clock Stretching Mode)

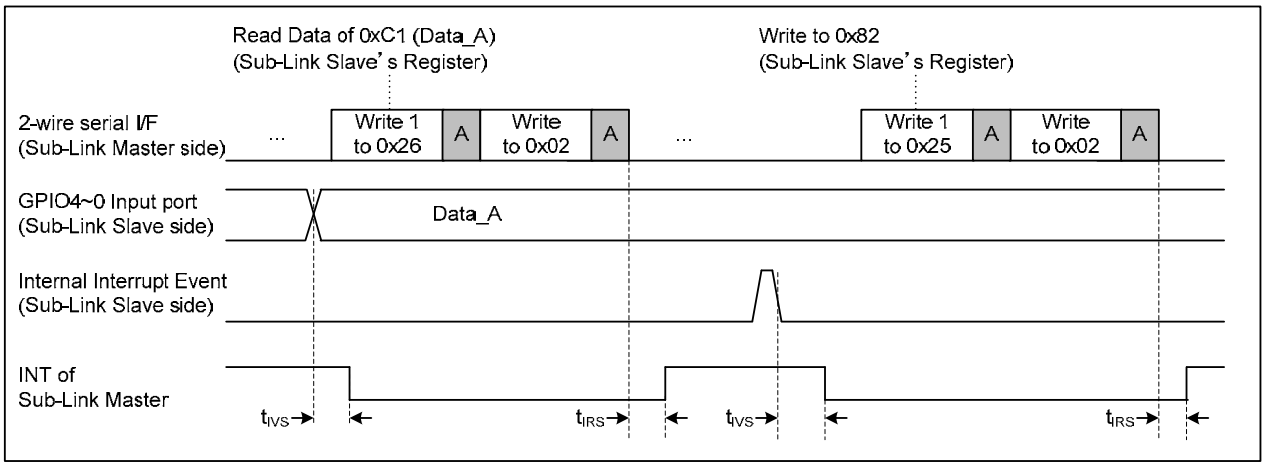


Figure 39. GPIO input and other interrupt event timing at Sub-Link Slave side (No Clock Stretching Mode)

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Low Speed Data Bridge Switching Characteristics

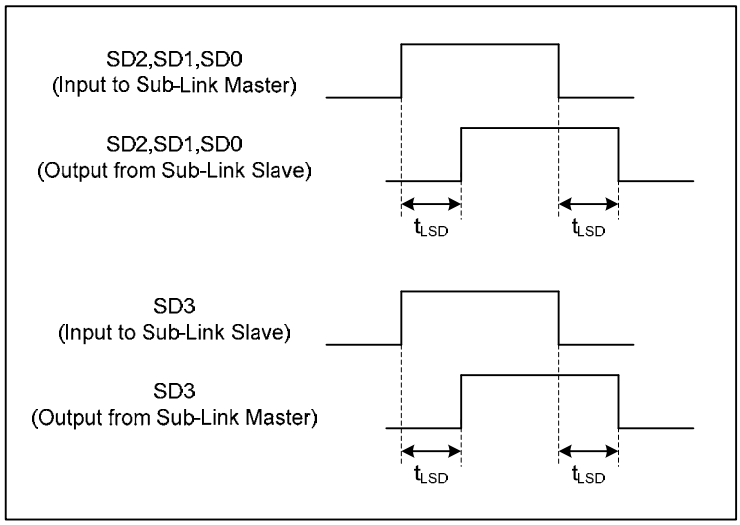


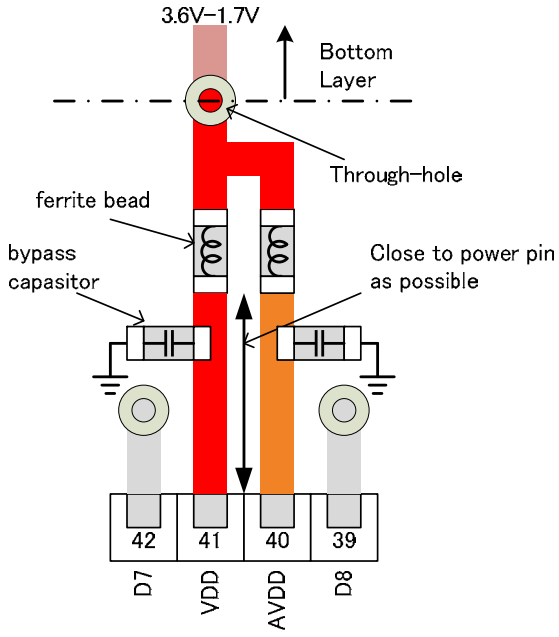
Figure 40. Low Speed Data Bridge Mode Data Delay

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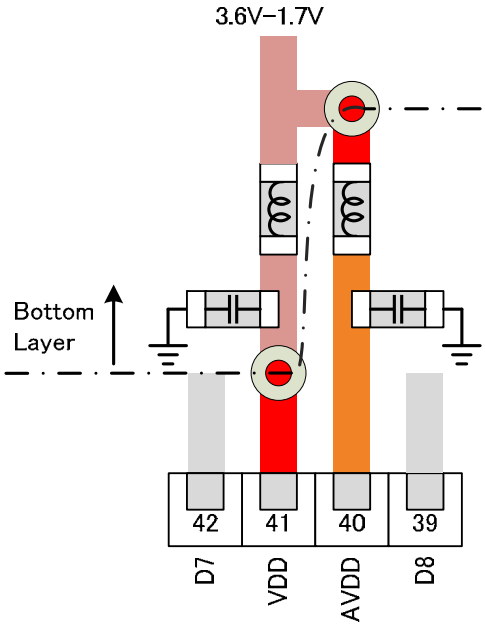
PCB Layout Guideline regarding VDD and AVDD for THCV236

When power is supplied from reverse side layer to AVDD, please place ferrite bead between through-hole and AVDD/VDD pins (Good Example1, 2). If it is needed to set ferrite beads on reverse side, please set GND-through-hole between AVDD and VDD, and separate the distance as possible (Example). Don't set through-holes next to each other between ferrite beads and AVDD/VDD pins (Bad Example).

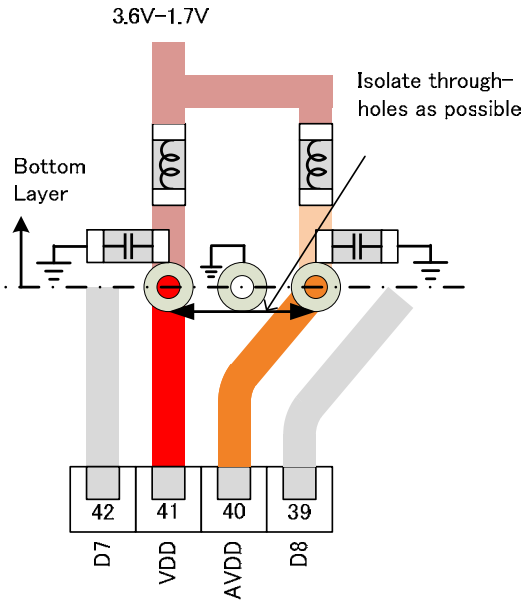
Good Example 1



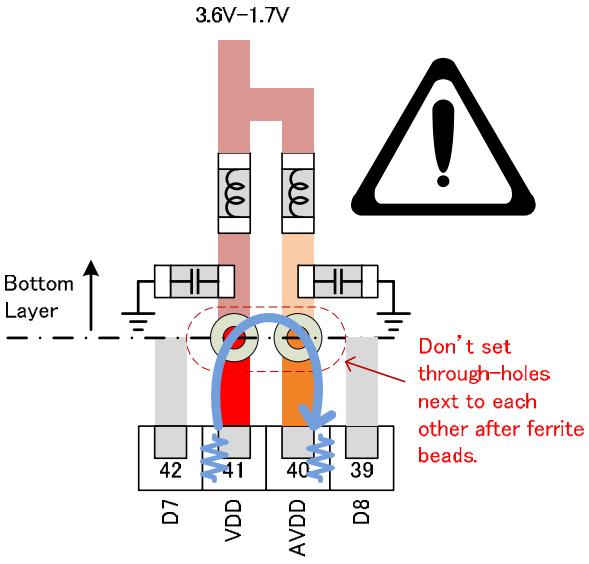
Good Example 2



Example

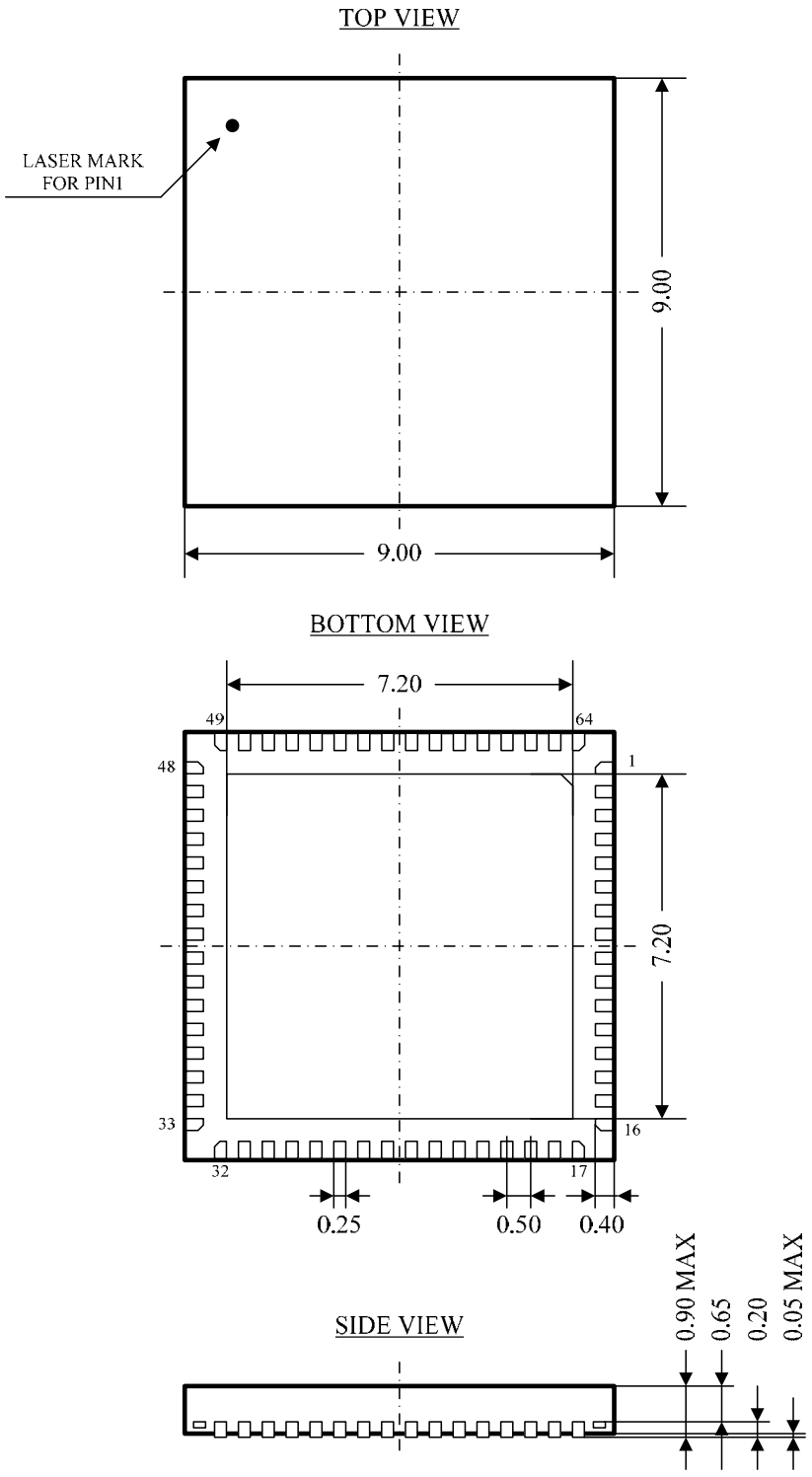


Bad Example



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Package



Unit : mm

Figure 41. 64-pin QFN package physical dimension

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10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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