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World's Leading Company in Mixed Signal Technologies

To Our Customers

Continuing it's rich tradition of partnering with high quality Japanese semiconductor suppliers, CEL is now partnering with THine from May of 2015 onwards.

THCS134

I/OSpreader TSSOP28

General Description

The THCS134 provides a function to serialize multiple parallel signals into single-ended serial line at least or to deserialize the data stream over single-ended serial line or single differential pair into multiple parallel signals.
This small number of transmission line simplifies system configuration and reduces system cost including cable width, connector size and pins and PCB layout area.

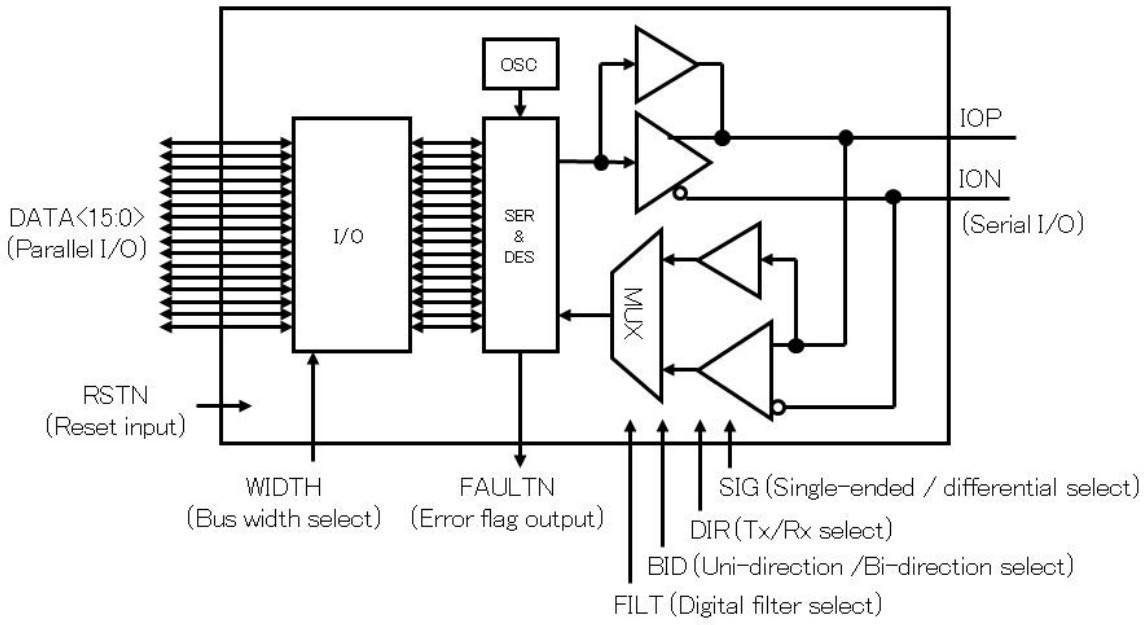
The THCS134 is offered in 8bit/16bit parallel IOs as host MPU interface. It can transfer 16bit independent parallel signals to remote side by only 1-line or 1-pair cable. Also, the THCS134 set as master device can control plural slave devices by transmitting and receiving data that is designated as a device address.
Transmitter, receiver or transceiver function can be selected by pins.

Features

- No External Clock Required.
-8bit/16bit Parallel IOs to MPU.
- Uni-directional/Bi-directional Mode Selectable
- Single-ended/Differential Mode (noise tolerant) Selectable
- AC Coupling Supported with Differential Mode
- Transmission Status Error Indicator Supported (Line Cut Detection and Packet Error Detection)
- Digital Filter Function.
- Power supply : 3.0 to 5.5V
- TSSOP 28-pin
- EU RoHS Compliant

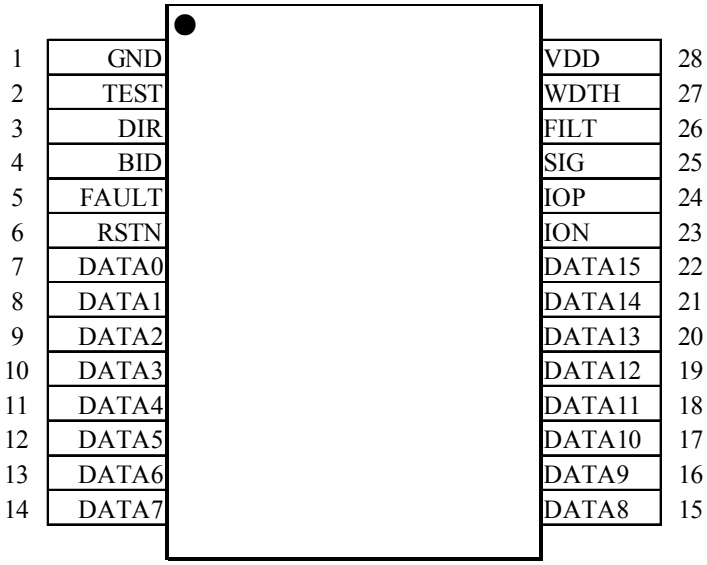
Block Diagram

THCS134



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Pin Diagram



Pin Description

Pin No.	Pin Name	Internal Processing	Description
1	GND	-	Ground
2	TEST	Input, Pull-down	Test pin. Please connect to GND.
3	DIR	Input, Pull-down	Transmitter/receiver select Low : Transmitter (Uni-direction) / Master (Bi-direction) High : Receiver (Uni-direction) / Slave (Bi-direction)
4	BID	Input, Pull-down	Uni-direction/Bi-direction mode select Low : Uni-direction High : Bi-direction
5	FAULTN	Output, Open-drain	Transmitter status error indicator Low : Abnormal operation detected
6	RSTN	Input, Pull-down	Reset input Low : Reset High : Normal operation
7-22	DATA0-15	Input/Output, Pull-down	Parallel data I/O bit : 0-15 Refer to the tables of “Parallel I/O Pin Function”
23	ION	Input/Output	Serial data differential mode(-) I/O
24	IOP	Input/Output	Serial data CMOS/differential mode(+) I/O
25	SIG	Input, Pull-down	Serial data I/O mode select Low : CMOS High : Differential
26	FILT	Input, Pull-down	Digital filter enable pin Low : OFF High : ON
27	WIDTH	Input, Pull-down	Data bit width select Low : 8bit High : 16bit
28	VDD	-	Power Supply

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Absolute Maximum Rating

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltage VDD	-	-0.4	-	6	V
Digital Input Voltage (DATA0-DAT15,WIDTH,BID,FILT,DIR,SIG, RSTN)	-	-0.4	-	6	V
Open-drain Output Pin(FAULTN)	-	-0.4	-	6	V
Allowable Power Dissipation	Ta=25℃	-	-	2	W
Storage Temperature	-	-55	-	150	℃
Junction Temperature	-	-	-	125	℃

Recommended Operating Condition

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltage VDD	-	3.0	-	5.5	V
Ambient Operating Temperature	-	-40	-	85	℃

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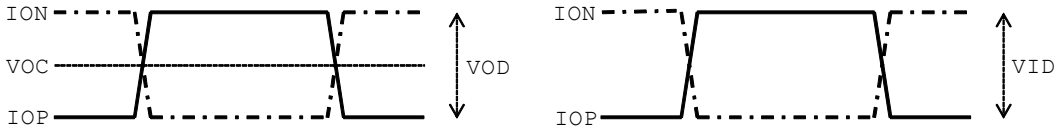
Electrical Characteristics DC Characteristics （at VDD＝5.0V, Ta=25℃, unless otherwise noted）

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Current	Mode E LVDS mode (Note)	-	20	30	mA
UVLO Threshold Voltage (VDD Rising)	-	-	2.6	2.8	V
UVLO Hysteresis Voltage	-	-	0.15	-	V
Digital Input High-level Voltage (VIH)	-	0.7VDD	-	-	V
Digital Input Low level Voltage (VIL)	-	-	-	0.3VDD	V
Digital Input Leakage Current 1	-	-	-	+/-50	uA
Digital Input Hysteresis Voltage	-	-	0.11VDD	-	V
Digital Output High-level Voltage (VOH)	VDD=3.0V Tj=125℃ IOH=-4mA	VDD-0.6	-	-	V
Digital Output High-level ON Resistance (RonH)	VDD=3.3V	-	56	-	Ω
	VDD=5.0V	-	46	-	Ω
Digital Output Low-level Voltage (VOL)	VDD=3.0V Tj=125 IOL=4mA	-	-	0.4	V
Digital Output Low-level ON Resistance (RonL)	VDD=3.3V	-	44	-	Ω
	VDD=5.0V	-	36	-	Ω
Open Drain Output Low-level Voltage	Iout=1mA FAULTN	-	-	0.4	V
LVDS Differential Input Voltage (VID)	IOP/ION	200	-	-	mV
LVDS Input Leakage Current	IOP/ION	-	-	+/-50	uA
LVDS Differential Output Voltage (VOD)	VDD=3.0V IOP/ION	350	-	-	mV
	VDD=5.0V IOP/ION	-	600	-	mV
	VDD=5.5V IOP/ION	-	-	750	mV
LVDS Output Common-mode Voltage (VOC)	IOP/ION	1.0	1.25	1.4	V
Pull-down Resistance	-	-	250	-	kΩ

Note: The power supply current is maximum in this condition.

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LVDS Input Output Differential Voltage

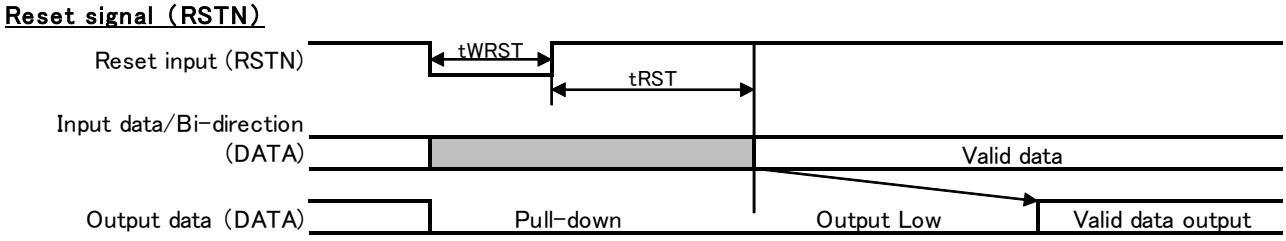


Electrical Characteristics AC Characteristics (Reset Section)

Mark	Parameter	Condition	Min	Typ	Max	Unit
tRST	Time from Reset (RSTN) Release to Valid Input	-	-	-	100 (Note)	us
tWRST	Reset (RSTN) Low Pulse Width	-	50	-	-	ns

Note : In AC coupling, tRST changes with the capacity to connect.

Timing Chart (Reset Section)



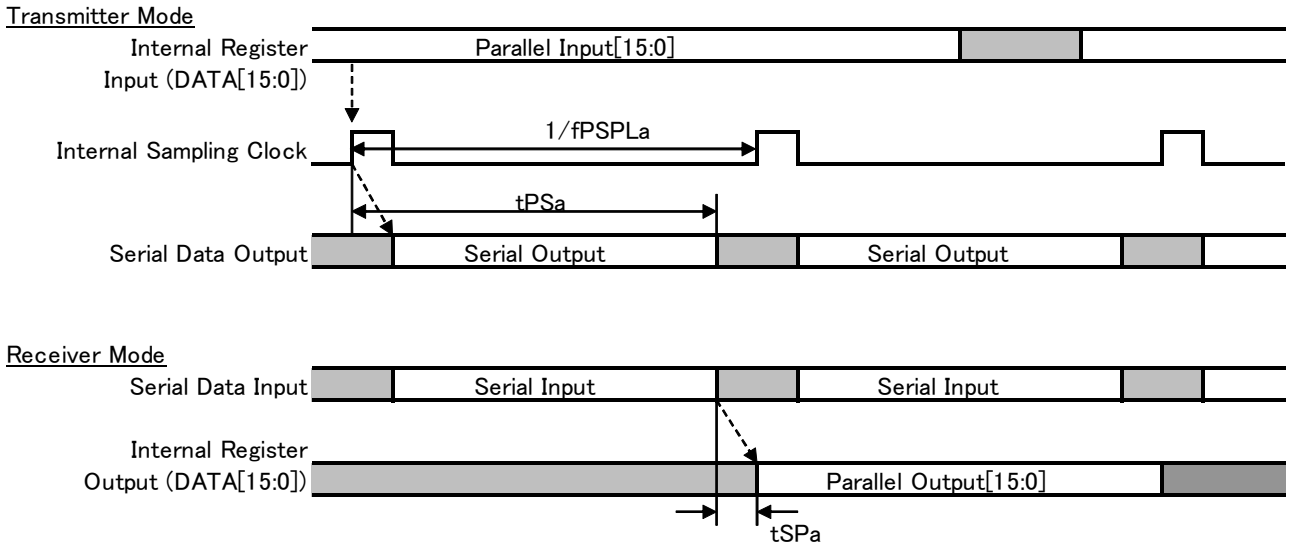
In the case of the mode F, output is controlled by signal of output enable (OEN_L/OEN_U), a pull-down state is continued until it sets signal of output enable to LOW.

Electrical Characteristics AC Characteristics (Serial Communication)

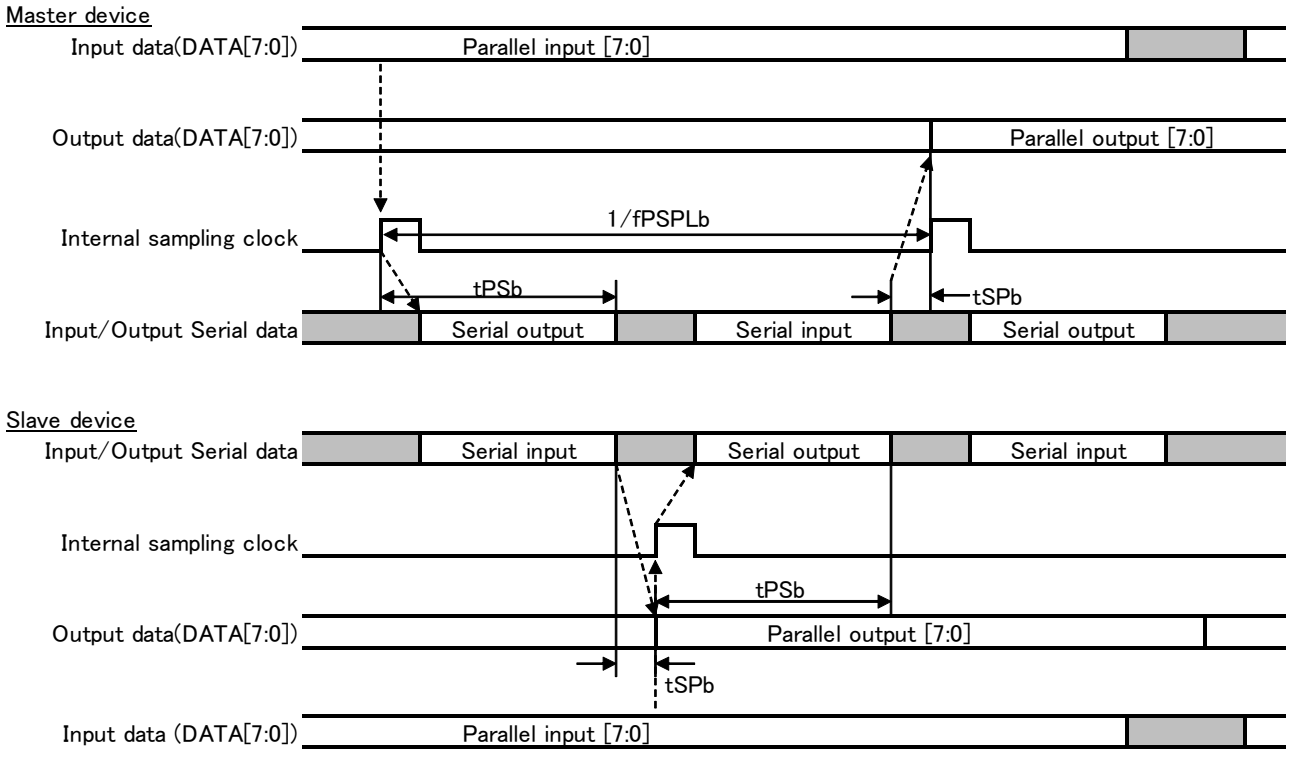
Mark	Item	Condition	Min	Typ	Max	Unit
fPSPLa	Serializer Input Sampling Frequency (Uni-direction)	BID=L	50	-	-	kHz
fPSPLb	Serializer Input Sampling Frequency (Bi-direction)	BID=H	30	-	-	kHz
tPSa	Time of Serializer Transmission (Uni-direction)	BID=L	-	-	18	us
tSPa	Deserializer Output Renewal Time (Uni-direction)	BID=L	-	-	2	us
tPSb	Time of Serializer Transmission (Bi-direction)	BID=H	-	-	14	us
tSPb	Deserializer Output Renewal Time (Bi-direction)	BID=H	-	-	2	us
fSTR	Serial Data Transmission Rate	-	-	2.5	-	MHz

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Timing Chart (Uni-direction Mode)



Timing Chart (Bi-direction Mode)



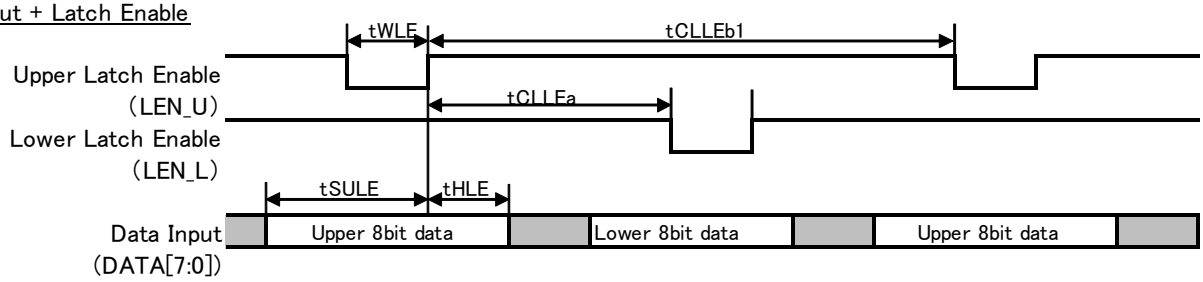
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Electrical Characteristics AC Characteristics (Latch Enable, Output Enable)

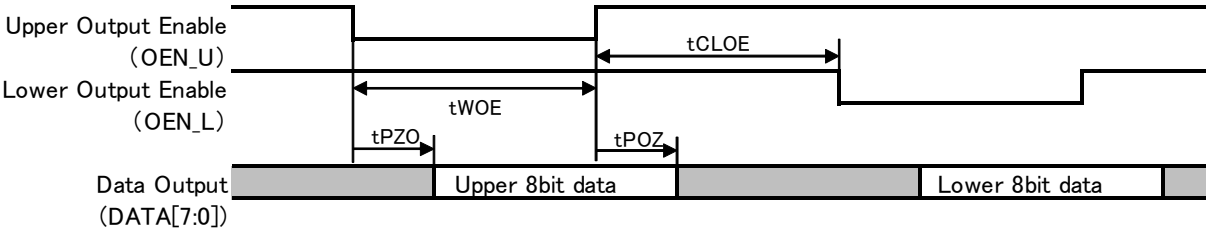
Symbol	Parameter	Condition	Min	Typ	Max	Unit
tWLE	Latch Enable（LEN_U/LEN_L/LEN）Pulse Width	-	130	-	-	ns
tSULE	Latch Enable （LEN_U/LEN_L/LEN）Rise Edge Setup Time	-	133	-	-	ns
tHLE	Latch Enable （LEN_U/LEN_L/LEN）Rise Edge Hold Time	-	20	-	-	ns
tCLLEa	Latch Enable （LEN_U/LEN_L/LEN） Clearance1	-	100	-	-	ns
tCLLEb1	Latch Enable （LEN_U/LEN_L/LEN） Clearance2 （Uni-direction）	-	20	-	-	us
tCLLEb2	Latch Enable （LEN）Clearance2（Bi-direction）	-	40	-	-	us
tWOE	Output Enable （OEN_U/OEN_L）Pulse Width	-	50	-	-	ns
tCLOE	Output Enable （OEN_U/OEN_L）Clearance	-	50	-	-	ns
tPZO	Output Enable （OEN_U/OEN_L）Delay Time	CL=25pF	-	-	50	ns
tPOZ	Output Disable （OEN_U/OEN_L）Delay Time	CL=25pF	-	-	38	ns

Timing Chart (Latch Enable, Output Enable)

8bit Input + Latch Enable



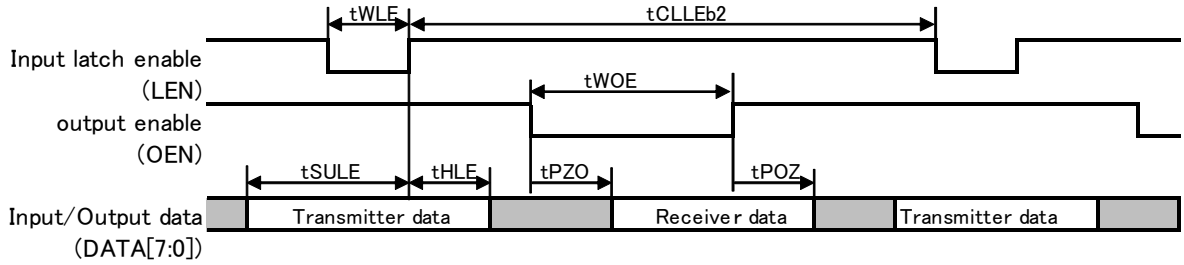
8bit Output+ Output Enable



When receiving new incoming data during OEN_U or OEN_L = Low, output data is updated to this new data.

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8bit Input/Output + Latch enable・Output enable



When receiving new incoming data during OEN = Low, output data is updated to this new data

Functional Description

・Functional Description List for Mode Pin

Mode Name	Pin Name					Operating Mode
	WIDTH	BID	DIR	DATA10	DATA11	
A	H	L	L	-	-	16bit / Bi-direction / Transmitter
B			H	-	-	16bit / Bi-direction / Receiver
C		H	L	-	-	8bit / Bi-direction / Transmitter・Receiver Master
D			H	-	-	8bit / Bi-direction / Transmitter・Receiver Slave
E	L	L	L	L	L	8bit（Upper・Lower）/ Uni-direction / Transmitter
F			H			8bit（Upper・Lower）/ Uni-direction / Receiver
G		H	L			8bit（Upper・Lower）/ Bi-direction / Transmitter・Receiver Master
H		L	H	-	H	8bit / Uni-direction / Transmitter Address Appointment
I		H				7-bit / Bi-direction / Transmitter Address Appointment Slave

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・Mode Connectable Table

Mode Name	A	B	C	D	E	F	G	H	I	Operating Mode
A		v				v		v		16bit / Uni-direction / Transmitter
B	v				v		v			16bit / Uni-direction / Receiver
C				v					v	8bit / Bi-direction / Transmitter・Receiver Master
D			v				v			8bit / Bi-direction / Transmitter・Receiver Master
E		v				v		v		8bit（Upper・Lower）/ Uni-direction / Transmitter
F	v				v					8bit（Upper・Lower）/ Uni-direction / Receiver
G		v		v					v	8bit（Upper・Lower）/ Bi-direction / Transmitter・Receiver Master
H	v				v					8bit / Uni-direction / Receiver Address Appointment
I			v				v			7-bit / Bi-direction / Transmitter Address Appointment Slave

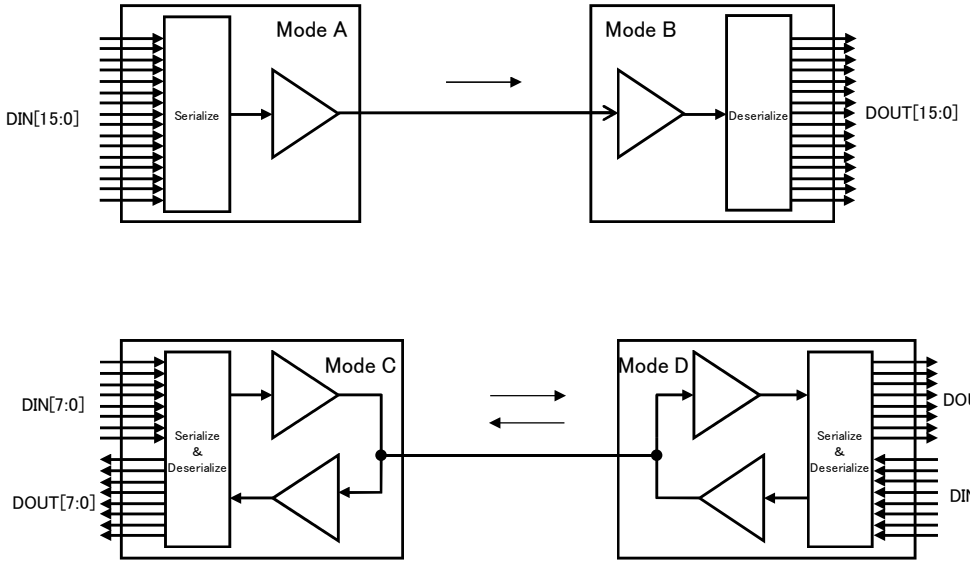
・「v」mark indicates a possible connection mode.

・Parallel I/O Pin Function (Mode A, B, C, D)

WIDTH	High（16bit）							
BID	Low（Uni-direction）		Low（Uni-direction）		High（Bi-direction）		High（Bi-direction）	
DIR	Low（Transmitter）		High（Receiver）		Low（Master）		High（Slave）	
Mode	A		B		C		D	
	I/O	Function Name	I/O	Function Name	I/O	Function Name	I/O	Function Name
DATA0	I	DIN0	O	DOUT0	I	DIN0	I	DIN0
DATA1	I	DIN1	O	DOUT1	I	DIN1	I	DIN1
DATA2	I	DIN2	O	DOUT2	I	DIN2	I	DIN2
DATA3	I	DIN3	O	DOUT3	I	DIN3	I	DIN3
DATA4	I	DIN4	O	DOUT4	I	DIN4	I	DIN4
DATA5	I	DIN5	O	DOUT5	I	DIN5	I	DIN5
DATA6	I	DIN6	O	DOUT6	I	DIN6	I	DIN6
DATA7	I	DIN7	O	DOUT7	I	DIN7	I	DIN7
DATA8	I	DIN8	O	DOUT8	O	DOUT0	O	DOUT0
DATA9	I	DIN9	O	DOUT9	O	DOUT1	O	DOUT1
DATA10	I	DIN10	O	DOUT10	O	DOUT2	O	DOUT2
DATA11	I	DIN11	O	DOUT11	O	DOUT3	O	DOUT3
DATA12	I	DIN12	O	DOUT12	O	DOUT4	O	DOUT4
DATA13	I	DIN13	O	DOUT13	O	DOUT5	O	DOUT5
DATA14	I	DIN14	O	DOUT14	O	DOUT6	O	DOUT6
DATA15	I	DIN15	O	DOUT15	O	DOUT7	O	DOUT7

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Connection Examples (Mode A, B, C, D)



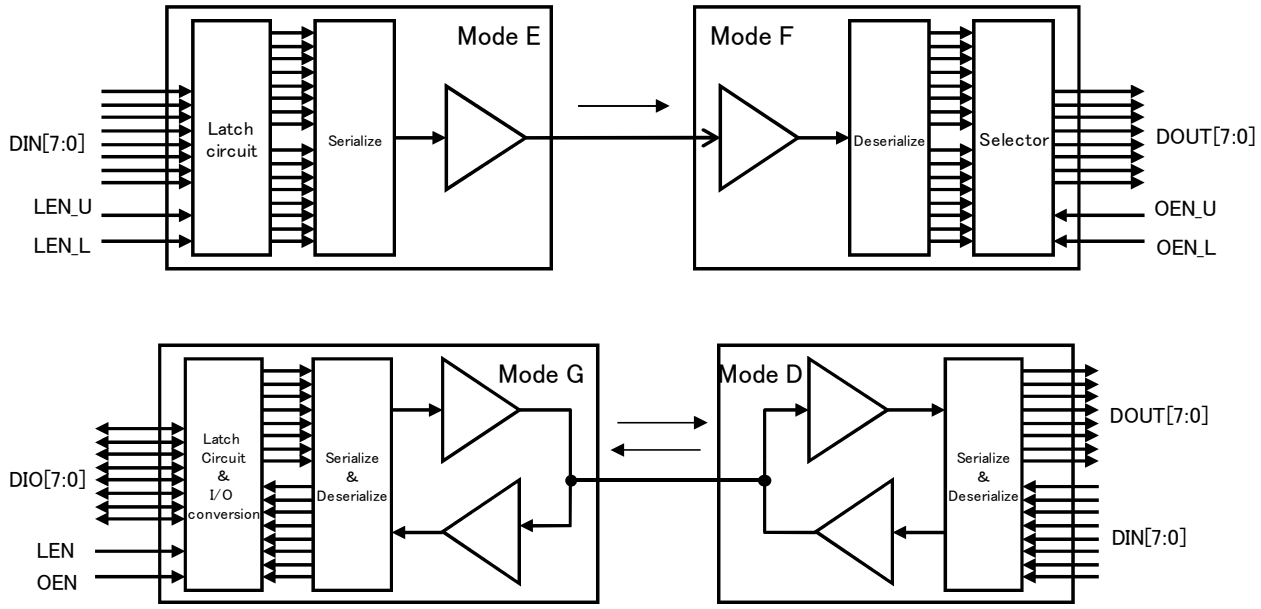
Parallel I/O Pin Function (Mode E, F, G)

WIDTH	Low（8bit Upper・Lower）					
BID	Low（Uni-direction）		Low（Uni-direction）		High（Bi-direction）	
DIR	Low（Transmitter）		High（Transmitter）		Low（Master）	
Mode	E		F		G	
	I/O	Function Name	I/O	Function Name	I/O	Function Name
DATA0	I	DIN0	O	DOUT0	IO	DIO0
DATA1	-	-	-	-	-	-
DATA2	I	DIN1	O	DOUT1	IO	DIO1
DATA3	-	-	-	-	-	-
DATA4	I	DIN2	O	DOUT2	IO	DIO2
DATA5	-	-	-	-	-	-
DATA6	I	DIN3	O	DOUT3	IO	DIO3
DATA7	-	-	-	-	-	-
DATA8	I	LEN_L	I	OEN_L	I	LEN
DATA9	I	LEN_U	I	OEN_U	I	OEN
DATA10	I	Low	I	Low	I	Low
DATA11	I	Low	I	Low	I	Low
DATA12	I	DIN4	O	DOUT4	IO	DIO4
DATA13	I	DIN5	O	DOUT5	IO	DIO5
DATA14	I	DIN6	O	DOUT6	IO	DIO6
DATA15	I	DIN7	O	DOUT7	IO	DIO7

*Non-functional pins marked as “-” are pulled down by 250kΩ internally

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Connection Example (Mode E, F, G)



・Latch Enable, Output Enable Truth Table

Mode E

LEN_U	LEN_L	Latch Enable Input
L	L	Lower 8bit is transmitted by sampling frequency (8bit through mode)
↑	H	Upper 8bit input latch
H	↑	Lower 8bit input latch and 16bit data reception
H	H	Keep data

The rising edge of LEN_L is the trigger for sampling of upper and lower data.

Mode F

OEN_U	OEN_L	Output Enable Input
L	L	Output disable （DATA pins are pulled down by 250kΩ internally）
L	H	Upper 8bit Output enable
H	L	Lower 8bit Output enable
H	H	Output disable （DATA pins are pulled down by 250kΩ internally）

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Mode G

LEN	OEN	Latch Enable、Output Enable Input
L	L	Prohibition
↑	H	8bit Input Latch
H	L	8bit Output enable
H	H	Output disable （DATA pins are pulled down by 250kΩ internally）

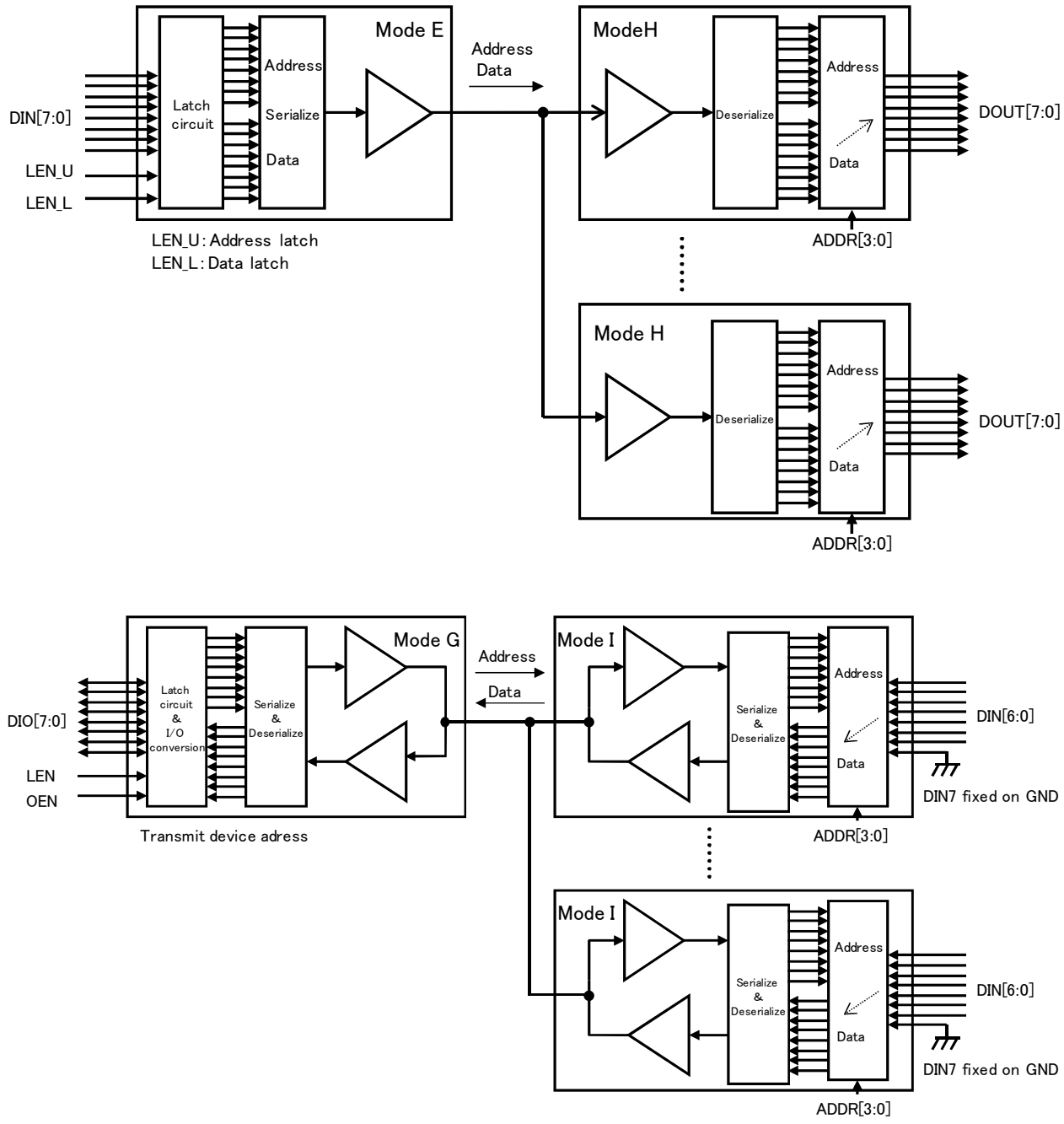
・Parallel I/O Pin Function (Mode H, I)

WIDTH	Low（8 / 7bit Upper・Lower）			
BID	Low（Uni-direction）		High（Bi-direction）	
DIR	High（Reception）		High（Reception）	
Mode	H		I	
	I/O	Function Name	I/O	Function Name
DATA0	O	DOUT0	I	DIN0
DATA1	O	DOUT1	I	DIN1
DATA2	O	DOUT2	I	DIN2
DATA3	O	DOUT3	I	DIN3
DATA4	O	DOUT4	I	DIN4
DATA5	O	DOUT5	I	DIN5
DATA6	O	DOUT6	I	DIN6
DATA7	O	DOUT7	I	Low
DATA8	-	-	-	-
DATA9	-	-	-	-
DATA10	-	-	-	-
DATA11	I	High	I	High
DATA12	I	ADDR0	I	ADDR0
DATA13	I	ADDR1	I	ADDR1
DATA14	I	ADDR2	I	ADDR2
DATA15	I	ADDR3	I	ADDR3

*Non-functional pins marked as "-" are pulled down by 250kΩ internally

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Connection Examples (Mode H, I)



Device Address (Mode H, I)

- As to transmitter device, set device address into upper 8bit and data into lower 8bit. The device address is selectable out of 15 addresses(10000001b～10001111b（81h～8Fh）)
- The upper 4 bits of receiver device address is fixed as 1000b, and lower 4 bits are set by ADDR[3:0] pins.
- Mode H offers to output the same data from all devices. Set to broadcast device address as 10000000b (80h). Mode I is not able to handle Broadcast.

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- Function Setup for Serial I/O Pins

  IOP and ION pins are set as 1 line CMOS I/O or 2-lane LVDS I/O with a SIG pin.

Pin Setup	Pin Function		Description
SIG	IOP	ION	
L	CMOS I/O	*	CMOS I/O
H	Differential mode I/O＋	Differential mode I/O	Differential mode I/O

＊: Please keep pin being opened(No connection)

- Function of Transmission Status Error Indicator, FAULTN (Receiver mode)

  FAULTN is the output pin. When the protocol of received data is not correct or serial data more than 50usec (typ) is not received, FAULTN pin will be changed into low level. The received data is canceled when a FAULTN pin outputs Low. When normal serial data is received, a FAULTN pin outputs High in case of pulled up externally.

- Digital Filter Function

  When FILT pin is set to high level, the digital filter function is active. If the receiver matches the 3 sampling frequency content with the deserialized parallel data, it is updated as the correct data.

- Writing and Reading of Parallel Data by Serial Communication

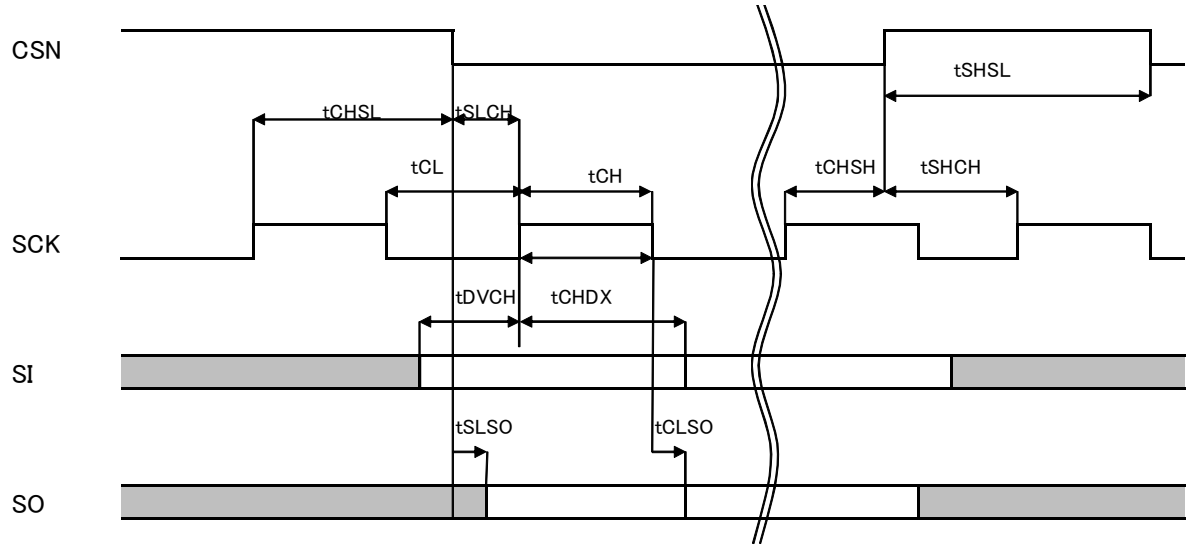
  The THCS134 is able to write and read data by 3-wire serial I/F on 16bit register.

Electrical Characteristic AC Characteristics (3-wire Serial I/O Unit)

Mark	Parameter	Condition	Min	Typ	Max	Unit
fSCK	SCK Frequency	-	-	-	10	MHz
tCH	SCK High period	-	50	-	-	ns
tCL	SCK Low period	-	50	-	-	ns
tDVCH	SI Setup time	-	10	-	-	ns
tCHDX	SI Hold time	-	15	-	-	ns
tCHSL	CSN Not Active Hold time	-	10	-	-	ns
tSLCH	CSN Active Setup time	-	200	-	-	ns
tCHSH	CSN Active Hold time	-	50	-	-	ns
tSHCH	CSN Not Active Set up time	-	50	-	-	ns
tSHSL	CSN Not Active period	-	2	-	-	us
tSLSO	Delay time From CSN Fall to SO Output	CL=25pF	-	-	190	ns
tCLSO	Delay time From SCK Fall to SO Output	CL=25pF	-	-	40	ns

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Timing Chart (3-wire Serial I/O Unit)



Function Description

- Mode Pin Function Setting List

Mode Name	Pin Name				Operating Mode
	WIDTH	BID	DIR	Etc	
A serial	L	L	L	DATA10:H DATA11:L	Serial / Uni-direction / Transmitter
B serial		L	H		Serial / Uni-direction / Receiver
C serial		H	L		Serial / Bi-direction / Master

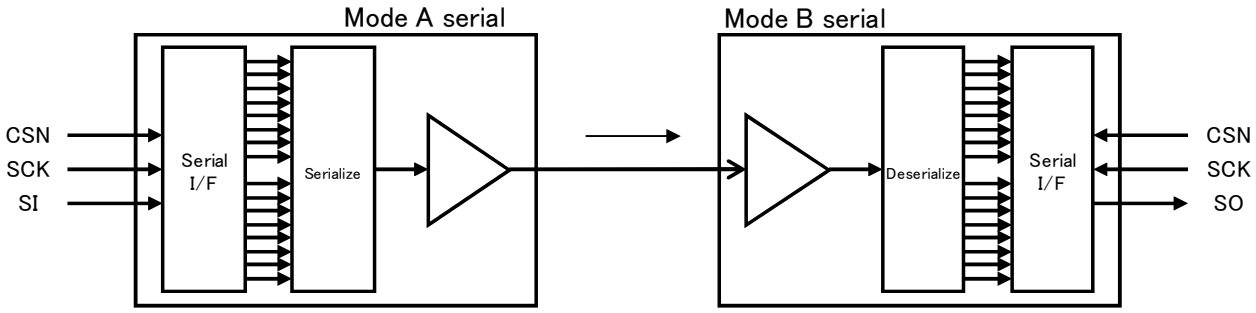
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- Parallel I/O Pin Function (Mode A serial, B serial, C serial)

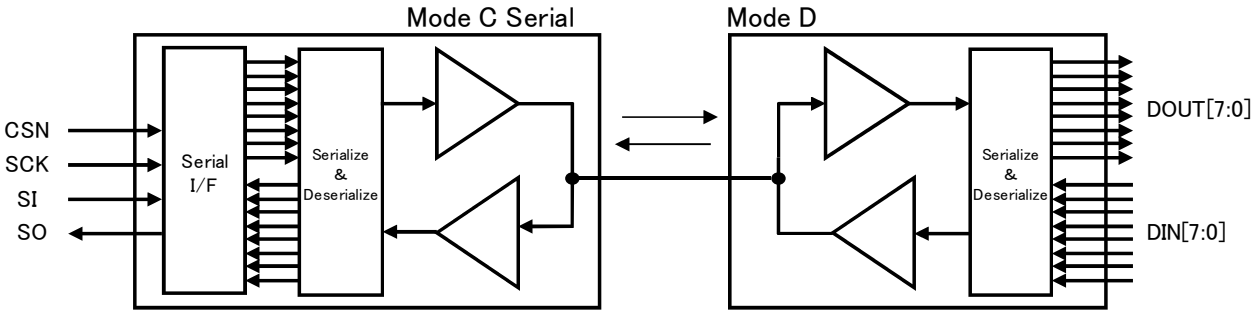
WIDTH	Low（3 lines serial）					
BID	Low（Uni-direction）		Low（Uni-direction）		High（Bi-direction）	
DIR	Low（Transmitter）		High（Transmitter）		Low（Master）	
Mode	A Serial		B Serial		C Serial	
	I/O	Function name	I/O	Function name	I/O	Function name
DATA0	I	CSN	I	CSN	I	CSN
DATA1	I	SCK	I	SCK	I	SCK
DATA2	I	SI	-	-	I	SI
DATA3	-	-	O	SO	O	SO
DATA4	-	-	-	-	-	-
DATA5	-	-	-	-	-	-
DATA6	-	-	-	-	-	-
DATA7	-	-	-	-	-	-
DATA8	-	-	-	-	-	-
DATA9	-	-	-	-	-	-
DATA10	I	High	I	High	I	High
DATA11	I	Low	I	Low	I	Low
DATA12	-	-	-	-	-	-
DATA13	-	-	-	-	-	-
DATA14	-	-	-	-	-	-
DATA15	-	-	-	-	-	-

* Unnamed pin is pulled down by 250kΩ internally.

- Connection Examples (Mode A serial, B serial, C serial)



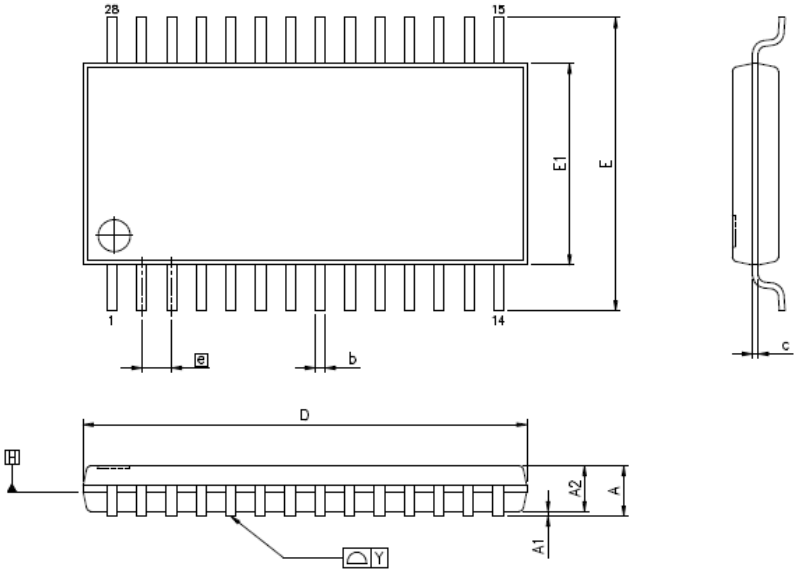
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Package

TSSOP-28pin



SYMBOLS	MIN.	NOM	MAX.
A	-	-	1.20
A1	0.00	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L1	0.45	0.60	0.75
S	0.20	-	-
θ	0°	-	8°
Y	0.10		

Unit: mm

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