THCS133

I/OSpreader

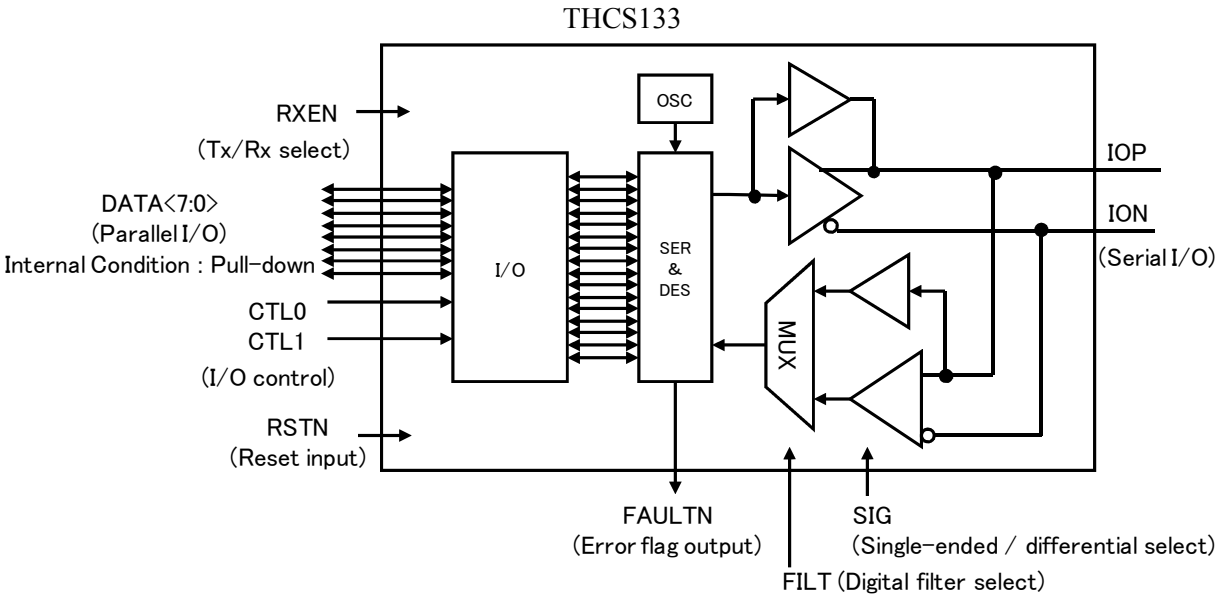
General Description

The THCS133 provides a function to serialize multiple parallel signals into single-ended serial line at least or to deserialize the data stream over single-ended serial line or single differential pair into multiple parallel signals.
This small number of transmission line simplifies system configuration and reduces system cost including cable width, connector size and pins and PCB layout area.
The THCS133 is offered in 8bit parallel IOs as host MPU interface.
It can transfer 8bit independent parallel signals to remote side by only 1-line or 1-pair cable.
Transmitter or receiver function can be selected by pin.

Features

- No External Clock Required.
-8bit Parallel IOs to MPU.
- Single-ended/Differential Mode (noise tolerant) Selectable
- AC Coupling Supported with Differential Mode
- Transmission Status Error Indicator Supported (Line Cut Detection and Packet Error Detection)
- Digital Filter Function
- Power supply : 3.0 to 5.5V
- DIP 20-pin Package
- EU RoHS Compliant

Block Diagram



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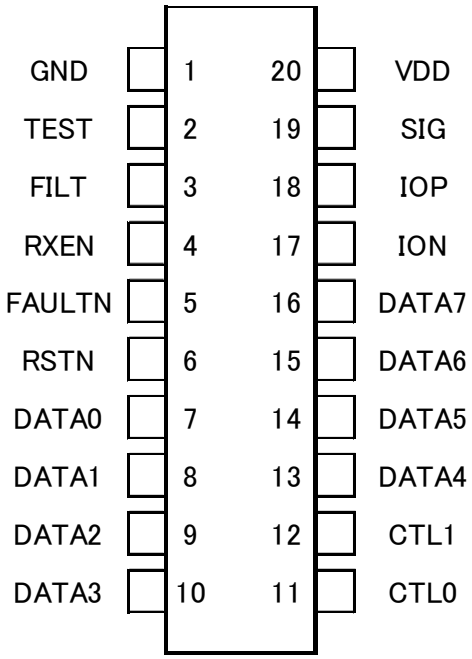
Pin Diagram



Pin Description

Pin No.	Pin Name	Internal Condition	Description
1	GND	-	Ground
2	TEST	Input, Pull-down	Test pin. Please connect to GND
3	FILT	Input, Pull-down	Digital filter enable pin Low : OFF High : ON
4	RXEN	Input, Pull-down	Receiver mode enable
5	FAULTN	Output, Open-drain	Transmitter status error indicator Low : Abnormal operation detected
6	RSTN	Input, Pull-down	Reset input Low : Reset High : Normal operation
7-10 13-16	DATA0-7	Input/Output, Pull-down	Parallel data I/O bit : 0-7
11	CTL0	Input, Pull-down	Lower 8bit input latch (Transmitter mode) Lower 8bit Output enable (Receiver mode)
12	CTL1	Input, Pull-down	Upper 8bit input latch (Transmitter mode) Upper 8bit Output enable (Receiver mode)
17	ION	Input/Output	Serial data differential mode(-) I/O
18	IOP	Input/Output	Serial data CMOS/differential mode(+) I/O
19	SIG	Input, Pull-down	Serial data I/O mode select Low : CMOS High : Differential
20	VDD	-	Power Supply

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Absolute Maximum Rating

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltage VDD	-	-0.4	-	6	V
Digital Input Voltage (DATA0-DAT7, FILT, RXEN, CTL0, CTL1, RSTN, SIG)	-	-0.4	-	6	V
Open-drain Output Pin(FAULTN)	-	-0.4	-	6	V
Allowable Power Dissipation	Ta=25℃	-	-	1	W
Storage Temperature	-	-55	-	150	℃
Junction Temperature	-	-	-	125	℃

Recommended Operating Condition

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Voltage VDD	-	3.0	-	5.5	V
Ambient Operating Temperature	-	-40	-	85	℃

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Electrical Characteristics DC Characteristics （at VDD＝5.0V, Ta=25℃, unless otherwise noted）

Parameter	Condition	Min	Typ	Max	Unit
Power Supply Current	Transmitter mode LVDS mode (Note)	-	20	30	mA
UVLO Threshold Voltage (VDD Rising)	-	-	2.6	2.8	V
UVLO Hysteresis Voltage	-	-	0.15	-	V
Digital Input High-level Voltage (VIH)	-	0.7VDD	-	-	V
Digital Input Low level Voltage (VIL)	-	-	-	0.3VDD	V
Digital Input Leakage Current 1	Except CTL1	-	-	+/-50	uA
Digital Input Leakage Current 2	CTL1	-	-	+/-150	uA
Digital Input Hysteresis Voltage	-	-	0.11VDD	-	V
Digital Output High-level Voltage (VOH)	VDD=3.0V Tj=125℃ Iout=4mA	VDD-0.6	-	-	V
Digital Output High-level ON Resistance (RonH)	VDD=3.3V	-	56	-	Ohm
	VDD=5.0V	-	46	-	Ohm
Digital Output Low-level Voltage (VOL)	VDD=3.0V Tj=125℃ Iout=4mA	-	-	0.4	V
Digital Output Low-level ON Resistance (RonL)	VDD=3.3V	-	44	-	Ohm
	VDD=5.0V	-	36	-	Ohm
Open Drain Output Low-level Voltage	Iout=1mA FAULTN	-	-	0.4	V
LVDS Differential Input Voltage (VID)	IOP/ION	200	-	-	mV
LVDS Input Leakage Current	IOP/ION	-	-	+/-50	uA
LVDS Differential Output Voltage (VOD)	VDD=3.0V IOP/ION	350	-	-	mV
	VDD=5.0V IOP/ION	-	600	-	mV
	VDD=5.5V IOP/ION	-	-	750	mV
LVDS Output Common-mode Voltage (VOC)	IOP/ION	1.0	1.25	1.4	V
Pull-down Resistance	-	-	250	-	kOhm

Note: The power supply current is maximum in this condition.

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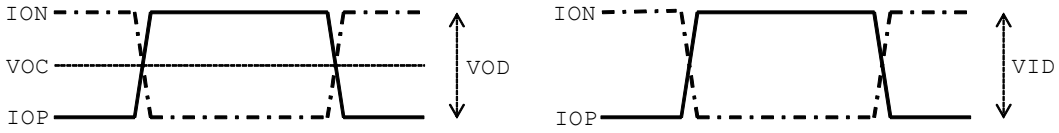
LVDS Input Output Differential Voltage

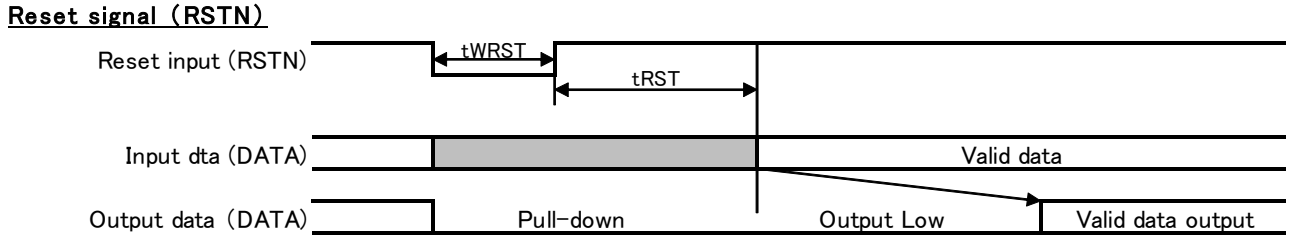


Electrical Characteristics AC Characteristics (Reset Section)

Mark	Parameter	Condition	Min	Typ	Max	Unit
tRST	Time from Reset (RSTN) Release to Valid Input	-	-	-	100 (Note)	us
tWRST	Reset (RSTN) Low Pulse Width	-	50	-	-	ns

Note : In AC coupling, tRST changes with the capacity to connect.

Timing Chart (Reset Section)



In case Output is controlled by signal of output enable (CTL0, CTL1), a pull-down state is continued until it sets signal of output enable to LOW.

Electrical Characteristics AC Characteristics (Serial Communication)

Mark	Item	Condition	Min	Typ	Max	Unit
fPSPL	Serializer Input Sampling Frequency	-	50	-	-	kHz
tPS	Time of Serializer Transmission	-	-	-	18	us
tSP	Deserializer Output Renewal Time	-	-	-	2	us
fSTR	Serial Data Transmission Rate	-	-	2.5	-	MHz

Timing Chart

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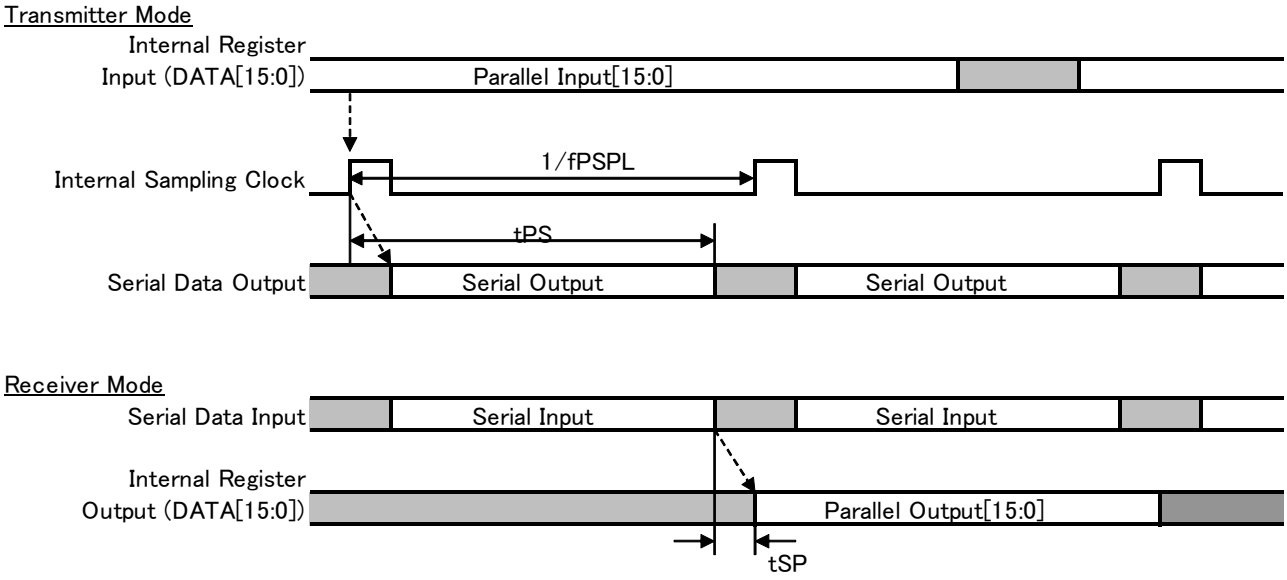
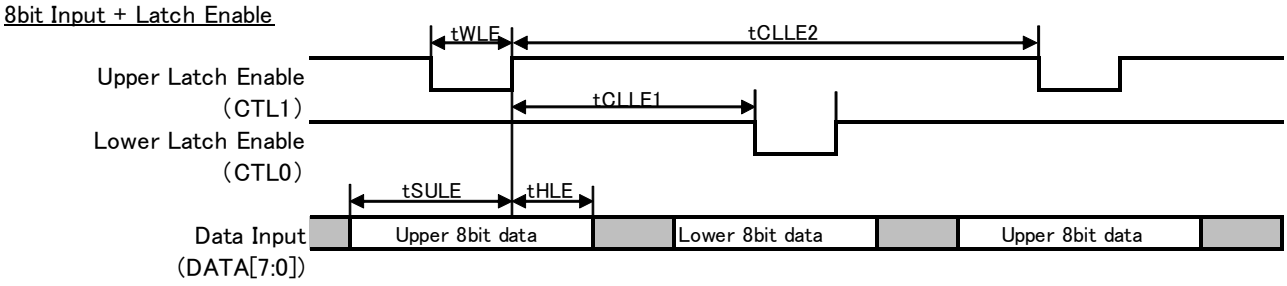


Internal sampling clock and CTL signals are asynchronous.

Electrical Characteristics AC Characteristics (Latch Enable, Output Enable)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tWLE	Latch Enable Pulse Width	-	130	-	-	ns
tSULE	Latch Enable Rise Edge Setup Time	-	133	-	-	ns
tHLE	Latch Enable Rise Edge Hold Time	-	20	-	-	ns
tCLLE1	Latch Enable Clearance1	-	100	-	-	ns
tCLLE2	Latch Enable Clearance2	-	20	-	-	us
tWOE	Output Enable Pulse Width	-	50	-	-	ns
tCLOE	Output Enable Clearance	-	50	-	-	ns
tPZO	Output Enable Delay Time	CL=25pF	-	-	50	ns
tPOZ	Output Disable Delay Time	CL=25pF	-	-	38	ns

Timing Chart (Latch Enable, Output Enable)



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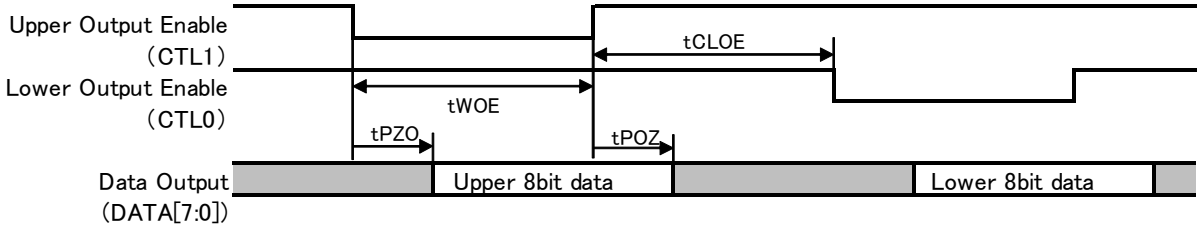
8bit Output + Output Enable



When receiving new incoming data during CTL0 or CTL1 = Low, output data is updated to this new data.

・Latch Enable, Output Enable Truth Table

Transmitter mode

CTL1	CTL0	Latch Enable Input
L	L	Lower 8bit data is transmitted by sampling frequency (8bit through mode)
↑	H	Upper 8bit input latch
H	↑	Lower 8bit input latch and 16-bit data reception
H	H	Keep data

The rising edge of CTL0 is the trigger for sampling of upper and lower data.

Receiver mode

CTL1	CTL0	Output Enable Input
L	L	Output disable (DATA pins are pulled down by 250kΩ internally)
L	H	Upper 8bit Output enable
H	L	Lower 8bit Output enable
H	H	Output disable (DATA pins are pulled down by 250kΩ internally)

・Transmitter or Receiver select

Pin RXEN	Description
H	Receiver mode (Serial to Parallel)
L	Transmitter mode (Parallel to Serial)

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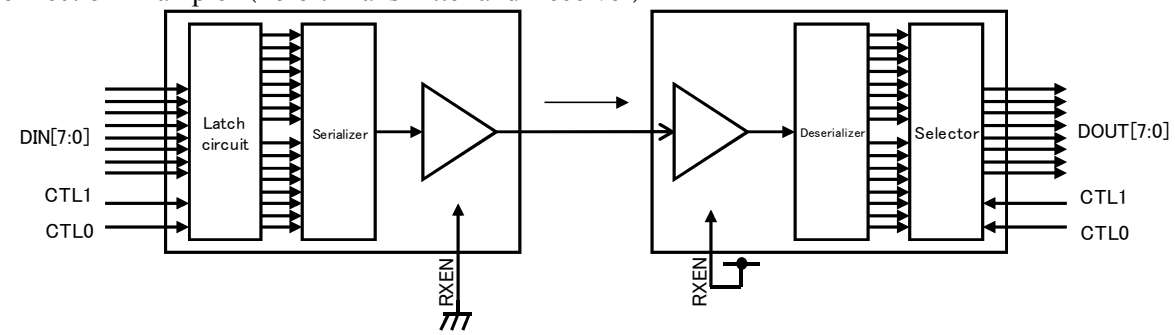
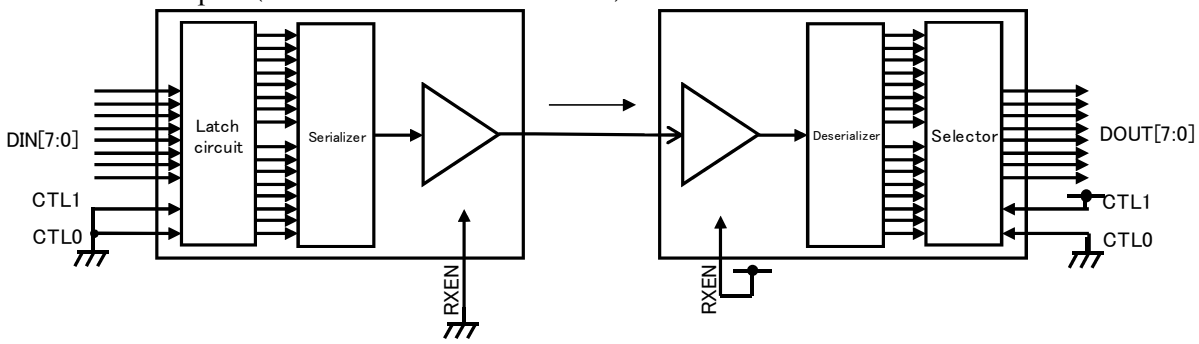
・Connection Example（16-bit Transmitter and Receiver）



・Connection Example（8bit Transmitter and Receiver）



・Function Setup for Serial I/O Pins

IOP and ION pins are set as 1 lane CMOS I/O or 2-lane LVDS I/O with a SIG pin.

Pin Setup	Function		Description
SIG	IOP	ION	
L	CMOS I/O	*	CMOS I/O
H	Differential mode I/O＋	Differential mode I/O-	Differential mode I/O

＊: Please keep pin open (No connection)

・Function of Transmission Status Error Indicator, FAULTN (Receiver mode)

FAULTN is the output pin. When the protocol of received data is not correct or serial data more than 50usec (typ) is not received, FAULTN pin will be changed into low level. The received data is canceled when a FAULTN pin outputs Low. When normal serial data is received, a FAULTN pin outputs High in case of pulled up externally.

・Digital Filter Function

When FILT pin is set to high level, the digital filter function is active. If the receiver matches the 3 sampling frequency content with the deserialized parallel data, it is updated as the correct data.

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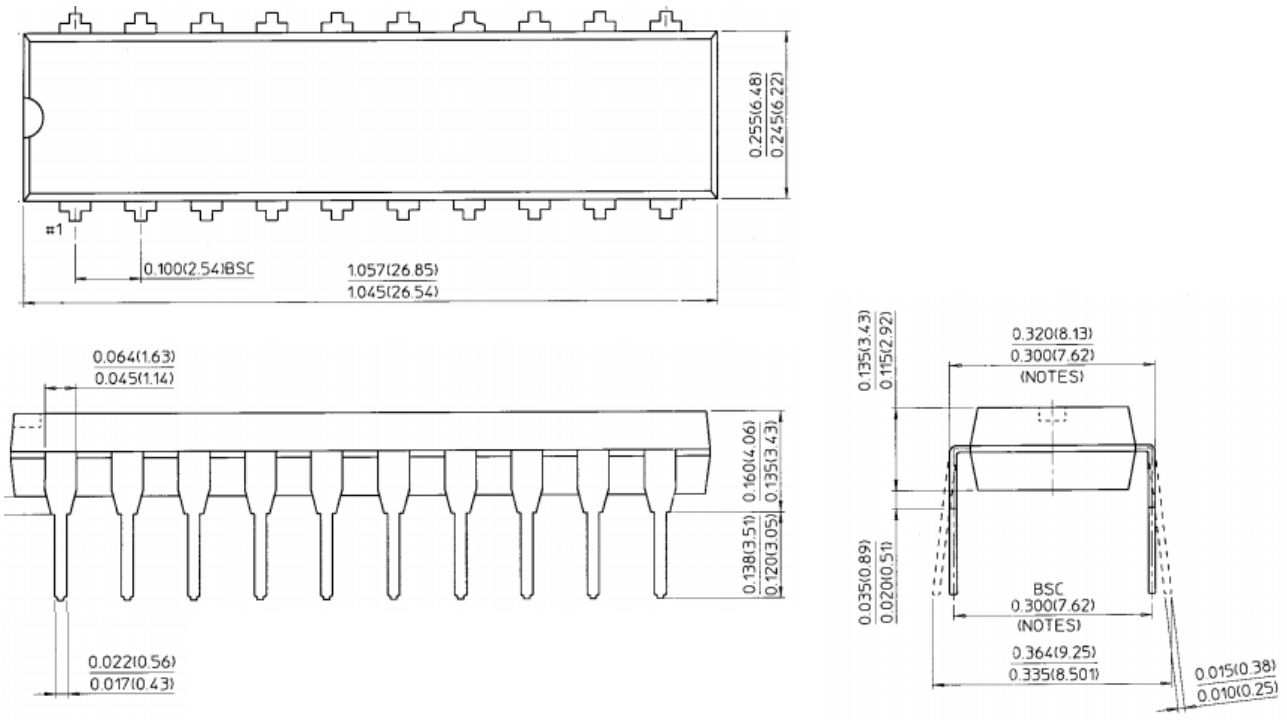
Package



Unit: inch (mm)

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