TH7301

Dual-Channel Programmable Low-Pass Filter

Description

The device incorporates two matching 4th-order Butterworth filters with voltage gain control to perform low-pass filtering on quadrature demodulated signals. The cutoff frequency and inband gain are programmable via a standard 3-wire interface. The cutoff frequency can be set between 0.8 MHz and 22.4 MHz and the inband voltage gain can be set between -3 dB and 20 dB. The cutoff frequency value is determined via a 10-bit control word, with smaller step sizes in the lower portion of the cutoff frequency range. The device contains an on-chip oscillator to adjust the cutoff frequency. Maintaining amplifiers configure the Butterworth filter as the phase shift component of the oscillator. The frequency of oscillation tracks the filter cutoff frequency. The cutoff frequency of the filter can be accurately set according to the resolution of the IC by measuring the frequency of oscillation.

Features

- ❑ Wide cutoff frequency range (0.8 MHz to 22.4 MHz)
- ❑ Dual-channel architecture produces superior matching and ease of use for quadrature signals
- ❑ Companding design provides higher resolution at lower cutoff frequencies
- ❑ Low power consumption (<105 mA, typical 55 mA from -5 V supply; Fc = 1 MHz @ 25°C)
- ❑ Single ended or differential input operation possible (AC coupled)
- ❑ No external components for trimming necessary
- ❑ Small package (16-pin SOP)

Applications

- ❑ Digital Broadcasting Systems (DBS) and Digital Video Broadcasting (DVB)
- ❑ Satellite and cable TV decoders
- ❑ Microwave point to point links

Block Diagram

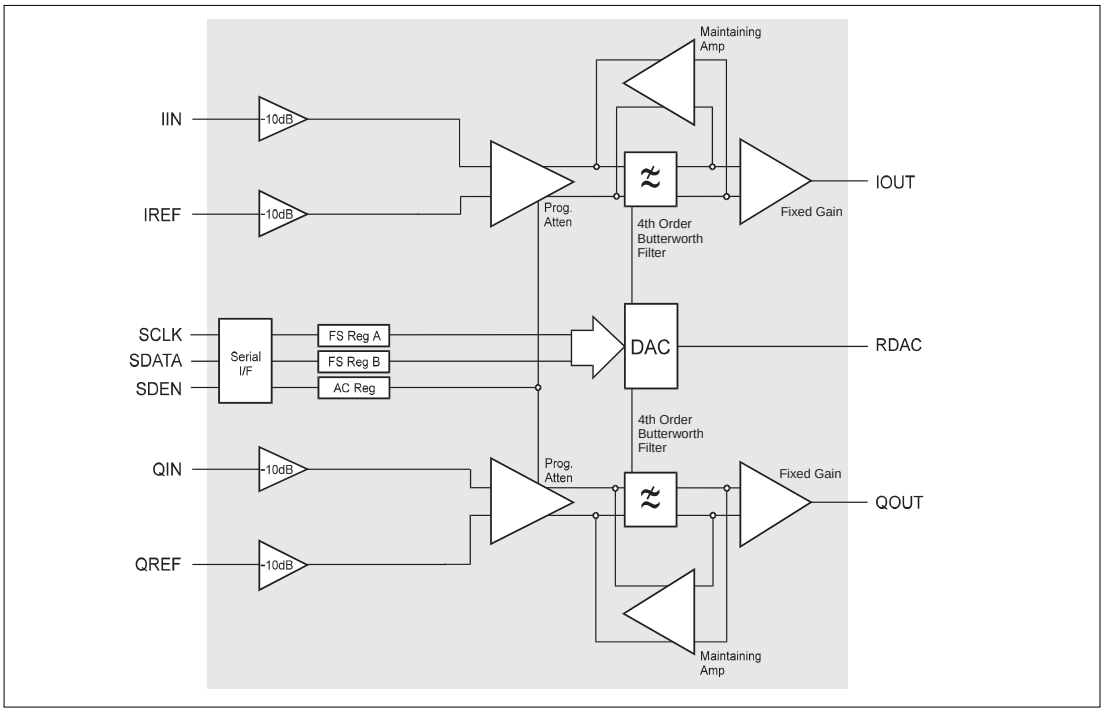


Figure 1: Block Diagram

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Theory of Operation

The IC is divided into I and Q channel signal paths each consisting of an input stage, gyrator 4th order Butterworth low-pass filter, output stage and feedback amplifier for an oscillator. A serial interface is provided to allow the gain and cutoff frequency to be programmed via a standard 3 wire interface. The digital cutoff frequency setting is converted to a current by a digital-to-analog converter. Internal bandgap references and biasing blocks provide top level biasing on voltage and current references for the complete device.

Input stage

The device incorporates programmable attenuation in the input stages to maintain filter linearity and to provide overall gain control for the IC. The attenuation can be programmed in coarse steps of 3 dB with fine control of 0.5 dB in the input transconductor of the gyrator filters. Internal multiplexers and back to back followers allow single-ended or differential input operation on both I and Q signal paths.

4th order Butterworth filter

The filter architecture is based on a fully balanced continuous time gyrator technique with 4th order Butterworth response. Linear current programmable transconductance elements are used to synthesise the two inductors and source and termination impedance of the filter. A termination to source impedance ratio of 2:1 is selected to minimise output noise while maintaining a realisable range of capacitor values.

The use of a differential architecture has three distinct advantages. Firstly the ultimate noise rejection is substantially better than that of the unbalanced LC filter. Secondly differential drive allows the use of a current programmable Gm stage with very much greater signal handling. And finally DC loading of the output is common mode and does not lead to differential DC offsets. This last point is especially important as the bias current within the filter can become very low at low cutoff frequencies.

Output stage

The output stage is designed to carry out differential to single ended conversion and provides the capability of driving up to 15 pF of capacitive load.

Oscillator

The maintaining and limiting amplifier is used as part of a phase shift oscillator circuit with the gyrator Butterworth filter as the phase shift element. The frequency of oscillation occurs at the -3 dB frequency of the filter as the phase shift through a 4th order Butterworth filter is 180 degrees at the -3 dB point. Voltage limiters are integrated into the gyrator filters and limit the differential voltage to 50 mVpp in order to ensure that the transconductance elements remain in their linear region of operation and hence the expected inductance values are synthesised.

Serial interface

The filter cutoff frequency and gain are programmed via a 3 wire serial interface bus. The interface consists of the serial data clock (SCLK), serial data input (SDATA) and a serial enable (SDEN). The filter is programmed by asserting SDEN and clocking the 8 bit serial data, MSB first, into the shift register. The two most significant bits represent the register address bits. The 6 LSB of data are loaded into the relevant register on the falling edge of SDEN.

The serial interface consists of: an 8 bit serial input to parallel output (SIPO) register, three 6-bit parallel load registers and register address decode logic.

Once SDEN is asserted, data is clocked into the SIPO on the positive edge of SCLK. When the data is loaded, the two address bits are decoded to determine which register should be updated. The data is transfered to the register on the falling edge of SDEN.

The serial interface does not contain a power on reset, thus all three registers must be programmed before reliable filter operation can be achieved.

DAC

The digital-to-analog converter is used to select the filter cutoff frequency via a programmable reference current. The fully companding DAC divides the frequency range into 5 chords, each with 128 equal frequency steps. The reference current is programmed by an external resistor placed between RDAC and Vee. The final output is mirrored for the I and Q channels to provide isolation.

The chords are selected by a 3 bit word and the frequency step by a 7 bit word. The companding law is generated by adding the chord currents and dividing the required chord into 128 step currents.

Pinout Information

The TH7301 is contained in a plastic 16 pin SOP package.

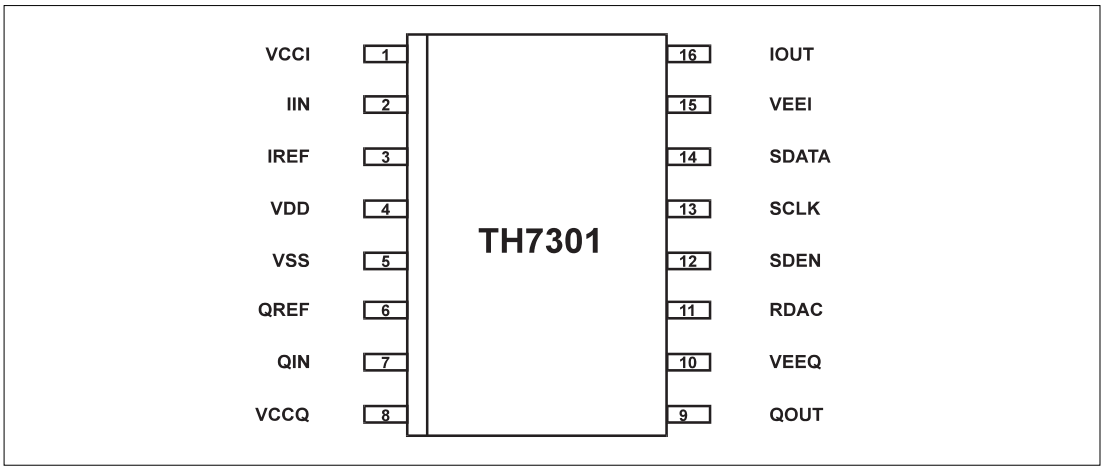


Figure 2: Pinout Schematic

Pin Definition List

Pin No.	Symbol	Function
1	VCCI	I channel positive supply
2	IIN	I channel signal input
3	IREF	I channel signal reference
4	VDD	Digital positive supply
5	VSS	Digital negative supply
6	QREF	Q channel signal reference
7	QIN	Q channel signal input
8	VCCQ	Q channel positive supply
9	QOUT	Q channel output
10	VEEQ	Q channel negative supply
11	RDAC	DAC reference current setting resistor connects between this pin and negative rail
12	SDEN	Serial data enable
13	SCLK	Serial data clock
14	SDATA	Serial data input
15	VEEI	I channel negative supply
16	IOUT	I channel output

Serial Interface Programming

The serial interface is a 3-wire bus used to program the filter cutoff frequency and voltage gain. Pin SDATA is the serial data input for an 8-bit shift register, SCLK is the shift register clock (active positive edge), SDEN (active high) is the serial interface enable. Note that logic levels are referenced to a - 5 V supply and that there is no global reset for the logic devices, so a reset word should be input after power up.

The timing diagram for the interface is shown below.

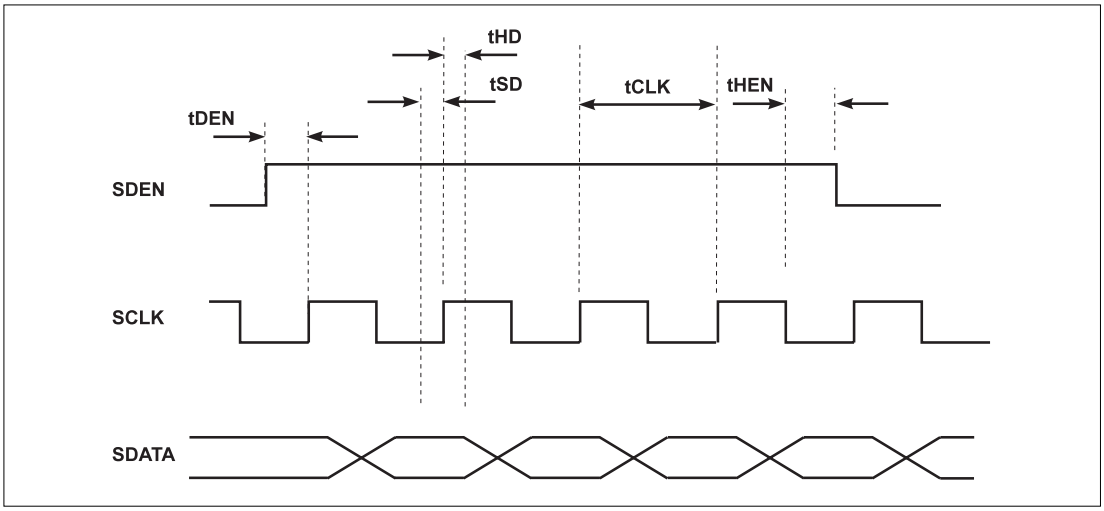


Figure 3: Serial Interface Timing Diagram

Operating conditions for the 3 wire interface

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Power supply voltage	VSS	-5.25	-5.0	-4.75	V	relative to VDD
High level input voltage	VIH	0.3 * VSS		VDD + 0.1V		note
Low level input voltage	VIL	VSS - 0.1V		0.7 * VSS		note
Serial data clock period	tCLK	50			ns	
Serial data setup time	tSD	10			ns	
Serial data hold time	tHD	10			ns	
Serial data enable delay time	tDEN	20			ns	
Serial data enable hold time	tHEN	20			ns	
Notes: Logic threshold levels for inputs SCLK, SDATA and SDEN. Note that this is a negative supply IC.						

The serial data is stored in one of 3 internal registers - gain control, frequency select A and frequency select B.

The first two bits of the serial data form an address code for the registers. The gain control bits AC(5...0) are decoded to select a voltage gain between 0 dB and 20.5 dB in 0.5 dB steps. The frequency select bits FC(2...0) select one of the octave chords while FS(6...0) select the step within each chord.

Additional bit OS0 (active high) controls the oscillator (for test issues only). The table below shows the address and data decoding of the serial data input.

The serial interface does not contain a power on reset, thus all three registers must be programmed after power on to prevent undefined logical states and to achieve reliable filter operation. I. e. a first reset word may reset all registers to 0.

Usage	Address Bits		Data Bits					
	D7	D6	D5	D4	D3	D2	D1	D0
Frequency Select A	0	0	FS2	FS1	FS0	FC2	FC1	FC0
Frequency Select B	0	1	OS0	0	FS6	FS5	FS4	FS3
Gain Control	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Definition of Terms

f_{cset} - cutoff frequency setting
f_c - cutoff frequency (-3dB bandwidth)
f_{step} - step size
A_v - voltage gain

Frequency Setting

To maintain frequency resolution at low frequencies a companding law is applied to the frequency code. The frequency range is selected as one of the five octaves in the total filter range controlled by bits FC(2...0). Each octave is divided linearly into 128 equally sized steps decoded by bits FS(6...0). This frequency range is for an external resistor value of 4.5 kΩ between pin RDAC and VEE. The range is designed to guarantee 0.8 MHz to 22.4 MHz cutoff range, taking process variations in top account without the need to change this external resistor. If there is a need to fine tune this frequency range for any reason, it may be re-centered by selecting a suitably valued external resistor.

The 128 steps within each octave are decoded by FS(6...0). The according control mechanism applies identically to all octaves refering to the appropriate step sizes of each octave, as shown in the tables and the example below.

Example:

FC(2...0) = 000
(frequency range 0.8 ... 1.5937 MHz,
Step size = 6.25 kHz)
FS(6...0) = 0000011
f_{cset} = 0.81875 MHz

The tables below show the selectable frequency settings.

FC (2..0)	Frequency range fmin ... fmax (MHz)	Step size fstep (kHz)
000	0.8 ... 1.5937	6.25
001	1.6 ... 3.1875	12.5
010	3.2 ... 6.375	25
011	6.4 ... 12.75	50
1xx	12.8 ... 25.5	100

FS (6...0)	Step N	Cutoff Frequency fcset = fmin + N*fstep (MHz)
0000000	0	fcset = fmin
0000001	1	fcset = fmin + fstep
0000010	2	fcset = fmin + 2*fstep
0000011	3	fcset = fmin + 3*fstep
. . .	. . .	. . .
1111111	127	fcset = fmin + 127*fstep

Gain Setting

The gain control bits AC(5...0) are decoded to select a voltage gain between -3 dB and 20.5 dB in 0.5 dB steps. The gain control is divided into 8 steps controlled by AC(2...0) with additive step sizes of 0.5 dB decoded by AC(5...3).

For example, to set the gain to 16 dB
AC(5...0) = 011001.

The table below shows the gain setting.

AC(2...0)	Gain (dB)
000	18
001	15
010	12
011	9
100	6
101	3
110	0
111	-3

AC(5...3)	Gain (dB)
000	2.5
001	2.0
010	1.5
011	1.0
100	0.5
101	0.0
110	0.0
111	0.0

Operating Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power supply voltage	VEE, VSS	-7		0.3	V	
Input voltage - logic inputs	Vi	VSS - 0.3V		0.3V		
Junction temperature	Tj	-40		+150	°C	
Storage temperature	Tstg	-40		+125	°C	
Notes: All voltages relative to VCC, VDD						

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power supply voltage	VEE, VSS	-5.25	-5.0	-4.75	V	relative to VCC, VDD
Operating temperature range	Top	0		70	°C	
Notes: The device has been designed for a negative supply system. It can be also used for positive supply systems if the input signals are referred to VCC, VDD.						

DC Characteristics

These characteristics are guaranteed for all settings of cutoff frequency and gain(unless otherwise stated). The value of the external DAC resistor is R_{DAC} = 4.5 kΩ.

Parameter	Symbol	Test level	Min.value	Typ.value	Max.value	Unit	Conditions
Digital Supply Current	I_{ss}	1			-5	mA	
Analog Supply Current (I + Q Channel)	I_{ee}	1			-60	mA	f_{cset}= 0.8 MHz; 25 °C
Analog Supply Current (I + Q Channel) at High Temperature	I_{ee}	3			-92	mA	f_{cset}= 22.4 MHz; 70 °C
DC Input Voltage	$V_{i,DC}$	1		-0.8		V	internal bias voltage
DC Output Voltage	$V_{o,DC}$	2	-3.2V	-2.5	-1.9	V	A_V = 20.5 dB gain setting
High Level Input Voltage	V_{IH}	1	0.3*VSS		VDD +0.1V		see note 1
Low Level Input Voltage	V_{IL}	1	VSS - 0.1V		0.7*VSS		see note 1

AC Characteristics

These characteristics are guaranteed for cutoff frequency settings f_{cset} = 0.8 ... 22.4 MHz (unless otherwise stated). The value of the external DAC resistor is R_{DAC} = 4.5 kΩ.

Parameter	Symbol	Testlevel	Min.	Typ.	Max.	Unit	Conditions
Initial Cutoff Frequency Accuracy	f_{cacc}	2	-15 -25		+25 +10	% %	$f_{cset} \le$ 6.375 MHz $f_{cset} \ge$ 6.4 MHz
Frequency Cutoff Resolution Accuracy	f_{cmon}	3	-3.0		3.0	%	referenced to f_c monotonicity guaranteed
Passband Amplitude Peaking	A_{pass}	3	-0.5		0.5	dB	10 Hz $\le f \le 0.5f_c$ see figure 7
Stopband Attenuation 1	A_{attn1}	3	12		14	dB	@ $f = 1.5f_c$
Stopband Attenuation 2	A_{attn2}	3	50		65	dB	$5f_c < f <$ 200 MHz

Operating Characteristics (continued)

Parameter	Symbol	Test level	Min.	Typ.	Max.	Unit	Conditions
Passband Group Delay Ripple	t_{pass}	3	6		12	ns	10 Hz ≤ f ≤ 0.5f_c see note 2, 3 and figure 8
Initial Gain Accuracy	A_{vacc}	2	-2.5		3.0	dB	see note 4 and figures 9 and 10
Gain Step Accuracy (monotonicity guaranteed)	A_{vmon}	3	- 1.0		1.0	dB	
Output Signal-to-Noise Ratio	SNR	3	37	38		dB	see note 5
Crosstalk between Channels	Xtalk	3	40	50		dB	see note 6, 7
Gain Match between Channels	A_{vmatch}	2	- 0.8		0.8	dB	
Bandwidth Match between Channels	f_{cmatch}	2	-10 -5		10 5	% %	f_{cset} ≤ 6.375 MHz f_{cset} ≥ 6.4 MHz
Passband Group Delay Match between Channels	t_{passm}	3	-3		+3	ns	10 Hz ≤ f ≤ 0.5f_c
Total Harmonic Distortion	THD	5		1.0	2.5	%	see note 8
Power Supply Rejection	PSR	4		40		dB	see note 9
Intermodulation Distortion	IMD	3		- 48	- 37	dBc	see note 10
Output Voltage	V_o	3			1.0	VPP	see note 11
Input Resistance	R_{in}	4		3.0		kΩ	
Input Capacitance	C_{in}	4		12		pF	
Load Resistance	R_{ld}	4	1			kΩ	see note 12
Load Capacitance	C_{ld}	4			15	pF	

Notes

1. Logic threshold levels for inputs SCLK, SDATA and SDEN. Note that this is a negative-supply device (VEE,VSS = -5 V, VCC, VDD = 0 V). It can be also used for positive-supply systems if the input signals are referred to VCC, VDD = +5 V and VEE,VSS = 0 V.
2. f_{cset} = 10 MHz, A_v = 10 dB
3. passband group delay ripple for an ideal 4 pole Butterworth under the same conditions is 6ns
4. measured at 0.25fc
5. V_o = 1 VPP, measured within the filter's noise bandwidth, f_{cset} = 10 MHz, A_v = 10 dB, $f_{in} < f_c$
6. V_o = 1 VPP, for $Xtalk_{IQ}$ I driven Q measured, $Xtalk_{QI}$ Q driven I measured, f_{cset} = 22.4 MHz, A_v = 20.5 dB,
7. f_{in} = 5 MHz
8. $f_{in} = 0.25f_c$; V_o = 1 VPP; C_{ld} = 15 pF, A_v = 10 dB
9. 100mVPP from 10 Hz to 1 MHz on VEE,VSS referred to the output.
10. f_{cset} = 10 MHz, A_v = 10 dB; tones at f_1= 15 MHz and f_2 = 25 MHz with 300 mVPP each
11. R_{ld} = 1 kΩ, for linear gain and not to exceed Xtalk, THD and IMD
12. AC coupled or DC coupled to VEE, VSS

Test levels (DC and AC Characteristics)

level 1: production tested at 25° C and over full power supply range
level 2: production tested at 25° C and VEE = -5.0 V
level 3: guaranteed by design and characterization test over full temperature and power supply range
level 4: typical value only, not confirmed by test
level 5: guaranteed by design and characterization at 25 °C and VEE = -5.0 V

Application Diagram

The application diagram below is an example diagram and provided to assist the customer in using the IC. The configuration can be changed for other applications.

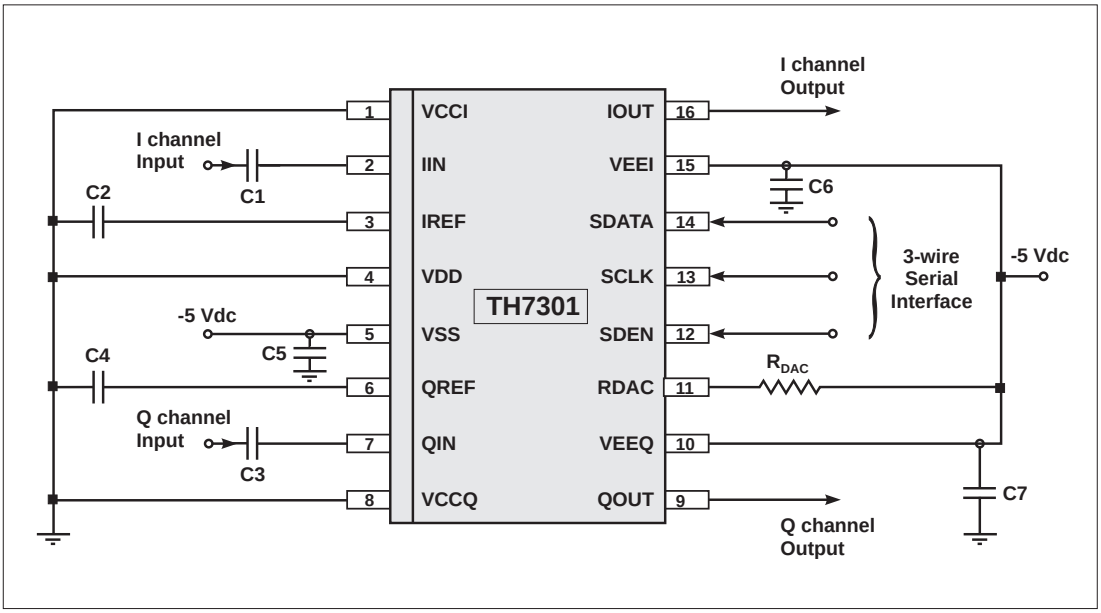


Figure 4: Application Diagram

Component List for Application Diagram

The AC coupling capacitors (C1-C4) will produce a high pass pole with the 3kΩ input resistance. Their value should be chosen such that this pole is below any frequencies of interest in the system.

The Rdac resistor is the current setting resistor for the DAC. The recommended values are listed below.

Component	Function	Value	Unit
C1, C2, C3, C4	AC coupling capacitors	100	nF
C5, C6, C7	AC coupling capacitors	22	nF
R_{DAC}	DAC current setting resistor	4.5	kΩ

Important notice

It is recommended to operate the device from a single power supply for both analog and digital sections of the device. Operation from separate power supplies on VEE and VSS and absence of the digital voltage may cause destruction of the device.

The serial interface does not contain a power on reset, thus all three registers must be programmed after power on to prevent undefined logical states and to achieve reliable filter operation. I. e. a first reset word may reset all registers to 0.

Filter Characteristics

The following diagrams illustrate some of the main functions and characteristics of the programmable low-pass filter. They represent evaluation results on the existing silicon.

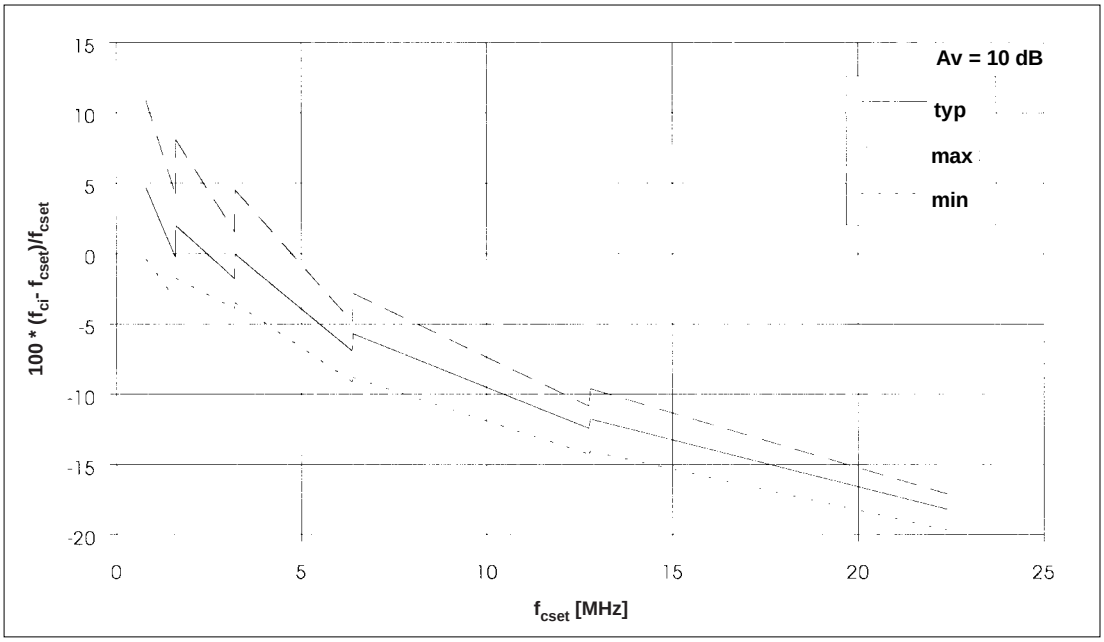


Figure 5: Measured cutoff frequency accuracy vs. settings (VEE = -5.00 V / T_a = 25°C)

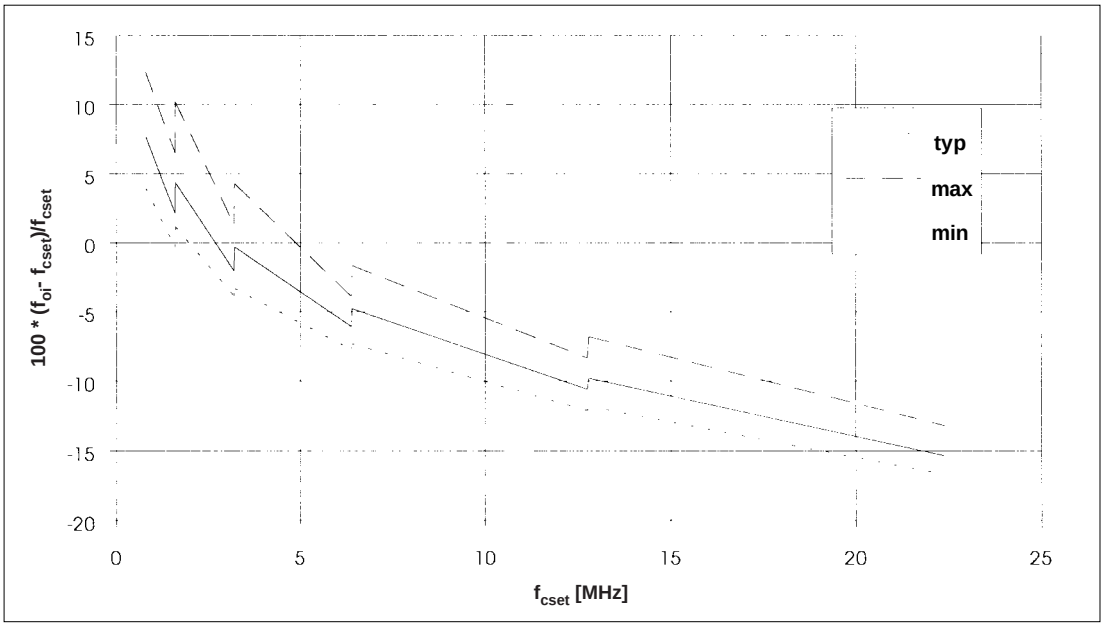


Figure 6: Measured oscillator frequency deviation vs. settings (VEE = -5.00 V / T_a = 25°C)

Filter Characteristics (continued)

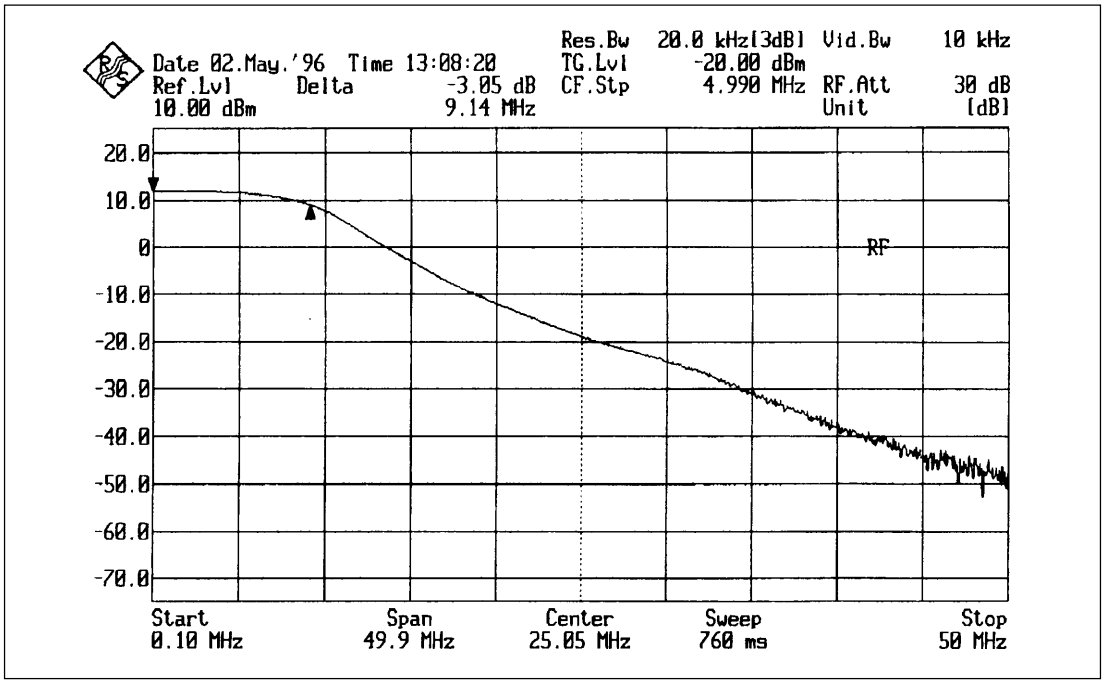


Figure 7: amplitude response (A_V = 10 dB, f_{cset} = 10 MHz, VEE= -5.0 V, T_a = 23° C)

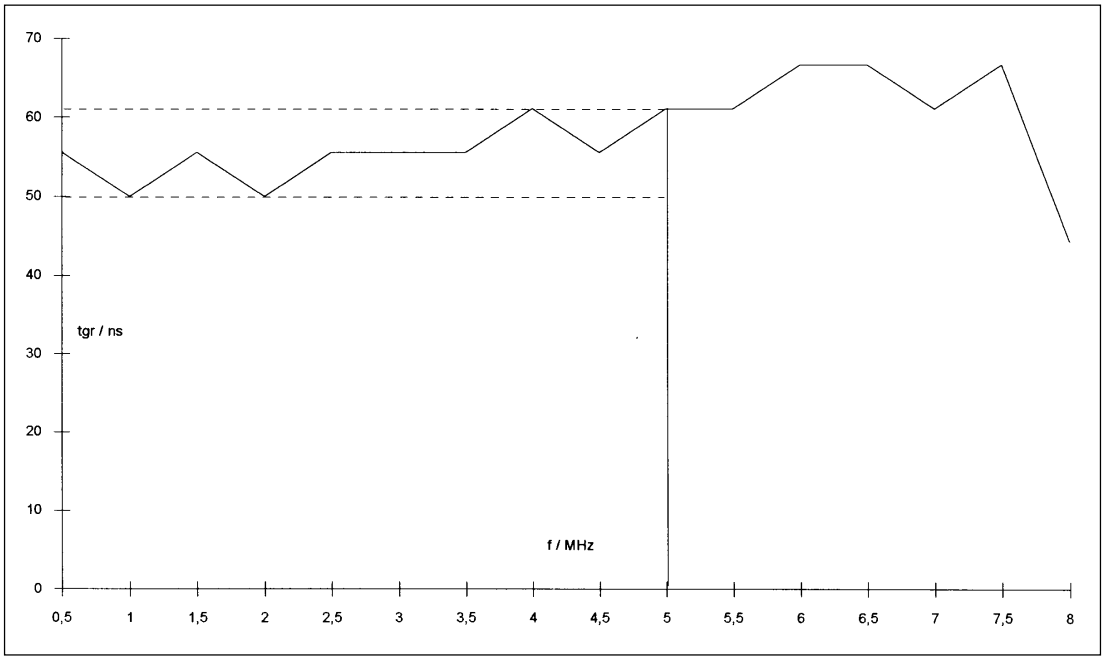


Figure 8: passband group delay ripple (A_V = 10 dB, f_{cset} = 10 MHz, VEE = -5.0 V, T_a = 23° C)

Filter Characteristics (continued)

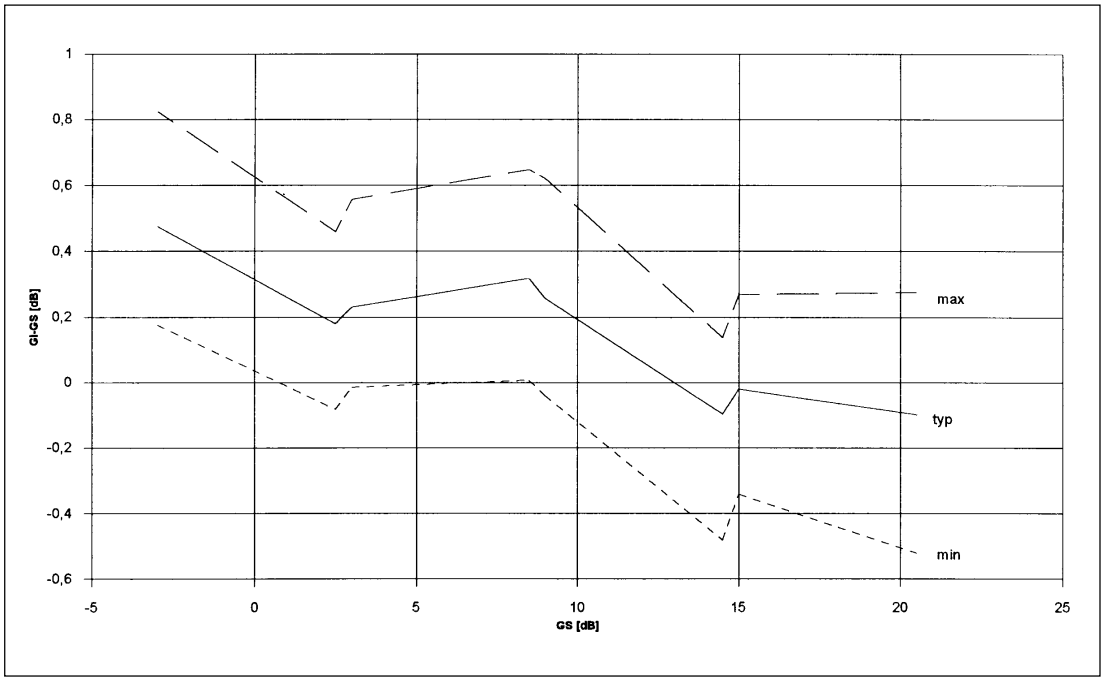


Figure 9: initial gain accuracy (f_{cset} = 0.8 MHz, f_{meas} = 0.2 MHz, VEE = -5.0 V, T_a = 23° C)

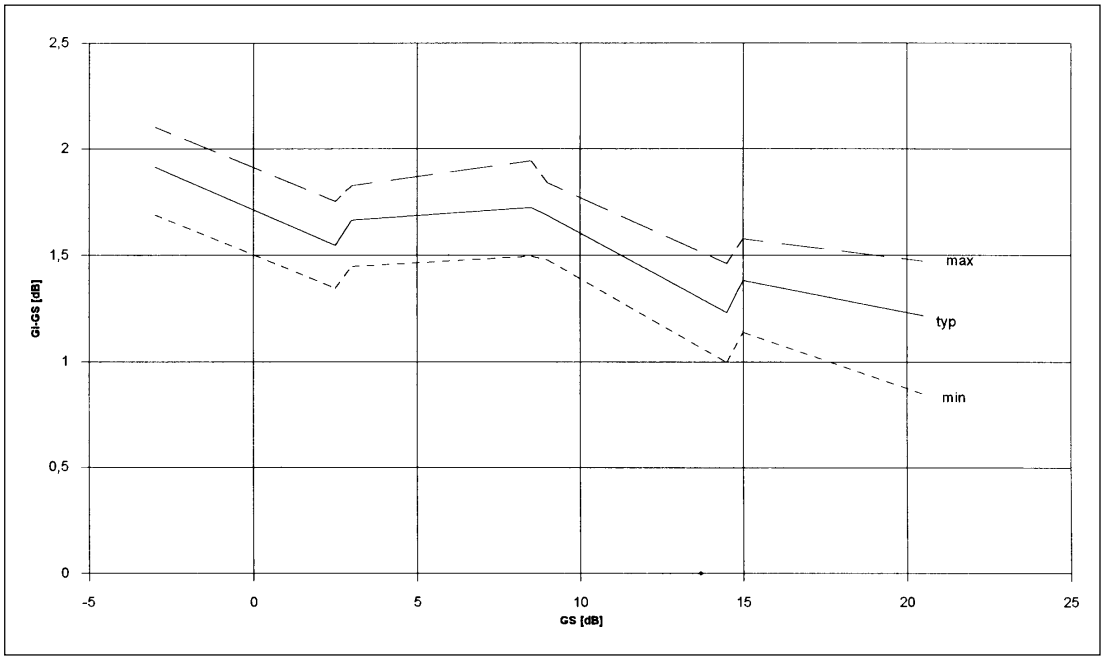
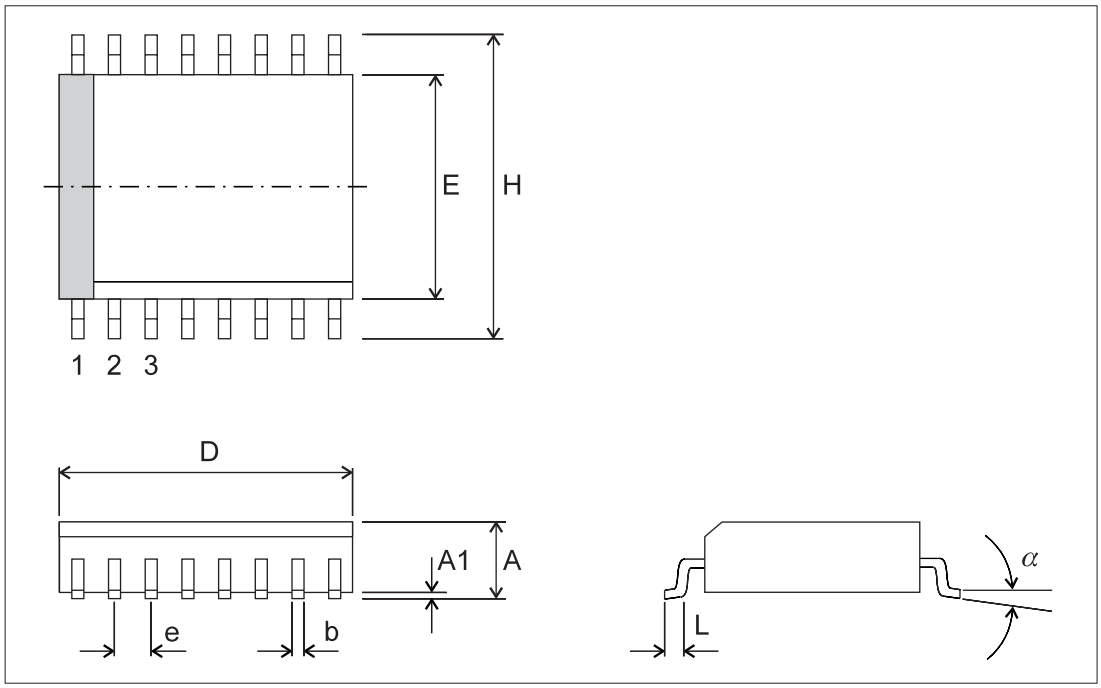


Figure 10: initial gain accuracy (f_{cset} = 22.4 MHz, f_{meas} = 5.0 MHz, VEE = -5.0 V, T_a = 23° C)

Package Information

The device is available in SOP WB 16 package.



Small Outline Package (SOP) SOP 16 Wide Body (WB)											
Package type		**D**	**E**	**H**	**A**	**A 1**	**e**	**b**	**L**	**α**	**Package code**
SOP WB 16	min max	0.398 0.413	0.283 0.300	0.393 0.419	0.091 0.111	0.002 0.014	0.05	0.013 0.020	0.012 0.050	10 °	DF16
Dimensions in inches, coplanarity < 0.004", original dimension: inch											

Small Outline Package (SOP) SOP 16 Wide Body (WB)											
Package type		**D**	**E**	**H**	**A**	**A 1**	**e**	**b**	**L**	**α**	**Package code**
SOP WB 16	min max	10.11 10.49	7.19 7.62	9.98 10.64	2.31 2.82	0.05 0.36	1.27	0.33 0.51	0.30 1.27	10 °	DF16
Dimensions in millimeters, coplanarity < 0.1 mm, original dimension: inch											

Ordering Information

The TH7301 Programmable Low-Pass Filter IC is available in a 16 pin SOP WB package and for the Operating Temperature range of 0 °C...+70 °C (Commercial).

The order number is **TH7301C** (C=Commercial).

Quality Data

Quality data is available on request. Contact:

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