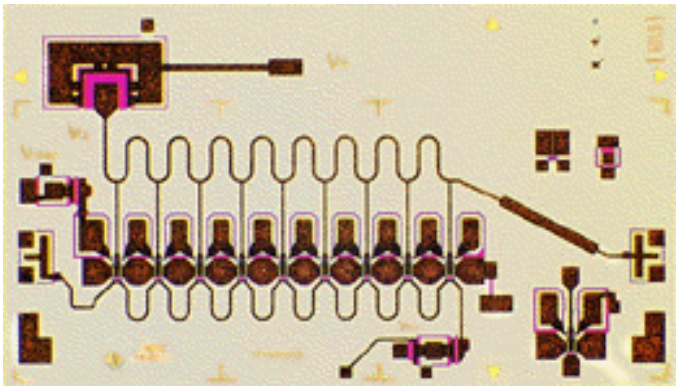
TriQuint SEMICONDUCTOR

Product Data Sheet
June 12, 2002

2 - 20 GHz Low Noise Amplifier TGA8310-SCC



Key Features and Performance

- 2 to 20- GHz Frequency Range
- 3.5 dB Noise Figure Midband
- 1.4:1 Typical Input/Output SWR
- 17.5 dBm Output Power at 1 dB Gain Compression
- 9 dB Typical Gain
- 4.1 x 2.4 x 0.1 mm (0.162 x 0.093 x 0.004 in.)

Description

The TriQuint TGA8310-SCC is a monolithic low noise distributed amplifier, which operates from 2 to 20 GHz. Typical noise figure is 4 dB. Nine 122 um gatewidth FETs typically provide 17.5 dBm of output power at 1 dB gain compression and 9 dB typical small signal gain. Typical input return loss is 17 dB from 2 to 20 GHz. Typical output return loss is 20 dB. Ground is provided to the circuitry through vias to the backside metallization

The TGA8310-SCC low noise distributed amplifier is suitable for a variety of wideband electronic warfare systems such as radar warning receivers, electronic counter measures, decoys, jammers and phased array systems.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic wire bonding processes. The TGA8310-SCC is supplied in chip form and is assembled using automated equipment.

TABLE I
MAXIMUM RATINGS 6/

SYMBOL	PARAMETER	VALUE	NOTES
V_D	POSITIVE DRAIN SUPPLY VOLTAGE	9 V	
V^+	POSITIVE SUPPLY VOLTAGE	12 V	1/, 5/
V_{G1}	NEGATIVE SUPPLY VOLTAGE RANGE	-5 V to 0 V	1/
V_{ctrl}	GAIN CONTROL VOLTAGE RANGE	-5 V to 4 V	2/
I_D	POSITIVE DRAIN CURRENT	I_{DSS}	5/, 7/
I^+	POSITIVE SUPPLY CURRENT	188 mA	5/, 7/
I^-	NEGATIVE GATE CURRENT	8.73 mA	7/
P_D	POWER DISSIPATION AT OR BELOW 25°C BASE PLATE TEMPERATURE	2.6 W	5/, 8/
P_{IN}	INPUT CONTINUOUS WAVE POWER	25.5 dBm	
T_{CH}	OPERATING CHANNEL TEMPERATURE	150 ^{0}C	3/ 4/, 8/
T_M	MOUNTING TEMPERATURE (30 SECONDS)	320 ^{0}C	
T_{STG}	STORAGE TEMPERATURE	-65 to 150 ^{0}C	

1/ $0V \le (V^+ - V_{G1}) \le 13V$

2/ $0V \le (V^+ - V_{G2}) \le 13V$

3/ These ratings apply to each individual FET

4/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

5/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

6/ These ratings represent the maximum operable values for this device.

7/ Total current for all stages

8/ For operation above 25°C base-plate temperature, derate linearly at the rate of 5.5 mW/°C

TABLE II
DC PROBE TESTS (100%)
(T_A = 25 °C ± 5 °C)

NOTES	SYMBOL	TEST CONDITIONS 3/	LIMITS		UNITS
			MIN	MAX	
4/	I_{DSS}	STD	97	292	mA
4/	G_M	STD	130	281	Ms
1/,2/,4/	$\|V_{P1}\|$	STD	0.5	2.1	V
1/,2/,4/	$\|V_{P2}\|$	STD	0.5	2.1	V
1/,4/	$\|V_{BVGD}\|$	STD	6	30	V
1/,4/	$\|V_{BVGS}\|$	STD	6	30	V
4/	RES	STD	42.7	79.3	Ω
4/	RES	STD	36.4	67.6	Ω
4/	RES	STD	173.0	321.0	Ω
4/	RES	STD	31.8	59.1	Ω

1/ V_P, V_{BVGD}, and V_{BVGS} are negative

2/ Subscripts are referred to Q1, Q2 accordingly.

3/ The measurement conditions are subject to change at the manufacture's discretion (with appropriate notification to the buyer).

4/ STD refers to Standard Test Conditions (see Table III for definitions)

TABLE III
AUTOPROBE FET PARAMETER MEASUREMENT CONDITIONS

FET Parameters	Test Conditions
I_{DSS} : Maximum drain current (I_{DS}) with gate voltage (V_{GS}) at zero volts.	V_{GS} = 0.0 V, drain voltage (V_{DS}) is swept from 0.5 V up to a maximum of 3.5 V in search of the maximum value of I_{DS}; voltage for I_{DSS} is recorded as VDSP.
G_m : Transconductance; $\frac{(I_{DSS} - IDS1)}{VG1}$	For all material types, V_{DS} is swept between 0.5 V and VDSP in search of the maximum value of I_{ds}. This maximum I_{DS} is recorded as IDS1. For Intermediate and Power material, IDS1 is measured at V_{GS} = VG1 = -0.5 V. For Low Noise, HFET and pHEMT material, V_{GS} = VG1 = -0.25 V. For LNBECOLC, use V_{GS} = VG1 = -0.10 V.
V_P : Pinch-Off Voltage; V_{GS} for I_{DS} = 0.5 mA/mm of gate width.	V_{DS} fixed at 2.0 V, V_{GS} is swept to bring I_{DS} to 0.5 mA/mm.
V_{BVGD} : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I_{BD}) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V_{GD}) measured is V_{BDGD} and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V_{BVGS} : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I_{BS}) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V_{GS}) measured is V_{BDGS} and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.

TABLE IV

RF WAFER SCREENING TESTS

(T_A = 25°C ± 5°C)

NOTES	PARAMETERS	PART DASH NO AFFECTED	MEASUREMENT CONDITIONS (V_D = 5V, V_{G2} = 1.5V, I^+ = 60mA, V_{G1} = ADJUST)	VALUE MIN	VALUE TYP	VALUE MAX	UNITS
1/	SMALL-SIGNAL GAIN MAGNITUDE	-2,-3	F = 2 – 20 GHz	8.0			dB
1/	NOISE FIGURE	-2,-3	F = 2 – 15 GHz			5.2	dB
			F = >15 – 18 GHz			6.2	
1/	OUTPUT POWER AT 1 dB GAIN COMPRESSION	-2,-3	F = 2 – 10 GHz	14			dBm
			F = 10 – 18 GHz	13			
1/	INPUT RETURN LOSS MAGNITUDE	-2,-3	F = 2.0 – 2.5 GHz	8			dB
			F = 2.5 – 20 GHz	9			
1/	OUTPUT RETURN LOSS MAGNITUDE	-2,-3	F = 2 - 18 GHz	9.5			dB
			F = 18 – 20 GHz	8.0			
	OUTPUT THIRD-ORDER INTERCEPT POINT		F = 2 GHz		29.5		dBm
			F = 6 GHz		27.0		
			F = 9 GHz		27.5		
			F = 12 GHz		26.5		
			F = 18 GHz		27.0		
	OUTPUT SECOND-ORDER INTERCEPT POINT		F_o = 2 GHz		32.5		dBm
			F_o = 4 GHz		29.5		
			F_o = 6 GHz		29.0		
			F_o = 9 GHz		28.0		
	OUTPUT THIRD HARMONIC AT 1-db GAIN COMPRESSION		F_o = 2 GHz		-29.0		dBc*
			F_o = 4 GHz		-24.5		
			F_o = 6 GHz		-19.5		
	OUTPUT SECOND HARMONIC AT 1-dB GAIN COMPRESSION		F_o = 2 GHz		-18.0		dBc*
			F_o = 4 GHz		-15.0		
			F_o = 6 GHz		-13.5		
			F_o = 9 GHz		-15.5		

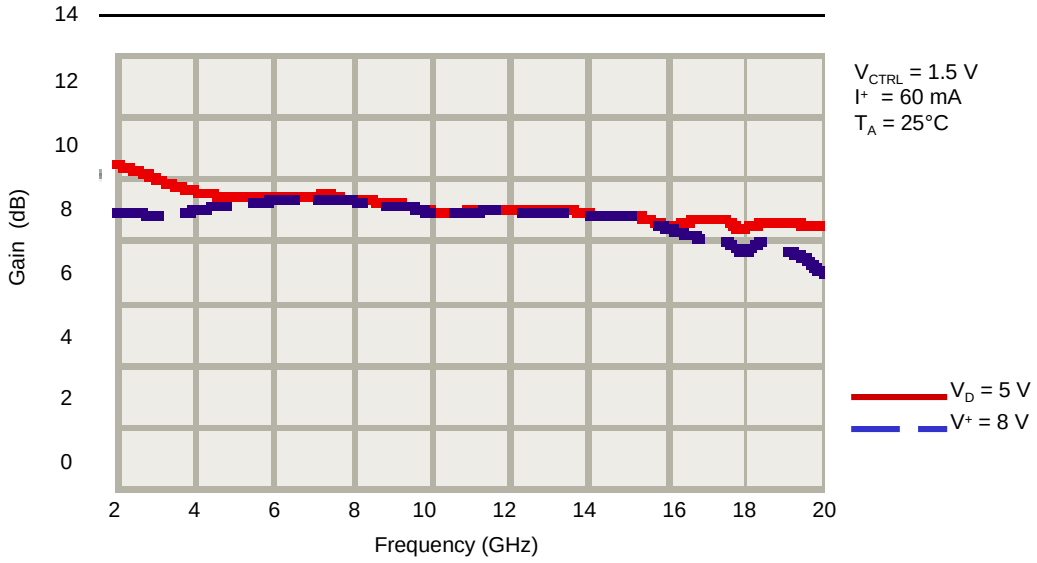
1/ These parameters are to be tested for wafer acceptance. Devices shall be selected from each wafer and supplied to the product/test engineer in accordance with 4.2. Wafer acceptance shall be based upon the results of this test.

* Unit dBc applies to decibels with respect to the carrier or fundamental frequency, F_o.

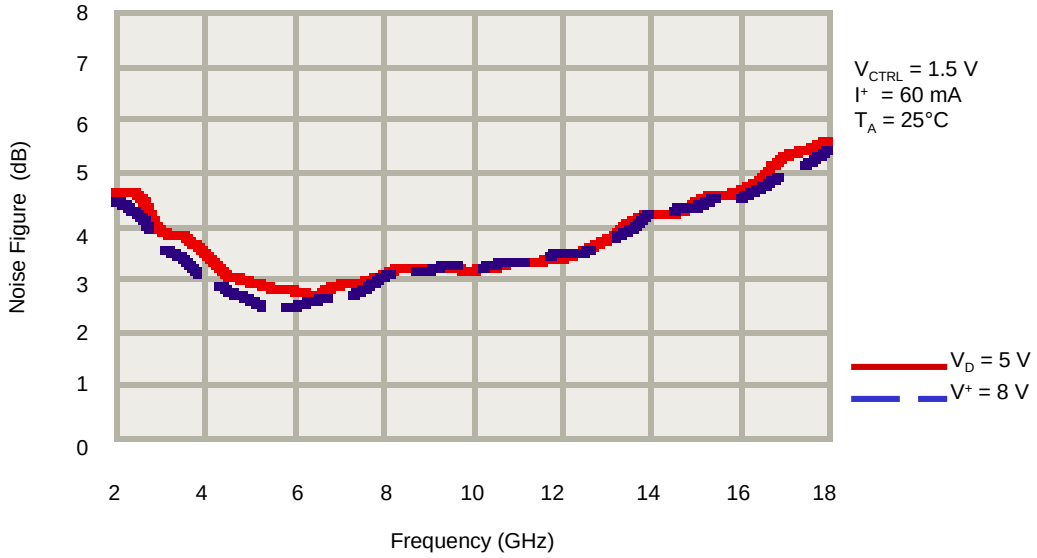
TABLE V
THERMAL INFORMATION

PARAMETER	TEST CONDITIONS		NOM	UNIT
R_{QJC} Thermal resistance (channel to backside)	V_{CTRL} = 1.5 V, I^+ = 60 mA	V^+ = 8 V	12	°C/W
		V_D = 5 V	20	

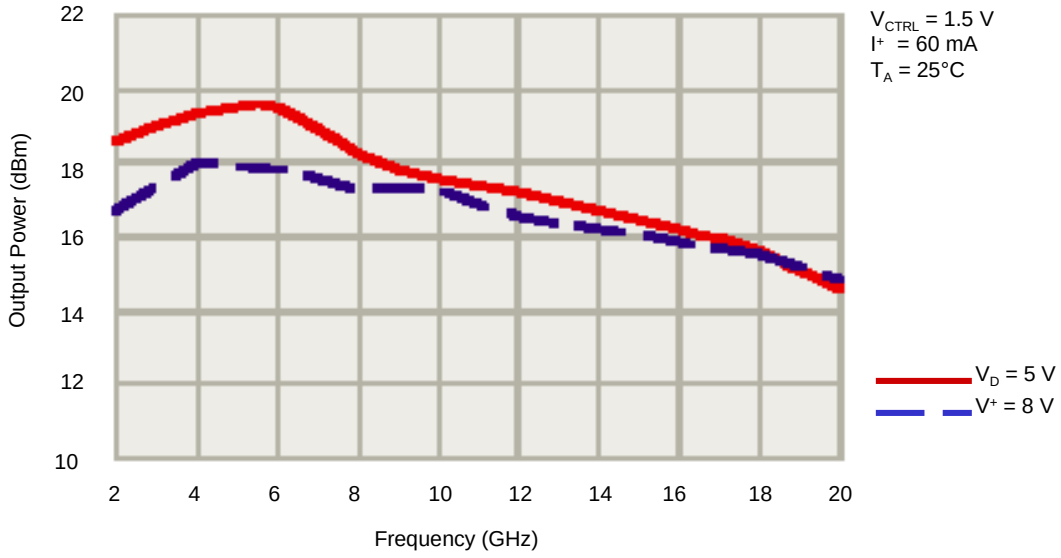
TYPICAL SMALL SIGNAL POWER GAIN



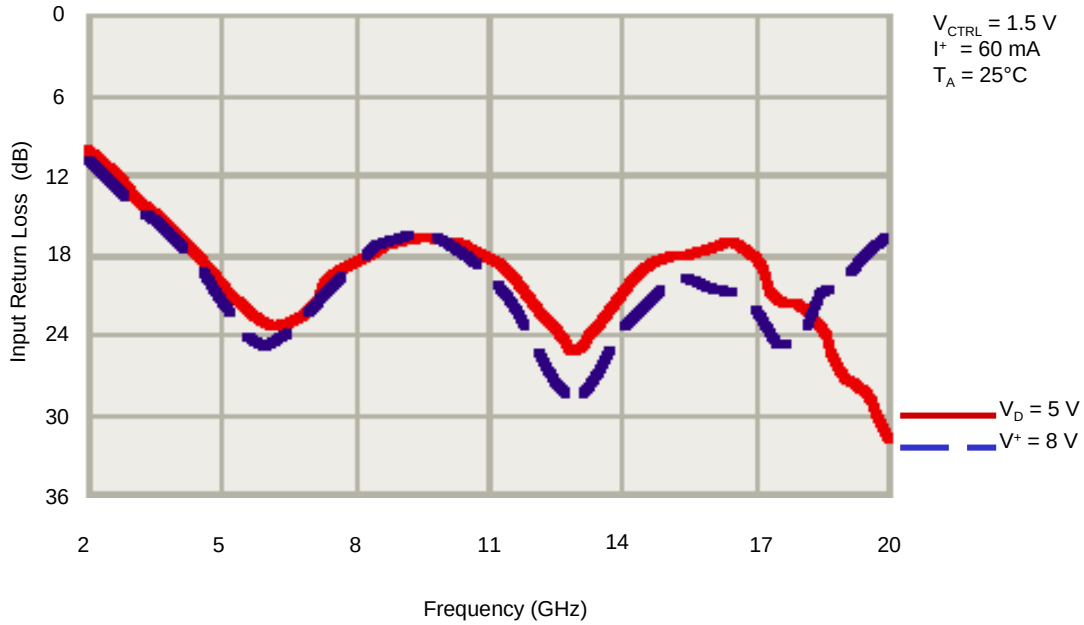
TYPICAL NOISE FIGURE



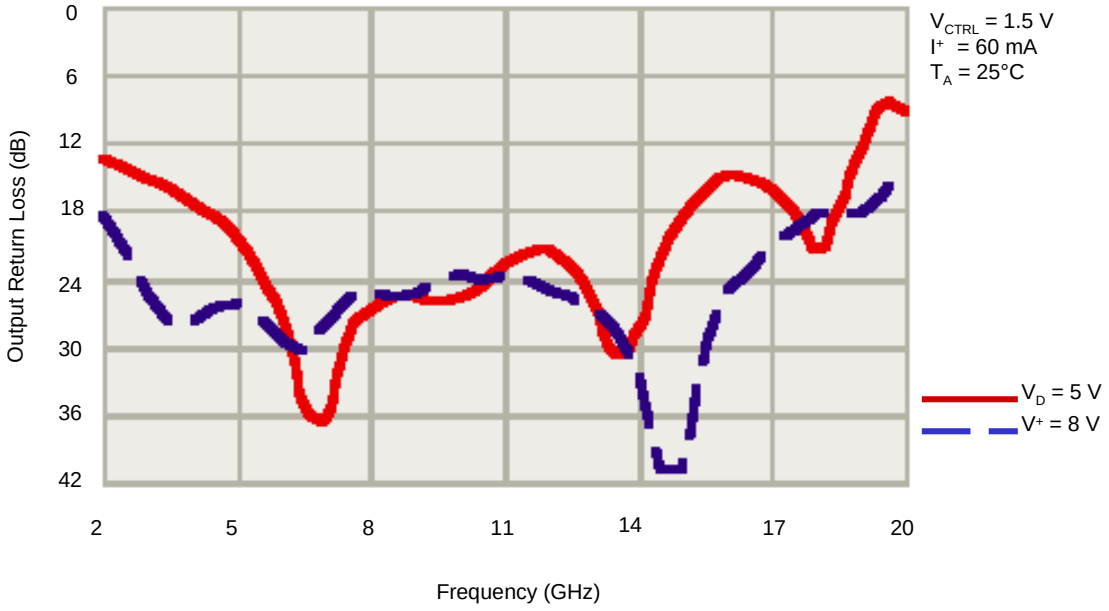
TYPICAL OUTPUT POWER P1dB



TYPICAL INPUT RETURN LOSS



TYPICAL OUTPUT RETURN LOSS



TYPICAL S-PARAMETERS

Frequenc	S_{11}		S_{21}		S_{12}		S_{22}		GAIN
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	(dB)
2.0	0.28	-155	2.76	108	0.007	37	0.12	-133	8.8
2.5	0.23	-178	2.75	90	0.008	19	0.08	-152	8.8
3.0	0.20	165	2.74	72	0.010	4	0.05	180	8.8
3.5	0.17	151	2.77	53	0.011	-12	0.04	134	8.8
4.0	0.14	140	2.79	35	0.012	-28	0.04	86	8.9
4.5	0.11	133	2.83	16	0.013	-45	0.05	55	9.0
5.0	0.08	132	2.84	-3	0.015	-63	0.05	32	9.1
5.5	0.06	138	2.87	-22	0.016	-80	0.04	8	9.2
6.0	0.06	154	2.88	-41	0.018	-99	0.03	-28	9.2
6.5	0.06	166	2.90	-60	0.019	-117	0.03	-82	9.2
7.0	0.08	165	2.88	-79	0.021	-136	0.04	-128	9.2
7.5	0.09	165	2.91	-98	0.022	-152	0.05	-157	9.3
8.0	0.12	160	2.88	-118	0.024	-171	0.06	173	9.2
8.5	0.13	154	2.87	-137	0.026	172	0.05	143	9.2
9.0	0.15	148	2.84	-157	0.027	156	0.05	111	9.1
9.5	0.15	141	2.81	-176	0.028	140	0.06	79	9.0
10.0	0.14	131	2.78	165	0.029	124	0.07	52	8.9
10.5	0.13	122	2.76	146	0.030	104	0.06	27	8.8
11.0	0.11	112	2.78	128	0.031	91	0.07	1	8.9
11.5	0.08	105	2.79	108	0.032	73	0.06	-29	8.9
12.0	0.06	105	2.76	88	0.032	55	0.06	-58	8.8
12.5	0.04	115	2.77	69	0.033	38	0.05	-85	8.9
13.0	0.03	147	2.76	49	0.034	20	0.05	-113	8.8
13.5	0.05	163	2.76	29	0.035	1	0.04	-147	8.8
14.0	0.06	161	2.75	8	0.037	-19	0.02	-173	8.8
14.5	0.08	150	2.74	-12	0.039	-39	0.01	163	8.7
15.0	0.10	133	2.72	-33	0.040	-59	0.01	-17	8.7
15.5	0.10	116	2.71	-54	0.042	-78	0.03	-37	8.7
16.0	0.09	103	2.60	-76	0.043	-96	0.06	-60	8.3
16.5	0.09	90	2.54	-96	0.046	-112	0.07	-76	8.1
17.0	0.08	65	2.52	-117	0.048	-131	0.09	-91	8.0
17.5	0.06	45	2.49	-139	0.050	-151	0.11	-112	7.9
18.0	0.06	81	2.39	-158	0.047	-170	0.13	-129	7.6
18.5	0.09	63	2.50	-179	0.051	177	0.12	-138	8.0
19.0	0.10	72	2.45	158	0.054	155	0.12	-135	7.8
19.5	0.13	85	2.34	133	0.053	132	0.15	-120	7.4
20.0	0.15	96	2.20	110	0.053	112	0.21	-118	6.8

T_A = 25°C, V_D = 8 V, V_{CTRL} = 1.5 V, I^+ = 60 mA

Reference planes for S-parameter data include bond wires as specified in the “Recommended Assembly Diagram”.

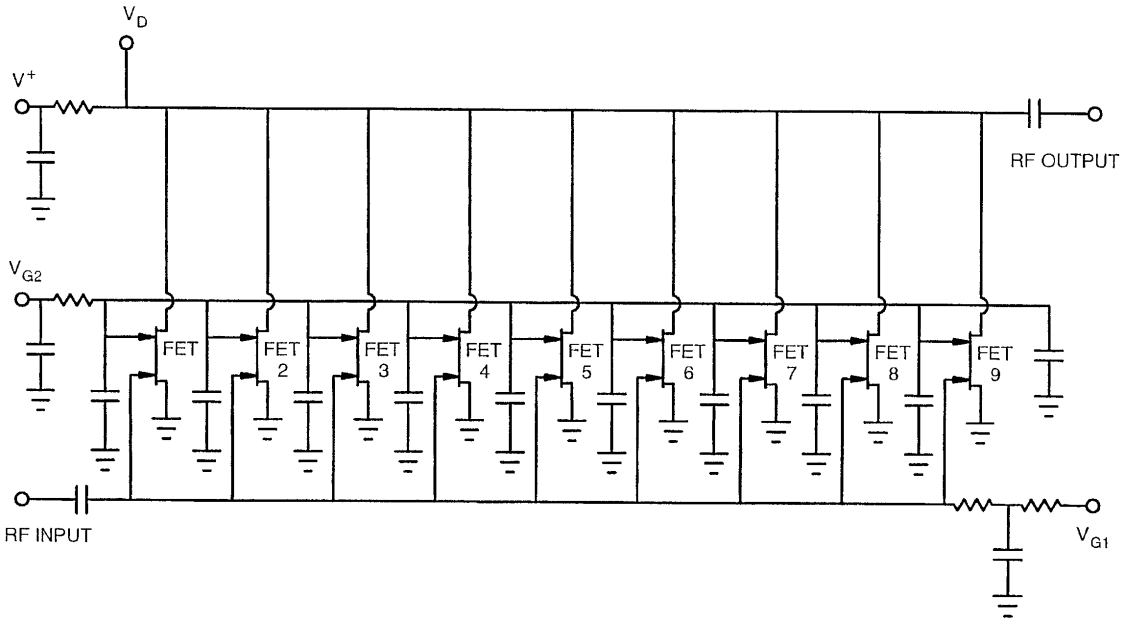
TYPICAL S-PARAMETERS

Frequenc	S_{11}		S_{21}		S_{12}		S_{22}		GAIN
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	(dB)
2.0	0.31	-154	3.32	119	0.009	61	0.22	-19	10.4
2.5	0.26	-175	3.23	96	0.010	32	0.19	-62	10.2
3.0	0.21	169	3.13	75	0.011	14	0.17	-98	9.9
3.5	0.18	155	3.06	54	0.012	-6	0.16	-132	9.7
4.0	0.15	145	3.00	35	0.013	-23	0.14	-162	9.6
4.5	0.12	137	2.97	16	0.014	-42	0.12	169	9.4
5.0	0.10	134	2.93	-3	0.014	-59	0.10	143	9.3
5.5	0.08	135	2.93	-22	0.016	-76	0.07	116	9.3
6.0	0.07	143	2.92	-41	0.018	-96	0.04	87	9.3
6.5	0.07	153	2.93	-60	0.019	-115	0.02	44	9.3
7.0	0.08	162	2.94	-79	0.021	-133	0.02	-92	9.4
7.5	0.10	162	2.95	-99	0.022	-153	0.04	-143	9.4
8.0	0.12	157	2.91	-118	0.024	-170	0.05	-170	9.3
8.5	0.13	152	2.90	-138	0.025	173	0.05	164	9.2
9.0	0.14	145	2.85	-157	0.027	156	0.05	133	9.1
9.5	0.14	137	2.83	-176	0.028	140	0.05	95	9.1
10.0	0.14	127	2.80	165	0.029	123	0.05	52	8.9
10.5	0.14	116	2.77	146	0.029	109	0.06	17	8.8
11.0	0.12	109	2.80	127	0.032	89	0.07	-25	8.9
11.5	0.11	100	2.80	107	0.032	73	0.08	-54	9.0
12.0	0.08	99	2.80	88	0.033	56	0.08	-82	8.9
12.5	0.07	107	2.80	68	0.035	37	0.07	-109	8.9
13.0	0.06	128	2.79	48	0.035	18	0.05	-141	8.9
13.5	0.07	147	2.79	28	0.037	0	0.03	153	8.9
14.0	0.09	150	2.77	8	0.038	-21	0.04	53	8.8
14.5	0.11	144	2.74	-13	0.039	-41	0.08	13	8.7
15.0	0.12	130	2.73	-33	0.041	-58	0.12	-14	8.7
15.5	0.12	121	2.70	-54	0.044	-76	0.16	-42	8.6
16.0	0.13	112	2.65	-74	0.046	-96	0.18	-70	8.5
16.5	0.14	99	2.66	-94	0.049	-115	0.18	-99	8.5
17.0	0.12	87	2.70	-115	0.052	-134	0.16	-131	8.6
17.5	0.09	81	2.71	-138	0.056	-155	0.13	-166	8.7
18.0	0.08	95	2.61	-159	0.053	-175	0.08	145	8.3
18.5	0.07	79	2.68	-180	0.056	168	0.13	57	8.6
19.0	0.04	88	2.67	156	0.058	142	0.24	-25	8.5
19.5	0.04	92	2.65	133	0.054	119	0.37	-87	8.5
20.0	0.03	86	2.64	110	0.051	102	0.34	-149	8.4

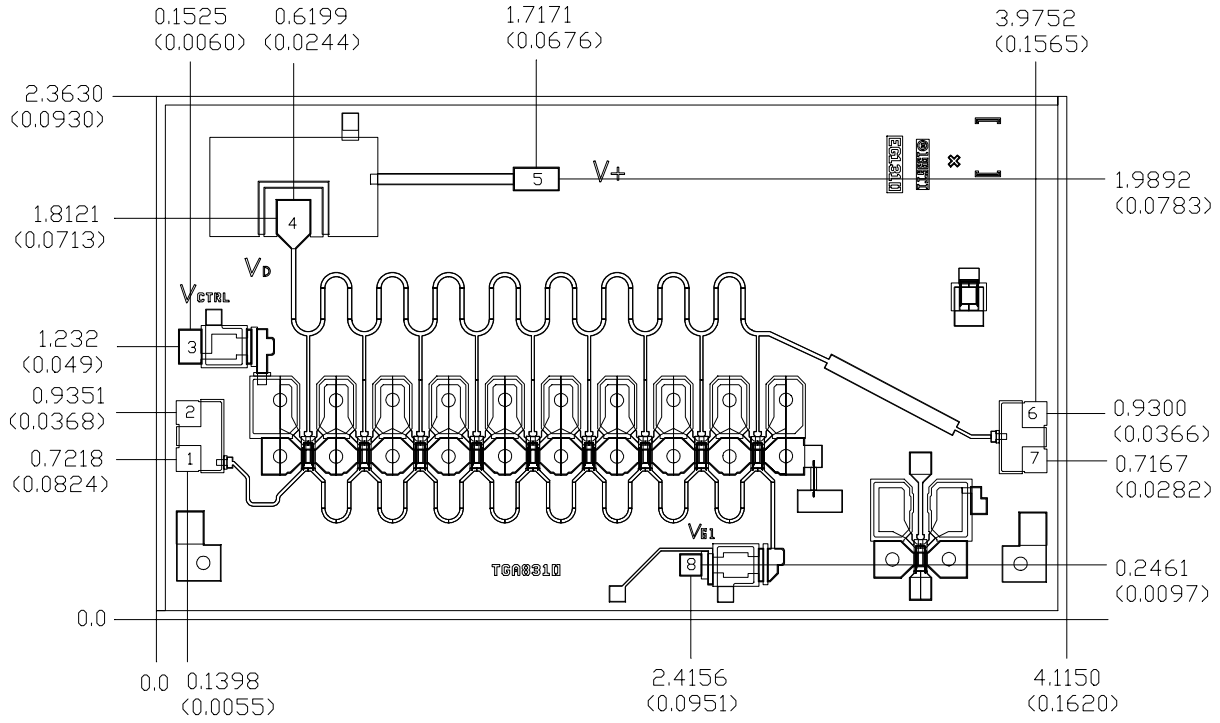
T_A = 25°C, V_D = 5 V, V_{CTRL} = 1.5 V, I^+ = 60 mA

Reference planes for S-parameter data include bond wires as specified in the “Recommended Assembly Diagram”.

EQUIVALENT SCHEMATIC



Mechanical Characteristics



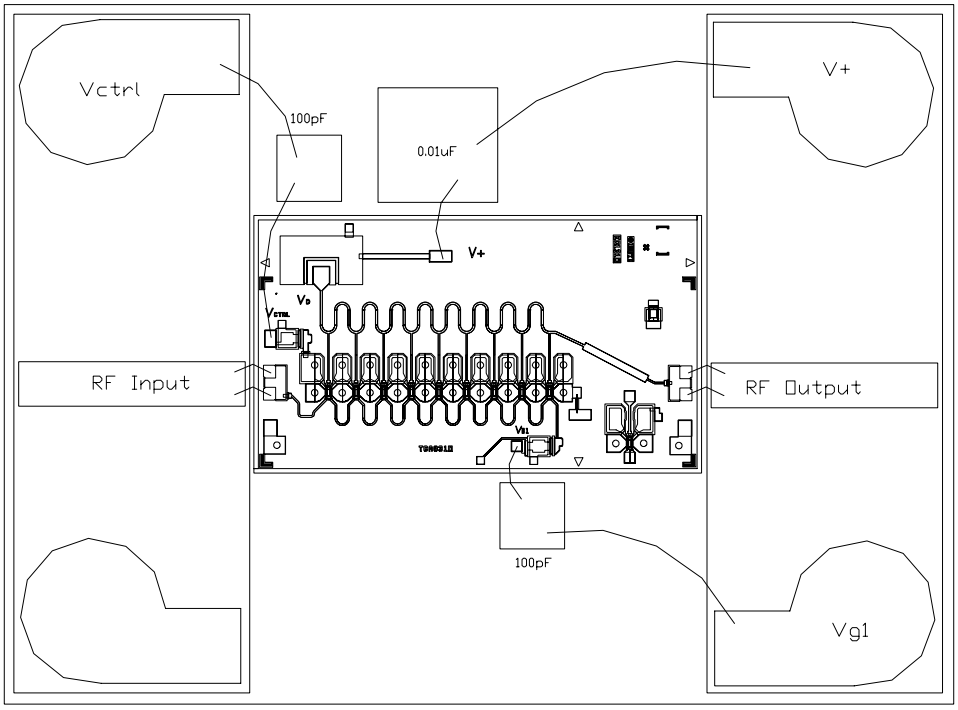
Units: millimeters (inches)
Thickness: 0.1016 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad.
Chip size: +/- 0.0508 (0.002)

Bond pad #1 (RF Input):	0.0940 x 0.0991 (0.0037 x 0.0039)
Bond pad #2 (RF Input):	0.0940 x 0.0991 (0.0037 x 0.0039)
Bond pad #3 (Vctrl):	0.1016 x 0.1524 (0.0040 x 0.0060)
Bond pad #4 (Vd):	0.1321 x 0.2108 (0.0052 x 0.0083)
Bond pad #5 (V+):	0.2032 x 0.1016 (0.0080 x 0.0040)
Bond pad #6 (RF Output):	0.0940 x 0.0991 (0.0037 x 0.0039)
Bond pad #7 (RF Output):	0.0940 x 0.0991 (0.0037 x 0.0039)
Bond pad #8 (Vg1):	0.0965 x 0.0965 (0.0038 x 0.0038)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Chip Assembly and Bonding Diagrams

RECOMMENDED ASSEMBLY DIAGRAM, 8 Volt Bias



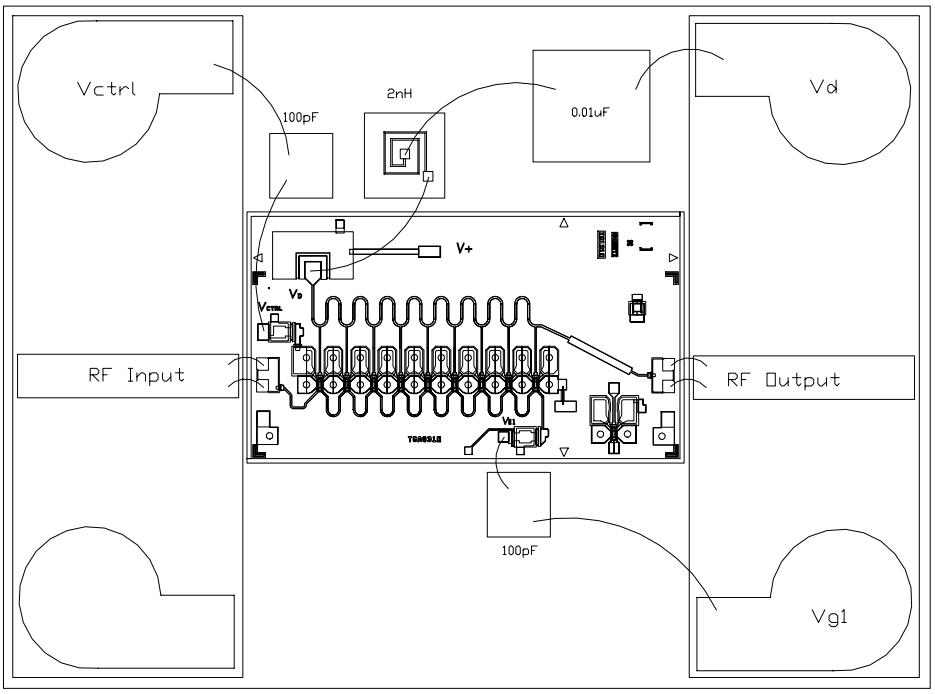
RF connections: bond using two 1-mil diameter, 20 to 25-mil-length gold bond wires at both RF Input and RF Output for optimum RF performance.

Close placement of external components is essential to stability

Refer to TriQuint Semiconductor Gallium Arsenide Products Designers' Information on TriQuint's website or order literature number GMNA002.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

RECOMMENDED ASSEMBLY DIAGRAM, 5 Volt Bias



RF connections: bond using two 1-mil diameter, 20 to 25-mil-length gold bond wires at both RF Input and RF Output for optimum RF performance.

Close placement of external components is essential to stability

Chip Assembly and Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.