DATA SHEET

TDA9880
Alignment-free multistandard vision and FM sound IF-PLL demodulator

Product specification
Supersedes data of 1998 Aug 12
File under Integrated Circuits, IC02

1999 Jul 21

Philips
Semiconductors

PHILIPS

Alignment-free multistandard vision and FM sound IF-PLL demodulator

TDA9880

FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response)
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free
- Digital acquisition help, VIF frequencies of 38.0, 38.9, 45.75 and 58.75 MHz
- 4 MHz reference frequency input [signal from Phase-Locked Loop (PLL) tuning system] or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector, fast reaction time
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0 and 6.5 MHz, controlled by reference signal
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- Digital frequency control, sound carrier frequencies 4.5, 5.5, 6.0 and 6.5 MHz
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- Electrostatic discharge (ESD) protection for all pins.

GENERAL DESCRIPTION

The TDA9880(T) is an integrated circuit for multistandard vision IF signal processing and FM demodulation in TV and VTR sets.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9880	SDIP20	plastic shrink dual in-line package; 20 leads (300 mil)	SOT325-1
TDA9880T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	note 1	4.5	5	5.5	V
I_P	supply current		85	100	115	mA
$V_{i(sens)(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	−1 dB video at output	–	50	100	μV
$G_{VIF(cr)}$	VIF gain control range	see Fig.4	65	69	–	dB
f_{VIF}	VIF frequencies	see Table 2	–	38.0	–	MHz
			–	38.9	–	MHz
			–	45.75	–	MHz
			–	58.75	–	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	referenced to f_{VIF}	–	±2.38	–	MHz
$V_{o(v)(p-p)}$	video output signal voltage (peak-to-peak value)	sound carrier off; see Fig.10	1.7	2.0	2.3	V
		trap bypass mode; see Fig.10	0.95	1.10	1.25	V
G_{dif}	differential gain	*"NTC-7 Composite"*	–	2	5	%
φ_{dif}	differential phase	*"NTC-7 Composite"*	–	2	4	deg
$B_{v(-3dB)(trap)}$	−3 dB video bandwidth including sound carrier trap	C_L < 20 pF; R_L > 1 kΩ; AC load; note 2				
		f_{trap} = 4.5 MHz (M/N standard)	3.95	4.05	–	MHz
		f_{trap} = 5.5 MHz (B/G standard)	4.90	5.00	–	MHz
α_{SC1}	trap attenuation at first sound carrier	M/N standard	30	36	–	dB
		B/G standard	30	36	–	dB
S/N_W	weighted signal-to-noise ratio of video signal	see Fig.6; note 3	56	60	–	dB
$PSRR_{13}$	power supply ripple rejection at pin 13	f_{ripple} = 70 Hz; video signal; grey level; see Fig.9	25	28	–	dB
$B_{v(-1dB)}$	−1 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load; trap bypass mode	5	6	–	MHz
$I_{ch(max)(20)}$	AGC maximum charge current at pin 20		6	8	10	μA
$I_{dch(max)(20)}$	AGC maximum discharge current at pin 20		7.5	10	12.5	μA
$I_{sink(14)}$	sink current of tuner AGC at pin 14	maximum tuner gain reduction; V_{14} = 1 V; see Fig.4	450	600	750	μA
AFC_{stps}	AFC steepness $\Delta I_{19}/\Delta f$		0.85	1.05	1.25	μA/kHz
$I_{o(source)(19)}$	AFC output source current at pin 19		160	200	240	μA
$I_{o(sink)(19)}$	AFC output sink current at pin 19		160	200	240	μA
$V_{o(intc)(rms)}$	intercarrier output voltage (RMS value)	$\frac{V_{i(SC)}}{V_{i(PC)}}$ = −24 dB ; note 4	–	49	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$B_{intc(-3dB)(ul)}$	upper limit −3 dB intercarrier bandwidth		7.5	9	–	MHz
$V_{o(AF)(8)(rms)}$	audio output signal voltage at pin 8 (RMS value)	25 kHz FM deviation; 75 μs de-emphasis	400	500	600	mV
THD_8	total harmonic distortion at pin 8		–	0.15	0.5	%
$B_{AF(-3dB)}$	−3 dB audio frequency bandwidth	without de-emphasis; dependent on loop filter at pin 4	100	120	–	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	black picture	50	56	–	dB
		white picture	45	51	–	dB
		6 kHz sine wave (black-to-white modulation)	40	46	–	dB
		sound carrier subharmonics; f = 2.25 MHz ±3 kHz	35	40	–	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	75 μs de-emphasis; AM: f = 1 kHz; m = 0.3 referenced to 25 kHz FM deviation	40	46	–	dB
$PSRR_8$	power supply ripple rejection at pin 8	f_{ripple} = 70 Hz; see Fig.9	14	20	–	dB
Δf_{FM}	frequency window of digital acquisition help for FM demodulator		–	±225	–	kHz
$f_{ref(15)}$	frequency of reference signal at pin 15		–	4.0	–	MHz
$V_{ref(15)(rms)}$	amplitude of reference signal source at pin 15 (RMS value)	operation as input terminal	80	–	400	mV

Notes

1. Values of video and sound parameters can be decreased at V_P = 4.5 V.
2. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18); $|H(s)|$ is the absolute value of transfer function.
3. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 13). B = 4.2 MHz (M/N standard) or B = 5.0 MHz (B/G, I and D/K standard) weighted in accordance with *"CCIR 567"*.
4. The intercarrier output signal at pin 11 can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)(rms)} = 1.1\ V\ (p\text{-}p) \times \frac{1}{2\sqrt{2}} \times 10^{\frac{\frac{V_{i(SC)}}{V_{i(PC)}}(dB) + 6\ dB\ \pm 3\ dB}{20}}$$

where:

$\frac{1}{2\sqrt{2}}$ = correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}(dB)$ = sound-to-picture carrier ratio at VIF input (pins 1 and 2) in dB, 6 dB = correction term of internal circuitry and ±3 dB = tolerance of video output and intercarrier output amplitude $V_{o(intc)(rms)}$.

BLOCK DIAGRAM

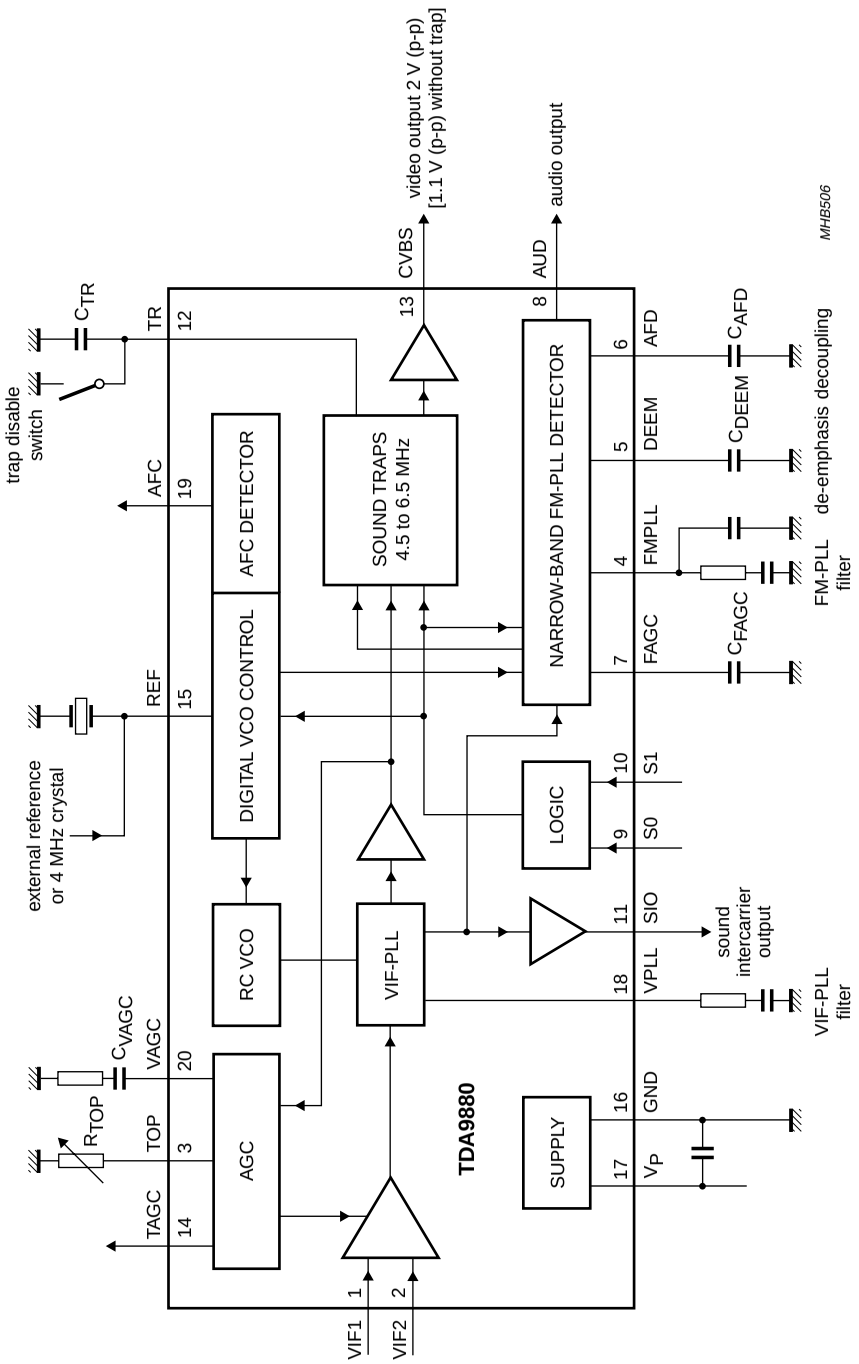


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
TOP	3	tuner AGC TakeOver Point (TOP)
FMPLL	4	FM-PLL filter
DEEM	5	de-emphasis capacitor
AFD	6	AF decoupling capacitor
FAGC	7	FM-PLL AGC capacitor
AUD	8	audio output
S0	9	switch input S0
S1	10	switch input S1

SYMBOL	PIN	DESCRIPTION
SIO	11	sound intercarrier output
TR	12	trap control
CVBS	13	video output
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference input
GND	16	ground supply
V_P	17	supply voltage (+5 V)
VPLL	18	VIF-PLL filter
AFC	19	AFC output
VAGC	20	VIF-AGC capacitor

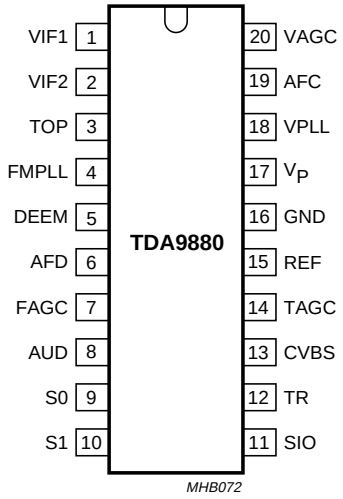


Fig.2 Pin configuration for SDIP20.

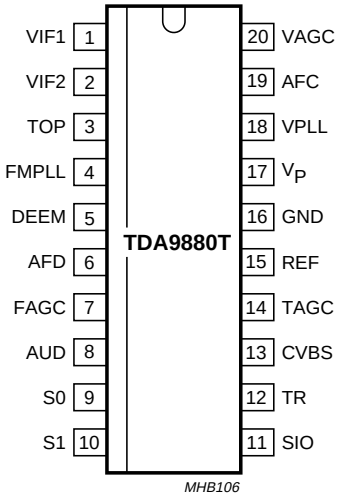


Fig.3 Pin configuration for SO20.

FUNCTIONAL DESCRIPTION

Figure 1 shows the simplified block diagram of the integrated circuit. The integrated circuit comprises the following functional blocks:

1. VIF amplifier
2. Tuner-AGC and VIF-AGC
3. VIF-AGC detector
4. Frequency Phase-Locked Loop (FPLL) detector
5. VCO and Travelling Wave Divider (TWD)
6. Digital acquisition help and AFC
7. Video demodulator and amplifier
8. Sound carrier trap
9. Intercarrier mixer
10. FM demodulator and acquisition help
11. Audio amplifier
12. Internal voltage stabilizer.

VIF amplifier

The VIF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

Tuner-AGC and VIF-AGC

The AGC capacitor voltage is converted to an internal VIF gain control signal, and is fed to the tuner AGC to generate the tuner AGC output current at pin TAGC (open-collector output). The tuner AGC takeover point can be adjusted with R_{TOP}. This allows the tuner to be matched to the SAW filter in order to achieve the optimum IF input level.

VIF-AGC detector

The AGC detector generates the required VIF gain control voltage for constant video output by charging or discharging the AGC capacitor. Gain control is performed by sync level detection. The newly developed AGC circuit provides fast reaction time to cope with ‘aeroplane fluttering’. The time constants for decreasing or increasing gain are nearly equal.

Frequency Phase-Locked Loop (FPLL) detector

The VIF amplifier output signal is fed into a Frequency Detector (FD) and into a Phase Detector (PD) via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal.

After frequency lock-in the phase detector produces a DC current proportional to the phase difference between the VCO and the input signal. The DC current of either the frequency detector or the phase detector is converted into a DC voltage via the VIF-PLL filter, which controls the VCO frequency.

VCO and Travelling Wave Divider (TWD)

The Resistor Capacitor (RC) VCO operates as an integrated relaxation oscillator at double the picture carrier frequency. The control voltage required to tune the VCO to actually double the picture carrier frequency is generated by the FPLL detector and fed via the loop filter to the VCO control input terminal.

The oscillator signal is divided-by-two with a TWD which generates two differential output signals with a 90 degrees phase difference independent of the frequency.

Digital acquisition help and AFC

The integrated relaxation oscillator has a very wide frequency range from approximately 30 to 70 MHz (after the TWD). To prevent false locking of the FPLL and with respect to the catching range of the frequency detector of maximum ±2.5 MHz, the Digital Acquisition Help (DAH) provides current into the loop filter until the VCO is in a frequency window of ±2.3 MHz around the wanted VIF frequency. In this case the analog operating FPLL will lock the VCO to the VIF carrier and the acquisition help does not provide any current to the loop filter.

The principle of the digital acquisition help is as follows: the VCO is connected to a downcounter, which is preset depending on the required VIF frequency. The counting time, as well as the counter control, is derived from a 4 MHz reference signal. This signal can be supplied from the internal 4 MHz crystal oscillator or from the 4 MHz reference oscillator of an external tuning system.
The counting result after a counting cycle corresponds to the actual VCO frequency.

The digital AFC is also derived from the counting result after a counting cycle by digital-to-analog converting the last four bits of the counter.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the ‘in phase’ signal of the travelling wave divider output.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics. The video signal of 1.1 V (p-p) for nominal vision IF modulation is fed internally to the integrated sound carrier trap as well as to the VIF-AGC detector. The second stage of the video amplifier converts and amplifies the differential output signal from the sound carrier trap to the single-ended CVBS output signal at pin 13 with a 2 V (p-p) amplitude.

Noise clipping is provided. Furthermore the trap can be bypassed by the implemented input switch of the second amplifier stage, forced by connecting pin 12 to ground.

Sound carrier trap

The sound carrier trap consists of a reference filter, a phase detector and the sound trap itself.

A sound carrier reference signal is fed into the reference low-pass filter and is shifted by a nominal 90 degrees. The phase detector compares the original reference signal with the signal shifted by the reference filter and produces, at the external capacitor C_{TR}, a DC voltage by charging or discharging the capacitor with a current proportional to the phase difference between both signals, respectively to the frequency error of the integrated filters. The DC voltage is converted to currents which control the frequency position of the reference filter and the sound trap.

The sound trap itself is constructed of three separate traps to realize sufficient suppression of the first and second sound carrier. The right frequency position of the different standards is set by the sound carrier reference signal.

Intercarrier mixer

The intercarrier mixer is realized by a multiplier, operating in quadrature mode for suppression of low frequency video signals. The VIF amplifier output signal is fed to the intercarrier mixer and converted to an intercarrier frequency by the regenerated 90 degree picture carrier from the VCO. The mixer output signal is fed via a band-pass filter and amplifier for attenuation of the high frequency video signal components and carrier harmonics to the output pin 11. The intercarrier signal is fed also to the integrated FM demodulator.

FM demodulator and acquisition help

The FM demodulator is realized as a narrow-band PLL with external loop filter, which provides the necessary selectivity. To achieve good selectivity, a linear phase detector and constant input level are required.
The intercarrier signal from the intercarrier mixer is fed via a gain controlled amplifier to the phase detector and it's output signal controls (via the loop filter) the integrated relaxation oscillator. The possible frequency range is from 4 to 7 MHz. As a result of locking the oscillator frequency tracks with the FM modulation of the input signal; therefore, the oscillator control voltage is superimposed by the AF voltage. In this way the FM-PLL operates as an FM demodulator. The AF voltage is present at the loop filter and is fed via a buffer with 0 dB gain to the audio amplifier.

The digital acquisition help operates in the same way as described in Section "Digital acquisition help and AFC".

Audio amplifier

The audio amplifier consists of two parts:

1. The AF preamplifier is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by 30 dB. A DC operating point control circuit (pin 6) decouples the AF amplifier from the DC voltage of the PLL. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal. If required, a de-emphasis network can be realized by the amplifier output resistance and an external capacitor.
2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to mute state, automatically controlled by the mute switching voltage from the digital acquisition help in order to avoid lock-in noise. During normal operation the automatic audio mute function is not active. Application of a 2.2 kΩ resistor between the intercarrier output (pin 11) and ground will activate the automatic audio mute function.

Internal voltage stabilizer

The band gap circuit internally generates a voltage of approximately 2.4 V, independent of the supply voltage and the temperature. A voltage regulator circuit, controlled by this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	I_P = 115 mA; T_{amb} = 70 °C; at maximum chip temperature of 125 °C	–	5.5	V
V_n	voltage at				
	pins 1 to 4, 6 to 10, 12 and 17 to 20		0	V_P	V
	pin 14		0	13.2	V
t_{sc}	short-circuit time to ground or V_P		–	10	s
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	ambient temperature		–20	+70	°C
V_{es}	electrostatic handling voltage for all pins	note 1	–250	+250	V
		note 2	–3000	+3000	V

Notes

1. Charge device model class A; machine model: discharging a 200 pF capacitor via a 0.75 μH inductance.
2. Charge device model class B; human body model: discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9880 (SDIP20)		85	K/W
	TDA9880T (SO20)		85	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; see Table 2 for input frequencies; M standard (f_{PC} = 45.75 MHz; f_{SC} = 41.25 MHz; PC/SC = 10 dB) is used for specification; $V_{i(VIF)(rms)}$ = 10 mV (sync level); IF input from 50 Ω via broadband transformer 1 : 1; DSB video modulation; 10% residual carrier; video signal in accordance with *"NTC-7 Composite"*; measurements taken in test circuit of Fig.19; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 17)						
V_P	supply voltage	note 1	4.5	5	5.5	V
I_P	supply current		85	100	115	mA
P_{tot}	total power dissipation		–	500	633	mW
VIF amplifier (pins 1 and 2)						
$V_{i(sens)(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	–1 dB video at output	–	50	100	μV
$V_{i(max)(rms)}$	maximum input signal voltage (RMS value)	1 dB video at output; note 2	110	–	–	mV
ΔV_{int}	internal IF amplitude difference between picture and sound carrier	within AGC range; Δf = 4.5 MHz	–	0.7	1	dB
$G_{VIF(cr)}$	VIF gain control range	see Fig.4	65	69	–	dB
$B_{VIF(-3dB)(ll)}$	lower limit –3 dB VIF bandwidth		–	15	25	MHz
$B_{VIF(-3dB)(ul)}$	upper limit –3 dB VIF bandwidth		70	100	–	MHz
$R_{i(dif)}$	differential input resistance	note 3	1.7	2.2	2.7	kΩ
$C_{i(dif)}$	differential input capacitance	note 3	1.2	1.7	2.5	pF
V_I	DC input voltage		–	3.35	–	V
FPLL and true synchronous video demodulator; note 4						
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	$f = 2f_{PC}$	120	140	–	MHz
f_{VIF}	vision carrier operating frequencies	see Table 2	–	38.0	–	MHz
			–	38.9	–	MHz
			–	45.75	–	MHz
			–	58.75	–	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	referenced to f_{VIF}	–	±2.38	–	MHz
t_{acq}	acquisition time	BL = 70 kHz; note 5	–	–	30	ms
$V_{i(sens)(VIF)(rms)}$	VIF input voltage sensitivity at pins 1 and 2 (RMS value)					
	for PLL to be locked	maximum IF gain	–	30	70	μV
	for C/N = 10 dB	notes 6 and 7	–	100	140	μV
SIGNAL AT PIN 18						
$I_{o(source)(PD)(max)}$	maximum source current of phase detector output		–	17	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{o(sink)(PD)(max)}$	maximum sink current of phase detector output		–	17	–	µA
$I_{o(source)(DAH)}$	output source current of digital acquisition help		–	23	–	µA
$I_{o(sink)(DAH)}$	output sink current of digital acquisition help		–	23	–	µA
$t_{W(min)(DAH)}$	minimum pulse width of digital acquisition help current		–	64	–	µs
$K_{O(VIF)}$	VCO steepness $\Delta f_{VIF}/\Delta V_{18}$		–	20	–	MHz/V
$K_{D(VIF)}$	phase detector steepness $\Delta I_{18}/\Delta\varphi_{VIF}$		–	23	–	µA/rad
Video output signal and sound carrier trap (pin 13; sound carrier off)						
$V_{o(v)(p-p)}$	video output signal voltage (peak-to-peak value)	see Fig.10	1.7	2.0	2.3	V
V_{sync}	sync pulse voltage level	see Fig.10	1.15	1.35	1.55	V
V_{zc}	zero carrier voltage level	see Fig.10	3.27	3.57	3.87	V
$V_{v(clu)}$	upper video clipping voltage level		V_P – 1.1	V_P – 1	–	V
$V_{v(cll)}$	lower video clipping voltage level		–	0.7	1.0	V
R_o	output resistance	note 3	–	–	30	Ω
$I_{bias(int)}$	internal DC bias current for emitter-follower		2.0	2.5	–	mA
$I_{o(source)(max)}$	maximum AC and DC output source current		2.4	–	–	mA
$I_{o(sink)(max)}$	maximum AC and DC output sink current		1.4	–	–	mA
ΔV_o	deviation of CVBS output signal voltage	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
$\Delta V_{o(bl)}$	black level tilt		–	–	1	%
G_{dif}	differential gain	*"NTC-7 Composite"*	–	2	5	%
φ_{dif}	differential phase	*"NTC-7 Composite"*	–	2	4	deg
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	C_L < 20 pF; R_L > 1 kΩ; AC load; note 8				
		f_{trap} = 4.5 MHz (M/N standard)	3.95	4.05	–	MHz
		f_{trap} = 5.5 MHz (B/G standard)	4.90	5.00	–	MHz
		f_{trap} = 6.0 MHz (I standard)	5.2	5.50	–	MHz
		f_{trap} = 6.5 MHz (D/K standard)	5.5	5.95	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{SC1}	trap attenuation at first sound carrier	M/N standard	30	36	–	dB
		B/G standard	30	36	–	dB
		I standard	26	32	–	dB
		D/K standard	26	32	–	dB
$\alpha_{SC1(60\ kHz)}$	trap attenuation at first sound carrier f_{SC1} ±60 kHz	M/N standard	21	27	–	dB
		B/G standard	24	30	–	dB
		I standard	20	26	–	dB
		D/K standard	20	26	–	dB
α_{SC2}	trap attenuation at second sound carrier	M/N standard	21	27	–	dB
		B/G standard	21	27	–	dB
		I standard	12	18	–	dB
		D/K standard	18	24	–	dB
$\alpha_{SC2(60\ kHz)}$	trap attenuation at second sound carrier f_{SC2} ±60 kHz	M/N standard	15	21	–	dB
		B/G standard	15	21	–	dB
		I standard	10	15	–	dB
		D/K standard	13	18	–	dB
$t_{d(g)(CC)}$	group delay at chrominance carrier frequency	3.58 MHz at M/N standard	110	180	250	ns
		4.43 MHz at B/G standard	110	180	250	ns
		4.43 MHz at I standard	–	90	160	ns
		4.28 MHz at D/K standard	–	60	130	ns
S/N_W	weighted signal-to-noise ratio	weighted in accordance with *"CCIR 567"*; see Fig.6; note 9	56	60	–	dB
S/N_{UW}	unweighted signal-to-noise ratio	note 9	47	51	–	dB
αd_{blue}	intermodulation attenuation at 'blue'	f = 0.92 MHz; see Fig.7; note 10	58	64	–	dB
		f = 2.76 MHz; see Fig.7; note 10	58	64	–	dB
αd_{yellow}	intermodulation attenuation at 'yellow'	f = 0.92 MHz; see Fig.7; note 10	60	66	–	dB
		f = 2.76 MHz; see Fig.7; note 10	59	65	–	dB
$\Delta V_{r(vc)(rms)}$	residual vision carrier (RMS value)	fundamental wave and harmonics	–	2	5	mV
$\alpha_{H(sup)}$	harmonics suppression in video signal	C_L < 20 pF; R_L > 1 kΩ; AC load; note 11a	35	40	–	dB
$\alpha_{H(spur)}$	spurious elements suppression in video signal	note 11b	40	–	–	dB
$PSRR_{13}$	power supply ripple rejection at pin 13	f_{ripple} = 70 Hz; video signal; grey level; see Fig.9	25	28	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video output signal (pin 13; trap bypass mode; V_{12} < 0.8 V; sound carrier off); see Fig.10; note 12						
$V_{o(v)(p-p)}$	video output signal voltage (peak-to-peak value)	see Fig.10	0.95	1.10	1.25	V
V_{sync}	sync pulse voltage level		1.4	1.5	1.6	V
V_{zc}	zero carrier voltage level		2.57	2.72	2.87	V
$V_{v(clu)}$	upper video clipping voltage level		3.1	3.25	–	V
$V_{v(cll)}$	lower video clipping voltage level		–	1.15	1.3	V
$B_{v(-1dB)}$	–1 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	5	6	–	MHz
$B_{v(-3dB)}$	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	7	8	–	MHz
S/N_W	weighted signal-to-noise ratio	weighted in accordance with *"CCIR 567"*; see Fig.6; note 9	56	60	–	dB
S/N_{UW}	unweighted signal-to-noise ratio	note 9	49	53	–	dB
Trap control (pin 12)						
$I_{o(source)(max)}$	maximum output source current		5	9	13	µA
$I_{o(sink)(max)}$	maximum output sink current		9	13	17	µA
$K_{D(trap)}$	frequency detector steepness $\Delta I_{12}/\Delta f_{trap}$	f_{trap} = 4.5 MHz (M/N standard)	–	–8	–	µA/MHz
		f_{trap} = 6.5 MHz (D/K standard)	–	–5.5	–	µA/MHz
V_{12}	operating voltage range of trap frequency control at pin 12		1.5	–	3.5	V
$I_{L(12)}$	leakage current at pin 12	Δf_{trap} < ±25 kHz	–	–	±80	nA
CR_{stps}	control steepness $\Delta f_{trap}/\Delta V_{12}$	f_{trap} = 4.5 MHz (M/N standard)	–	4.5	–	MHz/V
		f_{trap} = 6.5 MHz (D/K standard)	–	9	–	MHz/V
V_{sw}	switching voltage	trap bypass mode active	–	–	0.8	V
I_{source}	source current	trap bypass mode active; $V_{12} \leq 0.8$ V	–	185	–	µA
VIF-AGC detector (pin 20)						
$I_{ch(max)(20)}$	maximum charge current		6	8	10	µA
$I_{dch(max)(20)}$	maximum discharge current		7.5	10	12.5	µA
$t_{res(inc)}$	AGC response time to an increasing VIF step	6 dB; note 13	–	2.0	–	ms
		20 dB; note 13	–	2.5	–	ms
		40 dB; note 13	–	4.0	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{res(dec)}$	AGC response time to a decreasing VIF step	–6 dB; note 13	–	1.0	–	ms
		–20 dB; note 13	–	1.5	–	ms
		–40 dB; note 13	–	2.5	–	ms
V_{20}	gain control voltage range at pin 20		1.7	–	3.6	V
CR_{stps}	control steepness $\Delta G_{IF}/\Delta V_{20}$	V_{20} = 2.2 to 3.2 V	–	–40	–	dB/V
Tuner AGC (pin 14); see Figs 4 and 5						
$V_{i(VIF)(min)(rms)}$	VIF input signal voltage for minimum starting point of tuner takeover at pins 1 and 2 (RMS value)	R_{TOP} = 22 kΩ; I_{14} = 120 μA	–	2	5	mV
$V_{i(VIF)(max)(rms)}$	VIF input signal voltage for maximum starting point of tuner takeover at pins 1 and 2 (RMS value)	R_{TOP} = 0 Ω; I_{14} = 120 μA	45	90	–	mV
$QV_{i(VIF)(rms)}$	tuner takeover point accuracy (RMS value)	R_{TOP} = 12 kΩ; I_{14} = 120 μA	5	10	20	mV
V_o	permissible output voltage	from external source	–	–	13.2	V
V_{sat}	saturation voltage	I_{14} = 450 μA	–	–	0.2	V
$V_{i(VIF)(rms)}/\Delta T$	variation of takeover point with temperature	I_{14} = 120 μA	–	0.03	0.07	dB/K
I_{sink}	sink current	no tuner gain reduction; see Fig.4				
		V_{14} = 12 V	–	–	0.75	μA
		V_{14} = 13.2 V	–	–	1.5	μA
		maximum tuner gain reduction; V_{14} = 1 V; see Fig.4	450	600	750	μA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20% to 80%	–	5	8	dB
AFC circuit (pin 19); notes 14 and 15						
AFC_{stps}	AFC steepness $\Delta I_{19}/\Delta f_{VIF}$		0.85	1.05	1.25	μA/kHz
Qf_{VIF}	accuracy of AFC circuit	$I_{o(19)}$ = 0; f_{15} = 4.0 MHz	–20	–	+20	kHz
$V_{sat(ul)}$	upper limit saturation voltage	see Fig.8	V_P – 0.6	V_P – 0.3	–	V
$V_{sat(ll)}$	lower limit saturation voltage	see Fig.8	–	0.3	0.6	V
$I_{o(source)}$	output source current		160	200	240	μA
$I_{o(sink)}$	output sink current		160	200	240	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Intercarrier mixer (pin 11)						
$V_{o(intc)(rms)}$	intercarrier output voltage (RMS value)	$\frac{V_{i(SC)}}{V_{i(PC)}}$ = −24 dB ; note 16	–	49	–	mV
$B_{intc(-3dB)(ul)}$	upper limit −3 dB intercarrier bandwidth		7.5	9	–	MHz
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics	–	2	–	mV
R_o	output resistance	note 3	–	–	70	Ω
V_O	DC output voltage		1.85	2.05	2.35	V
$I_{bias(int)}$	internal DC bias current for emitter-follower		0.9	1.15	–	mA
$I_{o(source)(max)}$	maximum AC output source current	note 17	0.6	0.8	–	mA
$I_{o(sink)(max)}$	maximum AC output sink current	note 17	0.6	0.8	–	mA
$I_{O(source)}$	DC output source current	automatic audio mute function activated; note 17	0.75	0.93	1.20	mA
FM-PLL demodulator; notes 15 and 18 to 21						
f_{intc}	sound intercarrier operating frequencies	see Table 2	–	4.5	–	MHz
			–	5.5	–	MHz
			–	6.0	–	MHz
			–	6.5	–	MHz
Δf_{FM}	frequency window of digital acquisition help for FM demodulator		–	±225	–	kHz
$V_{FM(rms)}$	IF intercarrier level for gain controlled operation of FM-PLL (RMS value)	corresponding PC/SC ratio at input pins 1 and 2 is 7 to 40 dB	6	–	320	mV
$V_{FM(lock)(rms)}$	IF intercarrier level for lock-in of PLL (RMS value)		–	–	3	mV
G_{FM}	IF intercarrier gain control range		30	34	–	dB
SIGNAL AT PIN 7						
V_7	gain control voltage range at pin 7		1.5	–	3.5	V
$I_{ch(max)(7)}$	maximum charge current		1.5	2.2	2.9	µA
$I_{dch(max)(7)}$	maximum discharge current		1.5	2.2	2.9	µA
CR_{stps}	control steepness $\Delta G_{FM}/\Delta V_7$	V_7 = 2.2 to 2.7 V	–	−30	–	dB/V
SIGNAL AT PIN 8						
$V_{o(AF)(rms)}$	audio output signal voltage (RMS value)	25 kHz FM deviation	400	500	600	mV
		27 kHz FM deviation	432	540	648	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(AF)(cl)(rms)}$	audio output clipping signal voltage level (RMS value)	THD < 1.5%	1.3	1.4	–	V
THD	total harmonic distortion		–	0.15	0.5	%
$\Delta V_{o(AF)}/\Delta T$	temperature drift of AF output signal voltage		–	3×10^{-3}	7×10^{-3}	dB/K
Δf_{AF}	audio frequency deviation	THD < 1.5%; note 22	–	–	±55	kHz
$B_{AF(-3dB)}$	−3 dB audio frequency bandwidth	without de-emphasis; dependent on loop filter at pin 4; measured in accordance with Fig.19	80	100	–	kHz
S/N_W	weighted signal-to-noise ratio of audio signal	black picture	50	56	–	dB
		white picture	45	51	–	dB
		6 kHz sine wave (black-to-white modulation)	40	46	–	dB
		sound carrier subharmonics; f = 2.25 MHz ±3 kHz	35	40	–	dB
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics; without de-emphasis	–	–	2	mV
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	75 µs de-emphasis; AM: f = 1 kHz; m = 0.3 referenced to 25 kHz FM deviation	40	46	–	dB
$PSRR_8$	power supply ripple rejection at pin 8	f_{ripple} = 70 Hz; see Fig.9	14	20	–	dB
SIGNAL AT PIN 4						
$I_{o(source)(PD)(max)}$	maximum phase detector output source current		–	86	–	µA
$I_{o(sink)(PD)(max)}$	maximum phase detector output sink current		–	80	–	µA
$I_{o(source)(DAH)}$	output source current of digital acquisition help		–	110	–	µA
$I_{o(sink)(DAH)}$	output sink current of digital acquisition help		–	110	–	µA
$t_{W(DAH)}$	pulse width of digital acquisition help current		–	16	–	µs
$T_{cy(DAH)}$	cycle time of digital acquisition help		–	64	–	µs
$K_{O(FM)}$	VCO steepness $\Delta f_{FM}/\Delta V_4$		–	3.3	–	MHz/V
$K_{D(FM)}$	phase detector steepness $\Delta I_4/\Delta\varphi_{FM}$		–	9	–	µA/rad

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio amplifier (pins 5, 6 and 8)						
$R_{o(5)}$	output resistance at pin 5	note 23	4.4	5.0	5.6	kΩ
$V_{AF(5)(rms)}$	audio signal (RMS value) at pin 5		–	170	–	mV
$V_{O(5)}$	DC output voltage at pin 5		–	2.37	–	V
$R_{o(8)}$	output resistance at pin 8	note 3	–	–	200	Ω
$V_{O(8)}$	DC output voltage at pin 8		–	2.37	–	V
$I_{o(source)(max)(8)}$	maximum AC and DC output source current at pin 8		–	–	0.5	mA
$I_{o(sink)(max)(8)}$	maximum AC and DC output sink current at pin 8		–	–	0.5	mA
V_6	DC decoupling voltage at pin 6	dependent on intercarrier frequency f_{FM}	1.5	–	3.3	V
$I_{L(6)}$	leakage current at pin 6	$\Delta V_{O(8)} < \pm 50$ mV	–	–	±25	nA
$I_{ch(max)(6)}$	maximum charge current at pin 6		1.15	1.5	1.85	μA
$I_{dch(max)(6)}$	maximum discharge current at pin 6		1.15	1.5	1.85	μA
$B_{AF(-3dB)}$	−3 dB audio frequency bandwidth of audio amplifier	upper limit	150	–	–	kHz
		lower limit; note 24	–	–	20	Hz
$\alpha_{mute(8)}$	mute attenuation of AF signal at pin 8	note 17	70	75	–	dB
ΔV_8	DC jump voltage at pin 8 for switching AF output to mute state and vice versa	activated by digital acquisition help; note 17	–	±50	±150	mV
Standard switch (pins 9 and 10); see Table 2						
V_i	input voltage	pin open-circuit; $I_{i(9,10)} < 0.1$ μA	2.8	3.0	3.6	V
		for LOW	0	–	0.8	V
		for MID	1.3	1.8	2.3	V
		for HIGH	2.8	–	V_P	V
$I_{i(source)}$	input source current	$V_{i(9,10)} = 0$ V	87	105	122	μA
		$V_{i(9,10)} = 1.8$ V	33	39	45	μA
Reference input (pin 15); note 25						
V_I	DC input voltage		2.3	2.6	2.9	V
R_i	input resistance		2.5	3.0	3.5	kΩ
R_{xtal}	resonance resistance of crystal	operation as crystal oscillator	–	–	200	Ω
C_x	pull-up/down capacitance	note 26	–	–	–	pF
f_{ref}	frequency of reference signal		–	4.0	–	MHz
Δf_{ref}	tolerance of reference frequency	note 15	–	–	±0.1	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{ref(rms)}$	amplitude of reference signal source (RMS value)	operation as input terminal	80	–	400	mV
$R_{o(ref)}$	output resistance of reference source		–	–	4.7	kΩ
C_K	decoupling capacitance to external reference source	operation as input terminal	22	100	–	pF

Notes

1. Values of video and sound parameters can be decreased at V_P = 4.5 V.
2. This parameter is tested with 110 mV to ensure maximum input level.
3. This parameter is not tested during production and is only given as application information for designing the television receiver.
4. Loop bandwidth BL = 70 kHz (damping factor d = 1.9; calculated with sync level within gain control range). Calculation of the VIF-PLL filter can be done by use of the following formulae:

   $BL_{-3\,dB} = \frac{1}{2\pi} K_O K_D R$, valid for $d \geq 1.2$

   $d = \frac{1}{2} R \sqrt{K_O K_D C}$,

   where:

   K_O = VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D = phase detector steepness $\left(\frac{\mu A}{rad}\right)$;

   R = loop resistor; C = loop capacitor; $BL_{-3\,dB}$ = loop bandwidth for –3 dB; d = damping factor.
5. $V_{i(VIF)(rms)}$ = 10 mV; Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. $V_{i(VIF)}$ signal for nominal video signal.
7. Broadband transformer at VIF input. The C/N ratio at VIF input is defined as the VIF input signal (sync level, RMS value) related to a superimposed 4.2 MHz band-limited white noise signal (RMS value); white picture video modulation.
8. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18); $|H(s)|$ is the absolute value of transfer function.
9. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value, pin 13). B = 4.2 MHz (M/N standard) or B = 5.0 MHz (B/G, I and D/K standard).
10. The intermodulation figures are defined:

    $\alpha d_{0.92} = 20\ \log\left(\frac{V_0 \text{at 3.58 MHz}}{V_0 \text{at 0.92 MHz}}\right) + 3.6$ dB ; $\alpha d_{0.92}$ value at 0.92 MHz referenced to black or white signal;

    $\alpha d_{2.76} = 20\ \log\left(\frac{V_0 \text{at 3.58 MHz}}{V_0 \text{at 2.76 MHz}}\right)$; $\alpha d_{2.76}$ value at 2.76 MHz referenced to chrominance carrier.
11. Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz.
    a) Modulation Vestigial Side-Band (VSB); sound carrier off; f_{video} > 0.5 MHz.
    b) Sound carrier on; f_{video} = 10 kHz to 10 MHz.
12. The sound carrier trap can be disabled by switching pin 12 to ground (<0.8 V). In this way the full composite video spectrum appears at pin 13. The amplitude is 1.1 V (p-p).
13. Response time valid for a VIF input level range of 200 μV to 70 mV.

14. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.8. The AFC steepness can be changed by resistors R1 and R2.
15. The tolerance of the reference frequency determines the accuracy of the VIF AFC, FM demodulator centre frequency and maximum FM deviation.
16. The intercarrier output signal at pin 11 can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)(rms)} = 1.1\ V\ (p\text{-}p) \times \frac{1}{2\sqrt{2}} \times 10^{\frac{\frac{V_{i(SC)}}{V_{i(PC)}}(dB) + 6\ dB\ \pm 3\ dB}{20}}$$

where:

$\frac{1}{2\sqrt{2}}$ = correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}(dB)$ = sound-to-picture carrier ratio at VIF input (pins 1 and 2) in dB, 6 dB = correction term of internal circuitry and ±3 dB = tolerance of video output and intercarrier output amplitude $V_{o(intc)(rms)}$.

17. For normal operation no DC load at pin 11 is allowed, so the automatic audio mute function is not active. By connecting a 2.2 kΩ resistor between pin 11 and ground the automatic audio mute function will be activated. With this application also the series capacitor C_S of the loop filter at pin 4 should be changed from 33 nF to 4.7 nF.
18. Calculation of the FM-PLL filter can be done approximately by use of the following formulae:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{K_O K_D}{C_P}}$$

$$\vartheta = \frac{1}{2R\sqrt{K_O K_D C_P}}$$

$$BL_{-3\ dB} = f_o(1.55 - \vartheta^2)$$

The formulae are only valid under the following conditions:
$\vartheta \leq 1$ and $C_S > 5C_P$
where:

K_O = VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D = phase detector steepness $\left(\frac{\mu A}{rad}\right)$;

R_S = loop resistor; C_S = series capacitor; C_P = parallel capacitor; f_o = natural frequency of PLL; $BL_{-3\ dB}$ = loop bandwidth for −3 dB; ϑ = damping factor. For examples see Table 1.

19. For all S/N measurements the used vision IF modulator requires an incidental phase modulation for black-to-white jump of less than 0.5 degrees.
20. Measurements taken with SAW filter M1963M (Siemens) for vision and sound IF (sound shelf: 20 dB). Picture-to-sound carrier ratio of transmitter: PC/SC = 10 dB. Input level (at pins 1 and 2) $V_{i(VIF)(rms)}$ = 10 mV (sync level), 25 kHz FM deviation for sound carrier, f_{AF} = 400 Hz. Measurement in accordance with *"CCIR 468-4"*. De-emphasis = 75 μs.
21. The PC/SC ratio is calculated as the addition of TV transmitter PC/SC ratio and SAW filter PC/SC ratio. This PC/SC ratio is necessary to achieve the S/N_W values as noted. A different PC/SC ratio will change these values.
22. Measured with an FM deviation of 25 kHz, the typical AF output signal is 500 mV (RMS). By using R_x = 20 kΩ the AF output signal is attenuated by 6 dB, so 250 mV (RMS). For handling an FM deviation of more than 55 kHz the AF output signal has to be reduced by using R_x in order to avoid clipping (THD < 1.5%). For an FM deviation up to 100 kHz an attenuation of 6 dB is recommended.
23. C_{DEEM} = 10 nF results in τ = 50 μs and C_{DEEM} = 15 nF results in τ = 75 μs.

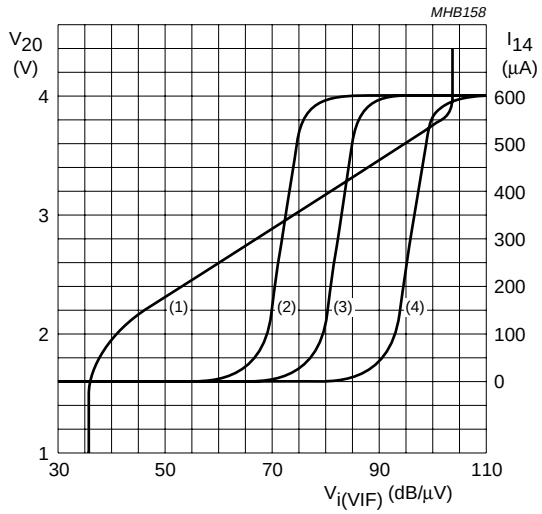
24. The lower limit of audio bandwidth depends on the value of the capacitor at pin 6. A value of C_{AFD} = 470 nF leads to $f_{AF(-3\ dB)} \approx 20$ Hz and C_{AFD} = 220 nF leads to $f_{AF(-3\ dB)} \approx 40$ Hz.
25. The reference input pin 15 is able to operate as a 1-pin crystal oscillator as well as an input terminal with external reference signal, e.g. from the tuning system.
26. The value of C_x determines the accuracy of the resonance frequency of the crystal. It depends on the type of crystal used.

Table 1 Examples to note 18 of Chapter “Characteristics”

$BL_{-3\ dB}$ (kHz)	C_S (nF)	C_P (pF)	R (kΩ)	ϑ
100	33	820	2.7	0.5
160	33	330	3.9	0.5

Table 2 Standard switch settings

S0	S1	f_{VIF} (MHz)	f_{intc} (MHz)	STANDARD	REMARK
LOW	LOW	38.9	5.5	B/G	Europe
LOW	MID	38.9	6.5	D/K	
LOW	HIGH	38.9	6.0	I	United Kingdom
MID	LOW	38.0	5.5	B/G	
MID	MID	38.0	6.0	I	
MID	HIGH	38.0	6.5	D/K	
HIGH	LOW	45.75	4.5	M/N	USA
HIGH	MID	38.0	4.5	M	
HIGH	HIGH	58.75	4.5	M	Japan



(1) VIF AGC voltage.
(2) I_{tuner}; R_{TOP} = 22 kΩ.
(3) I_{tuner}; R_{TOP} = 12 kΩ.
(4) I_{tuner}; R_{TOP} = 0 Ω.

Fig.4 Typical VIF and tuner AGC characteristic.

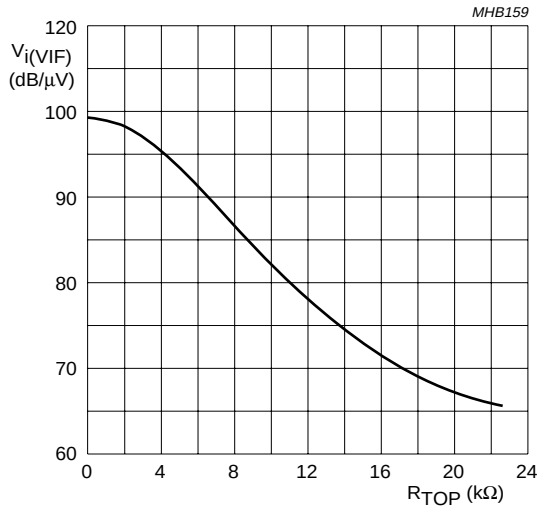


Fig.5 Typical tuner takeover point as a function of R_{TOP}.

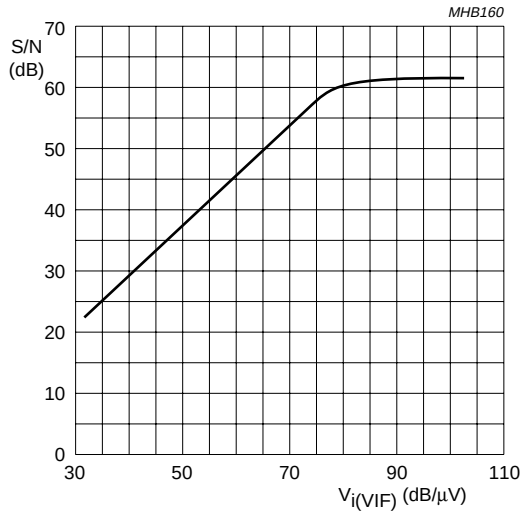
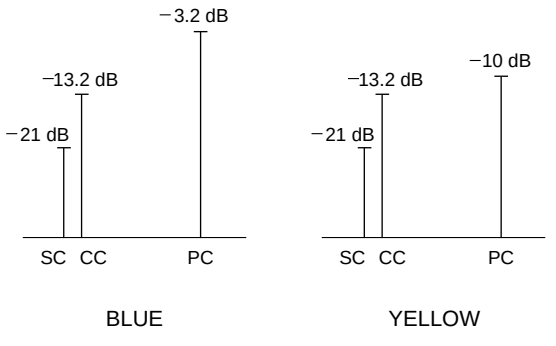


Fig.6 Typical signal-to-noise ratio as a function of VIF input voltage.



SC = sound carrier, with respect to sync level.
CC = chrominance carrier, with respect to sync level.
PC = picture carrier, with respect to sync level.
The sound carrier levels are taking into account a sound shelf attenuation of 20 dB (SAW filter M1963M).

Fig.7 Input signal conditions.

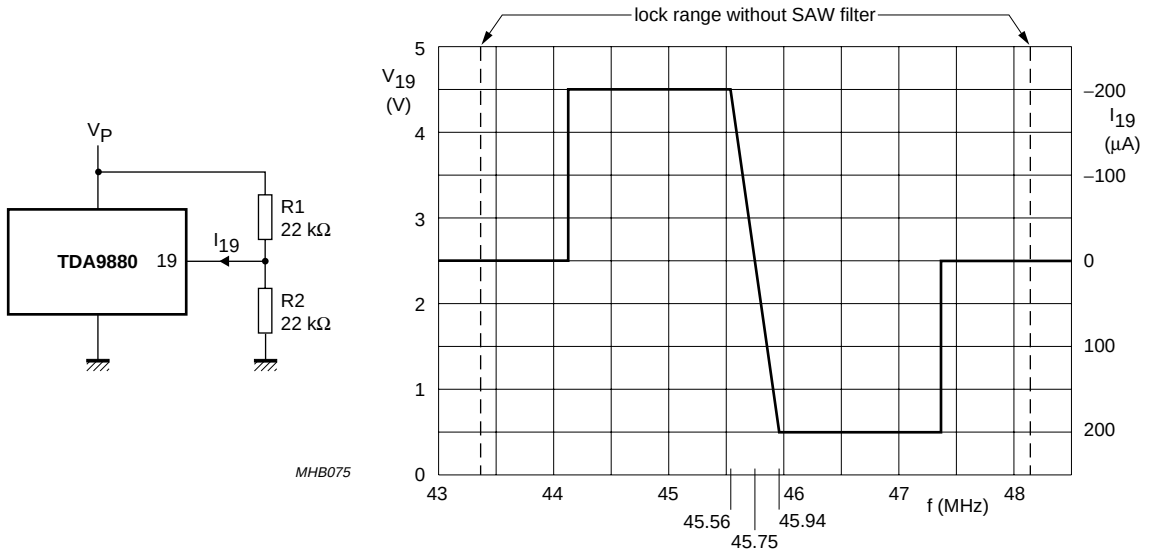


Fig.8 Measurement conditions and typical AFC characteristic.

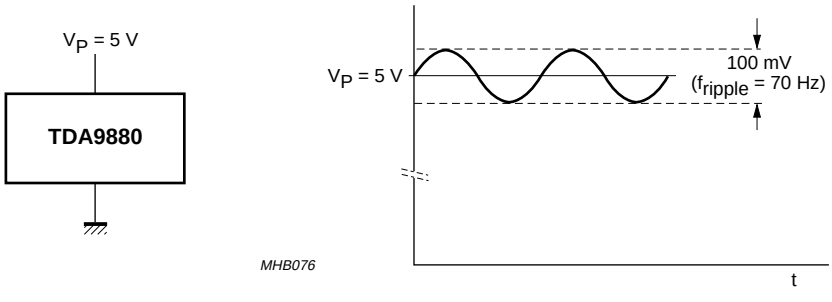


Fig.9 Ripple rejection condition.

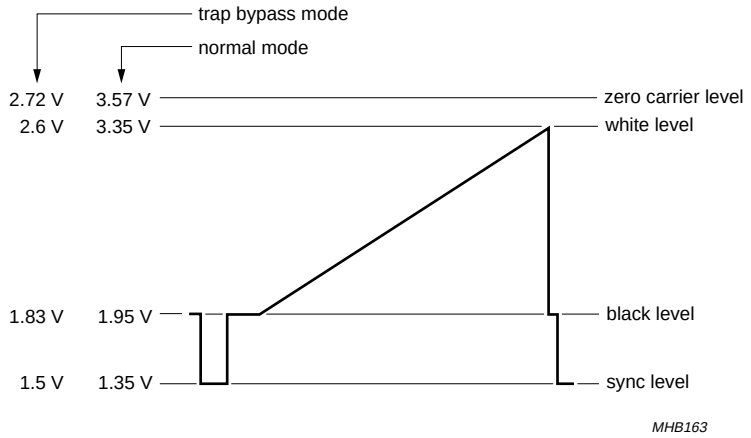
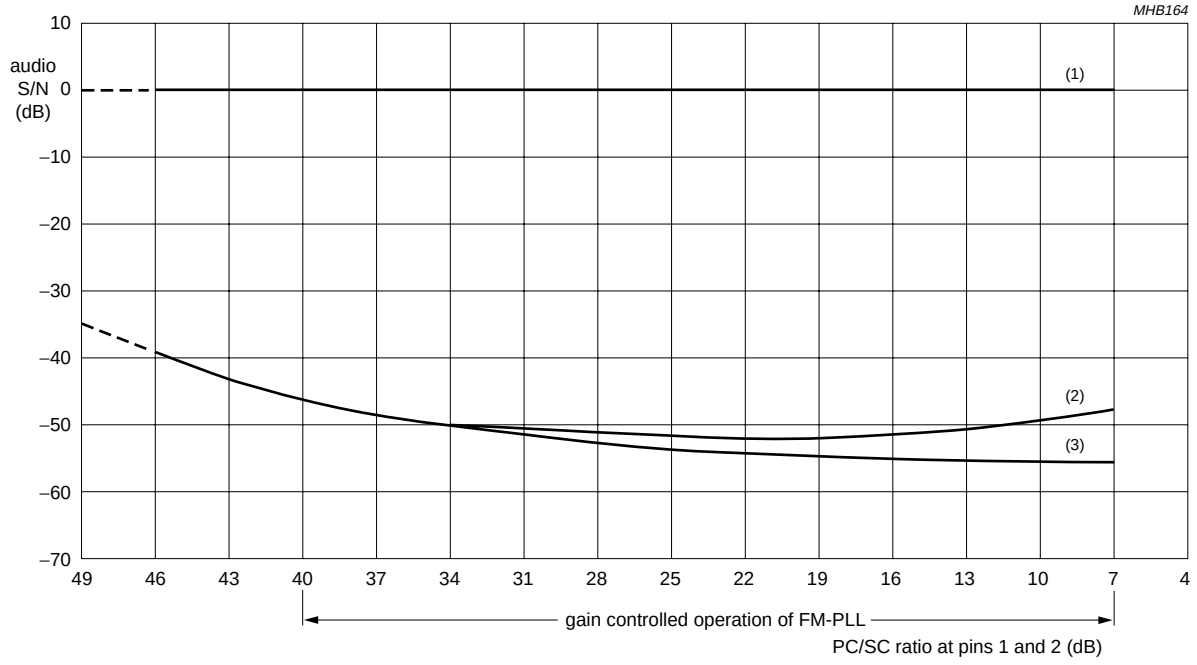


Fig.10 Typical video signal levels on output pin 13 (sound carrier off).



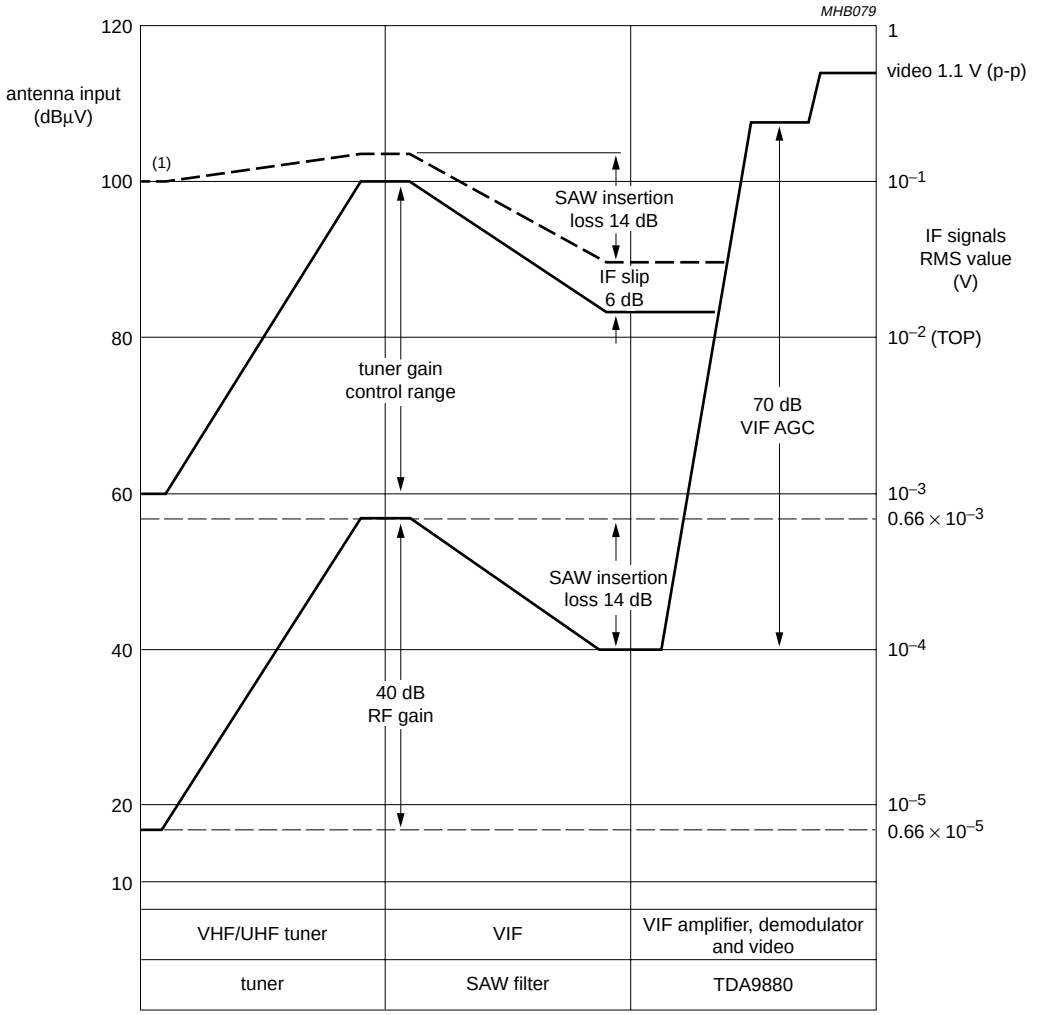
Conditions: 25 kHz FM deviation; 75 μs de-emphasis.

(1) Signal.

(2) Noise at H-picture.

(3) Noise at black picture.

Fig.0 Audio S/N as a function of picture-to-sound carrier ratio.



(1) Depends on TOP.

Fig.12 Front-end level diagram.

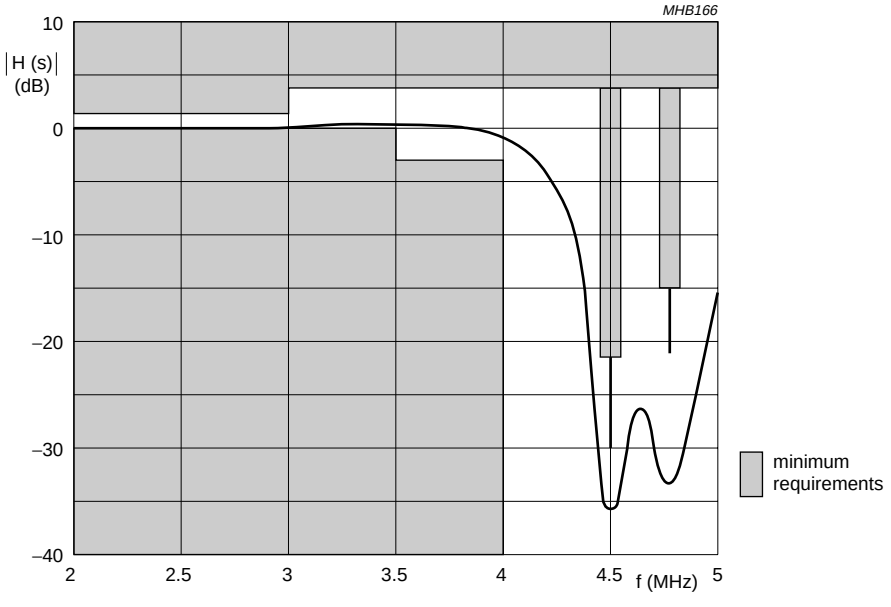
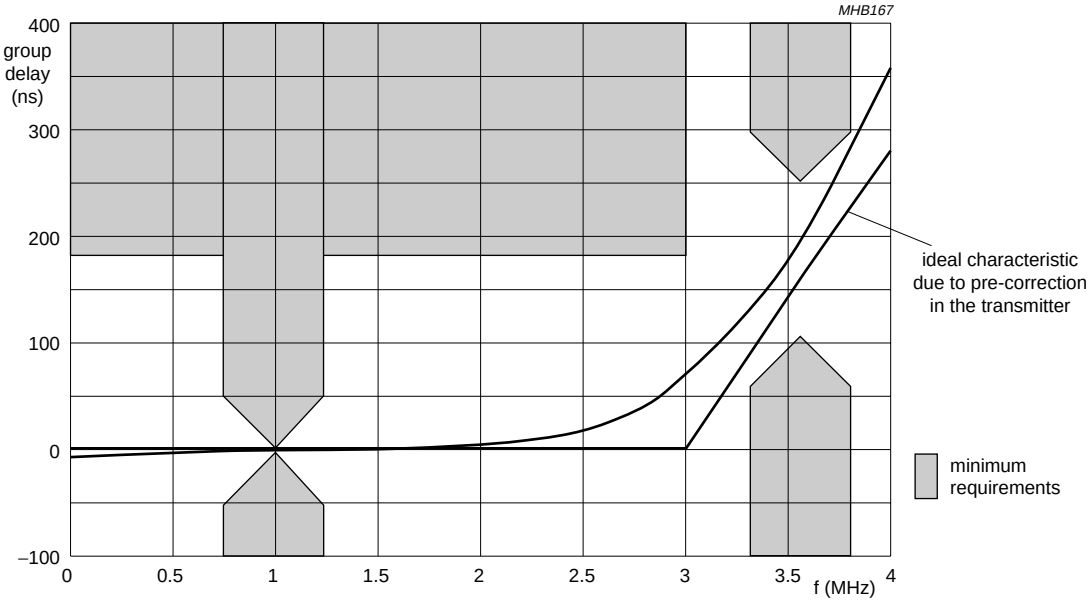


Fig.13 Typical amplitude response for sound trap at M/N standard (including Korea).



Remark: overall delay is not shown, here the maximum ripple is specified.

Fig.14 Typical group delay for sound trap at M/N standard.

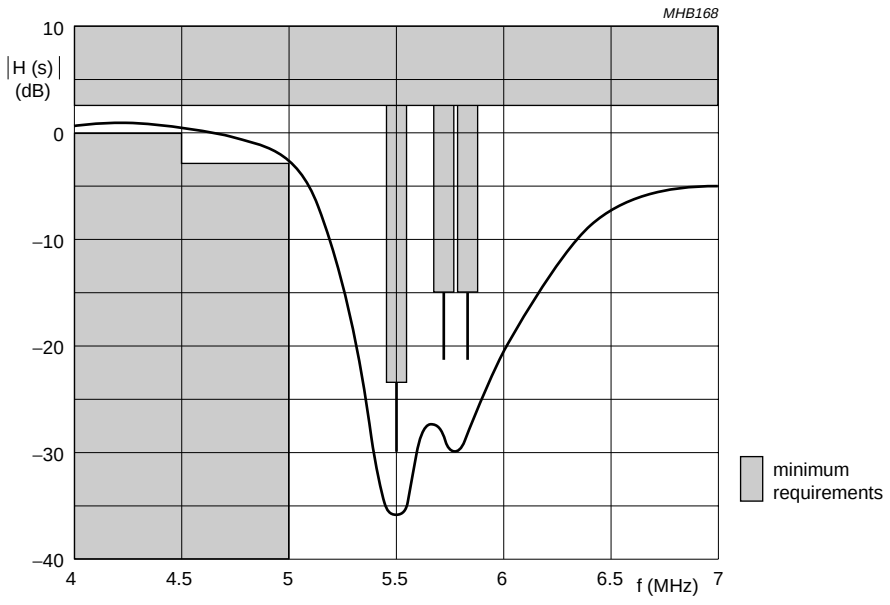
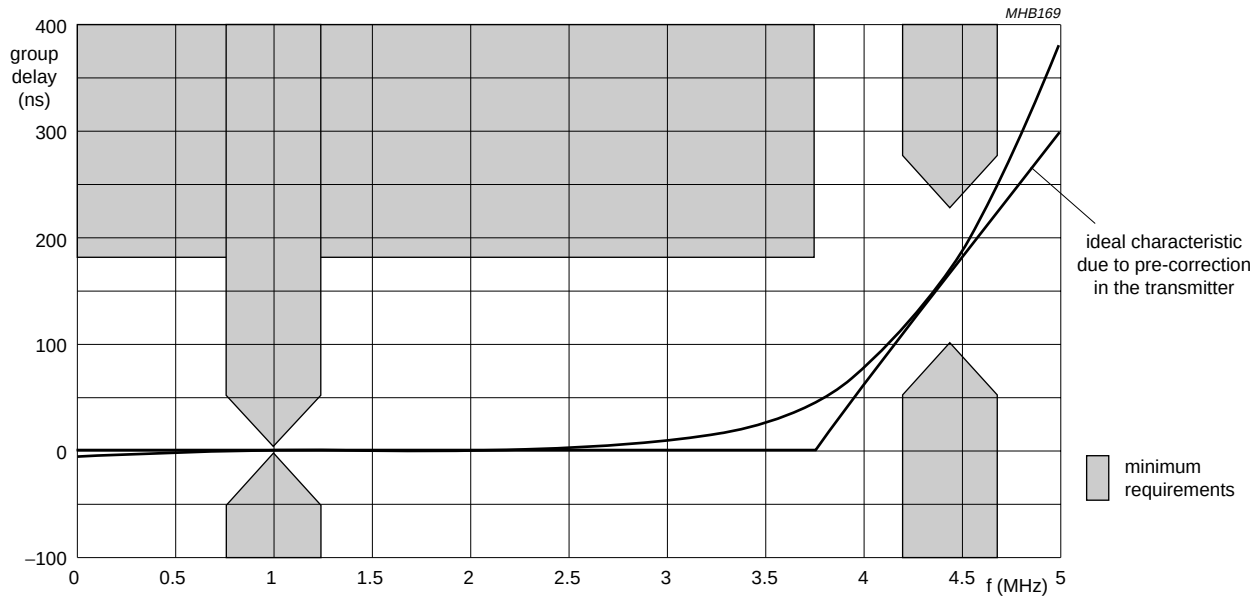


Fig.15 Typical amplitude response for sound trap at B/G standard.



Remark: Overall delay is not shown, here the maximum ripple is specified.

Fig.16 Typical group delay for sound trap at B/G standard.

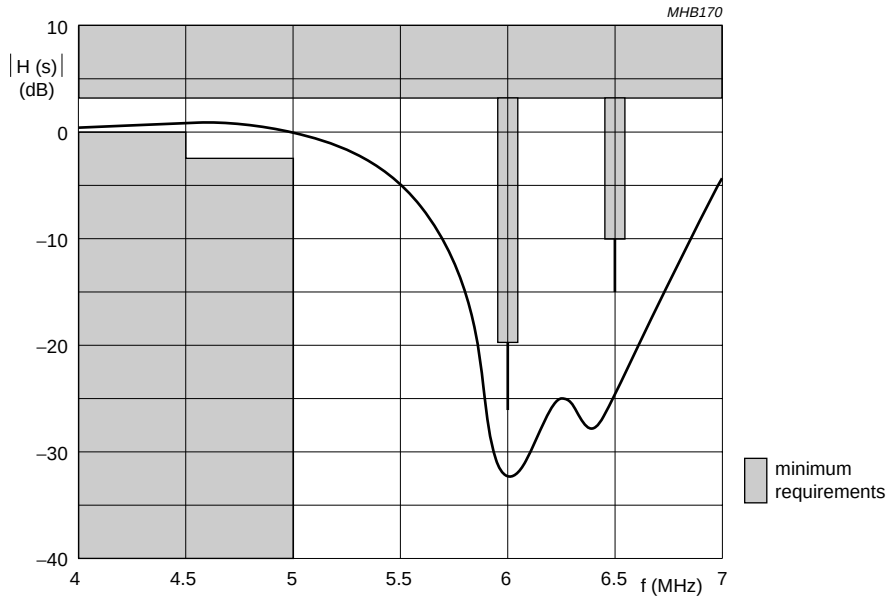


Fig.17 Typical amplitude response for sound trap at I standard.

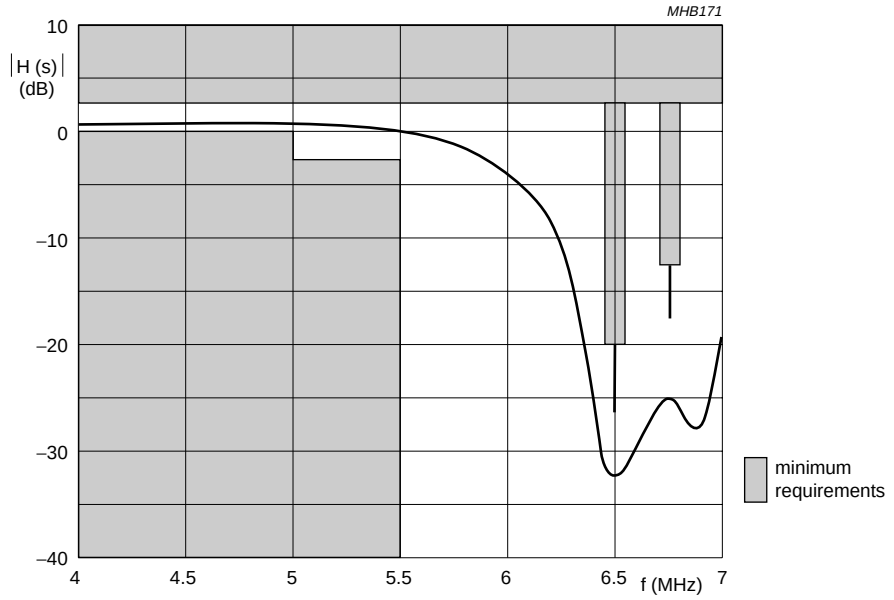


Fig.18 Typical amplitude response for sound trap at D/K standard.

TEST CIRCUIT

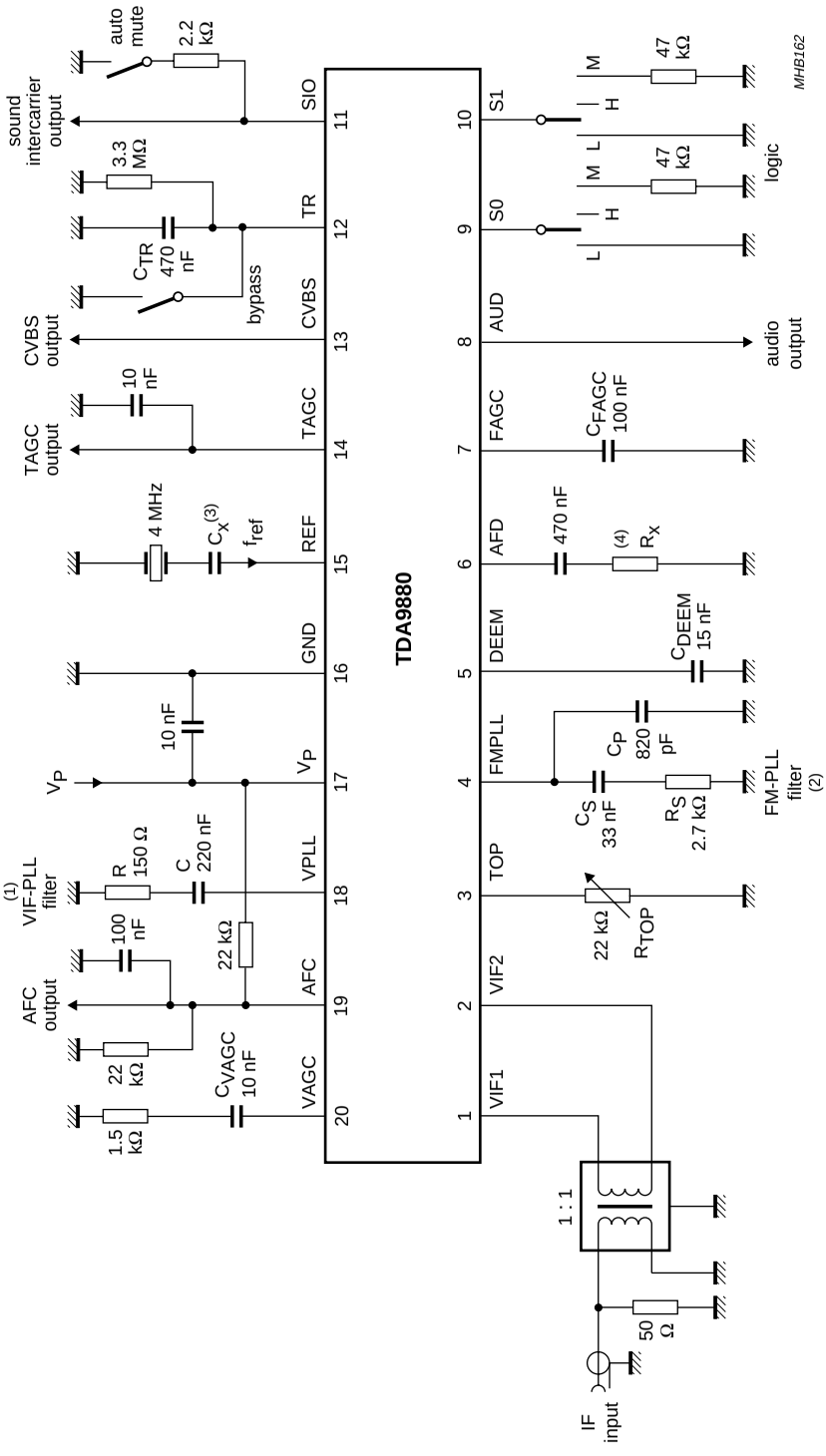


Fig.19 Test circuit.

(1) See note 4 of Chapter "Characteristics".
(2) See notes 17 and 18 of Chapter "Characteristics".
(3) See note 26 of Chapter "Characteristics".
(4) See note 22 of Chapter "Characteristics".

INTERNAL PIN CONFIGURATIONS

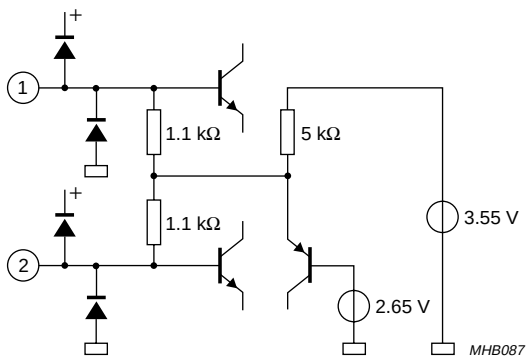


Fig.20 Pin 1 (VIF1) and pin 2 (VIF2).

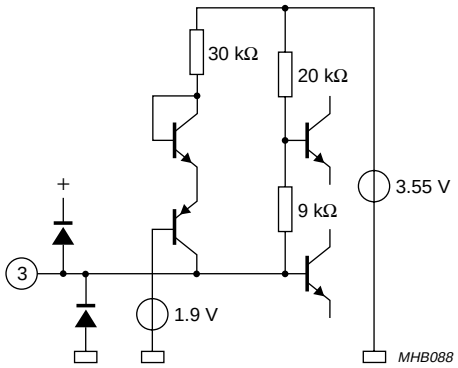


Fig.21 Pin 3 (TOP).

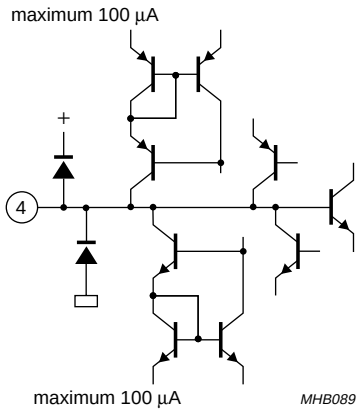


Fig.22 Pin 4 (FMPLL).

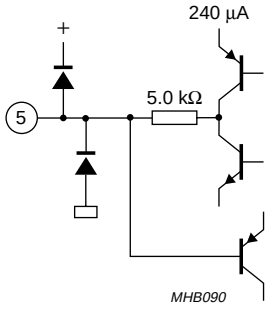


Fig.23 Pin 5 (DEEM).

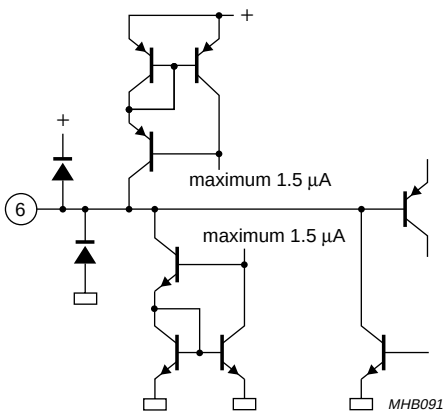


Fig.24 Pin 6 (AFD).

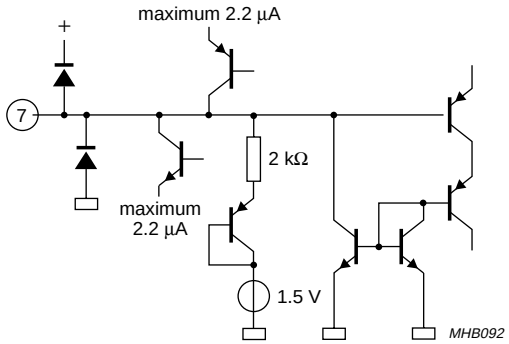


Fig.25 Pin 7 (FAGC).

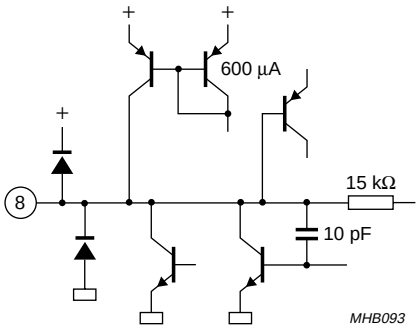


Fig.26 Pin 8 (AUD).

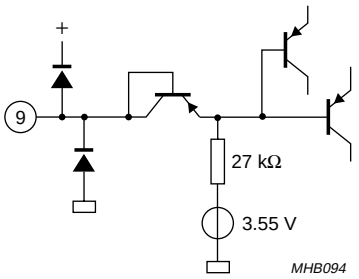


Fig.27 Pin 9 (S0).

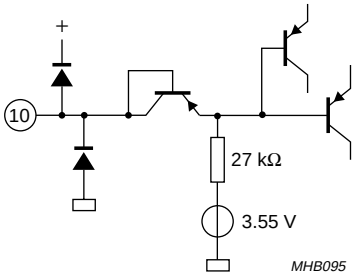


Fig.28 Pin 10 (S1).

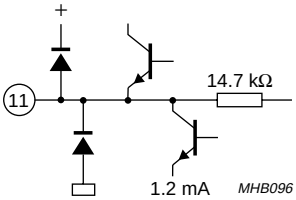


Fig.29 Pin 11 (SIO).

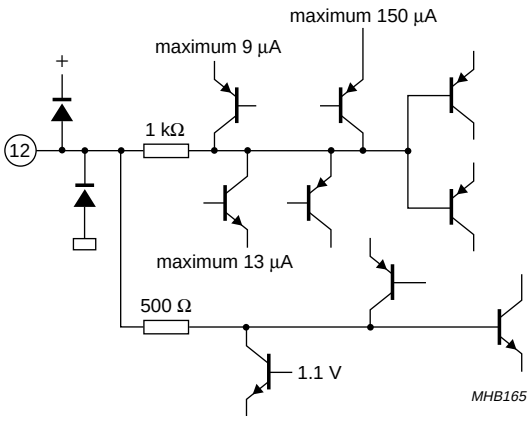


Fig.30 Pin 12 (TR).

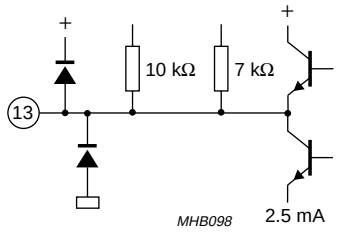


Fig.31 Pin 13 (CVBS).

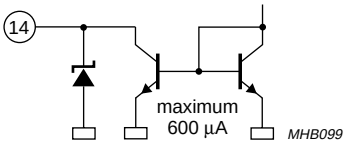


Fig.32 Pin 14 (TAGC).

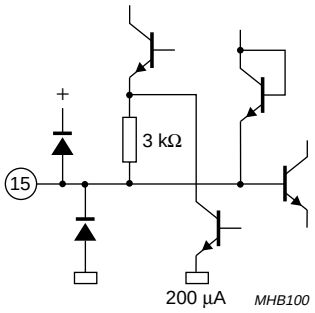


Fig.33 Pin 15 (REF).

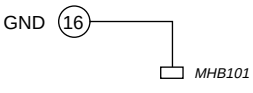


Fig.34 Pin 16 (GND).

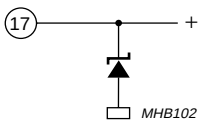


Fig.35 Pin 17 (V_P).

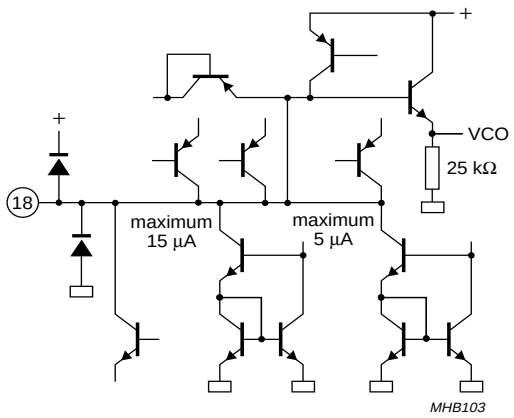


Fig.36 Pin 18 (VPLL).

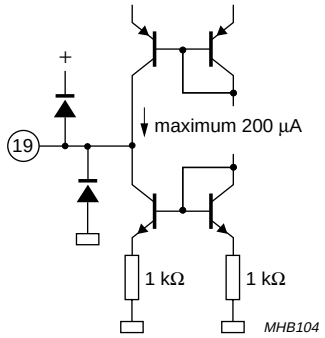


Fig.37 Pin 19 (AFC).

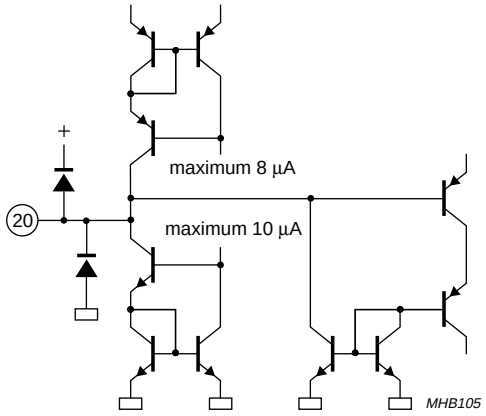
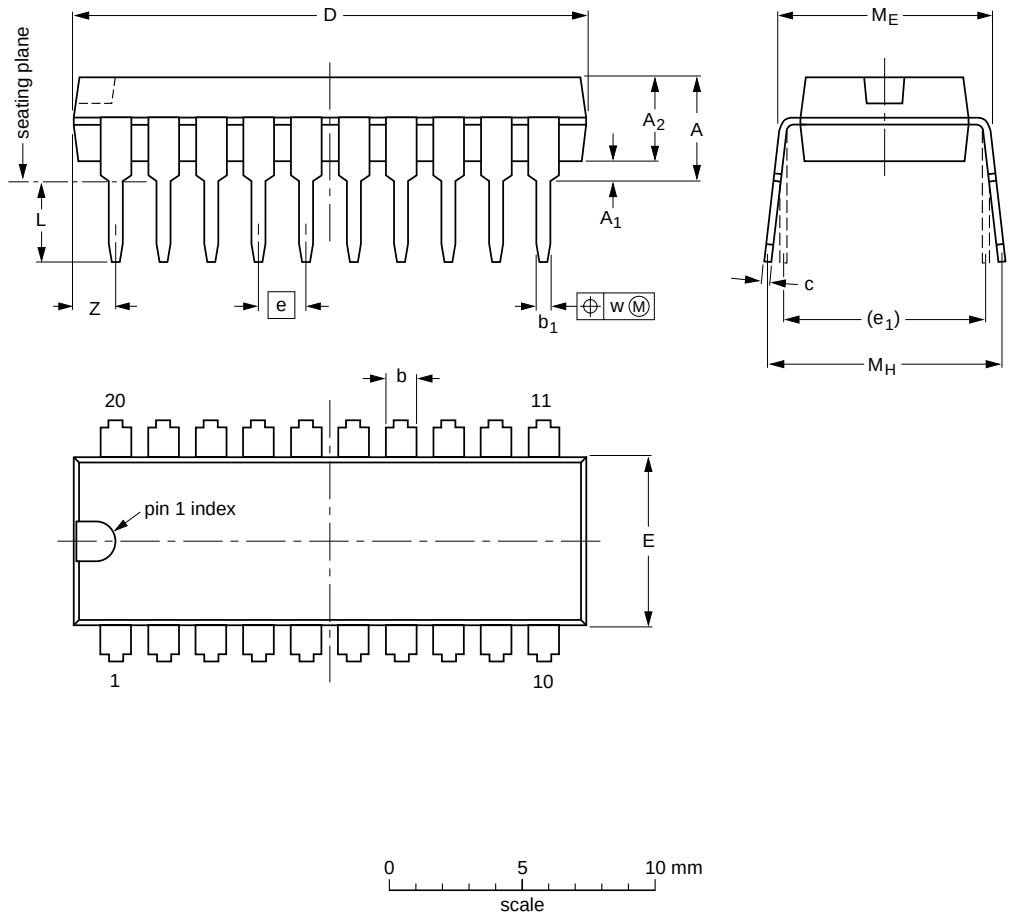


Fig.38 Pin 20 (VAGC).

PACKAGE OUTLINES

SDIP20: plastic shrink dual in-line package; 20 leads (300 mil) **SOT325-1**



DIMENSIONS (mm are the original dimensions)

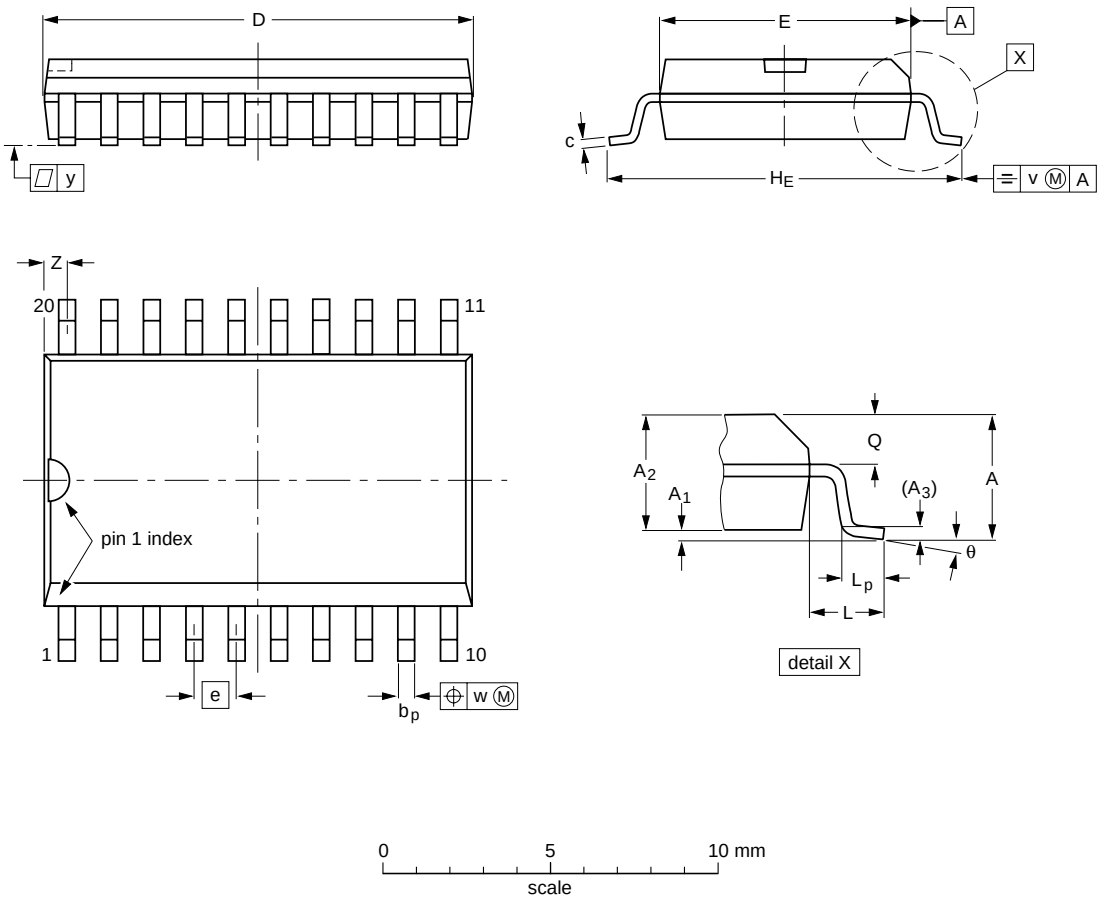
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.3 1.0	0.53 0.38	0.32 0.20	19.50 18.55	6.48 6.14	1.778	7.62	3.2 2.8	8.25 7.80	10.0 8.3	0.18	1.9

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT325-1						~~92-10-13~~ 95-02-04

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, SQFP	not suitable	suitable	–
	HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

© Philips Electronics N.V. 1999

SCA 67

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands 545004/03/pp40 Date of release: 1999 Jul 21 Document order number: 9397 750 05318

Let's make things better.

Philips Semiconductors

PHILIPS