# DATA SHEET

# TDA9176
## Luminance Transient Improvement (LTI) IC

Preliminary specification
Supersedes data of 1995 Jun 13
File under Integrated Circuits, IC02

1996 Jan 30

Philips
Semiconductors

PHILIPS

# Luminance Transient Improvement (LTI) IC TDA9176

## FEATURES

- Luminance transient improvement
- Line width control
- Can be used in 50 and 100 Hz environments (1FH and 2FH)
- Compensating chrominance delay
- YUV interface
- Black insertion or clamping are selectable
- Amplitude selection for optimum operation with 450 mV (p-p) and 1 $V_{bl\text{-}wh}$ luminance signals.

## GENERAL DESCRIPTION

The TDA9176 is a Luminance Transient Improvement (LTI) IC which is suitable for operation in both 50 and 100 Hz environments. The device can be used in conjunction with both LCD and CRT displays.

The TDA9176 also contains chrominance delay lines to compensate for the luminance delay. The device can be used as a low-power, cost effective alternative to (but also in combination with) Scan Velocity Modulation (SVM). The device operates at a supply voltage of 8 V. The device is contained in a 16 pin dual in-line package.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 7.2 | 8.0 | 8.8 | V |
| $I_{CC}$ | supply current | at 1FH | – | 24 | – | mA |
| | | at 2FH | – | 30 | – | mA |
| $V_{iY(\ p\text{-}p)}$ | Y input voltage (peak-to-peak value) | low amplitude mode | – | 0.45 | 0.63 | V |
| $V_{iY(bl\text{-}wh)}$ | Y input voltage (black-to-white) | high amplitude mode | – | 1.0 | 1.4 | V |
| $G_Y$ | Y path gain | | – | 1 | | |
| $V_{iU(p\text{-}p)}$ | U input voltage (peak-to-peak value) | | – | 1.33 | 1.90 | V |
| $V_{iV(p\text{-}p)}$ | V input voltage (peak-to-peak value) | | – | 1.05 | 1.50 | V |
| $G_{U.\ V}$ | U and V path gain | | – | 1 | – | |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA9176 | DIP16 | plastic dual in-line package; 16 leads (300 mil); long body | SOT38-1 |

## BLOCK DIAGRAM

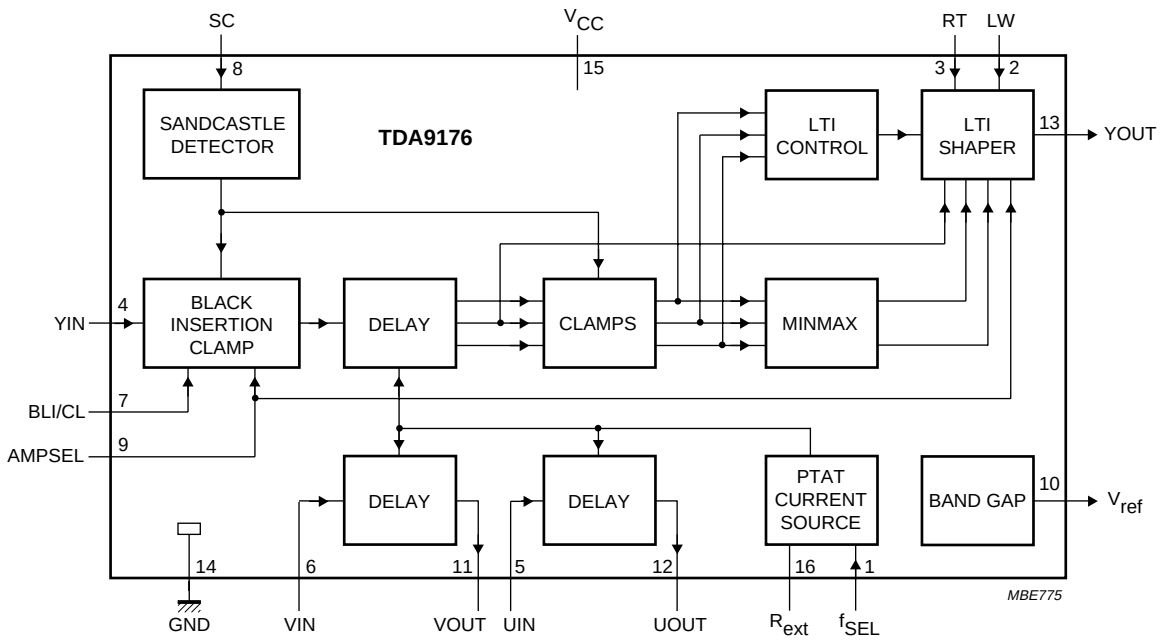



Fig.1 Block diagram.

**PINNING**

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $f_{SEL}$ | 1 | 1FH or 2FH mode selection |
| LW | 2 | vertical line width control input |
| RT | 3 | rise time control input |
| YIN | 4 | luminance signal input |
| UIN | 5 | U input (colour difference signal) |
| VIN | 6 | V input (colour difference signal) |
| BLI/CL | 7 | black level insertion/clamp mode selection |
| SC | 8 | synchronization input signal |
| AMPSEL | 9 | high/low amplitude luminance signal mode selection |
| $V_{ref}$ | 10 | internally generated reference voltage for line width control and rise time control |
| VOUT | 11 | V output (colour difference signal) |
| UOUT | 12 | U output (colour difference signal) |
| YOUT | 13 | luminance signal output |
| GND | 14 | ground (0 V) |
| $V_{CC}$ | 15 | supply voltage (+8 V) |
| $R_{ext}$ | 16 | external resistor for PTAT current source |

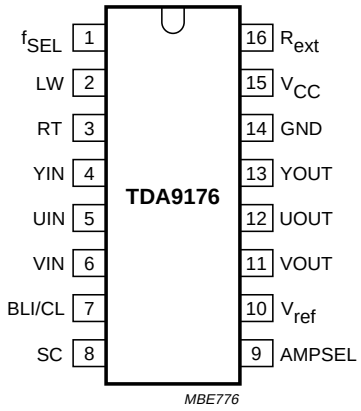



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

The TDA9176 is a Luminance Transient Improvement (LTI) IC which is suitable for operation in both 50 and 100 Hz environments. The IC also contains chrominance delay lines to compensate for the luminance delay. A diagram of the LTI processor is illustrated in Fig.3.

The LTI processor contains a delay line which drives a minimum/maximum (MINMAX) detector and a control circuit. When the control circuit discovers a transient, the LTI shaper switches from the minimum to the maximum signal (or vice-versa, depending on the sign of the transient). By mixing the original signal with the switched signal, a variable transient improvement is obtained. The 50% crossing point of the transient is not affected by the LTI circuit.

If the rise time improvement is active, the duty cycle of the output signal can be varied with the line width control input. This function delays the rising edge and advances the falling edge (or vice-versa). This can be used for example aperture correction. Figures 4 and 5 illustrate some waveforms of the LTI processor.

For correct operation the LTI circuit requires a number of fast clamps. To overcome problems where noise is superimposed on the input signal the device contains an input clamp that can either clamp to the black level of the input signal, or, insert a black level. When a black level is inserted, the internal clamps do not respond to the noise on the input signal (see Fig.1). When the input signal already has an inserted black level (e.g. when it is driven from the TDA9170 picture booster) it is recommended to set the device to the clamping mode. If no inserted black level is available on the input signal it is recommended to select the black insert mode of the input clamp.

The chrominance delay lines compensate for the delay of the luminance signal in the LTI circuit. This is to safeguard a correct colour fit.

Two and three level sandcastles can be used as a timing signal, only the clamp pulse of the sandcastle input is used in the device.

There are three selection inputs to select the modes of operation. These selections are as follows:

1. 1FH or 2FH, for the 50 or 100 Hz applications.
2. Amplitude selection, for optimum operation of the circuit with 450 mV (p-p) or 1 $V_{bl\text{-}wh}$ luminance signals.
3. Black insertion or clamping of the luminance signal.

The selection inputs must be directly connected to either ground or the supply rail. The modes are selected as follows:

Frequency selection: GND = 1FH mode, $V_{CC}$ = 2FH mode

Amplitude selection: GND = 450 mV (p-p), $V_{CC}$ = 1 $V_{bl\text{-}wh}$ mode

Black insertion/clamp: GND = clamp mode, $V_{CC}$ = black insert mode.

If the selection pins are left floating, internal 1 MΩ resistors connected to the pins set the device to, 1FH mode, black insert mode and 1 $V_{bl\text{-}wh}$ mode.

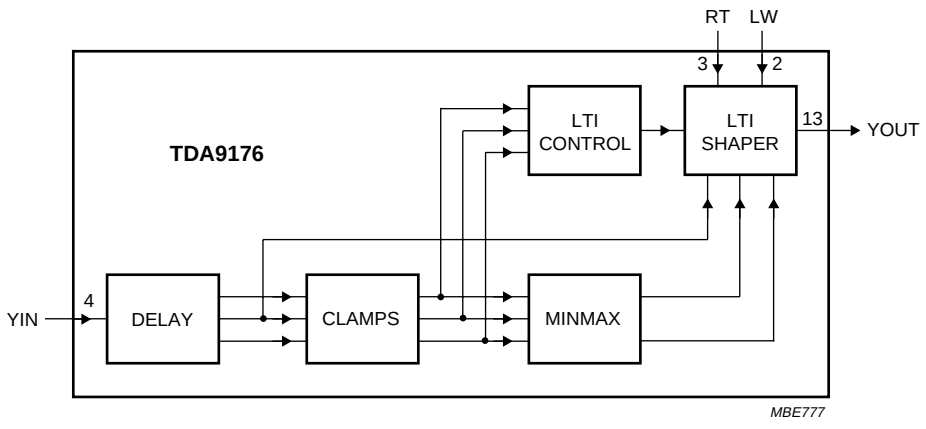



Fig.3 Block diagram of the LTI circuit.

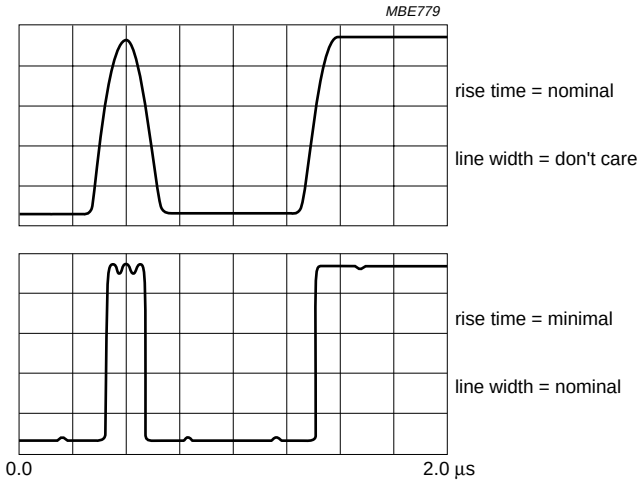



Fig.4 LTI waveforms for 2T pulse and step (1FH mode, rise time varied).

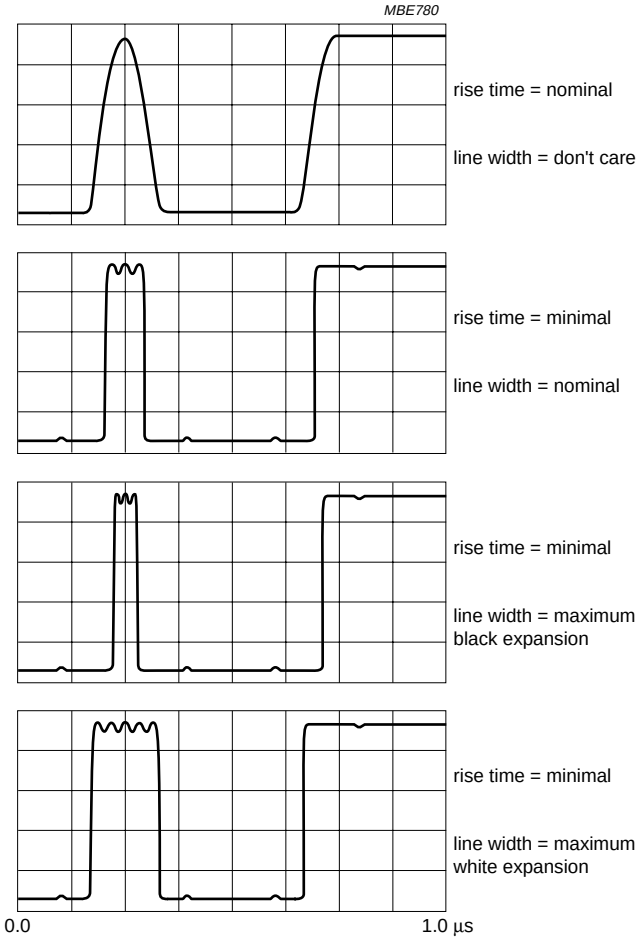



Fig.5 LTI waveforms for 2T pulse and step (2FH mode, line width varied).

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | – | – | 9.0 | V |
| $I_{CC}$ | supply current | | – | – | 35 | mA |
| $P_{tot}$ | total power dissipation | | – | – | 0.315 | W |
| $T_{stg}$ | storage temperature | | –55 | – | +150 | °C |
| $T_{amb}$ | operating ambient temperature | | –10 | – | +70 | °C |
| $V_{es}$ | electrostatic handling | note 1 | –3000 | – | +3000 | V |
| | | note 2 | –300 | – | +300 | V |

**Notes**

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (all pins).
2. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω resistor (all pins).

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th\ j\text{-}a}$ | thermal resistance from junction to ambient in free air | 69 | K/W |

## QUALITY SPECIFICATION

In accordance with SNW-FQ-611 part E. The numbers of the quality specification can be found in the *“Quality reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

## CHARACTERISTICS

$V_{CC}$ = 8 V; $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{CC}$ | supply voltage | | 7.2 | 8.0 | 8.8 | V |
| $I_{CC}$ | supply current | 1FH mode | – | 24 | – | mA |
| | | 2FH mode | – | 30 | – | mA |
| $P_{dis}$ | power dissipation | 1FH mode | – | 192 | – | mW |
| | | 2FH mode | – | 240 | – | mW |
| **Y channel;** note 1 | | | | | | |
| $V_{i(Y\ p-p)}$ | input voltage (peak-to-peak value) | LOW amplitude mode | – | 0.45 | 0.63 | V |
| $V_{iY(bl-wh)}$ | input voltage (black-to-white) | HIGH amplitude mode | – | 1.0 | 1.4 | V |
| $I_{i(Y)}$ | input current | | – | 0 | – | µA |
| $V_{BLos}$ | black offset voltage | black insert mode | – | – | 10 | mV |
| $V_{o(DC)}$ | DC output voltage level during clamping | low amplitude mode | – | 3.7 | – | V |
| | | high amplitude mode | – | 2.2 | – | V |
| $G_{(Y)}$ | gain | all modes | – | 1 | – | |
| $t_d$ | delay time | 1FH mode | – | 165 | – | ns |
| | | 2FH mode | – | 100 | – | ns |
| $V_{tr}$ | rise time control voltage | minimum rise time | 3.5 | – | 4.0 | V |
| | | nominal rise time | 0 | – | 0.5 | V |
| $V_{LW}$ | line width control voltage | normal width | – | 2.0 | – | V |
| | | maximum black expansion | 0 | – | 0.5 | V |
| | | maximum white expansion | 3.5 | – | 4.0 | V |
| $t_{r(min)}$ | minimum rise time | 1FH mode; note 2 | – | 20 | – | ns |
| | | 2FH mode; note 2 | – | 14 | – | ns |
| $\delta_{(min)}$ | minimum duty factor | $f_i$ = 2 MHz; line width minimum; maximum black expansion; note 3 | – | 33 | – | % |
| $\delta_{(max)}$ | maximum duty factor | $f_i$ = 2 MHz; line width maximum; maximum white expansion; note 3 | – | 67 | – | % |
| $B_Y$ | bandwidth | 1FH mode; nominal rise time; note 4 | 7 | – | – | MHz |
| | | 2FH mode; nominal rise time; note 4 | 14 | – | – | MHz |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **U and V channels** | | | | | | |
| $V_{iUV(p-p)}$ | input voltage (peak-to-peak value) | V channel | – | 1.05 | 1.50 | V |
| | | U channel | – | 1.33 | 1.90 | V |
| $I_{iUV}$ | input current | both channels | – | 0 | – | µA |
| $V_{oUV(DC)}$ | DC output voltage level during clamping | both channels | – | 3.0 | – | V |
| $G_{UV}$ | gain | both channels | – | 1 | – | |
| $t_{d(UV)}$ | delay time | 1FH mode | – | 165 | – | ns |
| | | 2FH mode | – | 100 | – | ns |
| $B_{UV}$ | bandwidth | both channels | 5 | – | – | MHz |
| **Sandcastle input** | | | | | | |
| $CL_{th}$ | clamping threshold | | – | $V_{top}$ – 0.6 | – | V |
| $V_{ripple}$ | allowed ripple on clamping pulse | | – | – | 0.4 | V |
| **Reference voltage** | | | | | | |
| $V_{ref(DC)}$ | DC reference voltage level | | – | 4.0 | – | V |
| $I_{source}$ | source current | note 5 | – | – | 1 | mA |

**Notes**

1. All data given is for a 3.0 kΩ external resistor connected to the PTAT current source (pin 16).
2. The test input is a step whose rising edge is the rising half of a sine wave. For the 1FH mode the input rise time is 250 ns (i.e. half of a 2 MHz sine wave). For the 2FH mode the input rise time is 125 ns (i.e. half of a 4 MHz sine wave). The output rise time is measured between the 10% and 90% points of the output signal.
3. The figures given on duty cycle variation refer to the following conditions: the device should be in 1FH mode (pin 1 at ground level) and the rise time should be at minimum (pin 3 connected to $V_{ref}$, pin 10).
4. In the transparent mode, i.e. at normal rise time, the bandwidth of the luminance path for which the group delay time constant is 7 MHz in the 1FH mode and 14 MHz in the 2FH mode. However, as the circuit uses all-pass filters, ringing on the output signal may occur if the bandwidth of the input signal is larger than 7 MHz in the 1FH mode or 14 MHz in the 2FH mode. As the LTI processor adds harmonics to the luminance signal, the bandwidth of the output signal is much larger than 14 MHz.
5. The maximum DC load on the reference voltage pin (pin 10) should not exceed 1 mA.

## TEST AND APPLICATION INFORMATION

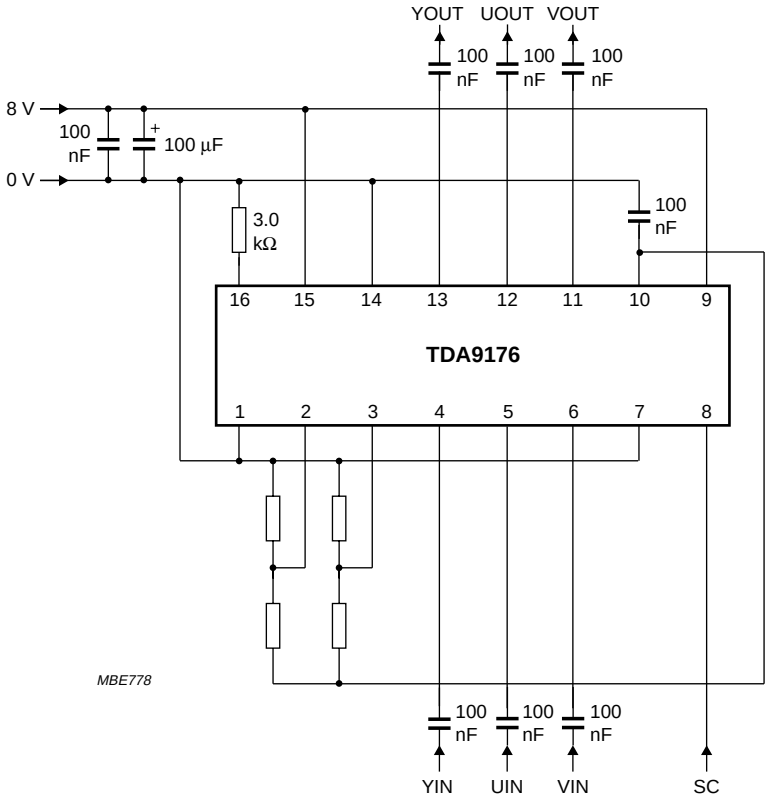



Fig.6 Application diagram for 50 Hz application with 1 $V_{bl\text{-}wh}$ input signal and luminance clamping.

**INPUT PIN CONFIGURATION**

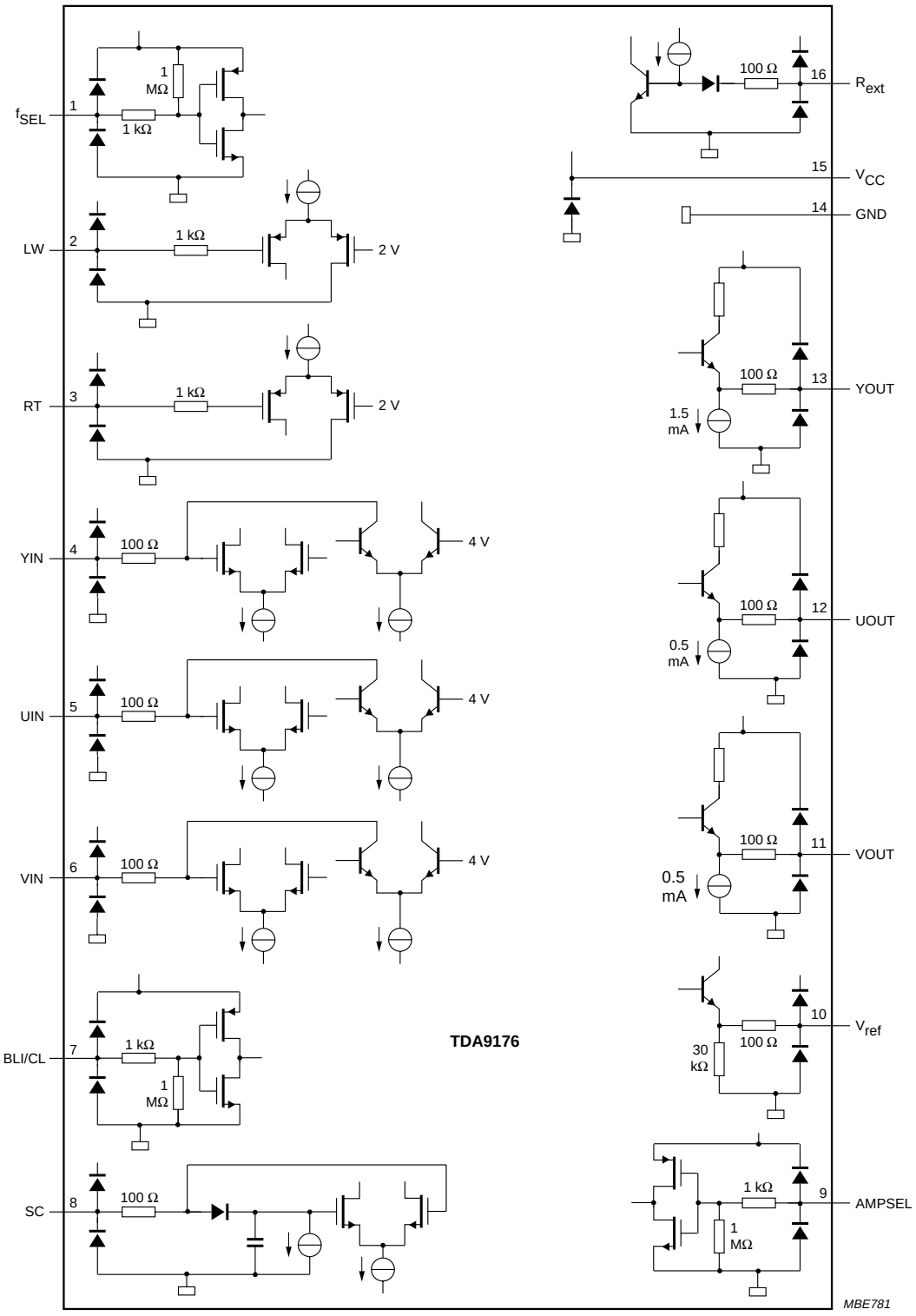
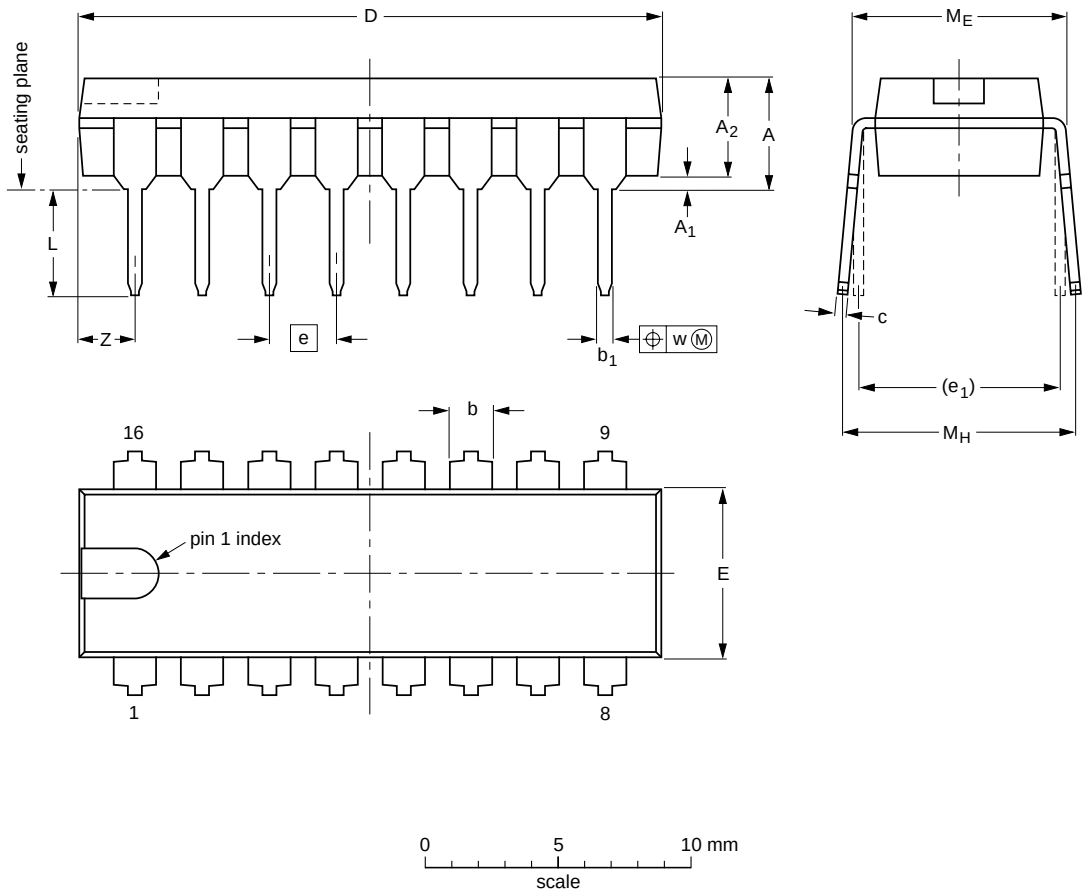



Fig.7 Input pin configuration.

## PACKAGE OUTLINE

**DIP16: plastic dual in-line package; 16 leads (300 mil); long body** **SOT38-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7 | 0.51 | 3.7 | 1.40<br>1.14 | 0.53<br>0.38 | 0.32<br>0.23 | 21.8<br>21.4 | 6.48<br>6.20 | 2.54 | 7.62 | 3.9<br>3.4 | 8.25<br>7.80 | 9.5<br>8.3 | 0.254 | 2.2 |
| inches | 0.19 | 0.020 | 0.15 | 0.055<br>0.045 | 0.021<br>0.015 | 0.013<br>0.009 | 0.86<br>0.84 | 0.26<br>0.24 | 0.10 | 0.30 | 0.15<br>0.13 | 0.32<br>0.31 | 0.37<br>0.33 | 0.01 | 0.087 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-1 | 050G09 | MO-001AE | | | | ~~92-10-02~~<br>95-01-19 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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