TDA8942P

2 x 1.5 W stereo Bridge Tied Load (BTL) audio amplifier

Rev. 02 — 14 March 2000 **Product specification**

1. General description

The TDA8942P is a dual-channel audio power amplifier for an output power of 2×1.5 W at a 16 Ω load and a 9 V supply. The circuit contains two Bridge Tied Load (BTL) amplifiers with an all-NPN output stage and standby/mute logic.
The TDA8942P comes in a 16-pin dual in-line (DIP) package.The TDA8942P is printed-circuit board (PCB) compatible with all other types in the TDA894x family. One PCB footprint accommodates both the mono and the stereo products.

2. Features

- Few external components
- Fixed gain
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Printed-circuit board compatible.

3. Applications

- Mains fed applications (e.g. TV sound)
- PC audio
- Portable audio.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		6	9	18	V
I_q	quiescent supply current	V_{CC} = 12 V; $R_L = \infty$	-	22	32	mA
I_{stb}	standby supply current		-	-	10	µA

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Table 1: Quick reference data...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	output power	THD = 10%; R_L = 16 Ω; V_{CC} = 9 V	1.2	1.5	-	W
THD	total harmonic distortion	P_o = 0.5 W	-	0.03	0.3	%
G_v	voltage gain		31	32	33	dB
SVRR	supply voltage ripple rejection		50	65	-	dB

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8942P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

6. Block diagram

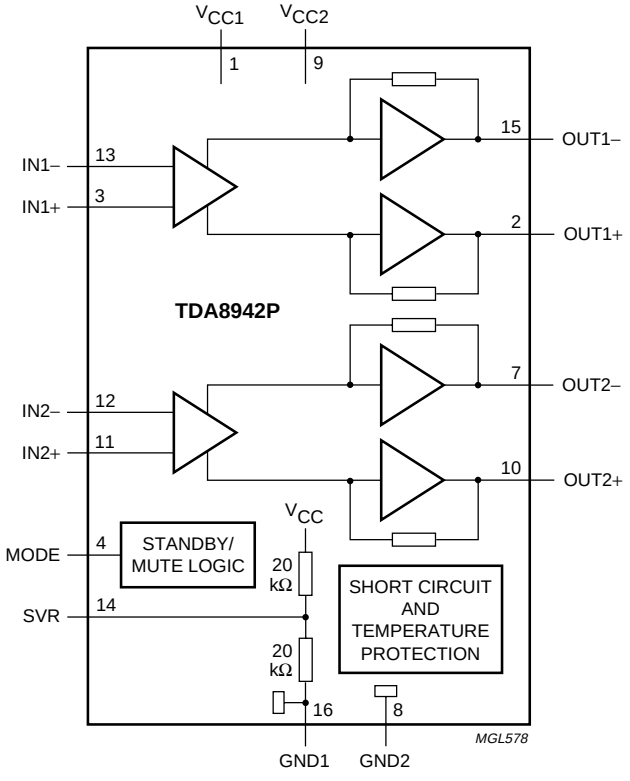


Fig 1. Block diagram.

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7. Pinning information

7.1 Pinning

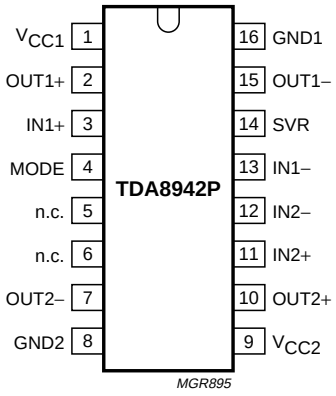


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
V_{CC1}	1	supply voltage channel 1
OUT1+	2	positive loudspeaker terminal 1
IN1+	3	positive input 1
MODE	4	mode selection input (standby, mute, operating)
n.c.	5	not connected
n.c.	6	not connected
OUT2–	7	negative loudspeaker terminal 2
GND2	8	ground channel 2
V_{CC2}	9	supply voltage channel 2
OUT2+	10	positive loudspeaker terminal 2
IN2+	11	positive input 2
IN2–	12	negative input 2
IN1–	13	negative input 1
SVR	14	half supply voltage decoupling (ripple rejection)
OUT1–	15	negative loudspeaker terminal 2
GND1	16	ground channel 1

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8. Functional description

The TDA8942P is a stereo BTL audio power amplifier capable of delivering 2 × 1.5 W output power to a 16 Ω load at THD = 10%, using a 9 V power supply. The voltage gain is fixed at 32 dB.

With the three-level MODE input the device can be switched from ‘standby’ to ‘mute’ and to ‘operating’ mode.

The TDA8942P outputs are protected by an internal thermal shutdown protection mechanism and a short-circuit protection.

8.1 Input configuration

The TDA8942P inputs can be driven symmetrical (floating) as well as asymmetrical. In the asymmetrical mode one input pin is connected via a capacitor to the signal ground which should be as close as possible to the SVR (electrolytic) capacitor ground. Note that the DC level of the input pins is half of the supply voltage V_{CC}, so coupling capacitors for both pins are necessary.

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(R_i \times C_i)} \quad (1)$$

For R_i = 45 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(45 \times 10^{3} \times 220 \times 10^{-9})} = 16\ \text{Hz} \quad (2)$$

As shown in Equation 1 and 2, large capacitor values for the inputs are not necessary; so the switch-on delay during charging of the input capacitors, can be minimized. This results in a good low frequency response and good switch-on behaviour.

Remark: To prevent HF oscillations do not leave the inputs open, connect a capacitor of at least 1.5 nF across the input pins close to the device.

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8.2 Power amplifier

The power amplifier is a Bridge Tied Load (BTL) amplifier with an all-NPN output stage, capable of delivering a peak output current of 2 A.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The ripple frequency on the supply voltage is twice the signal frequency
- No expensive DC-blocking capacitor
- Good low frequency performance.

8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10%; see Figure 8. The maximum output power is limited by the maximum power dissipation in the plastic dual in-line (DIP16) package.See also Section 14.2 on page 16.

8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom – compared to the average power output – for transferring the loudest parts without distortion. At V_{CC} = 9 V, R_L = 16 Ω and P_o = 1 W at THD = 1% (see Figure 6a), the Average Listening Level (ALL) – music power – without any distortion yields:

$P_{o(ALL)}$ = 1 W/15.85 = 63 mW.

The power dissipation can be derived from Figure 11 on page 11 for 0 dB respectively 12 dB headroom.

Table 4: Power rating as function of headroom

Headroom	Power output (THD = 0.1%)	Power dissipation (P)
0 dB	P_o = 1 W	2.35 W
12 dB	$P_{o(ALL)}$ = 63 mW	1.15 W

For the average listening level a power dissipation of 1.15 W can be used for calculation of the maximum ambient temperature $T_{amb(max)}$ (see Section 14.2).

8.3 Mode selection

The TDA8942P has three functional modes, which can be selected by applying the proper DC voltage to pin MODE. See Figure 4 and 5 for the respective DC levels, which depend on the supply voltage level. The MODE pin can be driven by a 3-state logic output stage: e.g. a microcontroller with additional components for DC-level shifting.

Standby — In this mode the current consumption is very low and the outputs are floating. The device is in standby mode when (V_{CC} – 0.5 V) < V_{MODE} < V_{CC}, or when the MODE pin is left floating (high impedance). The power consumption of the TDA8942P will be reduced to <0.18 mW.

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Mute — In this mode the amplifier is DC-biased but not operational (no audio output); the DC level of the input and output pins remain on half the supply voltage. This allows the input coupling and Supply Voltage Ripple Rejection (SVRR) capacitors to be charged to avoid pop-noise. The device is in mute mode when $3\ V < V_{MODE} < (V_{CC} - 1.5\ V)$.

Operating — In this mode the amplifier is operating normally. The operating mode is activated at $V_{MODE} < 0.5\ V$.

8.3.1 Switch-on and switch-off

To avoid audible plops during supply voltage switch-on or switch-off, the device is set to standby mode before the supply voltage is applied (switch-on) or removed (switch-off).

The switch-on and switch-off time can be influenced by an RC-circuit on the MODE pin. Rapid on/off switching of the device or the MODE pin may cause ‘click- and pop-noise’. This can be prevented by proper timing of the RC-circuit on the MODE pin.

8.4 Supply Voltage Ripple Rejection (SVRR)

The SVRR is measured with an electrolytic capacitor of 10 μF on pin SVR at a bandwidth of 10 Hz to 80 kHz. Figure 13 on page 12 illustrates the SVRR as function of the frequency. A larger capacitor value on the SVR pin improves the ripple rejection behaviour at the lower frequencies.

8.5 Built-in protection circuits

The TDA8942P contains two types of protection circuits, i.e. short-circuit and thermal shutdown.

8.5.1 Short-circuit protection

Short-circuit to ground or supply line — This is detected by a so-called ‘missing current’ detection circuit which measures the current in the positive supply line and the current in the ground line. A difference between both currents larger than 0.4 A, switches the power stage to standby mode (high impedance).

Short-circuit across the load — This is detected by an absolute-current measurement. An absolute-current larger than 2 A, switches the power stage to standby mode (high impedance).

8.5.2 Thermal shutdown protection

The junction temperature is measured by a temperature sensor; at a junction temperature of approximately 150 °C this detection circuit switches the power stage to standby mode (high impedance).

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9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	no signal	–0.3	+25	V
		operating	–0.3	+18	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		-	2	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
P_{tot}	total power dissipation		-	2.2	W
$V_{CC(sc)}$	supply voltage to guarantee short-circuit protection		-	12	V

10. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	57	K/W

11. Static characteristics

Table 7: Static characteristics

V_{CC} = 12 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; V_i = 0 V; measured in test circuit Figure 14; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		6	9	18	V
I_q	quiescent supply current	R_L = ∞	[1]	-	22	32	mA
I_{stb}	standby supply current	V_{MODE} = V_{CC}		-	-	10	µA
V_O	DC output voltage		[2]	-	4.5	-	V
ΔV_{OUT}	[3] differential output voltage offset			-	-	200	mV
V_{MODE}	mode selection input voltage	operating mode		0	-	0.5	V
		mute mode		3	-	V_{CC} – 1.5	V
		standby mode		V_{CC} – 0.5	-	V_{CC}	V
I_{MODE}	mode selection input current	0 < V_{MODE} < V_{CC}		-	-	20	µA

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the differential output voltage offset (ΔV_{OUT}) divided by the load resistance (R_L).

[2] The DC output voltage with respect to ground is approximately 0.5V_{CC}.

[3] $\Delta V_{OUT} = |V_{OUT+} - V_{OUT-}|$

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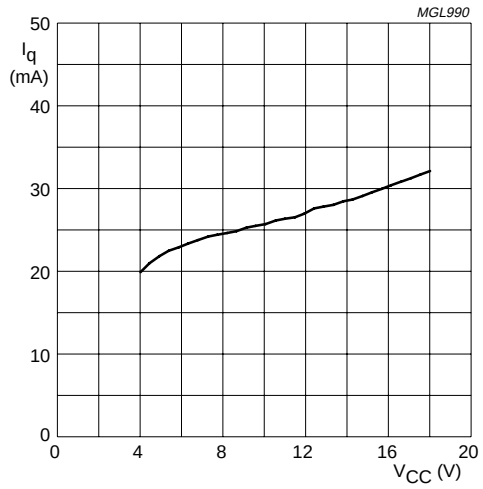


Fig 3. Quiescent supply current as function of supply voltage.

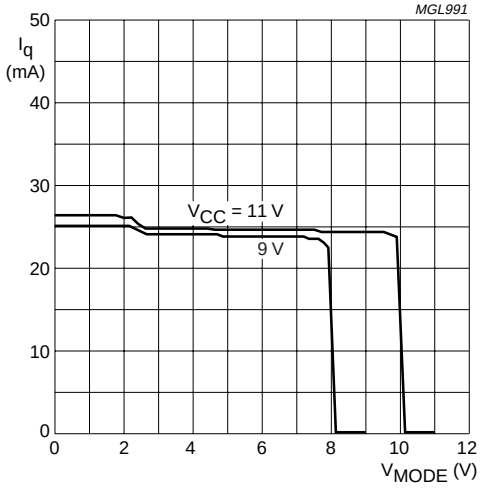


Fig 4. Quiescent supply current as function of mode voltage.

12. Dynamic characteristics

Table 8: Dynamic characteristics

V_{CC} = 12 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; measured in test circuit Figure 14; audio pass band 22 Hz to 22 kHz; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD = 10%		1.2	1.5	-	W
		THD = 0.5%		0.8	1	-	W
THD	total harmonic distortion	P_o = 0.5 W		-	0.03	0.3	%
G_v	voltage gain			31	32	33	dB
$Z_{i(dif)}$	differential input impedance			70	90	110	kΩ
$V_{n(o)}$	noise output voltage		[1]	-	90	120	μV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	50	65	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	60	-	dB
$V_{o(mute)}$	output voltage	mute mode	[3]	-	-	50	μV
α_{cs}	channel separation	R_S = 0 Ω		50	75	-	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance R_S = 0 Ω at the input.

[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 700 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with an input voltage of 1 V (RMS) in a bandwidth of 20 kHz, so including noise.

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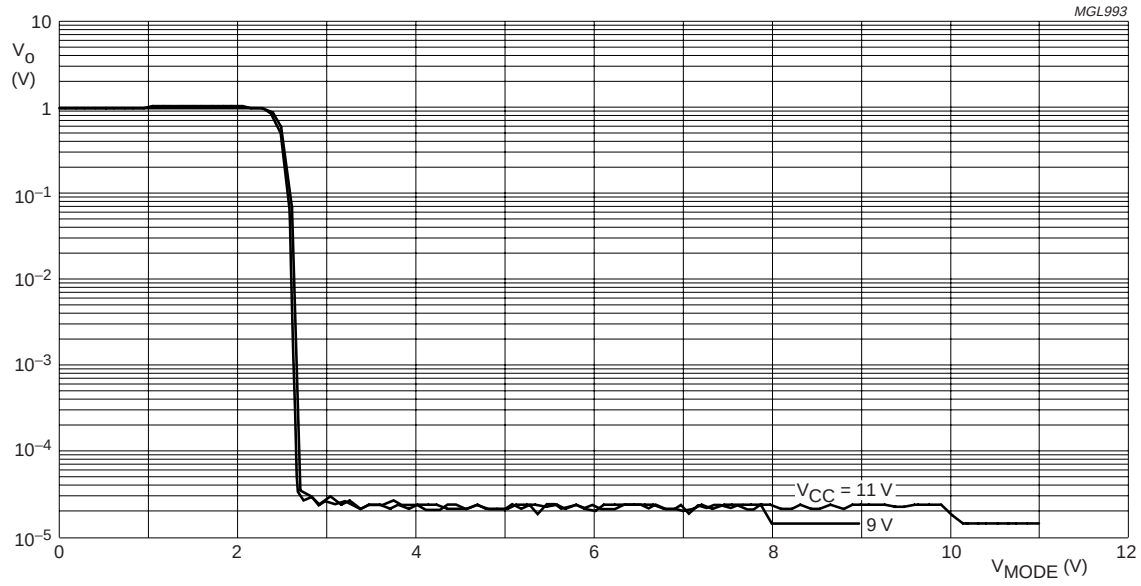
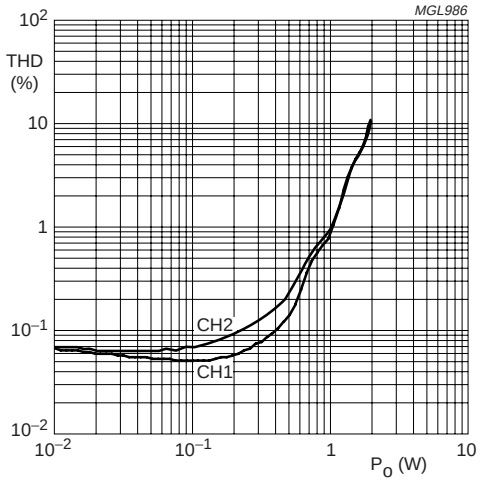
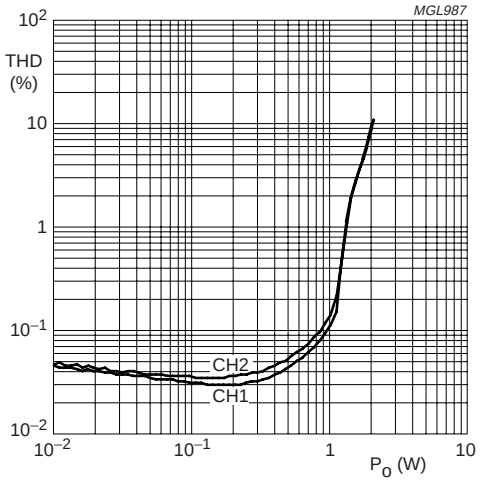


Fig 5. Output voltage as function of mode voltage.



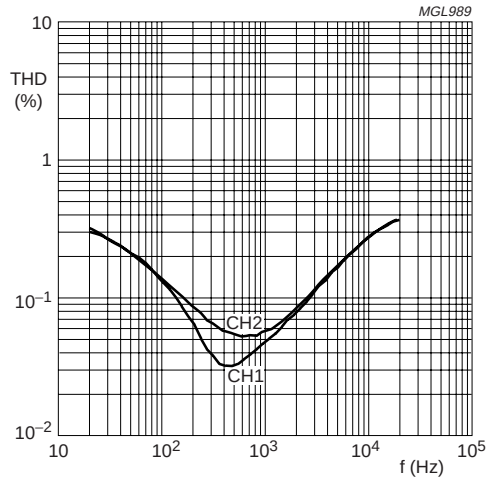
a. V_{CC} = 9 V; R_L = 16 Ω; f = 1 kHz.



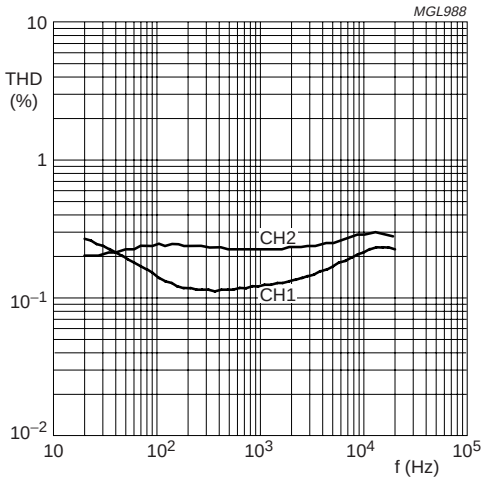
b. V_{CC} = 11 V; R_L = 25 Ω; f = 1 kHz.

Fig 6. Total harmonic distortion as function of output power.

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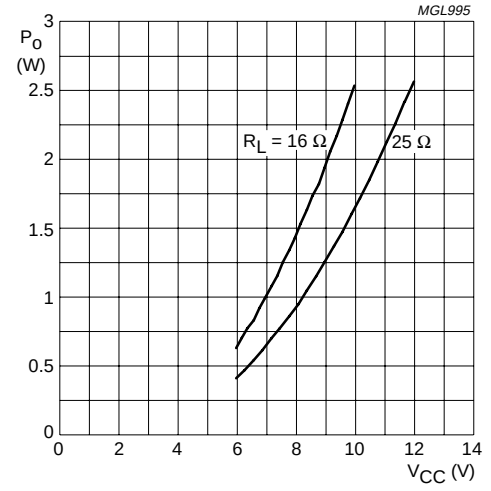
a. V_{CC} = 9 V; R_L = 16 Ω; P_o = 0.1 W.



b. V_{CC} = 9 V; R_L = 16 Ω; P_o = 0.5 W.

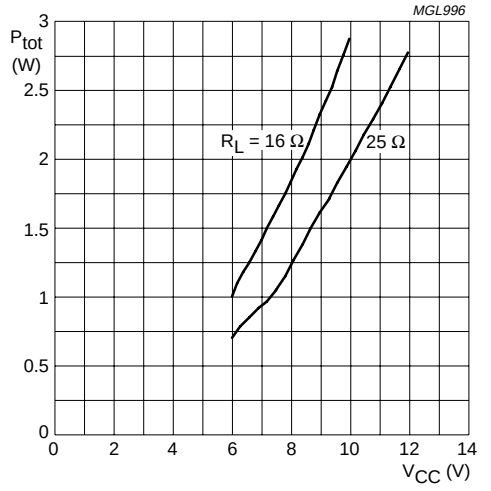
No bandpass filter applied.

Fig 7. Total harmonic distortion as function of frequency.



THD = 10%; f = 1 kHz.

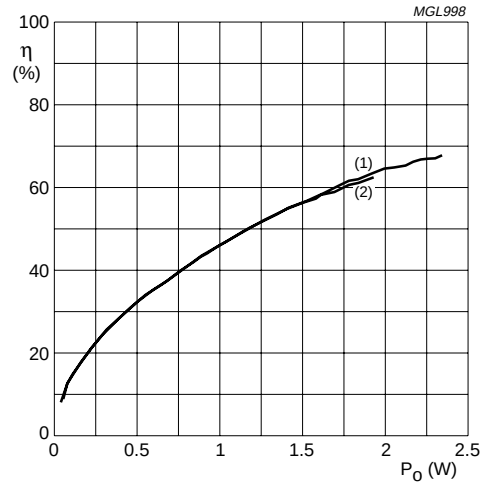
Fig 8. Output power as function of supply voltage.



f = 1 kHz.

Fig 9. Total power dissipation as function of supply voltage.

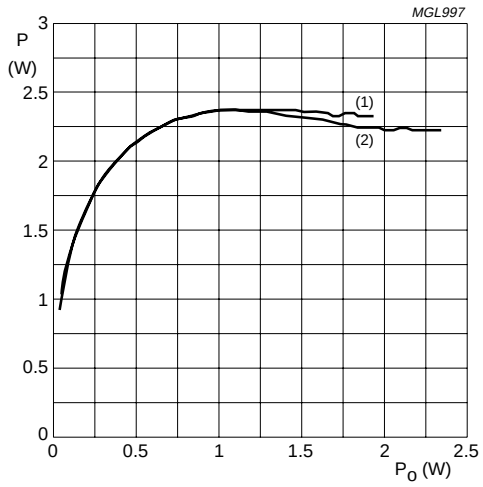
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(1) V_{CC} = 9 V.

(2) V_{CC} = 11 V.

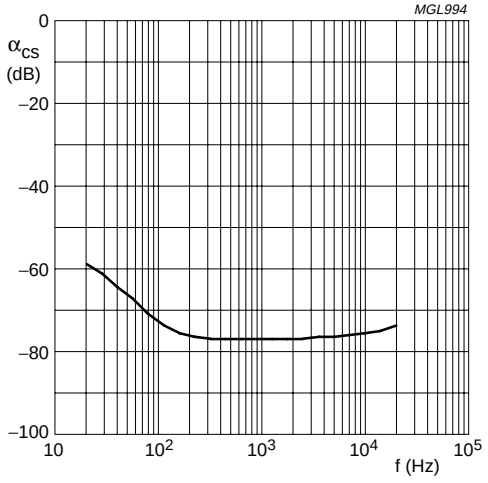
Fig 10. Efficiency as function of output power.



(1) V_{CC} = 9 V; R_L = 16 Ω.

(2) V_{CC} = 11 V; R_L = 25 Ω.

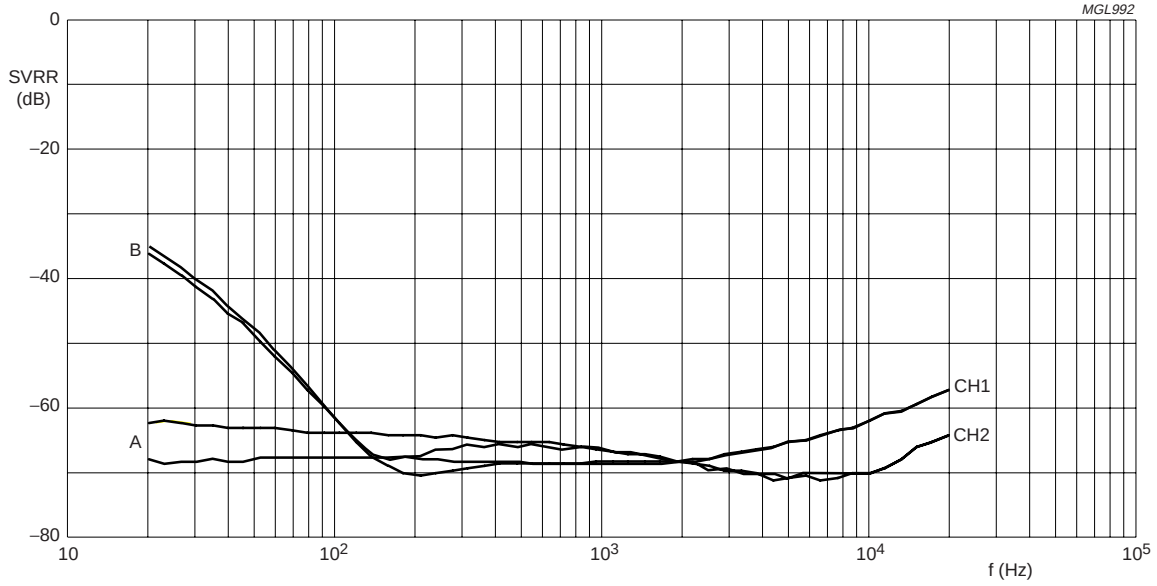
Fig 11. Power dissipation as function of output power.



No bandpass filter applied.

Fig 12. Channel separation as function of frequency.

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V_{CC} = 9 V; R_S = 0 Ω; V_{ripple} = 700 mV (RMS); no bandpass filter applied.

Curves A: inputs short-circuited

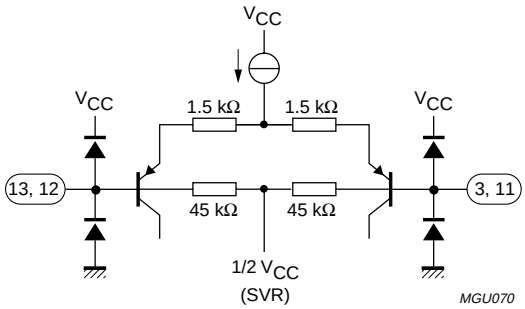
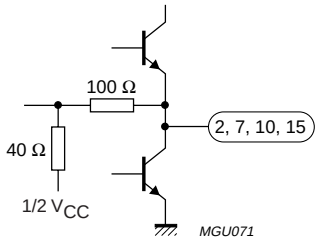
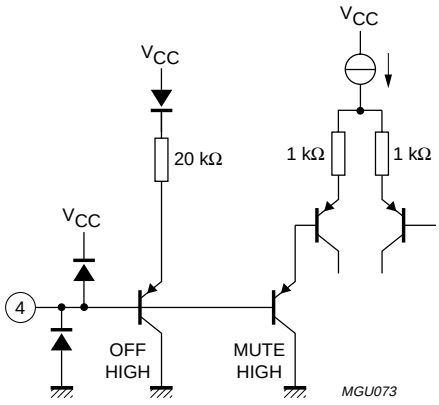
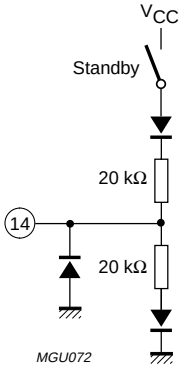
Curves B: inputs short-circuited and connected to ground (asymmetrical application)

Fig 13. Supply voltage ripple rejection as function of frequency.

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13. Internal circuitry

Table 9: Internal circuitry

Pin	Symbol	Equivalent circuit
3 and 13	IN1+ and IN1–	
11 and 12	IN2+ and IN2–	
15 and 2	OUT1– and OUT1+	
7 and 10	OUT2– and OUT2+	
4	MODE	
14	SVR	

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14. Application information

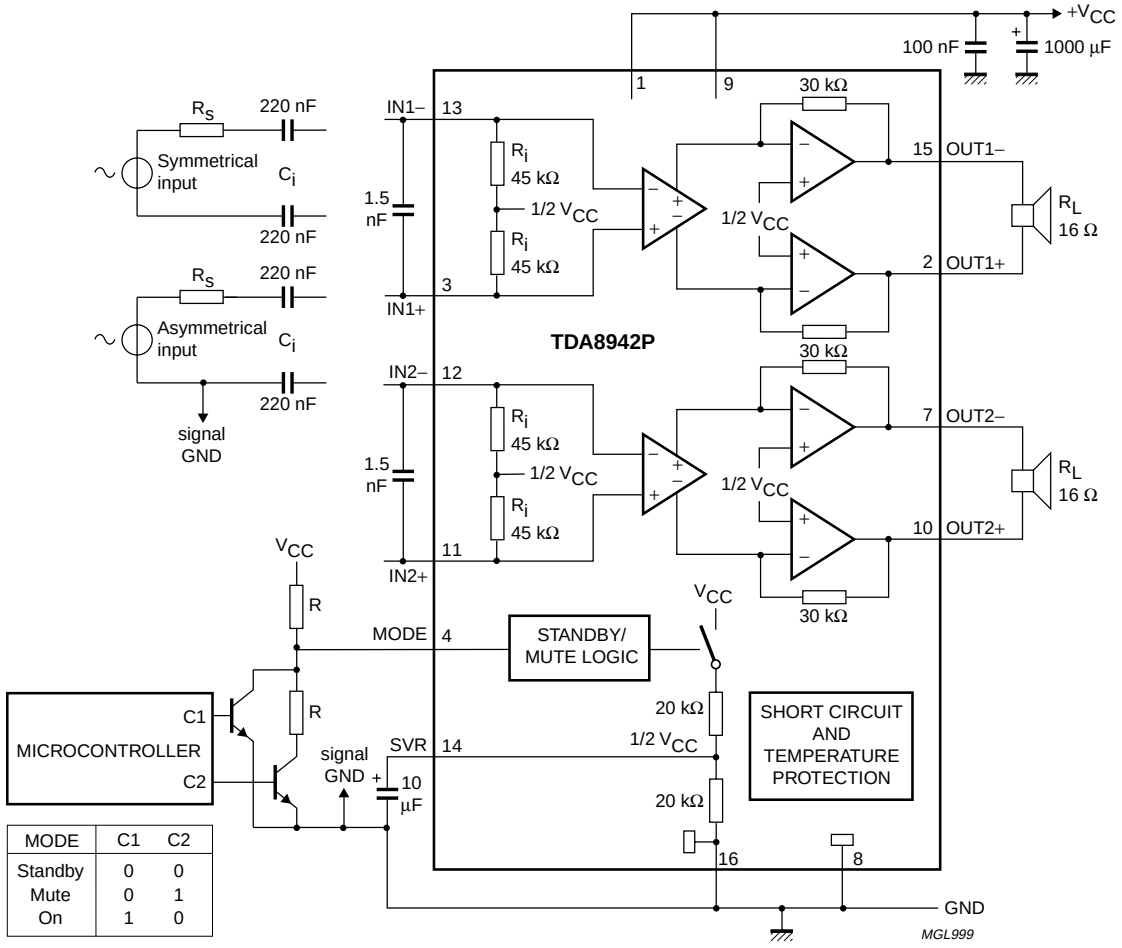


Fig 14. Application diagram.

14.1 Printed-circuit board (PCB)

14.1.1 Layout and grounding

For a high system performance level certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals.

The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

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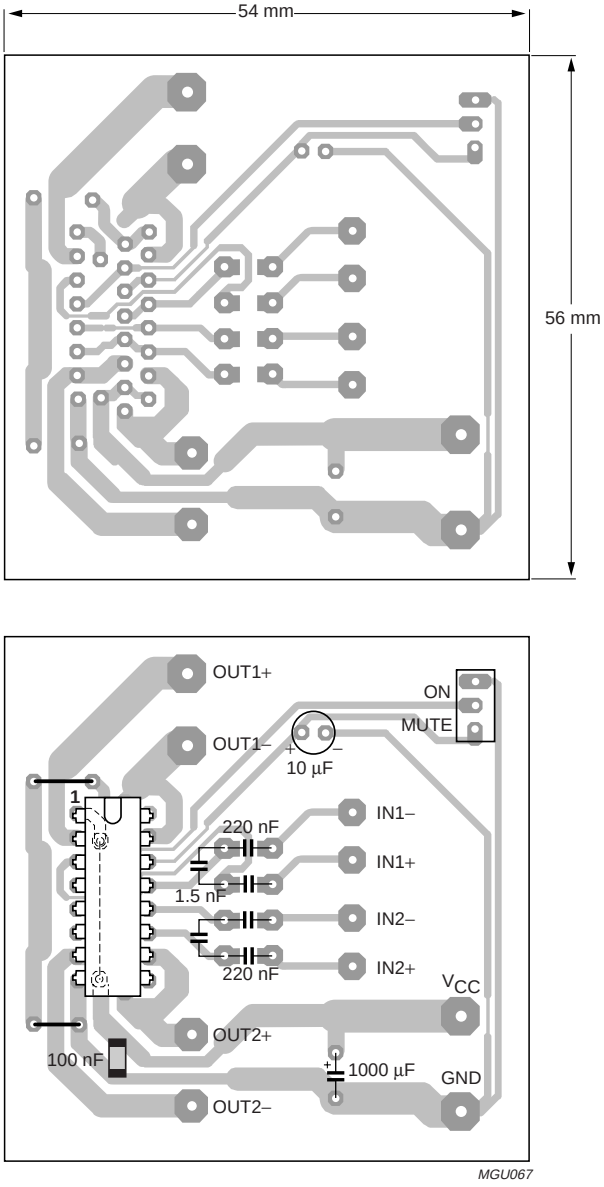


Fig 15. Printed-circuit board layout (single-sided); components view.

14.1.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor locations should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR – typical 100 nF – has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor – e.g. 1000 µF or greater – must be placed close to the device.

The bypass capacitor on the SVR pin reduces the noise and ripple on the midrail voltage. For good THD and noise performance a low ESR capacitor is recommended.

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14.2 Thermal behaviour and $T_{amb(max)}$ calculation

The measured maximum thermal resistance of the IC package, $R_{th(j-a)}$ is 57 K/W. A calculation for the maximum ambient temperature can be made, with the following parameters:

V_{CC} = 9 V and R_L = 16 Ω

$T_{j(max)}$ = 150 °C.

$R_{th(tot)}$ is the total thermal resistance between the junction and the ambient.

At V_{CC} = 9 V and R_L = 16 Ω the measured worst-case sine-wave dissipation is 2.35 W; see Figure 11. For $T_{j(max)}$ = 150 °C the maximum ambient temperature is:

$$T_{amb(max)} = 150 - 2.35 \times 57 = 16 \text{ °C}$$

The calculation above is for an application at worst-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation (see Section 8.2.2). For $T_{j(max)}$ = 150 °C the maximum ambient temperature is:

$$T_{amb(max)} = 150 - 1.15 \times 57 = 84.5 \text{ °C}$$

To increase the lifetime of the IC, $T_{j(max)}$ should be reduced to 125 °C. This results in:

$$T_{amb(max)} = 125 - 1.15 \times 57 = 59.5 \text{ °C}$$

15. Test information

15.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611D* is applicable.

15.2 Test conditions

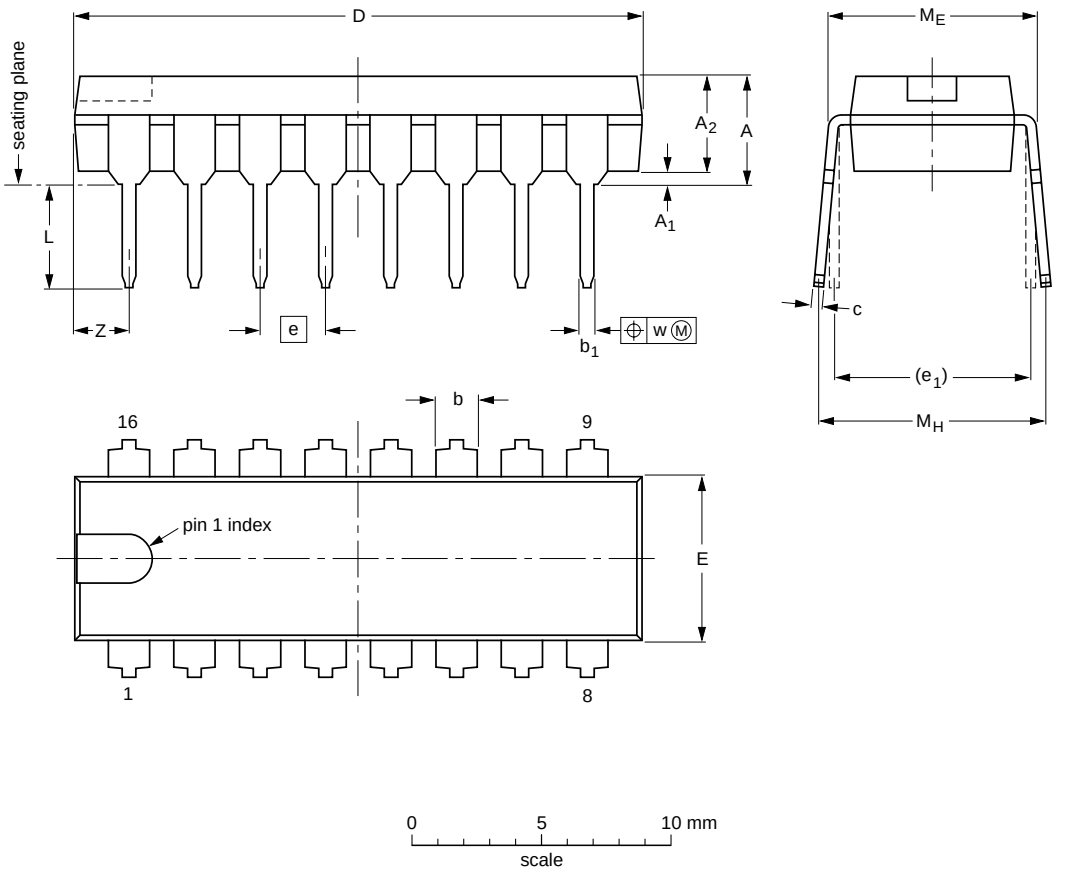
T_{amb} = 25 °C; V_{CC} = 9 V; f = 1 kHz; R_L = 16 Ω; audio pass band 22 Hz to 22 kHz; unless otherwise specified.

Remark: In the graphs as function of frequency no bandpass filter was applied; see Figure 7, 12 and 13.

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16. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001	SC-503-16			~~95-01-19~~ 99-12-27

Fig 16. DIP16 package outline.

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17. Soldering

17.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

17.4 Package related soldering information

Table 10: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable [1]

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

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18. Revision history

Table 11: Revision history

Rev	Date	CPCN	Description
02	20000314	-	**Product specification; second version; supersedes initial version TDA8942P-01 of 14 April 1999 (9397 750 04879). Modifications:** • Table 1 on page 1:THD: Max value 0.1% changed to → 0.3%; SVRR: Typ value 65 dB → added • Ordering options removed • Figure 1 on page 2: Block diagram; pin numbers changed OUT2– → 7 and OUT2+ → 10 • Figure 2 on page 3: Pin configuration; pin numbers changed OUT2– → 7 and OUT2+ → 10 • Table 3 on page 3: Pin description; pin numbers changed OUT2– → 7 and OUT2+ → 10 • Section 8 “Functional description”: – Section 8.1 “Input configuration” on page 4 → added. – Section 8.2 “Power amplifier” on page 5: ....., capable of delivering a peak output current of 1.5 A → changed to 2 A. – Section 8.2.1 “Output power measurement” on page 5 → added – Section 8.2.2 “Headroom” on page 5 → added • Section 8.3 “Mode selection”: – Standby mode: $V_{MODE} > (V_{CC} - 0.5\ V)$ → changed to $(V_{CC} - 0.5\ V) < V_{MODE} < V_{CC}$; The power consumption of the TDA8942P will be reduced to <0.18 mW → added. – Mute mode: the DC level of the input and output pins remain on half the supply voltage → added; – $2.5\ V < V_{MODE} < (V_{CC} - 1.5\ V)$ → changed to $3\ V < V_{MODE} < (V_{CC} - 1.5\ V)$ – Section 8.3.1 “Switch-on and switch-off” on page 6 → added. • Section 8.4 “Supply Voltage Ripple Rejection (SVRR)” on page 6 → added • Section 8.5 “Built-in protection circuits” on page 6 → added • Table 5 on page 7: – P_{tot} value added 2.2 W – $V_{CC(sc)}$ value added 12 V • Table 6 on page 7: $R_{th(j-a)}$ value 55 K/W changed to → 57 K/W • Table 7 on page 7: V_{MODE} - mute mode - value Min 2.5 → changed to 3 V • Table 8 on page 8: – THD: Max value 0.1% changed to → 0.3% – SVRR; Typ values 65 and 60 dB → added – α_{cs}; Typ value 75 dB → added – R_{source} changed to → R_S in table and associated table notes; Value added $R_S = 0\ \Omega$; – Table note [2]: .... 100 mV (RMS).... changed to → ... 700 mV (RMS).... • Figure 3 to 13: figures added • Section 13 “Internal circuitry” on page 13: → added • Figure 14: figure modified

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Table 11: Revision history *…continued*

Rev	Date	CPCN	Description
02	20000314	-	**Modifications:** • Section 14.1 “Printed-circuit board (PCB)” on page 14: → added • Figure 15: figure added • Section 14.2 “Thermal behaviour and $T_{amb(max)}$ calculation” on page 16: → added • Section 15 “Test information” on page 16: Section 15.1 → updated • Section 15.2 “Test conditions” on page 16: → added.
01	19990414	-	**Preliminary specification; initial version.**

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19. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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