DATA SHEET

TDA8753A
YUV 8-bit analog-to-digital interface

Product specification
Supersedes data of 1995 Mar 22
File under Integrated Circuits, IC02

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Philips
Semiconductors

PHILIPS

YUV 8-bit analog-to-digital interface TDA8753A

FEATURES

- Triple analog-to-digital converter
- 8-bit resolution
- Sampling rate up to 20 MHz
- Power dissipation of 500 mW (typical)
- Internal clamp functions
- 4 : 1 : 1 output data encoder
- Y binary output
- U, V two's complement outputs
- Sample rate converter permits programmable horizontal compression factors from 1 to 2
- Serial microcontroller interface
- TTL compatible inputs.

APPLICATIONS

- High-speed analog-to-digital conversion for video signal digitizing in 4 : 1 : 1 format
- 100 Hz improved definition TV for all formats (4/3, 16/9, 14/9 etc.).

GENERAL DESCRIPTION

The TDA8753A is a monolithic CMOS 8-bit video low-power analog-to-digital conversion interface for YUV signals. It converts the YUV analog input signal into 8-bit binary coded digital words in format 4 : 1 : 1 at a sampling rate of 20 MHz. All analog signal inputs are clamped. The device includes a digital sample rate converter for variable compression with a factor 1 to 2.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		4.75	5.0	5.25	V
I_{DDA}	analog supply current		–	55	63	mA
I_{DDD}	digital supply current		–	45	55	mA
INL	integral non-linearity	f_{clk} = 16 MHz; ramp input	–	±0.75	–	LSB
DLE	differential non-linearity	f_{clk} = 16 MHz; ramp input; Y	–	±0.5	0.75	LSB
		f_{clk} = 16 MHz; ramp input; U and V	–	±0.6	±0.9	LSB
SNR	signal-to-noise ratio without harmonics	note 1	43	–	–	dB
f_{clk}	maximum conversion rate		20	–	–	MHz
P_{tot}	total power dissipation	note 2	–	500	650	mW

Notes

1. The signal-to-noise ratio without harmonics is measured using a 16 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels).
2. The external resistor (between V_{DDA} and I_{ref}) fixing internal static currents influences P_{tot}. The value of the resistor should be 5.6 kΩ (5%).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8753A	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1

BLOCK DIAGRAM

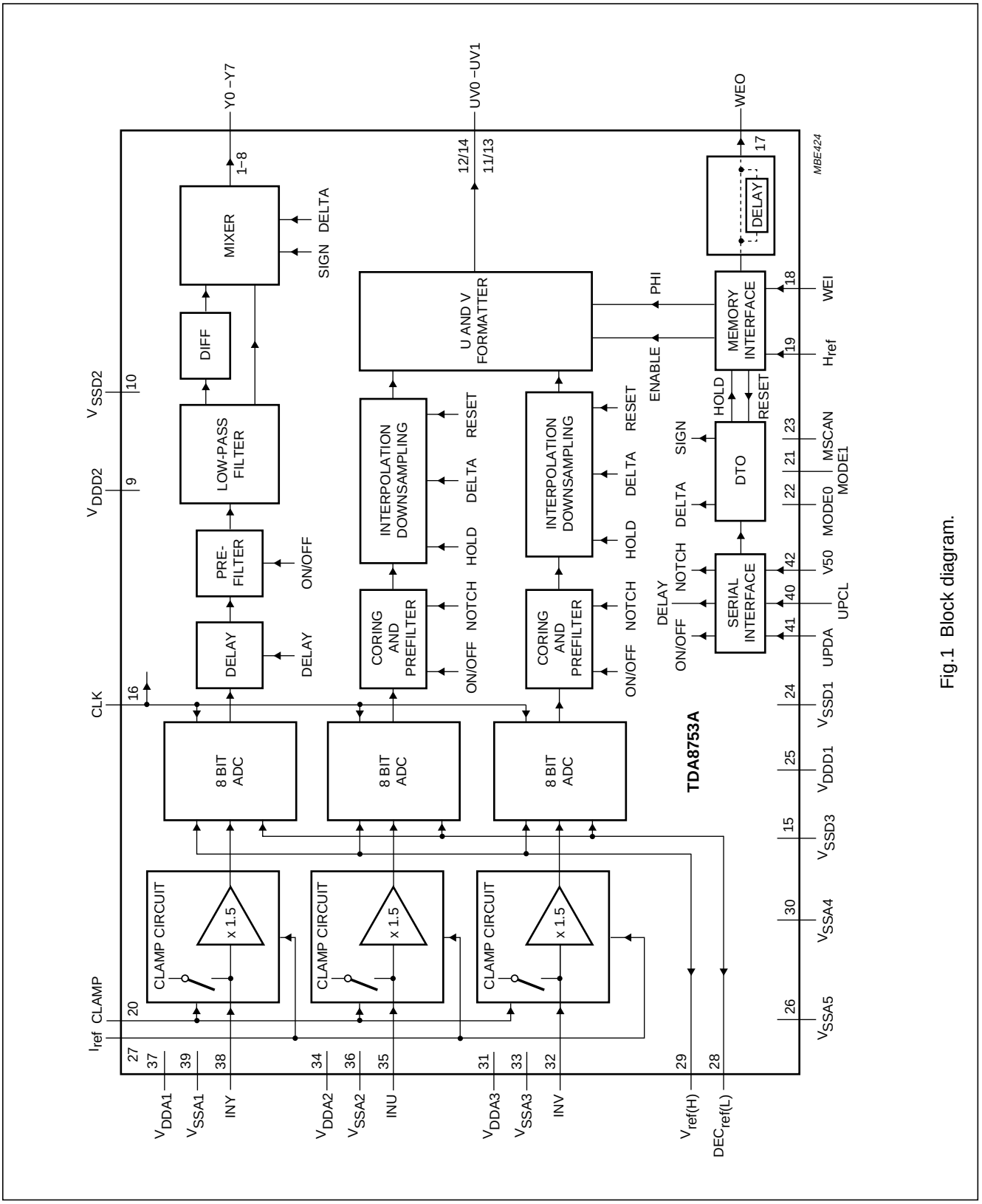


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
Y7	1	Y data output, bit 7 (MSB)
Y6	2	Y data output, bit 6
Y5	3	Y data output, bit 5
Y4	4	Y data output, bit 4
Y3	5	Y data output, bit 3
Y2	6	Y data output, bit 2
Y1	7	Y data output, bit 1
Y0	8	Y data output, bit 0 (LSB)
V_{DDD2}	9	digital supply voltage 2, (+5 V)
V_{SSD2}	10	digital ground 2
U1	11	U data output, bit 1 (n)
U0	12	U data output, bit 0 (n – 1)
V1	13	V data output, bit 1 (n)
V0	14	V data output, bit 0 (n – 1)
V_{SSD3}	15	digital ground 3
CLK	16	clock input
WEO	17	write enable output
WEI	18	write enable input
H_{ref}	19	horizontal reference signal input
CLAMP	20	clamp control input
MODE1	21	test mode select
MODE0	22	test mode select
MSCAN	23	test pin
V_{SSD1}	24	digital ground 1
V_{DDD1}	25	digital supply voltage 1 (+5 V)
V_{SSA5}	26	analog ground 5
I_{ref}	27	current level reference
$DEC_{ref(L)}$	28	decoupling output from reference LOW
$V_{ref(H)}$	29	reference voltage input (HIGH)
V_{SSA4}	30	analog ground 4
V_{DDA3}	31	analog supply voltage 3, (+5 V)
INV	32	V analog voltage input
V_{SSA3}	33	analog ground 3
V_{DDA2}	34	analog supply voltage 2 (+5 V)
INU	35	U analog voltage input
V_{SSA2}	36	analog ground 2
V_{DDA1}	37	analog supply voltage 1 (+5 V)
INY	38	Y analog voltage input
V_{SSA1}	39	analog ground 1
UPCL	40	control clock input
UPDA	41	serial interface data input
V50	42	data execution input

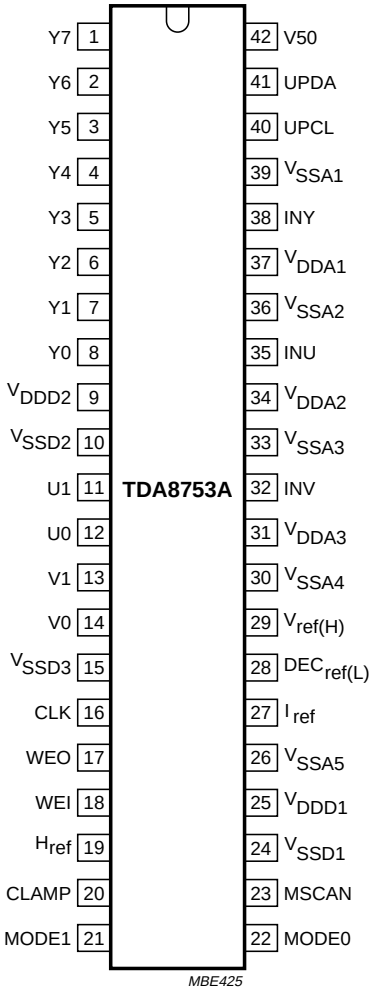


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Analog-to-digital converter

The TDA8753 implements 3 independent CMOS 8-bit analog-to-digital converters. The converters use a multi-step approach with offset compensated comparators.

Clamping

An internal clamping circuit is provided in each of the 3 analog channels. The analog pins INY, INV and INU are switched to on-chip clamping levels during an active pulse on the clamp input CLP.The clamping level in the Y channel is code level 16. The clamping level in the U/V channel is code level 128 (output code 0 in the 2's complement description) see Tables 3 and 4.

Sample rate converter

A sample rate converter is integrated in the TDA8753A to facilitate programming of the horizontal aspect ratio which can be varied from a factor 1 to 2.
This includes conversion from 16/9 to 14/9 and 4/3. In the U/V channel a linear interpolation is sufficient because of the four times oversampling.

Discrete time oscillator (DTO)

A discrete time oscillator is used to calculate for every sample of the phase delay that is needed for a given compression factor.

Serial interface (SIO)

All controls are sent to the TDA8753A via a serial microprocessor interface. Data from this interface will be made active at the vertical input pulse V50.

The TDA8753A has three addressable control registers which can be loaded via the signals UPDA and UPCL. The format of this bus is fixed according to mode 0 of the 8051 family UART at 1 Mbaud (8 bits are transmitted, LSB first).

Serial interface protocol

POWER-ON STATE

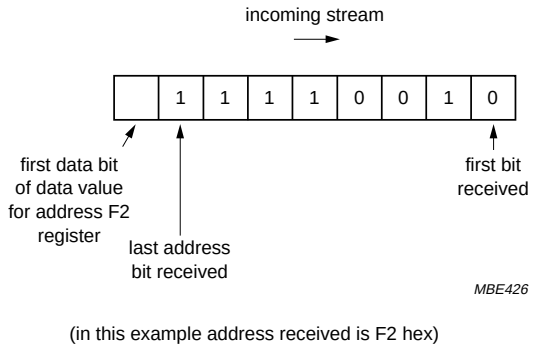
When powered up the SIO is in an unknown state and all data in the registers is random. When signals are applied to UPCL and UPDA in this state, the behaviour is unpredictable. The only way to exit from this state to a known state is apply a V50 signal to the TDA8753A.

INITIALIZATION STATE

From power-on or any other state, the INIT state is entered (at the latest) one TDA8753A clock period after the end of the V50 HIGH state. In this state the F0, F1 and F2 TDA8753A registers are loaded with the values that are in the corresponding line buffers BF0, BF1 and BF2. The first time V50 is issued after power-on, this data is unknown. After a rising UPCL edge has been detected, the address reception state is entered.

ADDRESS RECEPTION STATE

Bits are counted at each rising UPCL edge. The next 8 bits received on UPDA line are considered as address bits. The address reception is illustrated in Fig.3.



(in this example address received is F2 hex)

Fig.3 Address reception.

The TDA8753A registers have address F0, F1 and F2 hexadecimal notation. Whenever the received address (decoded on the first 8 bits received) is one of these, the event is recorded in such a way that the next data received by the TDA8753A will be captured in the line buffer BF0, BF1 and BF2 respectively.

When 8 bits have been received, the data reception state is entered. The address reception state can also be exited at any time when V50 goes HIGH. The F0, F1 and F2 registers may not be loaded properly if there is some activity in progress on the incoming line.

DATA RECEPTION STATE

The next 8 bits are considered as data bits according to the format of Fig.4.

When 8 data bits have been received, the data is recorded in the BF0, BF1 or BF2 line buffers if the previous address recorded was F0 hex, F1 hex or F2 hex respectively. The bit count is then reset to zero and the address reception state is entered. This state may be ended any time when V50 goes HIGH but in that condition F0, F1 and F2 registers may not be loaded properly.

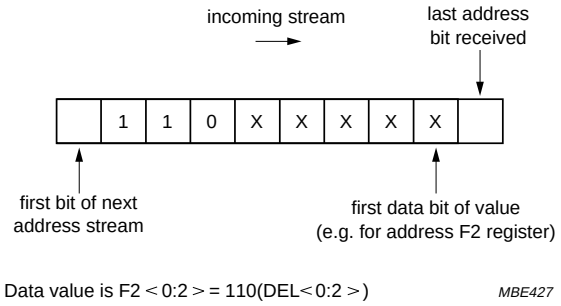


Fig.4 Data reception.

Table 1 Data allocation

ADDRESS	PARAMETER	FUNCTION	NUMBER OF BITS	BIT POSITION
F0H	CF	compression factor value will be (1 + cf/255) which results in a range from 1 to 2	8	7:0
F1H	UV_CORING	coring definition in U and V channels; see Table 5	2	1:0
	UV_FILTER_TYPE	notch filter selection in U and V channels (0 = 4 MHz; 1 = 2 MHz)	1	2
	PRE_ON	luminance prefilter active	1	3
	NOTCH_ON	notch prefilter active	1	4
	DTO_ON	DTO control	1	5
	SEL_DTO_RES	select DTO reset (0 = WE; 1 = H_{ref})	1	6
	WEO_DEL_SEL	select delay in WEO		
F2H	Y_VAR_DELAY	luminance delay compression (see Table 5)		
		not used; load 0	5	7:2

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.3	6.5	V
V_{DDA}	analog supply voltage		–0.3	6.5	V
$V_{DDA} - V_{DDD}$	supply voltage difference		–0.5	+0.5	V
V_I	input voltage	referenced to AGND	–	V_{DDA}	V
$V_{clk(p-p)}$	AC input voltage for switching (peak-to-peak value)	referenced to DGND	–	V_{DDD}	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	45	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 4.75$ to 5.25 V; V_{SSA} and V_{SSD} shorted together; $V_{DDA} - V_{DDD} = -0.1$ to +0.1 V (see note 1); $V_{ref(H)} = 2.38$ V; $f_{clk} = 20$ MHz with 50% duty cycle; 5.6 kΩ (5%) connected between I_{ref} and V_{DDA}; CL = 15 pF; $T_{amb} = 0$ to 70 °C; typical values measured at $V_{DDA} = V_{DDD} = 5$ V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDD}	digital supply voltage		4.75	5.0	5.25	V
I_{DDA}	analog supply current		–	55	63	mA
I_{DDD}	digital supply current		–	45	55	mA
Digital inputs and clock input (WE, H_{ref}, CLAMP, MODE1, MODE0, SCCL, UPCL, UPDA and V50)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{DDD}	V
C_I	input capacitance		–	7	15	pF
$\lvert IL_I \rvert$	input leakage current	$V_I = 0$ V; $V_{DDD} = 5$ V	–10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamp and references [I_{ref}, $DEC_{ref(L)}$ and $V_{ref(H)}$]						
A_{CL}	clamping accuracy	Y	–4	–	+1	LSB
		U and V	–1	–	+1	LSB
C_{clamp}	serial clamp capacitor		10	22	–	nF
Z_{ADC}	internal impedance between pin 29 and V_{SSA}		–	420	–	Ω
$V_{ref(H)}$	converter reference HIGH, applied to pin 29		–	2.38	–	V
$V_{DECref(L)}$	converter reference voltage LOW, applied to pin 28	$V_{ref(H)}$ = 2.38 V	–	0.39	–	V
Y analog input (INY); $V_{ref(H)}$ = 2.38 V, $V_{ref(L)}$ = 0.39 V; see Table 4						
$V_{i(p-p)}$	input voltage, full range (peak-to-peak value)	ramp input	–	1.26	–	V
I_i	input current	clamp non-active	–	5	100	nA
C_I	input capacitance		–	–	15	pF
U,V analog inputs (INU and INV); $V_{ref(H)}$ = 2.38 V, $V_{ref(L)}$ = 0.39 V; see Table 4						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	ramp input	–	1.26	–	V
I_i	input current	clamp non-active	–	5	100	nA
C_I	input capacitance		–	–	15	pF
Inputs isolation						
α_{act}	crosstalk between INY, INU and INV		–	–	–50	dB
Digital outputs (Y0 to Y7, U1, U0, V1 and V0); see Table 3						
V_{OL}	LOW level output voltage	I_{OL} = 1.6 mA	0	–	0.5	V
V_{OH}	HIGH level output voltage	I_{OH} = 0.4 mA	2.4	–	V_{DDD}	V
Analog signal processing (f_{CLK} = 20 MHz)						
G_{diff}	differential gain	note 2	–	1.5	–	%
Φ_{diff}	differential phase	note 2	–	1.0	–	deg
f_{all}	harmonics (full scale) all components	note 3; Y	–	–53	–	dB
		U and V	–	–55	–	dB
SVR	supply voltage ripple rejection	note 4	–	2	–	%/V
B	bandwidth	–1 dB; note 5	–	6	–	MHz
Transfer function (f_{clk} = 16 MHz)						
INL	integral non-linearity	ramp input	–	±0.75	–	LSB
DNL	differential non-linearity	ramp input; Y	–	±0.5	±0.75	LSB
		ramp input; U and V	–	±0.6	±0.9	LSB
SNR	signal-to-noise ratio without harmonics	note 6; Y	41	44.5	–	dB
		U and V	42	46	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (f_{clk} = 20 MHz; C_L = 15 pF); see Figs 7 and 10; note 7						
f_{clk}	maximum input clock frequency		20	–	–	MHz
$t_{CP(H)}$	clock pulse width HIGH		22	–	–	ns
$t_{CP(L)}$	clock pulse width LOW		22	–	–	ns
t_{ds}	sampling delay		–	4	–	ns
t_{hd}	output hold time		7	–	–	ns
t_d	output delay time		–	–	32	ns
t_{CLKr}	clock rise time		3	5	–	ns
t_{CLKf}	clock fall time		3	5	–	ns
$t_{su;Href}$	HREF set-up time		7	–	–	ns
$t_{hd;Href}$	HREF hold time		3	–	–	ns
t_r	data output rise time		–	10	–	ns
t_f	data output fall time		–	10	–	ns
t_{CLP}	minimum time for active clamp pulse width		2.3	2.5	–	µs
$t_{su;WE}$	WE set-up time		7	–	–	ns
$t_{hd;WE}$	WE hold time		3	–	–	ns
t_{XLXL}	serial port clock cycle time	f_{xtal} = 12 MHz	1	–	–	µs
t_{QVXH}	output data set-up to rising edge of clock		700	–	–	ns
t_{XHQH}	output data hold time after rising edge of clock		50	–	–	ns
t_W	V50 pulse duration		2	–	–	ms
t_{VC}	V50 to clock time		2	–	–	ms
Sample rate converter (f_{clk} = 20 MHz)						
ΦY	Y phase accuracy	f_{iY} = 0 to 5 MHz	–	±1	–	ns
FUV	UV phase accuracy	f_{iUV} = 0 to 1.5 MHz	–	±4	–	ns
Y_{fr}	Y frequency response	f_{iY} = 0 to 5 MHz	–	±0.5	–	dB
UV_{fr}	UV frequency response	f_{iUV} = 0 to 1.5 MHz	–	±0.5	–	dB
Y_{step}	Y step size		–	1	–	ns
UV_{step}	UV step size		–	4	–	ns

Notes to the Characteristics

1. V_{DDA} and V_{DDD} should be supplied from the same power supply and decoupled separately.
2. Measurement carried out using video amplifier type VM700A, where the video analog signal (Y channel) is reconstructed via the DAC.
3. The input conditions are related as follows:
   Y – $V_{i(p-p)}$ = 1.26 V, f_i = 4.43 MHz
   U and V – $V_{i(p-p)}$ = 1.26 V, f_i = 1.5 MHz.
4. Supply voltage ripple rejection: SVR; relative variation of the full-scale range of analog input for a supply voltage variation of 0.5 V. SVR = $[\Delta (V_{I(0)} - V_{I(255)}]/[V_{I(o)} - V_{I(255)}]/\Delta V_{DDA}$.
5. The –1 dB bandwidth is the frequency value for which the analog reconstructed (glitch-free) output signal is compressed in term of number of codes, by –1 dB (respectively for –3 dB bandwidth).
6. The signal-to-noise ratio without harmonics is measured under a 16 MHz clock frequency. This value is given for a 4.43 MHz input frequency on the Y channel (1.5 MHz on the U and V channels).
7. Output data acquisition: Output data is available after the maximum delay of t_d.

Table 2 Mode selection

MODE1	MODE0	MODE
0	0	normal configuration

Table 3 Output data coding

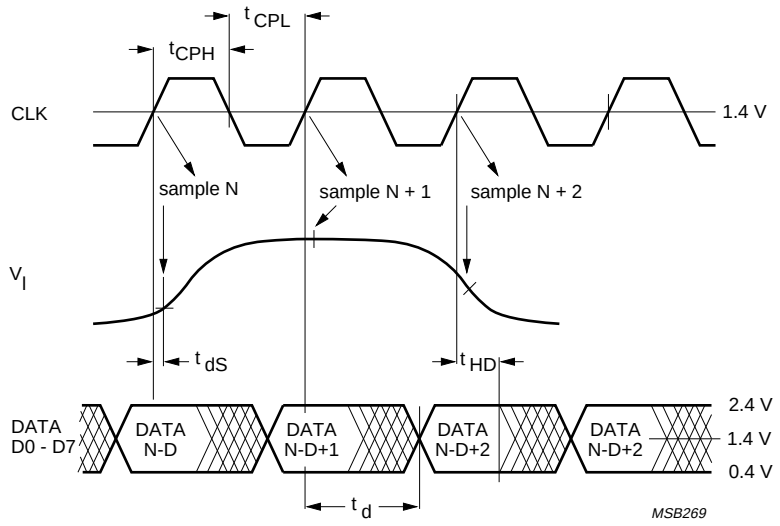
OUTPUT PORT	BIT	OUTPUT DATA			
Y	Y7	$Y_0$7	$Y_1$7	$Y_2$7	$Y_3$7
	Y6	$Y_0$6	$Y_1$6	$Y_2$6	$Y_3$6
	Y5	$Y_0$5	$Y_1$5	$Y_2$5	$Y_3$5
	Y4	$Y_0$4	$Y_1$4	$Y_2$4	$Y_3$4
	Y3	$Y_0$3	$Y_1$3	$Y_2$3	$Y_3$3
	Y2	$Y_0$2	$Y_1$2	$Y_2$2	$Y_3$2
	Y1	$Y_0$1	$Y_1$1	$Y_2$1	$Y_3$1
	Y0	$Y_0$0	$Y_1$0	$Y_2$0	$Y_3$0
U	U1	$\overline{U}_0$7	$U_0$5	$U_0$3	$U_0$1
	U0	$U_0$6	$U_0$4	$U_0$2	$U_0$0
V	V1	$\overline{V}_0$7	$V_0$5	$V_0$3	$V_0$1
	V0	$V_0$6	$V_0$4	$V_0$2	$V_0$0

Table 4 Internal ADC data coding as a function of the analog input

STEP	INPUT VOLTAGE	INTERNAL BINARY OUTPUTS	REMARKS
Underflow	<0.26	00000000	
0	0.26	00000000	$V_{DECref(L)}$ /1.5
1	-	00000001	
....	....	.....	
16	0.34	00010000	clamp level of Y channel
....	....	.....	
128	0.89	10000000	clamp level of U and V channels
....	....	.....	
254	–	11111110	
255	1.52	11111111	$V_{ref(H)}$ – 0.1 V/1.5
Overflow	>1.52	11111111	

Table 5 Coring and luminance delay

UV_CORING		INTERNAL CORING CORRECTION IN U AND V CHANNELS (AROUND CODE 128 LEVEL)	Y_VAR_DELAY		INTERNAL DELAY FOR Y PATH AT PREFILTER INPUT (CLOCK PULSE)
F1:1	F1:0		F2:1	F2:0	
0	0	coring off	0	0	0
0	1	+1/–1	0	1	1
1	0	+1/–0	1	0	2
1	1	+2/–1	1	1	3



The value D is equal to 15.

Fig.5 Timing diagram.

TIMING

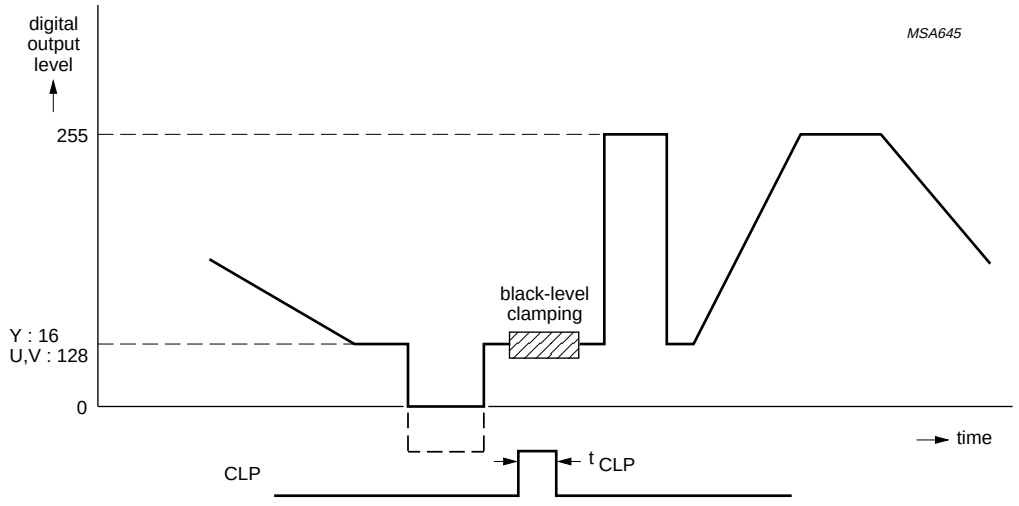
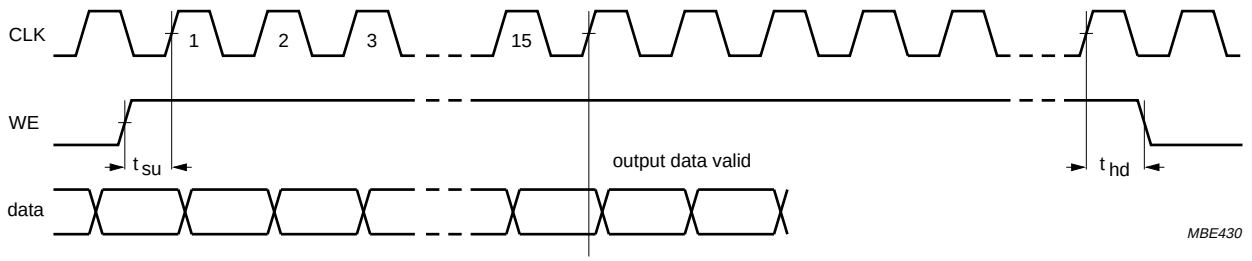
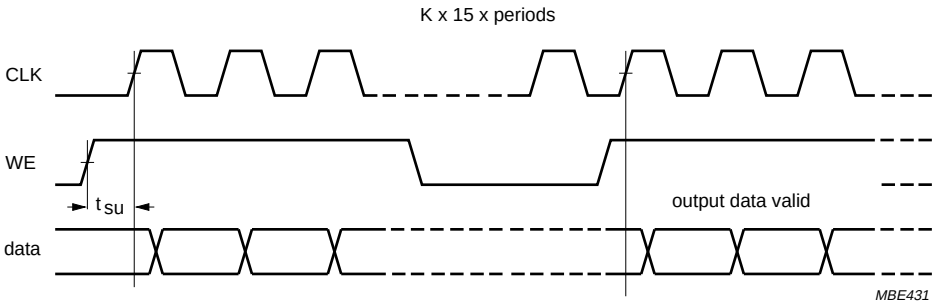


Fig.6 Clamp control timing.



The output data is valid 15 clock periods after WE goes HIGH.

Fig.7 Set-up and hold time definition; WE signal.



When the WE period is a whole multiple of 15 clock periods, the output data is valid without any clock delay.
The internal circuit always gives an internal 15 clock period as illustrated in Fig.7.

Fig.8 Timing diagram; WE signal.

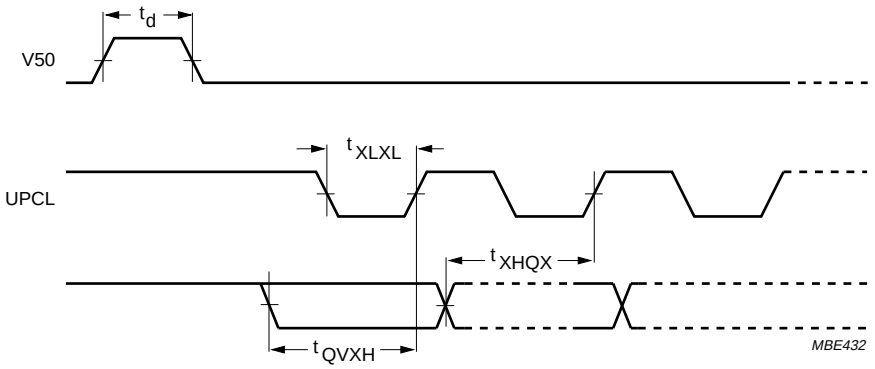


Fig.9 Timing of the asynchronous interface.

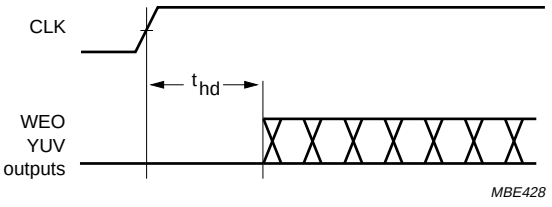


Fig.10 Outputs hold time.

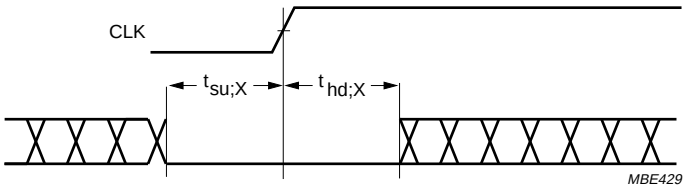


Fig.11 Digital inputs WE and H_{REF}; set-up and hold time.

INTERNAL PIN CONFIGURATION

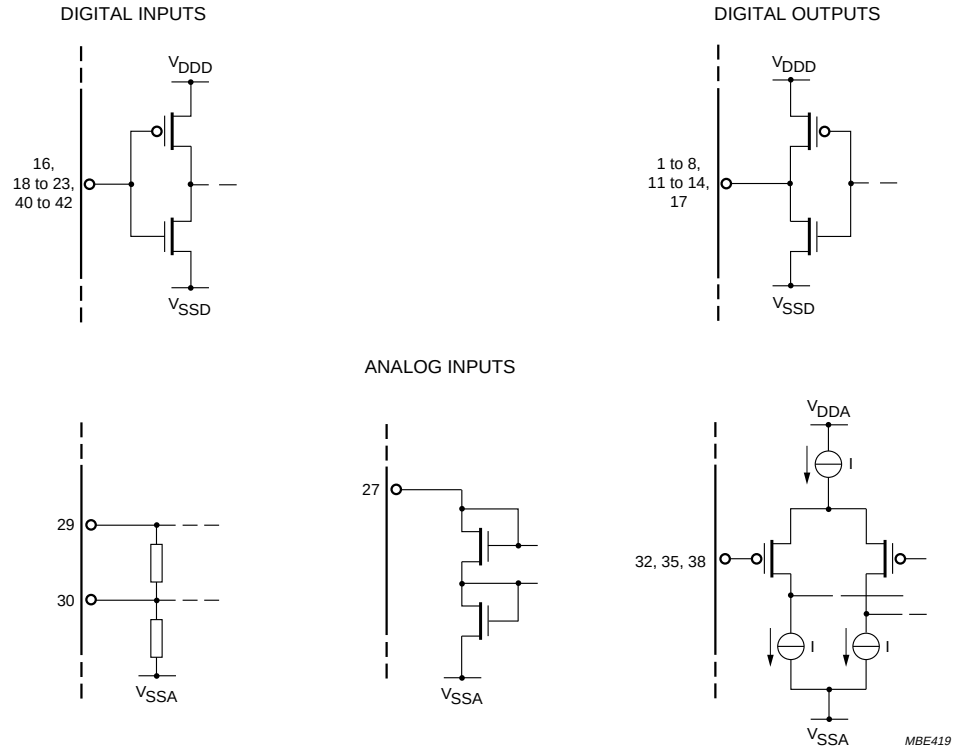
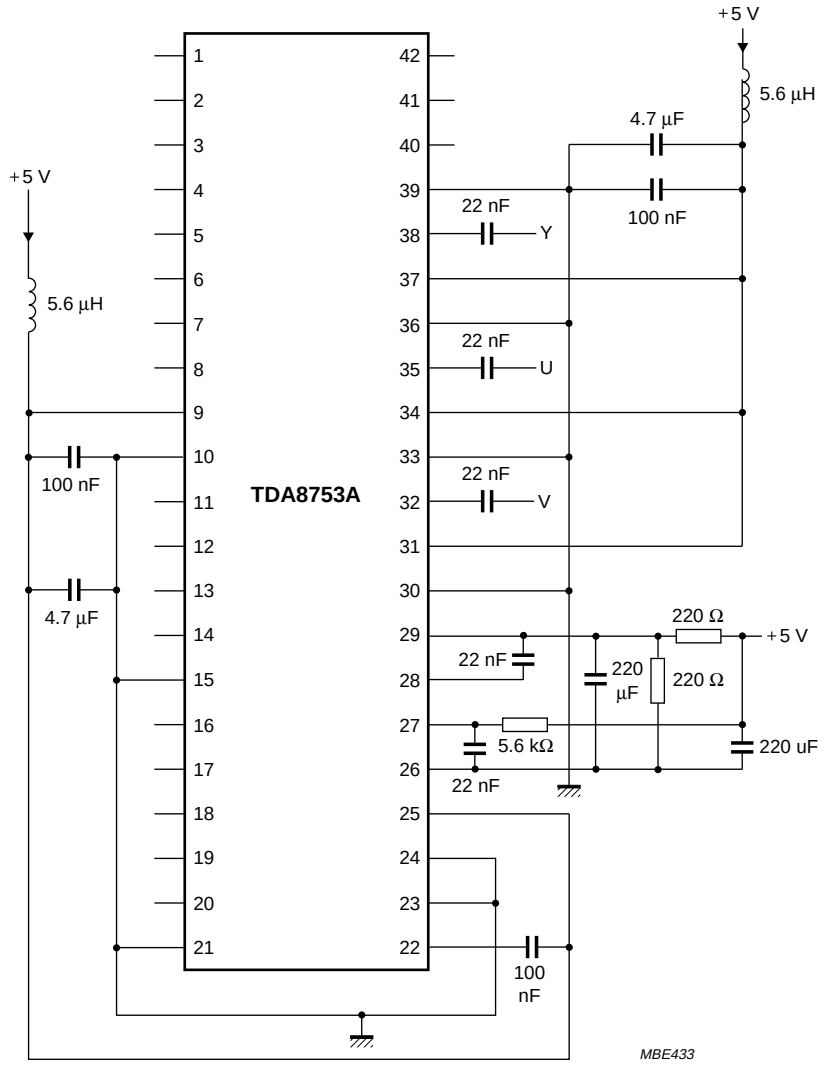


Fig.12 Internal pin configuration.

APPLICATION INFORMATION

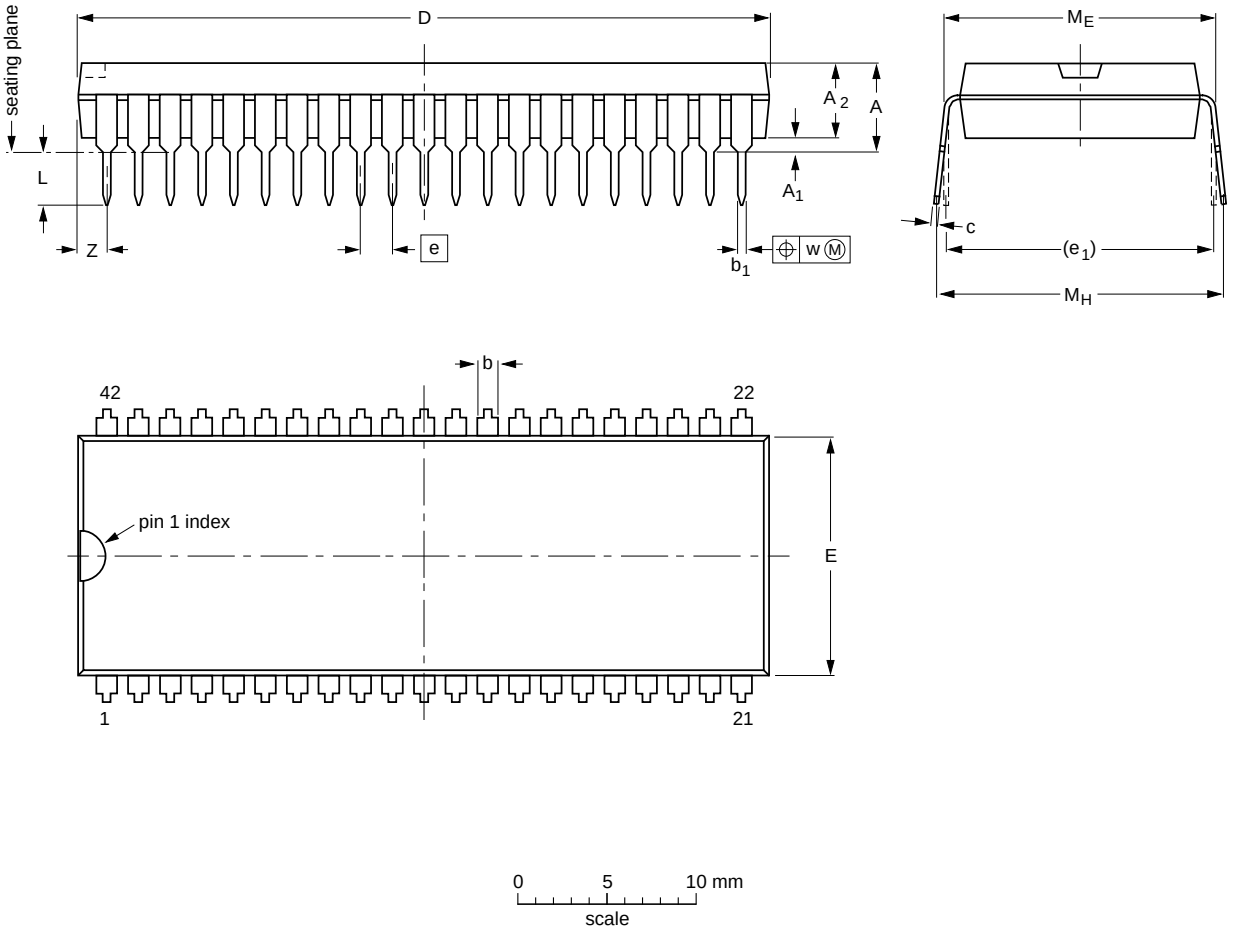


Analog and digital supplies should be separated and decoupled. Test pins MODE1, MODE0 and MSCAN must be connected to digital ground.

Fig.13 Application diagram.

PACKAGE OUTLINE

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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