# TDA8594

## I²C-bus controlled 4 × 50 W power amplifier

Rev. 5 — 11 June 2013 Product data sheet

## 1. General description

The TDA8594 is a complementary quad Bridge Tied Load (BTL) audio power amplifier made in BCDMOS technology. It contains four independent amplifiers in BTL configuration. Through the I²C-bus, diagnosis of temperature warning and clipping level is fully programmable and the information available via two diagnostic pins is selectable. The status of each amplifier (output offset, load or no load, short-circuit or speaker incorrectly connected) can be read separately.

## 2. Features and benefits

### 2.1 General

- Operates in legacy mode (non I²C-bus) and I²C-bus mode (3.3 V and 5 V compliant)
- Three hardware-programmable I²C-bus addresses
- Drives 4 Ω or 2 Ω loads
- Speaker fault detection
- Independent short-circuit protection per channel
- Loss of ground and open $V_P$ safe (with 200 mΩ series impedance and a supply decoupling capacitor of 2200 μF maximum)
- All outputs short-circuit proof to ground, supply voltage and across the load
- All pins short-circuit proof to ground
- Temperature-controlled gain reduction to prevent audio holes at high junction temperatures
- Low battery voltage detection
- Offset detection
- This part has been qualified in accordance with AEC-Q100

### 2.2 I²C-bus mode

- DC load detection: open-circuit, short-circuit and load present
- AC load (tweeter) detection
- During start-up, can detect which load is connected so the appropriate gain can be selected without audio pop
- Independently selectable soft mute of front channels (channel 1 and channel 3) and rear channels (channel 2 and channel 4)
- Programmable gain (26 dB and 16 dB) of front channels (channel 1 and channel 3) and rear channels (channel 2 and channel 4)

- Fully programmable diagnostic levels can be set:
  - Programmable clip detection: 2 %, 5 % or 10 %
  - Programmable thermal pre-warning
- Selectable information on the DIAG and STB pins:
  - The STB pin can be programmed/multiplexed with second clip detection
  - Clip information of each channel can be directed separately to the DIAG pin or the STB pin
  - Independent enabling of thermal, clip or load fault detection (short across or to $V_P$ or to ground) on DIAG pin

## 3. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_P$ | supply voltage | $R_L$ = 4 Ω | 8 | 14.4 | 18 | V |
| $I_q$ | quiescent current | no load | - | 270 | 400 | mA |
| $P_o$ | output power | $V_P$ = 14.4 V | | | | |
| | | $R_L$ = 4 Ω; THD = 0.5 % | 19 | 22 | - | W |
| | | $R_L$ = 4 Ω; THD = 10 % | 26 | 28 | - | W |
| | | $R_L$ = 4 Ω; maximum power; $V_i$ = 2 V (RMS) square wave | 42 | 44 | - | W |
| | | $R_L$ = 2 Ω; maximum power; $V_i$ = 2 V (RMS) square wave | 70 | 75 | - | W |
| THD | total harmonic distortion | $R_L$ = 4 Ω; f = 1 kHz; $P_o$ = 1 W to 12 W | - | 0.01 | 0.1 | % |
| $V_{n(o)}$ | output noise voltage | filter 20 Hz to 22 kHz; $R_S$ = 1 kΩ | | | | |
| | | normal mode | - | 45 | 65 | μV |
| | | line driver mode | - | 22 | 29 | μV |

## 4. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA8594J | DBS27P | plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm) | SOT827-1 |
| TDA8594SD | RDBS27P | plastic rectangular-DIL-bent-SIL (reverse bent) power package; 27 leads (row spacing 2.54 mm) | SOT878-1 |

## 5. Block diagram

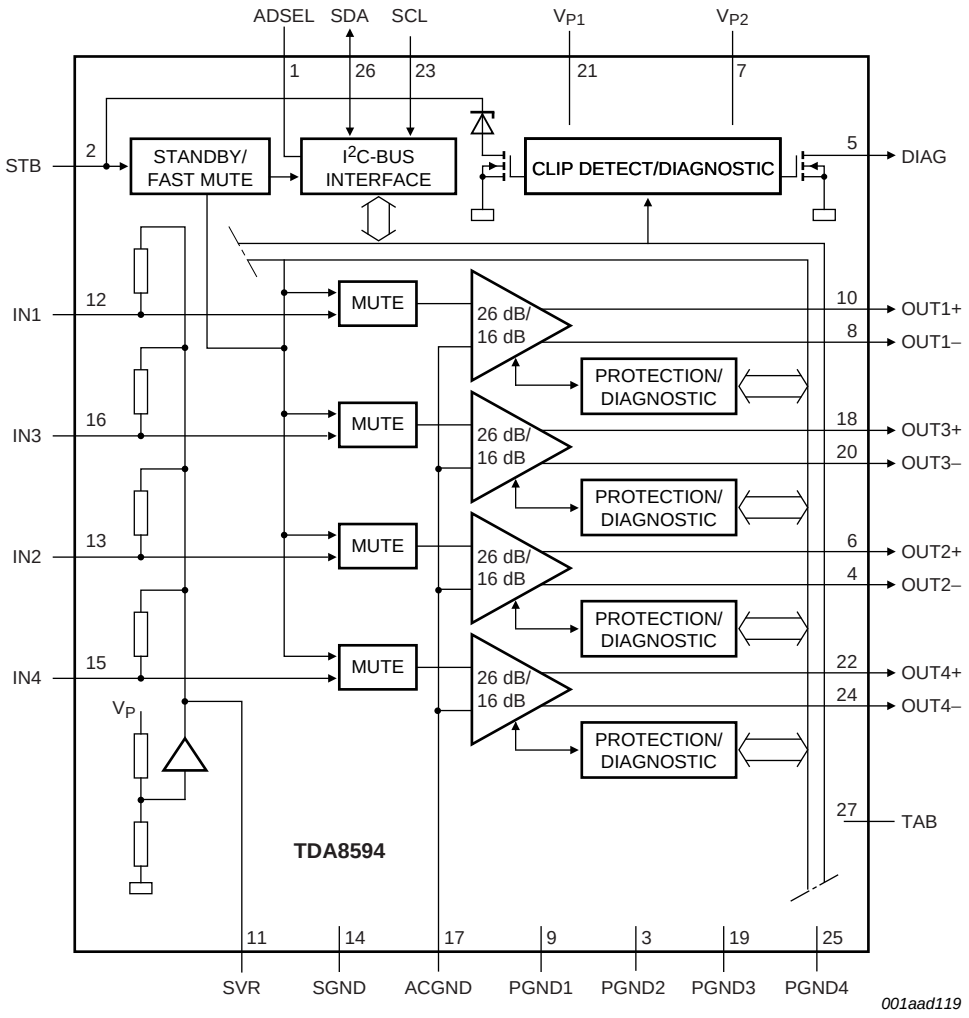



**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning

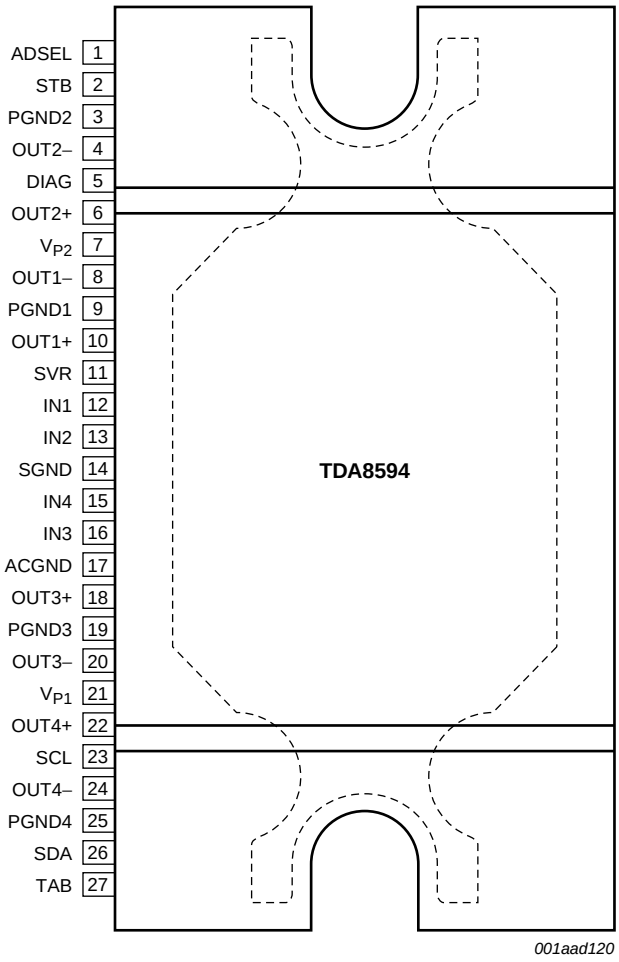



**Fig 2. Pin configuration**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| ADSEL | 1 | I²C-bus address select input |
| STB | 2 | standby (I²C-bus mode) or mode pin (legacy mode); programmable second clip indicator |
| PGND2 | 3 | power ground channel 2 |
| OUT2– | 4 | negative channel 2 output |
| DIAG | 5 | diagnostic/clip detection output |
| OUT2+ | 6 | positive channel 2 output |
| $V_{P2}$ | 7 | supply voltage 2 |

**Table 3. Pin description** *...continued*

| Symbol | Pin | Description |
|---|---|---|
| OUT1− | 8 | negative channel 1 output |
| PGND1 | 9 | power ground channel 1 |
| OUT1+ | 10 | positive channel 1 output |
| SVR | 11 | half supply filter capacitor |
| IN1 | 12 | channel 1 input |
| IN2 | 13 | channel 2 input |
| SGND | 14 | signal ground |
| IN4 | 15 | channel 4 input |
| IN3 | 16 | channel 3 input |
| ACGND | 17 | AC ground input |
| OUT3+ | 18 | positive channel 3 output |
| PGND3 | 19 | power ground channel 3 |
| OUT3− | 20 | negative channel 3 output |
| $V_{P1}$ | 21 | supply voltage 1 |
| OUT4+ | 22 | positive channel 4 output |
| SCL | 23 | I²C-bus clock input |
| OUT4− | 24 | negative channel 4 output |
| PGND4 | 25 | power ground channel 4 |
| SDA | 26 | I²C-bus data input/output |
| TAB | 27 | heatsink connection, must be connected to ground |

To keep the output pins on the front side, special reverse bending is applied.

# 7. Functional description

The TDA8594 is a complementary quad BTL audio power amplifier made in BCDMOS technology. It contains four independent amplifiers in BTL configuration (see Figure 1). Through the I²C-bus, the diagnostic functions of temperature level and clip level are fully programmable and the information to be shown on the two diagnostic pins can be selected. The status of each amplifier (output offset, load or no load, short-circuit or speaker incorrectly connected) can be read separately. The TDA8594 is protected against overvoltage, short-circuit, over-temperature, open ground and open $V_P$ connections.

Three different I²C-bus addresses are selected with an external resistor connected to the ADSEL pin. If the ADSEL pin is short-circuit to ground, the TDA8594 operates in legacy mode. In this mode, no I²C-bus is needed and the function of the STB pin will change from two-level (Standby mode and On mode) to a three-level pin (Standby mode, On mode and mute).

## 7.1 Input stage

The input stage is a high-impedance pseudo-differential input stage. The negative inputs of the four channels are combined on the ACGND pin. For the best performance on supply voltage ripple rejection and pop noise, the capacitor connected to the ACGND pin must be four times the value of the input capacitor (or as close to the value as possible).

## 7.2 Output stage

The output stage of each amplifier channel consists of two PMOS power transistors and two NMOS transistors in a BTL configuration. The process used is the BCDMOS process with an isolated substrate, Silicon On Insulator (SOI) process, which has almost no parasitic components and therefore prevents latch-up.

## 7.3 Distortion (clip) detection

If the output of the amplifier starts clipping to the supply voltage or to ground, the output will become distorted. If the distortion per channel exceeds a selectable threshold (2 %, 5 % or 10 %), one of the two diagnostic pins (DIAG pin or STB pin) will be activated. To be able to detect if, for instance, the front channels (channel 1 and channel 3) or rear channels (channel 2 and channel 4) are clipping, the clip information can be directed per channel to the DIAG pin or the STB pin. It is possible to have only the clip information on the diagnostic pins by disabling the temperature and load information on the DIAG pin. In this mode the temperature and load protection are still functional but can only be read via the I²C-bus.

## 7.4 Output protection and short-circuit operation

When a short-circuit to ground, $V_P$ or across the load occurs on one or more outputs of an amplifier, only the amplifier with the short-circuit is switched off. The channel that has a short-circuit and the type of short-circuit can be read-back via the I²C-bus. If the DIAG pin is enabled for load fault information (IB2[D4] = 0) the DIAG pin will be pulled LOW. After 16 ms the amplifier will be switched on again and, if the short-circuit conditions still occur, the amplifier will be switched off.

The 16 ms cycle will reduce the dissipation. To prevent audible distortion, the amplifier channel with the short-circuit can be disabled via the I²C-bus.

## 7.5 SOAR protection

The output transistors are protected by Safe Operating ARea (SOAR) protection. The TDA8594 has a two-stage SOAR protection:

- If the differential output voltage across the load is less than 1 V, and the current through the load is more than 4 A, the amplifier channel will be switched off for 16 ms. To prevent incorrect switch-off with an inductive load or very high input signals, the condition ($V_o$ < 1 V and $I_L$ > 4 A) must exist for more than 300 μs.
- If the differential output voltage across the load is more than 1 V, and the current through the load is more than 8 A, the amplifier channel will be switched off for 16 ms.

## 7.6 Speaker protection

To prevent damage of the speaker when one side of the speaker is connected to ground, a missing current protection is implemented. When in one channel the current in the high side power is not equal to the current in the low side power, a fault condition is assumed and the channel will be switched off. The speaker protection will be activated under the following conditions:

- $V_o$ < 1.75 V and $I_{missing(det)}$ > 1 A for 80 μs
- $V_o$ > 1.75 V and $I_{missing(det)}$ > 3 A for 80 μs

## 7.7 Standby and mute operation

The function of the STB pin is different in legacy mode and I²C-bus mode.

### 7.7.1 Legacy mode (pin ADSEL connected to ground)

The function of the STB pin will change from standby/operating to standby/mute/operating and the amplifier will start directly when the STB is put into mute or operating mode. Mute operating is controlled via an internal timer (20 ms) to minimize mute-on pops. When the STB pin is switched directly from operating to standby, first the fast mute will be activated (switching to mute within 100 μs) and then the amplifier will shut-down.

### 7.7.2 I²C-bus mode

When the STB pin is LOW, the total quiescent current is low, and the I²C-bus lines will not be loaded.

When the STB pin is switched HIGH, the TDA8594 is put in operating condition and will perform a Power-On Reset (POR), which results in a LOW level DIAG pin. The TDA8594 will start up when instruction bit IB1[D0] is set. Bit D0 will also reset the ‘power-on reset occurred’ bit (DB2[D7]) and releases the DIAG pin.

The soft mute and fast mute can be activated via the I²C-bus. The soft mute can be activated independently for the front channels (channel 1 and channel 3) and rear channels (channel 2 and channel 4), and mutes the audio in 20 ms. The fast mute activates the mute for all channels at the same time and mutes the audio in 0.1 ms. Releasing the mute after a fast mute will be by a soft un-mute of approximately 20 ms.

When the STB pin is switched to Standby mode and the amplifier has started, first the fast mute will be activated and then the amplifier will shut-down. For instance, during an engine start, it is possible to fully mute the amplifiers within 100 μs by switching the STB pin to zero.

## 7.8 Start-up and shut-down sequence

To prevent the amplifier producing switch-on or switch-off pop noise, the capacitor on the SVR pin is used for smooth start-up and shut-down. Increasing the value of the SVR capacitor will mean a longer start-up and shut-down time. The amplifier output voltage is charged to half the supply voltage minus 1.4 V in mute condition, independent of the I²C-bus mute settings in I²C-bus mode or STB voltage in legacy mode. The last 1.4 V, where the output will reach half the supply voltage, is used to release the mute if the I²C-bus bits were set to mute off (IB2[D2:D0] = 000; $V_{STB}$ > 6.5 V in legacy mode), or will stay in mute when the bits were set to mute (2.6 V < $V_{STB}$ < 4.5 V in legacy mode).

When the amplifier is switched off by pulling the STB pin LOW, the amplifier is first muted (fast mute) and then the capacitor on the SVR pin is discharged. With an SVR capacitor of 22 μF, the standby current has reached 1 second after the STB pin is switched to zero (see Figure 3, Figure 4, Figure 5 and Figure 6).

The start-up and shut-down pop can be further decreased by activating the low pop mode. When the low pop mode is enabled (IB2[D3] = 0), the output voltage rise from ground level during start-up will be slower (see Figure 5). This will decrease the pop even more but will increase the start-up time.

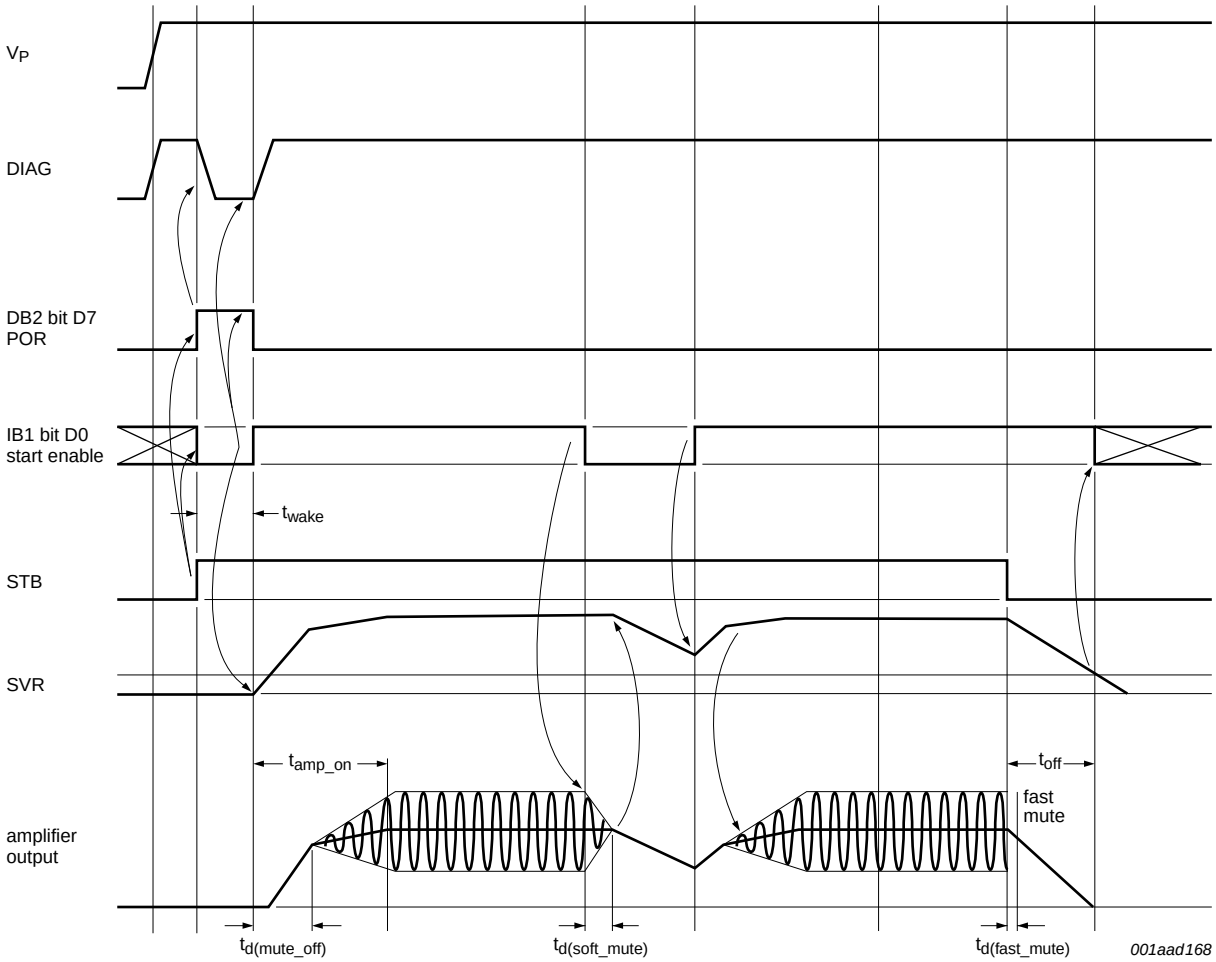



**Fig 3. Start-up and shut-down timing in I²C-bus mode**

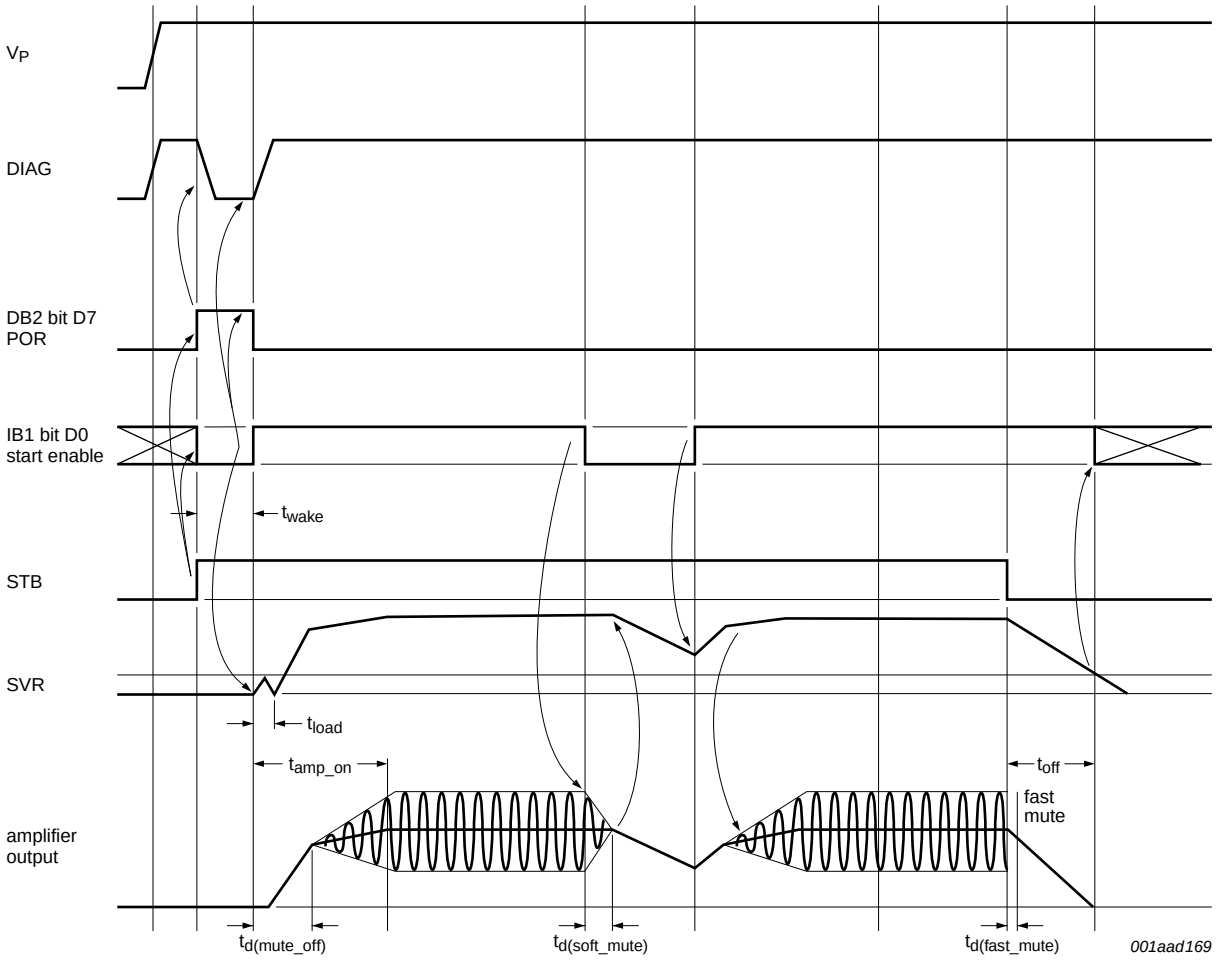



**Fig 4. Start-up and shut-down timing with DC load active in I²C-bus mode**

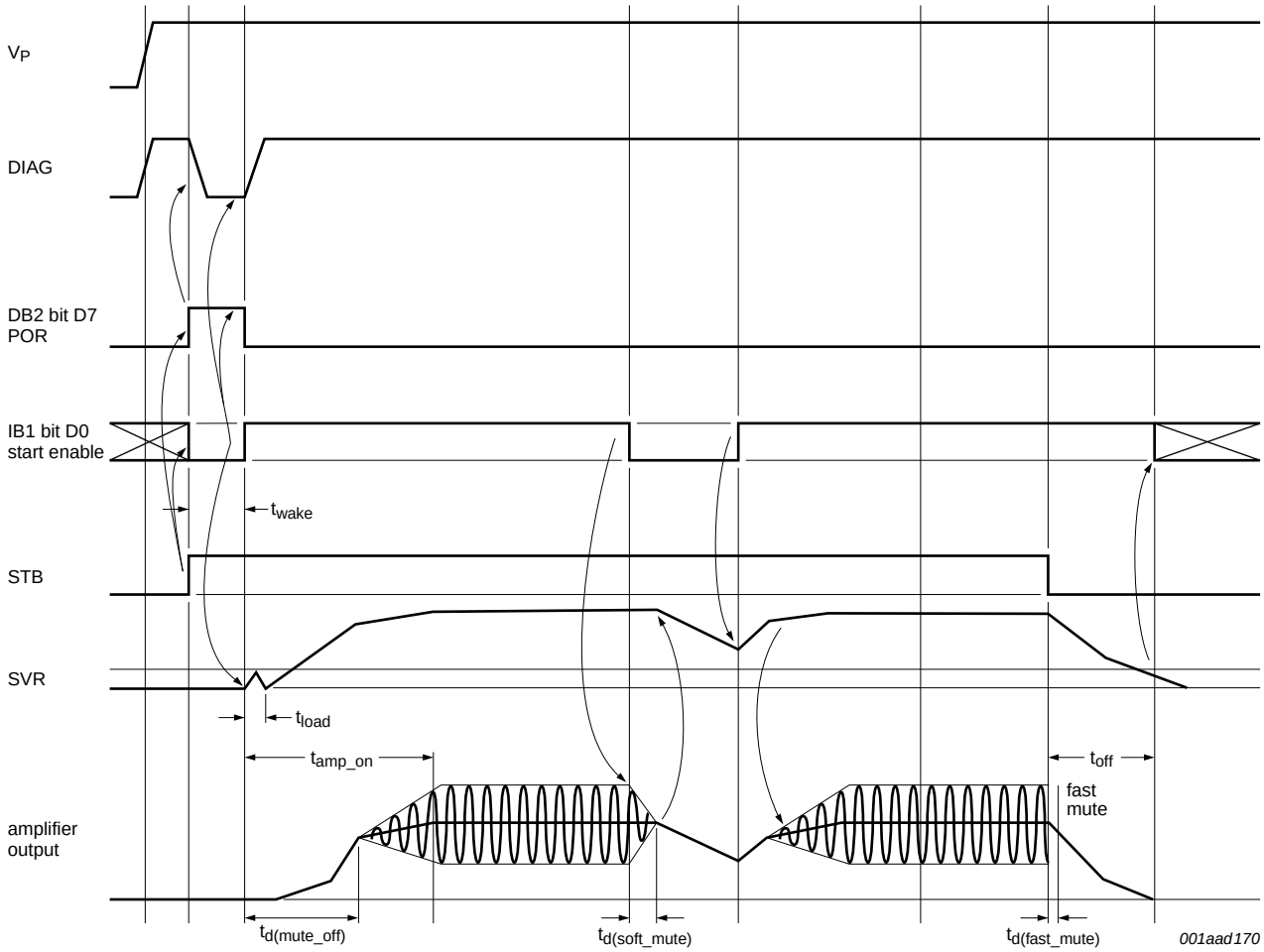



**Fig 5. Start-up and shut-down timing with low audible pop and DC load activated**

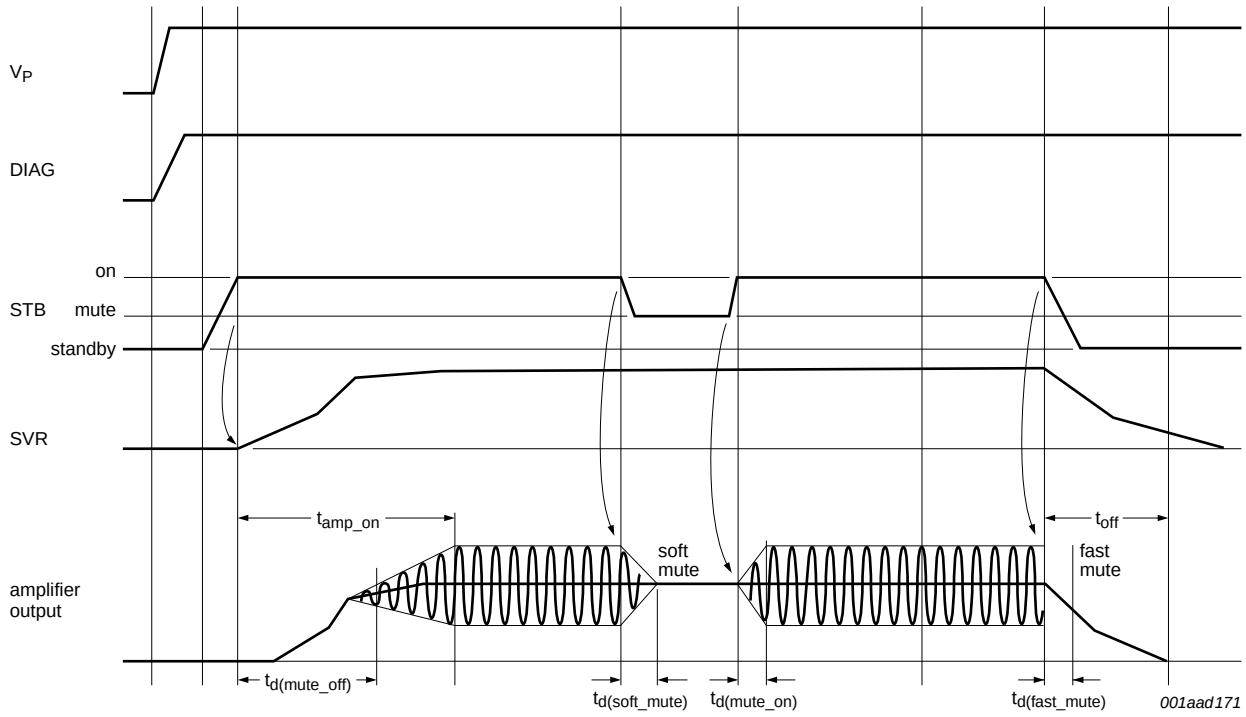



**Fig 6. Start-up and shut-down timing in legacy mode**

## 7.9 Power-on reset and supply voltage spikes

If in I²C-bus mode the supply voltage drops below 5 V (see Figure 9), the content of the I²C-bus latches cannot be guaranteed and the power-on reset will be activated. All latches are reset, the amplifier is switched off and the DIAG pin is pulled LOW to indicate that a power-on reset has occurred (bit DB2[D7]). When IB1[D0] is set, the power-on flag is reset, the DIAG pin will be released and the amplifier will start up.

In legacy mode a supply voltage drop below 5 V will switch off the amplifier and the DIAG pin will not be pulled LOW.

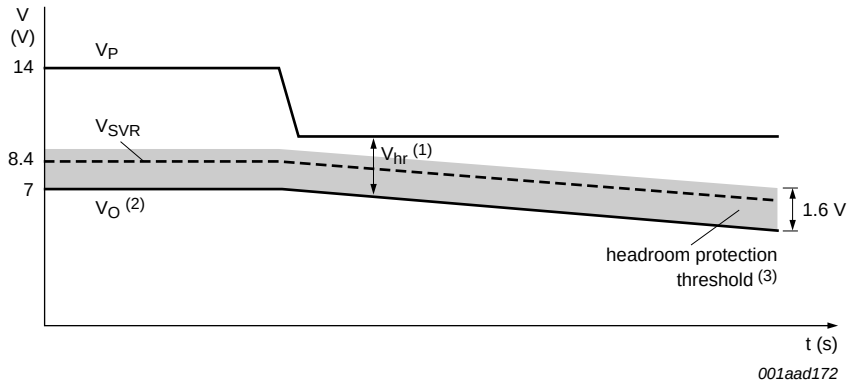
## 7.10 Engine start and low voltage operation

The DC output voltage of the amplifier ($V_O$) is set to half of the supply voltage and is related to the voltage on the SVR pin (see Figure 7; $V_O = V_{SVR} - 1.4$ V). A capacitor is connected on the SVR pin to suppress the ripple on the power supply.

If the supply voltage drops, for instance, during an engine start, the output follows slowly due to the SVR capacitor. The headroom voltage is the voltage needed for good operation of the amplifier and is defined as $V_{hr} = V_P - V_O$ (see Figure 7). If the headroom voltage becomes lower than the headroom protection threshold of 1.6 V, the headroom protection is activated to prevent pop noise at the output. This protection first activates the fast mute and then discharges the capacitors on the SVR and ACGND pins to generate more headroom for the amplifier (see Figure 8).

When the SVR capacitor has discharged, the amplifier starts up again if the $V_P$ voltage is above the low $V_P$ mute threshold, typically 7.5 V. Below the low $V_P$ mute threshold, the outputs of the amplifier remain low. In I²C-bus mode, a supply voltage drop below $V_{P(reset)}$, typically 5 V, results in setting bit DB2[D7] and not starting of the amplifiers but waiting for an I²C-bus command to start.

The amplifier prevents audio pops during engine start. To prevent pops on the output caused by the application during an engine start (for instance tuner regulator out of regulation), the STB pin can be made zero when an engine start is detected. The STB pin activates the fast mute and disturbances at the amplifier inputs are suppressed.

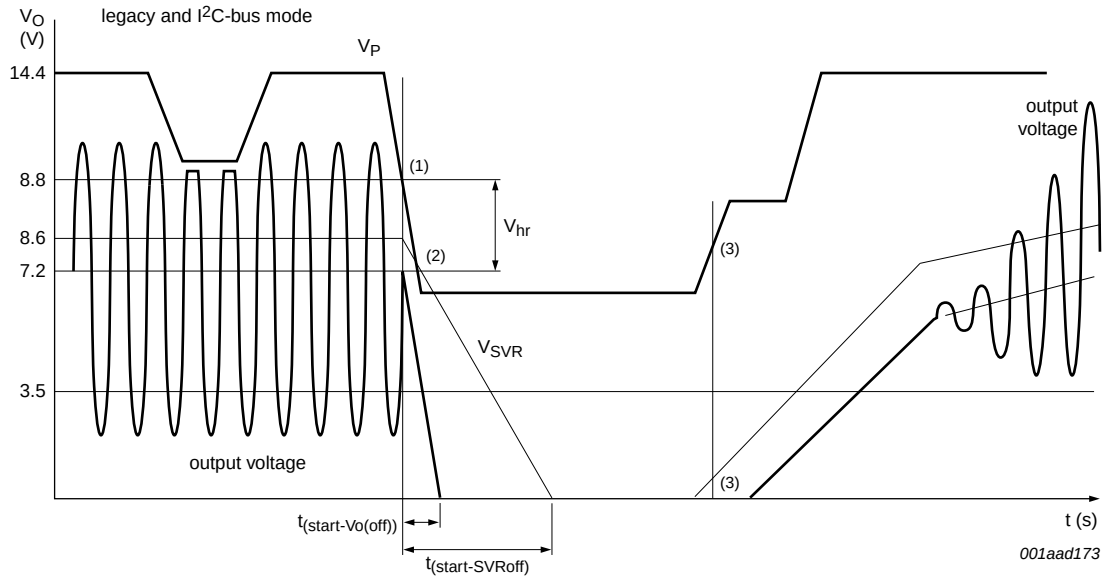



(1) Headroom voltage $V_{hr} = V_P - V_O$.

(2) Steady state output voltage $V_O = V_{SVR} - 1.4$ V.

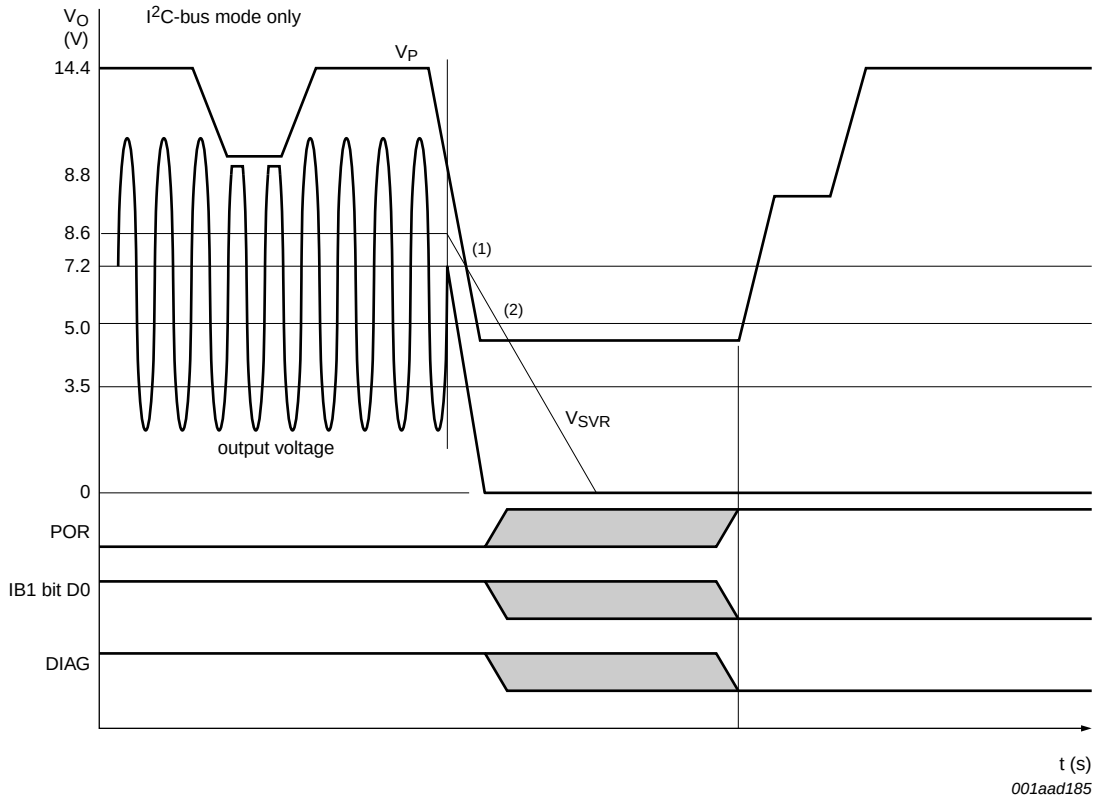
(3) Headroom protection threshold = $V_O + 1.6$ V.

**Fig 7. Low headroom protection**




(1) Headroom protection activated:
  a) Fast mute
  b) Discharge of SVR.
(2) Low $V_P$ mute activated.
(3) Low $V_P$ mute released.

**Fig 8. Low $V_P$ behavior; legacy and I²C-bus modes**




(1) Low $V_P$ mute activated.

(2) $V_{POR}$: $V_P$ level at which Power-On Reset (POR) is activated.

**Fig 9. Low $V_P$ behavior; I²C-bus mode only**

## 7.11 Overvoltage and load dump protection

When the battery voltage $V_P$ is higher than 22 V, the amplifier stage will be switched to high-impedance. The TDA8594 is protected against load dump voltage with supply voltage up to 50 V.

## 7.12 Thermal pre-warning and thermal protection

If the average junction temperature reaches a level that is adjustable via the I²C-bus, selected with IB3[D4], the pre-warning will be activated resulting in a LOW level on pin DIAG (if selected) and can be read out via the I²C-bus. The default setting for the thermal pre-warning is IB3[D4] = 0 setting the warning level at 145 °C. In legacy mode the thermal pre-warning is set at 145 °C.

If the temperature increases further, the temperature controlled gain reduction will be activated for all four channels to reduce the output power (see Figure 10). If this does not reduce the average junction temperature, all four channels will be switched off at the absolute maximum temperature $T_{off}$, typical 175 °C.

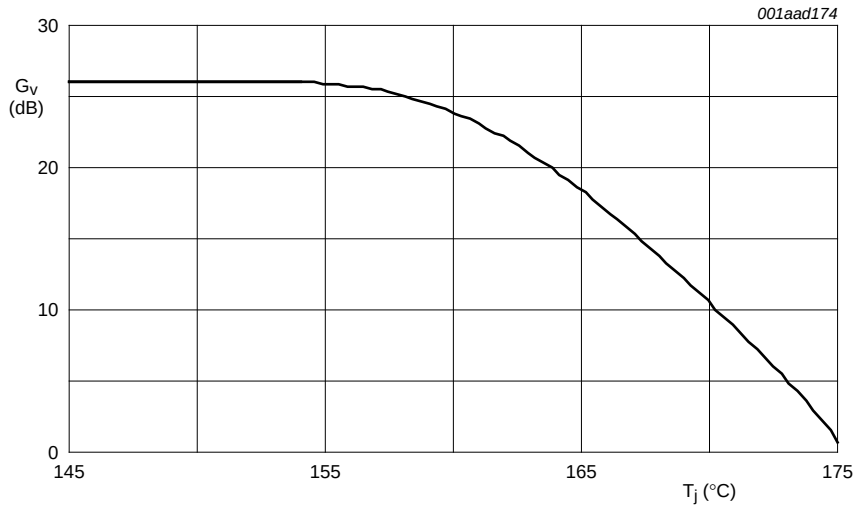



**Fig 10. Temperature controlled amplifier gain**

## 7.13 Diagnostics

Diagnostic information can be read via the I²C-bus, and can also be available on the DIAG pin or on the STB pin. The DIAG pin has both fixed information (power-on reset occurred, low battery and high battery) and, via the I²C-bus, selectable information (temperature, load fault and clip). This information will be seen at the DIAG pin as a logic OR. In case of a failure, the DIAG pin remains LOW and the failure information can be read from the microprocessor via the I²C-bus (the DIAG pin can be used as a microprocessor interrupt to minimize I²C-bus traffic). When the failure is removed, the DIAG pin will be released.

To have full control over the clipping information, the STB pin can be programmed as a second clip detection pin. The clip detection level can be selected for all channels at once. It is possible to select whether the clip information is available on the DIAG pin or on the STB pin for each channel separately. It is, for instance, possible to distinguish between clipping of the front and the rear channels.

Diagnostic information selection possibilities are shown in Table 4.

**Table 4. Diagnostic information availability**

| Diagnostic information | I²C-bus mode | | Legacy mode |
|---|---|---|---|
| | DIAG pin | STB pin | DIAG pin |
| POR | after power-on reset, DIAG pin will remain LOW until amplifier has been started | no | no |
| Low battery | yes | no | yes |
| Clip detection | can be enabled per channel | can be enabled per channel | yes, fixed level for all channels on 2 % |
| Temperature pre-warning | can be enabled | no | yes, pre-warning level is 145 °C |
| Short | can be enabled | no | yes |
| Speaker protection (missing current) | can be enabled | no | yes |

**Table 4. Diagnostic information availability** *...continued*

| Diagnostic information | I²C-bus mode | | Legacy mode |
|---|---|---|---|
| | DIAG pin | STB pin | DIAG pin |
| Offset detection | no | no | no |
| Load detection | no | no | no |
| Overvoltage | yes | no | yes |

## 7.14 Offset detection

The offset detection can be performed with no input signal (for instance when the digital signal processor is in mute after a start-up) or with an input signal. In I²C-bus mode, if an I²C-bus read of the output offset is performed, the I²C-bus latches DBx[D2] will be set. When the amplifier BTL output voltage is within a window with a threshold of 1.75 V typical, the latches DBx[D2] are reset and setting is disabled. If, for instance, after 1 second an I²C-bus read is performed again and the offset bits are still set, the output has not crossed the offset threshold during the last 1 second (see Figure 11). This can mean the applied frequency is below 1 Hz (I²C-bus read interval = 1 s) or an output offset of more than 1.75 V is present.

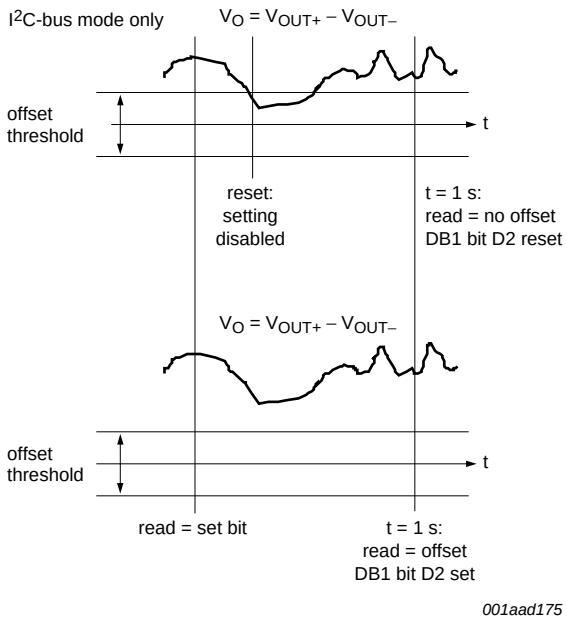



**Fig 11. Offset detection**

## 7.15 DC load detection

When the DC load detection is enabled with IB1[D1], a DC offset is slowly applied at the output of the amplifiers during the start-up cycle and the load currents are measured. Different load levels will be detected to differentiate between normal load, line driver load or open load.

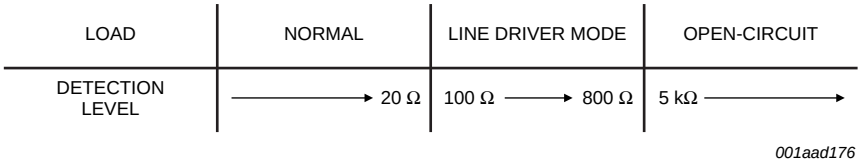



**Fig 12. DC load detection levels**

If the amplifier is used as line driver and the external booster has an input impedance of more than 100 Ω and less than 800 Ω (DC-coupled), the DC load bits will contain DBx[D5:D4] = 10, independent of the gain setting (see Table 5).

**Table 5. DC load detection**

| DC load bits | | Meaning (when IB1[D2] = 0) |
|---|---|---|
| DBx[D5] | DBx[D4] | |
| 0 | 0 | normal load |
| 1 | 0 | line driver load |
| 1 | 1 | open load |
| 0 | 1 | not valid |

By reading the I²C-bus bits the microprocessor can determine, after the start-up of the amplifier, whether a speaker or an external booster is connected.

Depending on these bits, the amplifier gain can be selected, 26 dB for normal mode or 16 dB for line driver mode. If the gain select is performed when the amplifier is muted, the gain select will be pop free.

The DC load bits are combined with the AC load bits and are only valid when the AC load detection is disabled. When the AC load detection is enabled (IB1[D2] = 1), the bits DBx[D4] will show the content of the AC load detection. When the AC load detection is disabled again, bit DBx[D4] will show the content of the DC load measurement, which was stored during the AC load measurement. The AC load detection can only be performed after the amplifier has completed its start-up cycle and will not conflict with the DC load detection.

## 7.16 AC load detection

The AC load detection, enabled with IB1[D2] = 1, is used to detect if AC-coupled speakers, for example tweeters, are connected correctly during assembly. The detection is audible because a sine wave of a certain frequency (e.g. 19 kHz) needs to be applied to the inputs of the amplifier. The output voltage over the load impedance will generate an amplifier current. If the amplifier peak current triggers a 460 mA (peak) threshold detector three times, the AC load detection bit will be set. A three ‘threshold cross’ counter is used to prevent false AC load detection when switching the input signal on or off.

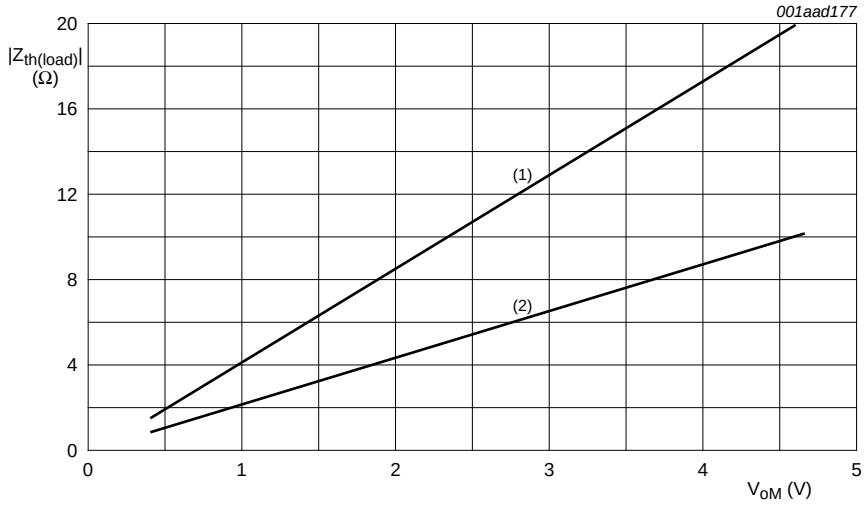
An AC-coupled speaker will reduce the impedance at the output of the amplifier in a certain frequency band. The presence of an AC-coupled speaker can be determined using 460 mA (peak) and 230 mA (peak) threshold current detection. For instance, at an output voltage of 2 V (peak) the total impedance must be less than 4 Ω to detect the AC-coupled load, or more than 8 Ω to guarantee only a DC connection is detected.

The interpretation of line driver and normal mode DC load bit settings for AC load detection is shown in Table 6.

**Table 6. AC load detection**

| DBx[D4] | Meaning (when IB1[D2] = 1) |
|---|---|
| 0 | no AC load detected |
| 1 | AC load detected |

When bit IB1[D2] = 1, the AC load detection is enabled. The AC load detection can only be performed after the amplifier has completed its start-up cycle and will not conflict with the DC load detection.




(1) $I_{th(o)det(load)AC}$ < 230 mA (no load detection level)

(2) $I_{th(o)det(load)AC}$ > 460 mA (load detection level)

**Fig 13. AC load impedance as a function of peak output voltage**

## 7.17 I²C-bus diagnostic readout

The diagnostic information of the amplifier can be read via the I²C-bus. The I²C-bus bits are set on a failure and will be reset with the I²C-bus read command. Even when the failure is removed, the microprocessor will know what was wrong by reading the I²C-bus. The consequence of this procedure is that old information is read during the I²C-bus readout. Most actual information will be gathered after two successive read commands.

The DIAG pin will give actual diagnostic information (when selected). When a failure is removed, the DIAG pin will be released instantly, independently of the I²C-bus latches.

# 8. I²C-bus specification

**Table 7. TDA8594 hardware address select**

| Pin ADSEL | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ |
|---|---|---|---|---|---|---|---|---|
| Open | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 = write to TDA8594 |
| | | | | | | | | 1 = read from TDA8594 |
| 51 kΩ to ground | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 = write to TDA8594 |
| | | | | | | | | 1 = read from TDA8594 |
| 10 kΩ to ground | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 = write to TDA8594 |
| | | | | | | | | 1 = read from TDA8594 |
| Ground | no I²C-bus; legacy mode | | | | | | | |

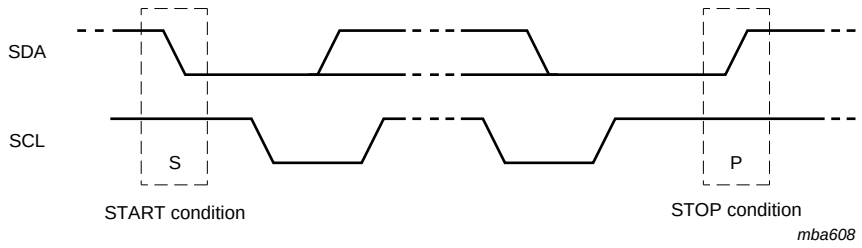



**Fig 14. Definition of START and STOP conditions**

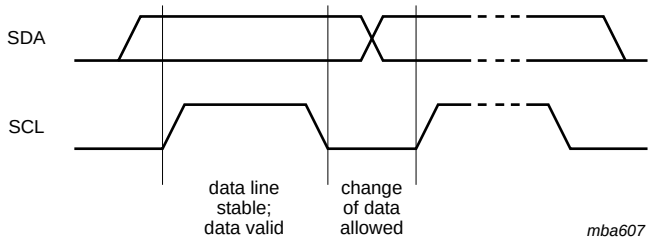



**Fig 15. Bit transfer**

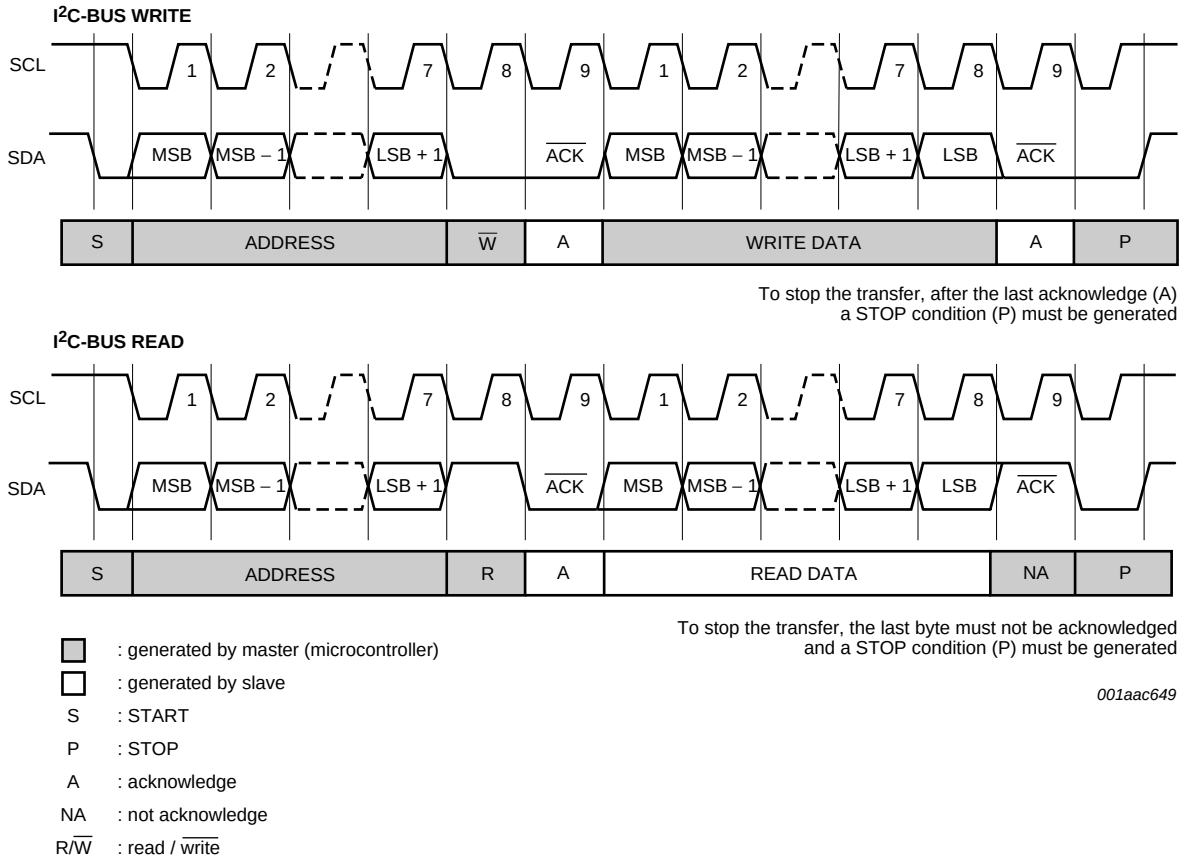



**Fig 16. I²C-bus read and write modes**

## 8.1 Instruction bytes

I²C-bus mode:

- If bit R/$\overline{W}$ = 0, the TDA8594 expects three instruction bytes; IB1, IB2 and IB3
- After a power-on reset, all instruction bits are set to zero.

Legacy mode:

- All bits equal to zero define the setting, with the exception of bit IB1[D0] which is ignored; see Table 8.

**Table 8. Instruction byte IB1**

| Bit | Description |
|---|---|
| D7 | don't care |
| D6 | channel 3 clip information on DIAG or STB pin |
| | 0 = clip information on DIAG pin |
| | 1 = clip information on STB pin |
| D5 | channel 1 clip information on DIAG or STB pin |
| | 0 = clip information on DIAG pin |
| | 1 = clip information on STB pin |

**Table 8. Instruction byte IB1** *…continued*

| Bit | Description |
|---|---|
| D4 | channel 4 clip information on DIAG or STB pin |
| | 0 = clip information on DIAG pin |
| | 1 = clip information on STB pin |
| D3 | channel 2 clip information on DIAG or STB pin |
| | 0 = clip information on DIAG pin |
| | 1 = clip information on STB pin |
| D2 | AC load detection enable |
| | 0 = AC load detection disabled |
| | 1 = AC load detection enabled; DBx[D4] bits not available for DC load detection |
| D1 | DC load detection enable |
| | 0 = DC load detection disabled |
| | 1 = DC load detection enabled |
| D0 | amplifier start enable |
| | 0 = amplifier not enabled, DIAG pin will remain LOW |
| | 1 = amplifier will start up, power-on occurred (DB2[D7] will be reset) and DIAG pin will be released |

**Table 9. Instruction byte IB2**

| Bit | Description |
|---|---|
| D7 and D6 | clip detection level |
| | 00 = clip detection level 2 % |
| | 01 = clip detection level 5 % |
| | 10 = clip detection level 10 % |
| | 11 = clip detection level disabled |
| D5 | temperature information on DIAG pin |
| | 0 = temperature information on DIAG pin |
| | 1 = no temperature information on DIAG pin |
| D4 | load fault information (shorts, missing current) on DIAG pin |
| | 0 = fault information on DIAG pin |
| | 1 = no fault information on DIAG pin |
| D3 | low pop (slow start) enable |
| | 0 = low pop enabled |
| | 1 = low pop disabled |
| D2 | soft mute channel 1 and channel 3 (mute delay 20 ms) |
| | 0 = no mute |
| | 1 = mute |
| D1 | soft mute channel 2 and channel 4 (mute delay 20 ms) |
| | 0 = no mute |
| | 1 = mute |

**Table 9. Instruction byte IB2** *…continued*

| Bit | Description |
|---|---|
| D0 | fast mute all amplifier channels (mute delay 100 μs) |
| | 0 = no mute |
| | 1 = mute |

**Table 10. Instruction byte IB3**

| Bit | Description |
|---|---|
| D7 | don't care |
| D6 | amplifier channel 1 and channel 3 gain select |
| | 0 = 26 dB |
| | 1 = 16 dB |
| D5 | amplifier channel 2 and channel 4 gain select |
| | 0 = 26 dB |
| | 1 = 16 dB |
| D4 | temperature pre-warning level |
| | 0 = warning level on 145 °C |
| | 1 = warning level on 122 °C |
| D3 | disable channel 3 |
| | 0 = channel 3 enabled |
| | 1 = channel 3 disabled |
| D2 | disable channel 1 |
| | 0 = channel 1 enabled |
| | 1 = channel 1 disabled |
| D1 | disable channel 4 |
| | 0 = channel 4 enabled |
| | 1 = channel 4 disabled |
| D0 | disable channel 2 |
| | 0 = channel 2 enabled |
| | 1 = channel 2 disabled |

## 8.2 Data bytes

I²C-bus mode:

- If bit R/$\overline{W}$ = 1, the TDA8594 sends four data bytes to the microprocessor: DB1, DB2, DB3, and DB4
- All bits except DB1[D7] and DB3[D7] are latched.
- All bits except DBx[D4] and DBx[D5] are reset after a read operation. Bit DBx[D2] is set after a read operation; see Section 7.14
- For explanation of AC and DC load detection bits; see Section 7.15 and Section 7.16.

**Table 11. Data byte DB1**

| Bit | Description |
|---|---|
| D7 | temperature pre-warning |
| | 0 = no warning |
| | 1 = junction temperature too high |
| D6 | speaker fault channel 2 (missing current) |
| | 0 = no missing current |
| | 1 = missing current |
| D5 and D4 | channel 2 DC load or AC load detection |
| | if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning |
| | 0 = no AC load |
| | 1 = AC load detected |
| | if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection |
| | 00 = normal load |
| | 01 = not valid |
| | 10 = line driver load |
| | 11 = open load |
| D3 | channel 2 shorted load |
| | 0 = not shorted load |
| | 1 = shorted load |
| D2 | channel 2 output offset |
| | 0 = no output offset |
| | 1 = output offset |
| D1 | channel 2 short to $V_P$ |
| | 0 = no short to $V_P$ |
| | 1 = short to $V_P$ |
| D0 | channel 2 short to ground |
| | 0 = no short to ground |
| | 1 = short to ground |

**Table 12. Data byte DB2**

| Bit | Description |
|---|---|
| D7 | power-on reset and amplifier status |
| | 0 = amplifier on |
| | 1 = power-on reset has occurred; amplifier off |
| D6 | speaker fault channel 4 (missing current) |
| | 0 = no missing current |
| | 1 = missing current |

**Table 12. Data byte DB2** *…continued*

| Bit | Description |
|---|---|
| D5 and D4 | channel 4 DC load or AC load detection |
| | if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning |
| | 0 = no AC load |
| | 1 = AC load detected |
| | if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection |
| | 00 = normal load |
| | 01 = not valid |
| | 10 = line driver load |
| | 11 = open load |
| D3 | channel 4 shorted load |
| | 0 = not shorted load |
| | 1 = shorted load |
| D2 | channel 4 output offset |
| | 0 = no output offset |
| | 1 = output offset |
| D1 | channel 4 short to $V_P$ |
| | 0 = no short to $V_P$ |
| | 1 = short to $V_P$ |
| D0 | channel 4 short to ground |
| | 0 = no short to ground |
| | 1 = short to ground |

**Table 13. Data byte DB3**

| Bit | Description |
|---|---|
| D7 | maximum temperature protection |
| | 0 = no protection |
| | 1 = maximum temperature protection |
| D6 | speaker fault channel 1 (missing current) |
| | 0 = no missing current |
| | 1 = missing current |

**Table 13. Data byte DB3** *…continued*

| Bit | Description |
|---|---|
| D5 and D4 | channel 1 DC load or AC load detection |
| | if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning |
| | 0 = no AC load |
| | 1 = AC load detected |
| | if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection |
| | 00 = normal load |
| | 01 = not valid |
| | 10 = line driver load |
| | 11 = open load |
| D3 | channel 1 shorted load |
| | 0 = not shorted load |
| | 1 = shorted load |
| D2 | channel 1 output offset |
| | 0 = no output offset |
| | 1 = output offset |
| D1 | channel 1 short to $V_P$ |
| | 0 = no short to $V_P$ |
| | 1 = short to $V_P$ |
| D0 | channel 1 short to ground |
| | 0 = no short to ground |
| | 1 = short to ground |

**Table 14. Data byte DB4**

| Bit | Description |
|---|---|
| D7 | reserved |
| D6 | speaker fault channel 3 (missing current) |
| | 0 = no missing current |
| | 1 = missing current |
| D5 and D4 | channel 3 DC load or AC load detection |
| | if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning |
| | 0 = no AC load |
| | 1 = AC load detected |
| | if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection |
| | 00 = normal load |
| | 01 = not valid |
| | 10 = line driver load |
| | 11 = open load |

**Table 14. Data byte DB4** *…continued*

| Bit | Description |
|---|---|
| D3 | channel 3 shorted load |
| | 0 = not shorted load |
| | 1 = shorted load |
| D2 | channel 3 output offset |
| | 0 = no output offset |
| | 1 = output offset |
| D1 | channel 3 short to $V_P$ |
| | 0 = no short to $V_P$ |
| | 1 = short to $V_P$ |
| D0 | channel 3 short to ground |
| | 0 = no short to ground |
| | 1 = short to ground |

## 9. Limiting values

**Table 15. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_P$ | supply voltage | operating | 8 | 18 | V |
| | | non operating | −1 | +50 | V |
| | | load dump protection; duration 50 ms, rise time > 2.5 ms | - | 50 | V |
| $V_{P(r)}$ | reverse supply voltage | $t_{max}$ = 10 minutes | - | −2 | V |
| $I_{OSM}$ | non-repetitive peak output current | | - | 13 | A |
| $I_{ORM}$ | repetitive peak output current | | - | 8 | A |
| $T_{j(max)}$ | maximum junction temperature | | - | 150 | °C |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| $T_{amb}$ | ambient temperature | | −40 | +105 | °C |
| $V_{(prot)}$ | protection voltage | AC and DC short-circuit of output pins and across the load | - | $V_P$ | V |
| $V_x$ | voltage on pin x | pins SCL and SDA | 0 | 6.5 | V |
| | | pins IN1, IN2, IN3, IN4, SVR, ACGND and DIAG | 0 | 13 | V |
| | | pin STB | 0 | 24 | V |

**Table 15. Limiting values** *...continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $P_{tot}$ | total power dissipation | $T_{case}$ = 70 °C | - | 80 | W |
| $V_{esd}$ | electrostatic discharge voltage | human body model; C = 100 pF; $R_S$ = 1.5 kΩ | - | 2000 | V |
| | | machine model; C = 200 pF; $R_S$ = 10 Ω; $L_S$ = 0.75 μH | - | 200 | V |

## 10. Thermal characteristics

**Table 16. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-c)}$ | thermal resistance from junction to case | | 1 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 40 | K/W |

## 11. Characteristics

**Table 17. Characteristics**

*Refer to Figure 29 at $V_P = V_{P1} = V_{P2}$ = 14.4 V; $R_L$ = 4 Ω; f = 1 kHz; $R_S$ = 0 Ω; normal mode; unless otherwise specified. Tested at $T_{amb}$ = 25 °C; guaranteed for $T_{amb}$ = −40 °C to +105 °C.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply voltage behavior** | | | | | | |
| $V_P$ | supply voltage | $R_L$ = 4 Ω | 8 | 14.4 | 18 | V |
| | | $R_L$ = 2 Ω [1] | 8 | 14.4 | 16 | V |
| $I_q$ | quiescent current | no load | - | 270 | 400 | mA |
| $I_{stb}$ | standby current | $V_{STB}$ = 0.4 V | - | 4 | 15 | μA |
| $V_O$ | output voltage | | 6.7 | 7 | 7.2 | V |
| $V_{P(low)(mute)}$ | low supply voltage mute | with rising supply voltage | 6.9 | 7.5 | 8 | V |
| | | with falling supply voltage | 6.3 | 6.8 | 7.4 | V |
| $\Delta V_{P(low)(mute)}$ | low supply voltage mute hysteresis | | 0.1 | 0.7 | 1 | V |
| $V_{th(ovp)}$ | overvoltage protection threshold voltage | | 18 | 20 | 22 | V |
| $V_{hr}$ | headroom voltage | when headroom protection is activated; see Figure 7 | 1.1 | 1.6 | 2.0 | V |
| $V_{POR}$ | power-on reset voltage | see Figure 9 | 4.1 | 5.0 | 5.8 | V |
| $V_{O(offset)}$ | output offset voltage | amplifier on | −95 | 0 | +95 | mV |
| | | amplifier mute | −25 | 0 | +25 | mV |
| | | line driver mode | −40 | 0 | +40 | mV |
| $R_{L(tol)}$ | load resistance tolerance | $V_P \leq 18$ V | 3.2 | 4 | - | Ω |
| | | $V_P \leq 16$ V | 1.6 | 2 | - | Ω |

**Table 17. Characteristics** *...continued*

*Refer to Figure 29 at $V_P = V_{P1} = V_{P2} = 14.4$ V; $R_L = 4\ \Omega$; $f = 1$ kHz; $R_S = 0\ \Omega$; normal mode; unless otherwise specified. Tested at $T_{amb} = 25$ °C; guaranteed for $T_{amb} = -40$ °C to +105 °C.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Mode select and second clip detection: pin STB** | | | | | | | |
| $V_{STB}$ | voltage on pin STB | Standby mode selected | | | | | |
| | | I²C-bus mode | | - | - | 1 | V |
| | | legacy mode (I²C-bus off) | | - | - | 1 | V |
| | | mute selected | | | | | |
| | | legacy mode (I²C-bus off) | | 2.5 | - | 4.5 | V |
| | | Operating mode selected | | | | | |
| | | I²C-bus mode | | 2.5 | - | $V_P$ | V |
| | | legacy mode (I²C-bus off) | | 6.5 | - | $V_P$ | V |
| | | low voltage on pin STB when pulled down during clipping | [2] | | | | |
| | | $I_{STB}$ = 150 μA | | 5.6 | - | 6.1 | V |
| | | $I_{STB}$ = 500 μA | | 6.1 | - | 7.2 | V |
| $I_{STB}$ | current on pin STB | $V_{STB}$ = 0 V to 8.5 V | | | | | |
| | | clip detection not active; I²C-bus mode | | - | 4 | 30 | μA |
| | | legacy mode | | - | 10 | 70 | μA |
| **Start-up, shut-down and mute timing** | | | | | | | |
| $t_{wake}$ | wake-up time | time after wake-up via STB pin before first I²C-bus transmission is recognized; see Figure 3 | | - | 300 | 500 | μs |
| $I_{LO(SVR)}$ | output leakage current on pin SVR | | | - | - | 10 | μA |
| $t_{d(mute\_off)}$ | mute off delay time | 10 % of output signal; $I_{LO}$ = 0 μA | [3] | | | | |
| | | I²C-bus mode; with $I_{LO}$ = 10 μA → +15 ms; no DC load (IB1[D1] = 0); low pop disabled (IB2[D3] = 1); see Figure 3 | | 295 | 465 | 795 | ms |
| | | I²C-bus mode; with $I_{LO}$ = 10 μA → +20 ms; DC load active (IB1[D1] = 1); low pop disabled (IB2[D3] = 1); see Figure 4 | | 500 | 640 | 940 | ms |
| | | I²C-bus mode; with $I_{LO}$ = 10 μA → +20 ms; DC load active (IB1[D1] = 1); low pop enabled (IB2[D3] = 0); see Figure 5 | | 640 | 830 | 1190 | ms |
| | | legacy mode; with $I_{LO}$ = 10 μA → +20 ms; $V_{STB}$ = 7 V; $R_{ADSEL}$ = 0 Ω; see Figure 6 | | 430 | 650 | 1030 | ms |

**Table 17. Characteristics** *...continued*

*Refer to Figure 29 at $V_P = V_{P1} = V_{P2} = 14.4$ V; $R_L = 4\ \Omega$; $f = 1$ kHz; $R_S = 0\ \Omega$; normal mode; unless otherwise specified. Tested at $T_{amb} = 25$ °C; guaranteed for $T_{amb} = -40$ °C to +105 °C.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{amp\_on}$ | amplifier on time | time from amplifier mute to amplifier on; 90 % of output signal; $I_{LO} = 0$ µA | [3] | | | | |
| | | I²C-bus mode; with $I_{LO} = 10$ µA → +30 ms; no DC load (IB1[D1] = 0); low pop disabled (IB2[D3] = 1); see Figure 3 | | 360 | 520 | 870 | ms |
| | | I²C-bus mode; with $I_{LO} = 10$ µA → +35 ms; DC load active (IB1[D1] = 1); low pop disabled (IB2[D3] = 1); see Figure 4 | | 565 | 695 | 1015 | ms |
| | | I²C-bus mode; with $I_{LO} = 10$ µA → +30 ms; DC load active (IB1[D1] = 1); low pop enabled (IB2[D3] = 0); see Figure 5 | | 710 | 890 | 1270 | ms |
| | | legacy mode; with $I_{LO} = 10$ µA → +20 ms; $V_{STB} = 7$ V; $R_{ADSEL} = 0\ \Omega$; see Figure 6 | | 510 | 720 | 1120 | ms |
| $t_{off}$ | amplifier switch-off time | time to DC output voltage < 0.1 V; I²C-bus mode; $I_{LO} = 0$ µA | [3] | | | | |
| | | with $I_{LO} = 10$ µA → +0 ms; low pop enabled (IB2[D3] = 0); see Figure 4 | | 120 | 245 | 530 | ms |
| | | with $I_{LO} = 10$ µA → +0 ms; low pop disabled (IB2[D3] = 1); see Figure 5 | | 140 | 280 | 620 | ms |
| $t_{d(mute-on)}$ | mute to on delay time | from 10 % to 90 % of output signal; IB2[D1] and IB2[D2] = 1 to 0; $V_i = 50$ mV; see Figure 6 | | - | 20 | 40 | ms |
| $t_{d(soft\_mute)}$ | soft mute delay time | from 90 % to 10 % of output signal; $V_i = 50$ mV; IB2[D1] and IB2[D2] = 0 to 1 (soft mute); see Figure 6 | | - | 20 | 40 | ms |
| $t_{d(fast\_mute)}$ | fast mute delay time | from 90 % to 10 % of output signal; $V_{STB}$ from 8 V to 1.3 V (fast mute); see Figure 6 | | - | 0.1 | 1 | ms |
| $t_{(start-Vo(off))}$ | engine start to output off time | $V_P$ from 14.4 V to 7 V; $V_o < 0.5$ V; see Figure 8 | | - | 0.1 | 1 | ms |
| $t_{(start-SVRoff)}$ | engine start to SVR off time | $V_P$ from 14.4 V to 7 V; $V_{SVR} < 2$ V; see Figure 8 | | - | 40 | 75 | ms |
| **I²C-bus interface** | | | [4] | | | | |
| $V_{IL}$ | LOW-level input voltage | pins SCL and SDA | | - | - | 1.5 | V |
| $V_{IH}$ | HIGH-level input voltage | pins SCL and SDA | | 2.3 | - | 5.5 | V |
| $V_{OL}$ | LOW-level output voltage | pin SDA; $I_L = 5$ mA | | - | - | 0.4 | V |

**Table 17. Characteristics** *...continued*

*Refer to Figure 29 at $V_P = V_{P1} = V_{P2} = 14.4$ V; $R_L = 4\ \Omega$; $f = 1$ kHz; $R_S = 0\ \Omega$; normal mode; unless otherwise specified. Tested at $T_{amb} = 25$ °C; guaranteed for $T_{amb} = -40$ °C to +105 °C.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | - | 400 | - | kHz |
| $R_{ADSEL}$ | resistance on pin ADSEL | I²C-bus address A[6:0] = 110 1100 | 155 | - | - | kΩ |
| | | I²C-bus address A[6:0] = 110 1101 | 42 | 51 | 57 | kΩ |
| | | I²C-bus address A[6:0] = 110 1111 | 7 | 10 | 15 | kΩ |
| | | legacy mode | - | - | 0.5 | kΩ |
| **Diagnostic** | | | | | | |
| $V_{OL(DIAG)}$ | LOW-level output voltage on pin DIAG | fault condition; $I_{DIAG} = 1$ mA | - | - | 0.3 | V |
| $V_{O(offset\_det)}$ | output voltage at offset detection | | ±1.5 | ±1.75 | ±2.2 | V |
| $THD_{clip}$ | total harmonic distortion clip detection level | IB2[D7:D6] = 10 | 5 | 10 | 18 | % |
| | | IB2[D7:D6] = 01 | 3 | 5 | 9 | % |
| | | IB2[D7:D6] = 00 | 1 | 2 | 3 | % |
| $\Delta THD_{clip}$ | total harmonic distortion clip detection level variation | no overlap between IB2[D7:D6] = 10 and IB2[D7:D6] = 01 | 1 | 4 | 9 | % |
| | | no overlap between IB2[D7:D6] = 01 and IB2[D7:D6] = 00 | 1 | 3.5 | 6 | % |
| $T_{j(AV)(pwarn)}$ | pre-warning average junction temperature | IB3[D4] = 0 | 135 | 145 | 155 | °C |
| | | IB3[D4] = 1 | 112 | 122 | 132 | °C |
| $T_{j(AV)(G(-0.5dB))}$ | average junction temperature for 0.5 dB gain reduction | $V_i = 0.05$ V | 150 | 155 | 160 | °C |
| $\Delta T_{j(pw\text{-}G(-0.5dB))}$ | prewarning to 0.5 dB gain reduction junction temperature difference | | 7 | 10 | 13 | °C |
| $\Delta T_{j(G(-0.5dB)\text{-}of)}$ | junction temperature difference between 0.5 dB gain reduction and off | from thermal foldback to when all outputs are switched off | 10 | 15 | 20 | °C |
| $\Delta G_{(th\_fold)}$ | gain reduction of thermal foldback | all channels switched off | - | 20 | - | dB |
| $Z_{th(load)}$ | load detection threshold impedance | I²C-bus mode | | | | |
| | | normal load detection | - | - | 20 | Ω |
| | | line driver load detection | 100 | - | 800 | Ω |
| $Z_{th(open)}$ | open load detection threshold impedance | I²C-bus mode | 5000 | - | - | Ω |
| $I_{th(o)det(load)AC}$ | AC load detection output threshold current | I²C-bus mode | | | | |
| | | AC load bit is set | 460 | - | - | mA |
| | | AC load bit is not set | - | - | 230 | mA |

**Table 17. Characteristics** *...continued*

*Refer to Figure 29 at $V_P = V_{P1} = V_{P2} = 14.4$ V; $R_L = 4\ \Omega$; $f = 1$ kHz; $R_S = 0\ \Omega$; normal mode; unless otherwise specified. Tested at $T_{amb} = 25$ °C; guaranteed for $T_{amb} = -40$ °C to +105 °C.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Amplifier** | | | | | | | |
| $P_o$ | output power | $R_L = 4\ \Omega$; $V_P = 14.4$ V; THD = 0.5 % | | 19 | 22 | - | W |
| | | $R_L = 4\ \Omega$; $V_P = 14.4$ V; THD = 10 % | | 26 | 28 | - | W |
| | | $R_L = 4\ \Omega$; $V_P = 14.4$ V; maximum power; $V_i = 2$ V (RMS) square wave | | 42 | 44 | - | W |
| | | $R_L = 4\ \Omega$; $V_P = 15.2$ V; maximum power; $V_i = 2$ V (RMS) square wave | | 47 | 50 | - | W |
| | | $R_L = 2\ \Omega$; $V_P = 14.4$ V; THD = 0.5 % | | 34 | 37 | - | W |
| | | $R_L = 2\ \Omega$; $V_P = 14.4$ V; THD = 10 % | | 45 | 48 | - | W |
| | | $R_L = 2\ \Omega$; $V_P = 14.4$ V; maximum power; $V_i = 2$ V (RMS) square wave | | 70 | 75 | - | W |
| THD | total harmonic distortion | $P_o = 1$ W to 12 W; $f = 1$ kHz; $R_L = 4\ \Omega$ | | - | 0.01 | 0.1 | % |
| | | $P_o = 1$ W to 12 W; $f = 10$ kHz | | - | 0.09 | 0.3 | % |
| | | $P_o = 1$ W to 12 W; $f = 20$ kHz | | - | 0.14 | 0.4 | % |
| | | line driver mode; $V_o = 1$ V (RMS) and 5 V (RMS), $f = 20$ Hz to 20 kHz; complex load; see Figure 31 | | - | 0.02 | 0.05 | % |
| $\alpha_{cs}$ | channel separation | $f = 1$ kHz; $R_S = 1$ kΩ; $R_{ACGND} = 250\ \Omega$ | [5] | 65 | 80 | - | dB |
| | | $f = 10$ kHz; $R_S = 1$ kΩ; $R_{ACGND} = 250\ \Omega$ | [5] | 60 | 65 | - | dB |
| SVRR | supply voltage ripple rejection | 100 Hz to 10 kHz; $R_S = 1$ kΩ; $R_{ACGND} = 250\ \Omega$ | [5] | 55 | 70 | - | dB |
| CMRR | common mode rejection ratio | normal mode; $V_{cm} = 0.3$ V (p-p); $f = 1$ kHz to 3 kHz; $R_S = 1$ kΩ; $R_{ACGND} = 250\ \Omega$ | [5] | 45 | 65 | - | dB |
| $V_{cm(max)(rms)}$ | maximum common mode voltage (RMS value) | $f = 1$ kHz | | - | - | 0.6 | V |
| $V_{n(o)}$ | output noise voltage | filter 20 Hz to 22 kHz; $R_S = 1$ kΩ | | | | | |
| | | mute mode | | - | 19 | 26 | μV |
| | | line driver mode | | - | 22 | 29 | μV |
| | | normal mode | | - | 45 | 65 | μV |
| $G_v$ | voltage gain | single-ended in; differential out | | | | | |
| | | normal mode | | 25.5 | 26 | 26.5 | dB |
| | | line driver mode | | 15.5 | 16 | 16.5 | dB |

**Table 17. Characteristics** *...continued*

*Refer to Figure 29 at $V_P = V_{P1} = V_{P2} = 14.4$ V; $R_L = 4\ \Omega$; $f = 1$ kHz; $R_S = 0\ \Omega$; normal mode; unless otherwise specified. Tested at $T_{amb} = 25$ °C; guaranteed for $T_{amb} = -40$ °C to +105 °C.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $Z_i$ | input impedance | $T_{amb}$ = –40 °C to +105 °C | 50 | 70 | 95 | kΩ |
| | | $T_{amb}$ = 0 °C to 105 °C | 60 | 70 | 95 | kΩ |
| $\alpha_{mute}$ | mute attenuation | $V_o$ / $V_{o(mute)}$; $V_i$ = 50 mV | 80 | 92 | - | dB |
| $V_{o(mute)(RMS)}$ | RMS mute output voltage | $V_i$ = 1 V (RMS); filter 20 Hz to 22 kHz | - | 25 | - | μV |
| $B_p$ | power bandwidth | –1 dB | - | 20 to 20000 | - | Hz |

[1] Operation above 16 V in a 2 Ω mode with reactive load can trigger the amplifier protection. The amplifier switches off and will restart after 16 ms resulting in an 'audio hole'.

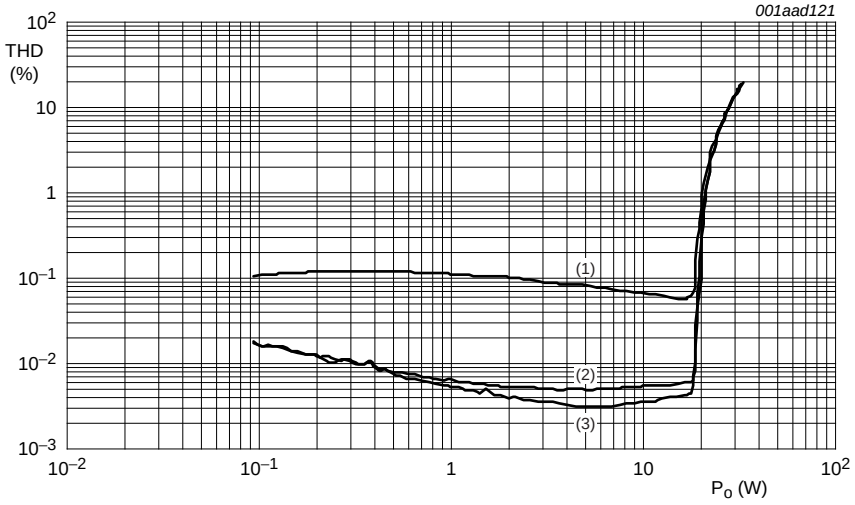
[2] $V_{STB}$ depends on the current into the STB pin: minimum = (1429 × $I_{STB}$) + 5.4 V, maximum = (3143 × $I_{STB}$) + 5.6 V.

[3] The times are specified without leakage current. For a leakage current of 10 μA on the SVR pin, the delta time is specified. If the capacitor value on the SVR pin changes with ±30 %, the specified time will also change with ±30 %. The specified times include an Equivalent Series Resistance (ESR) of 15 Ω for the capacitor on the SVR pin.

[4] Standard I²C-bus specification: maximum LOW level = 0.3 × $V_{DD}$, minimum HIGH level = 0.7 × $V_{DD}$. To comply with 5 V and 3.3 V logic, the maximal LOW level is defined by $V_{DD}$ = 5 V and the minimum HIGH level by $V_{DD}$ = 3.3 V.

[5] For optimum channel separation, supply voltage ripple rejection and common mode rejection ratio, a resistor $R_{ACGND} = \frac{R_S}{4}\ \Omega$ should be in series with the ACGND capacitor.

## 12. Performance diagrams



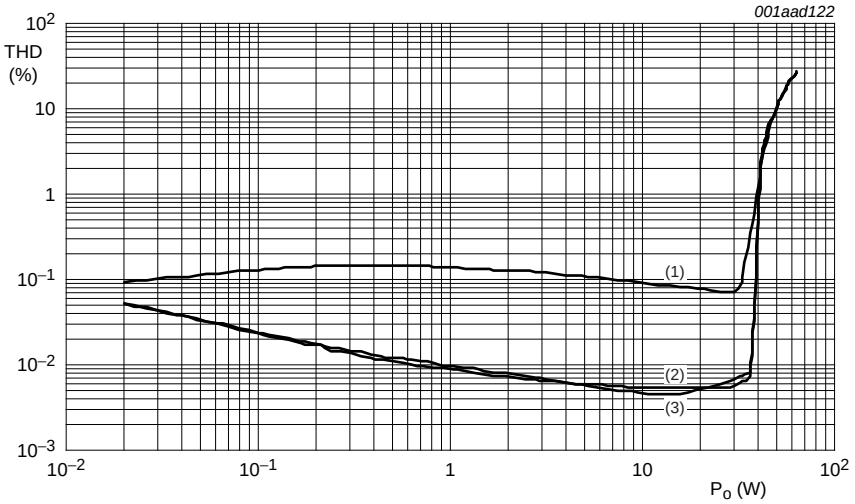

$V_P$ = 14.4 V; $R_L$ = 4 Ω.

(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

**Fig 17. Total harmonic distortion as a function of output power**



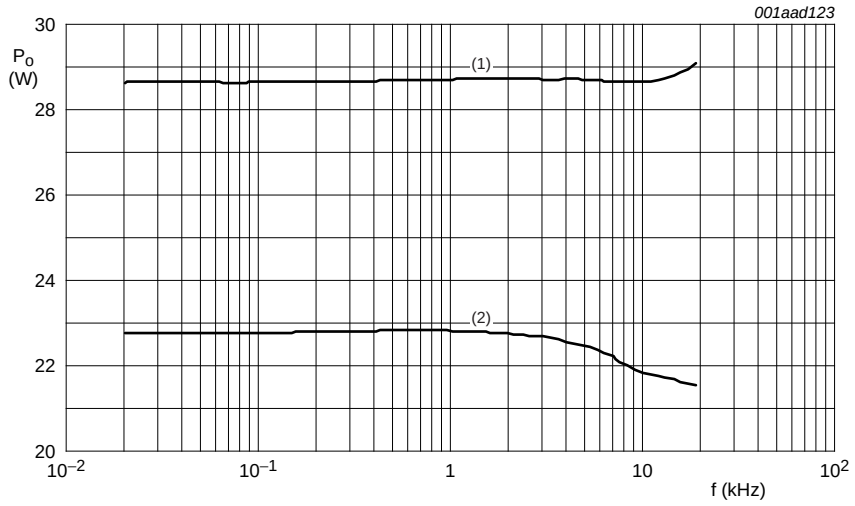

$V_P$ = 14.4 V; $R_L$ = 2 Ω.

(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

**Fig 18. Total harmonic distortion as a function of output power**

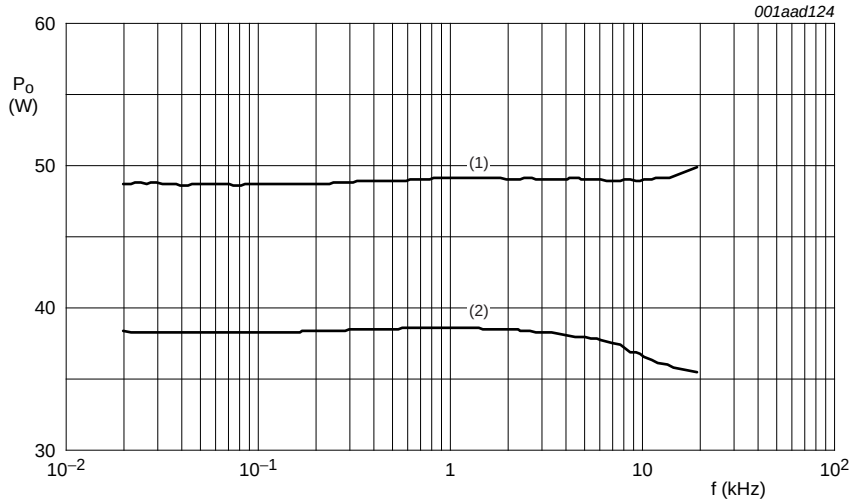



$V_P$ = 14.4 V; $R_L$ = 4 Ω.

(1) THD = 10 %.

(2) THD = 0.5 %.

**Fig 19. Output power as a function of frequency**

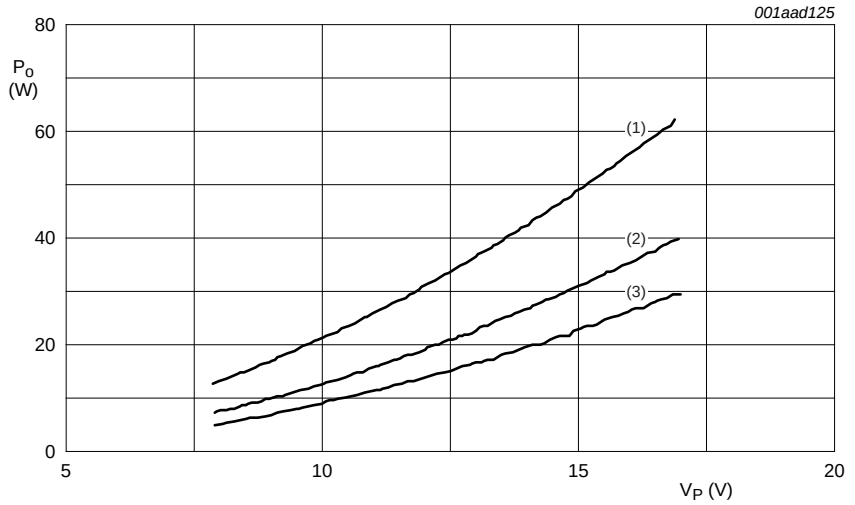



$V_P$ = 14.4 V; $R_L$ = 2 Ω.

(1) THD = 10 %.

(2) THD = 0.5 %.

**Fig 20. Output power as a function of frequency**



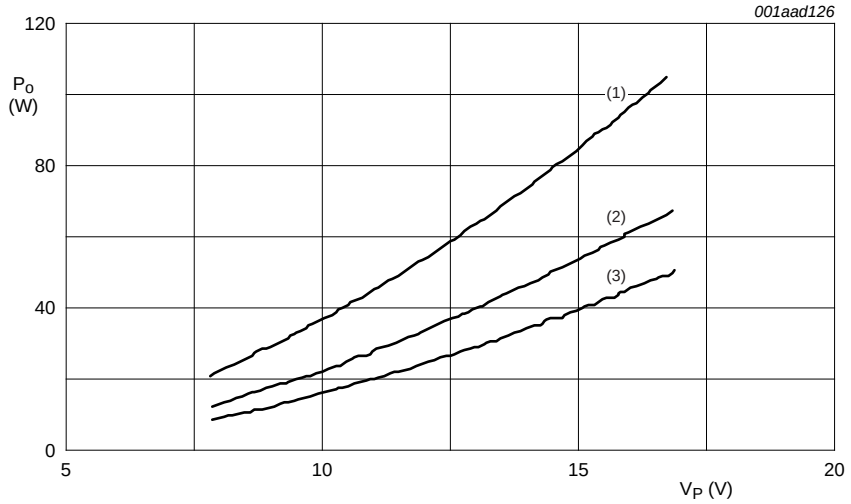

$V_P$ = 14.4 V; $R_L$ = 4 Ω.

(1) $P_{o(max)}$.

(2) THD = 10 %.

(3) THD = 0.5 %.

**Fig 21. Output power as a function of supply voltage**



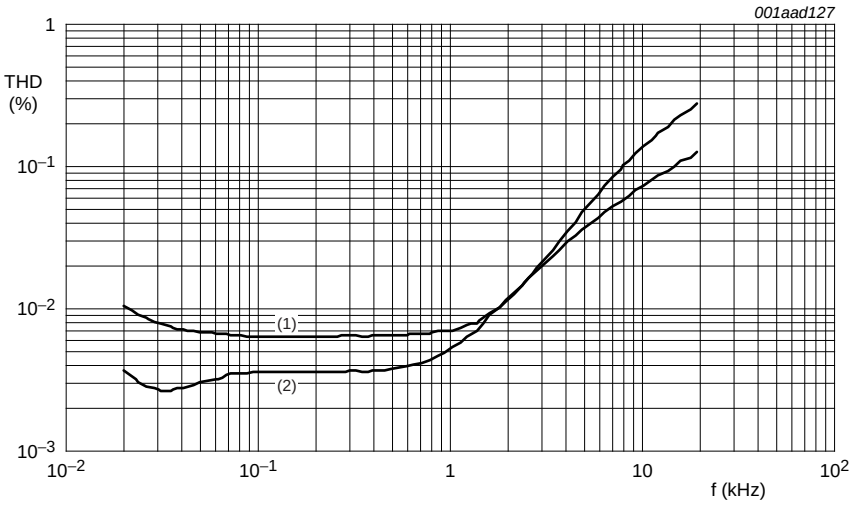

$V_P$ = 14.4 V; $R_L$ = 2 Ω.

(1) $P_{o(max)}$.

(2) THD = 10 %.

(3) THD = 0.5 %.

**Fig 22. Output power as a function of supply voltage**

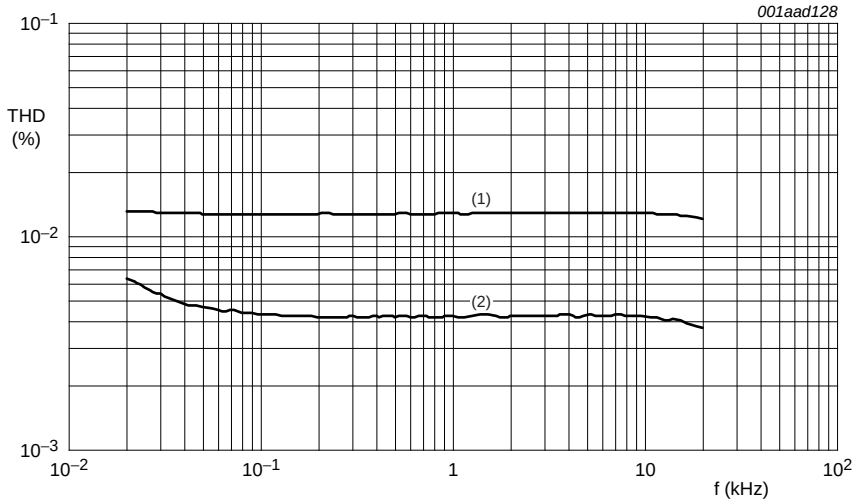



$V_P$ = 14.4 V; $R_L$ = 4 Ω.

(1) $P_o$ = 1 W.

(2) $P_o$ = 10 W.

**Fig 23. Total harmonic distortion as a function of frequency; in normal mode**

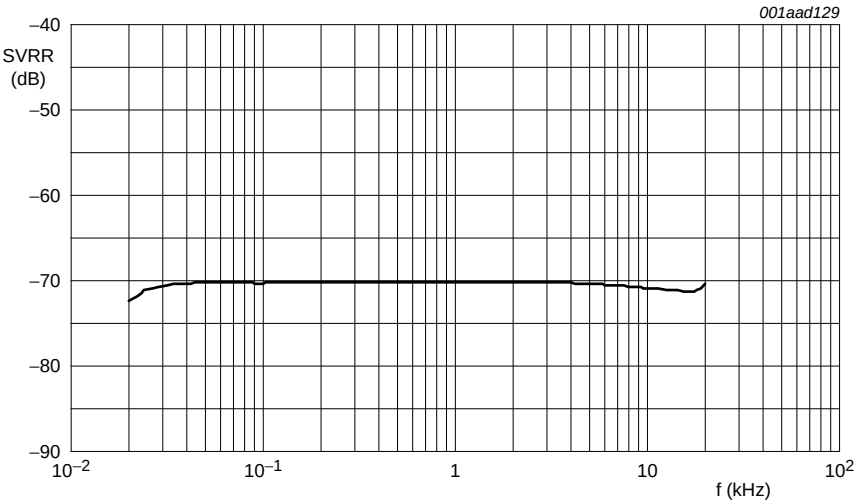



$V_P$ = 14.4 V; $R_L$ = 600 Ω.

(1) $V_o$ = 1 V.

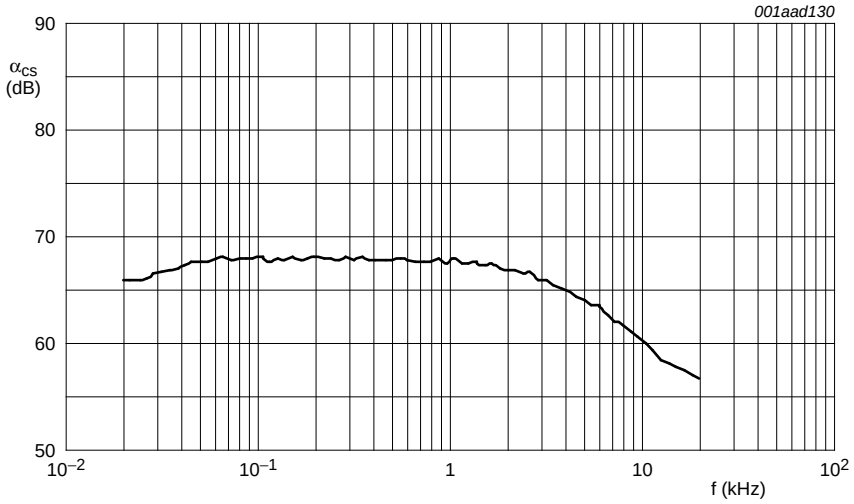
(2) $V_o$ = 5 V; front channels.

**Fig 24. Total harmonic distortion as a function of frequency in line driver mode**



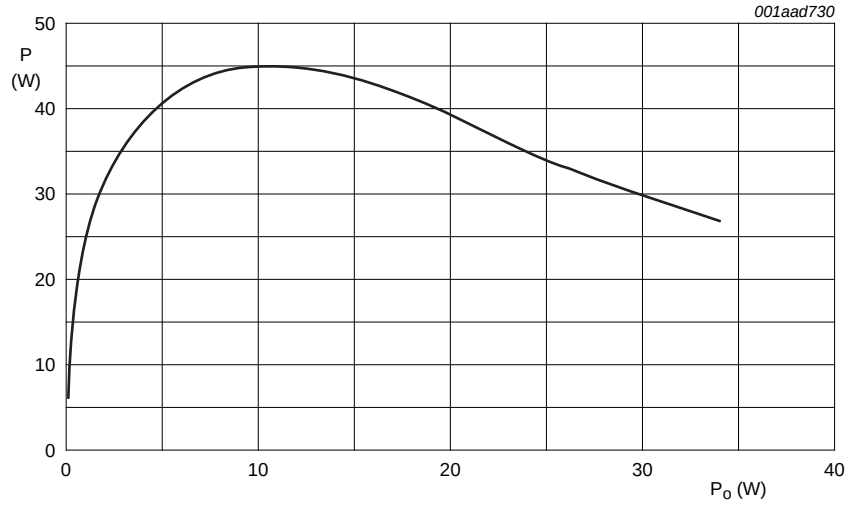

$V_P$ = 14.4 V; $R_L$ = 4 Ω; $R_S$ = 1 kΩ; $V_{ripple}$ = 2 V (p-p).

**Fig 25. Supply voltage ripple rejection as a function of frequency**



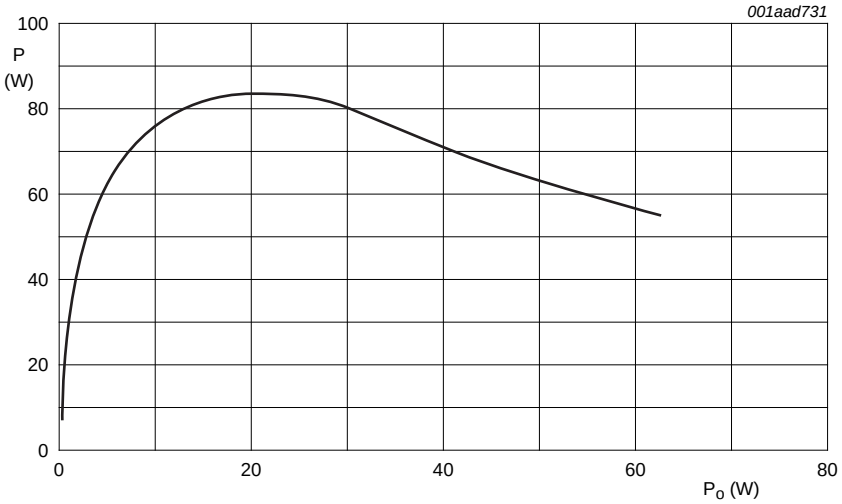

$V_P$ = 14.4 V; $R_L$ = 4 Ω; $R_S$ = 1 kΩ; $P_o$ = 1 W.

**Fig 26. Channel separation as a function of frequency**




$V_P$ = 14.4 V; $R_L$ = 4 Ω; f = 1 kHz.

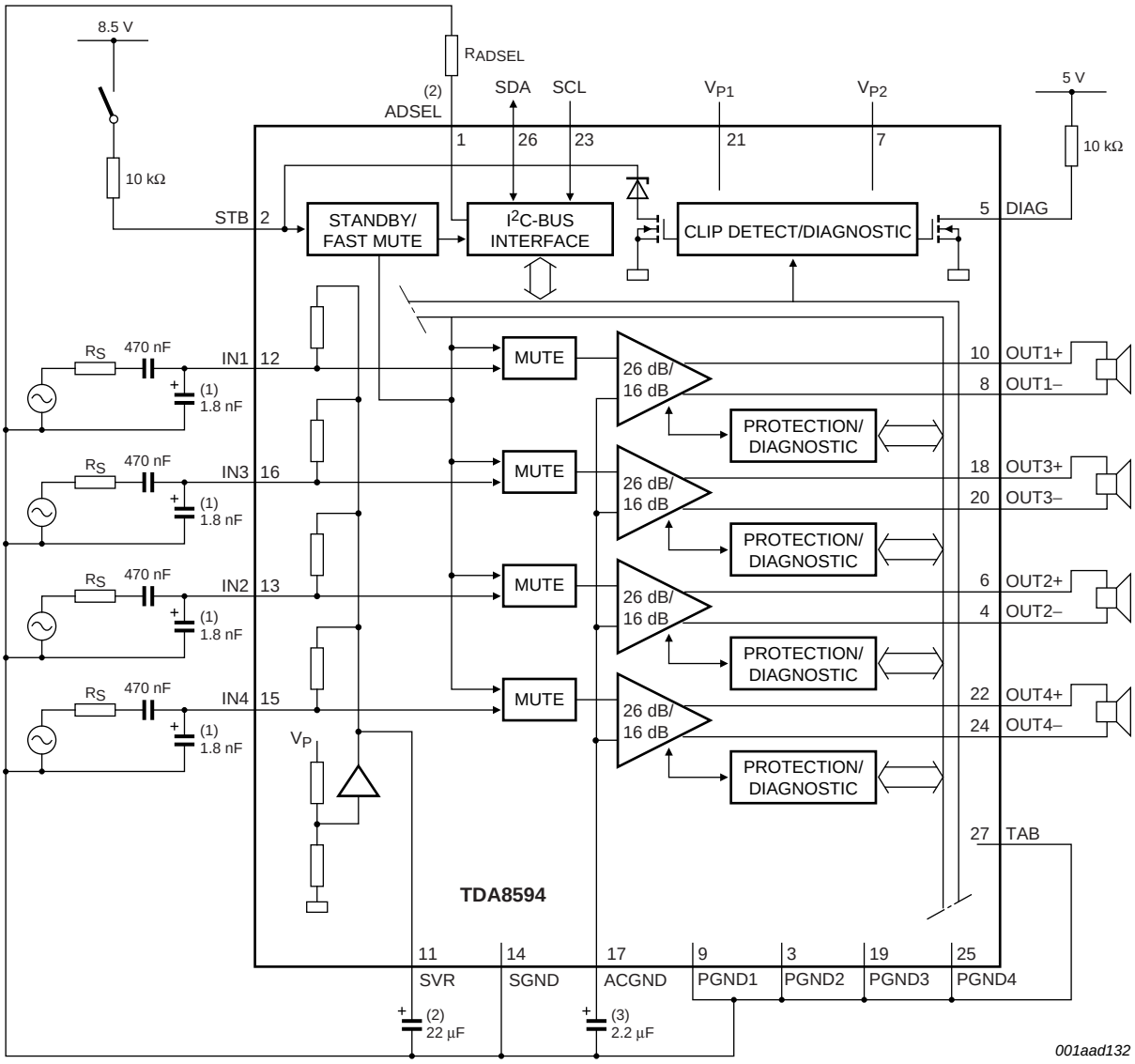
**Fig 27. Power dissipation as a function of output power**




$V_P$ = 14.4 V; $R_L$ = 2 Ω; f = 1 kHz.

**Fig 28. Power dissipation as a function of output power**

## 13. Application information




For EMC reasons, a 10 nF capacitor (not shown) can be added from each amplifier output to ground.

(1) For EMC reasons a capacitor of 1.8 nF from the input pin to SGND is advised (optional).

(2) The SVR and ACGND capacitors and the $R_{ADSEL}$ resistor should first be connected to SGND before connecting to PGNDn pins.

(3) ACGND capacitor value must be close to 4 × input capacitor value; 4 × 470 nF capacitors can be used as an alternative to the 2.2 µF capacitor shown.

**Fig 29. Test and application diagram**

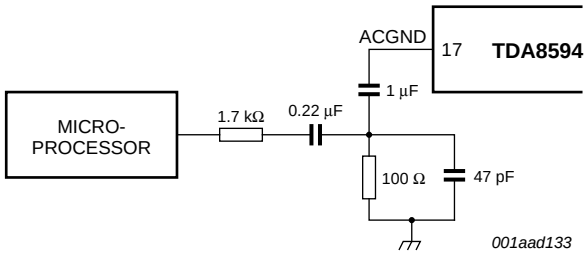



**Fig 30. Beep input circuit (gain = 0 dB) to apply a microprocessor beep signal to all four amplifiers**

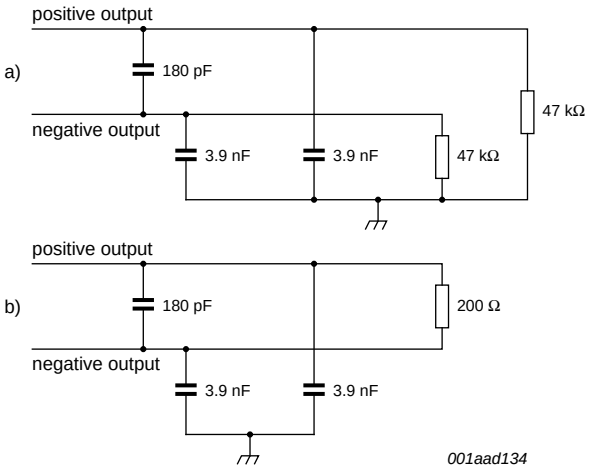



**Fig 31. Complex loads for measuring THD in line driver mode**

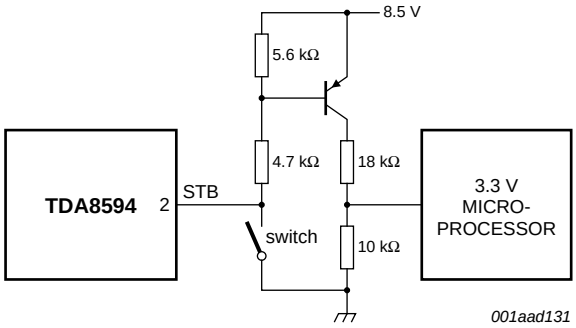
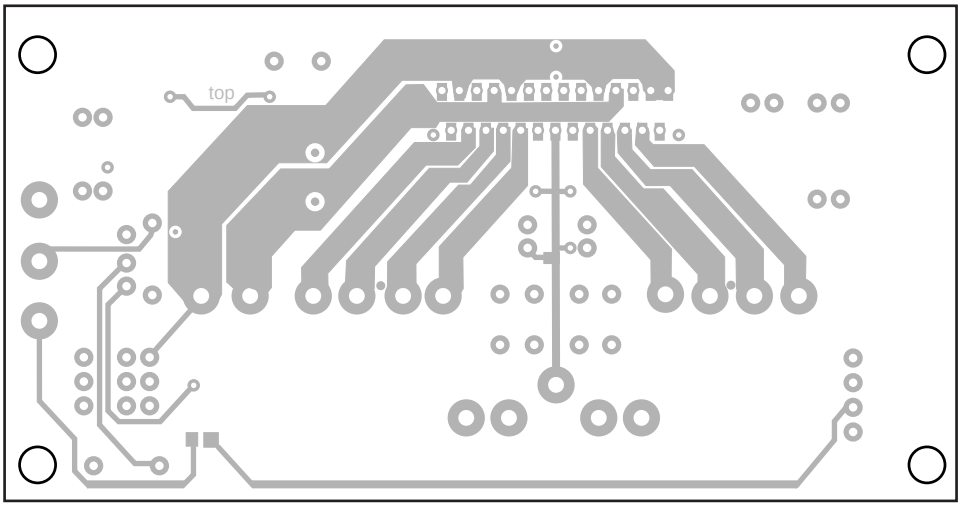


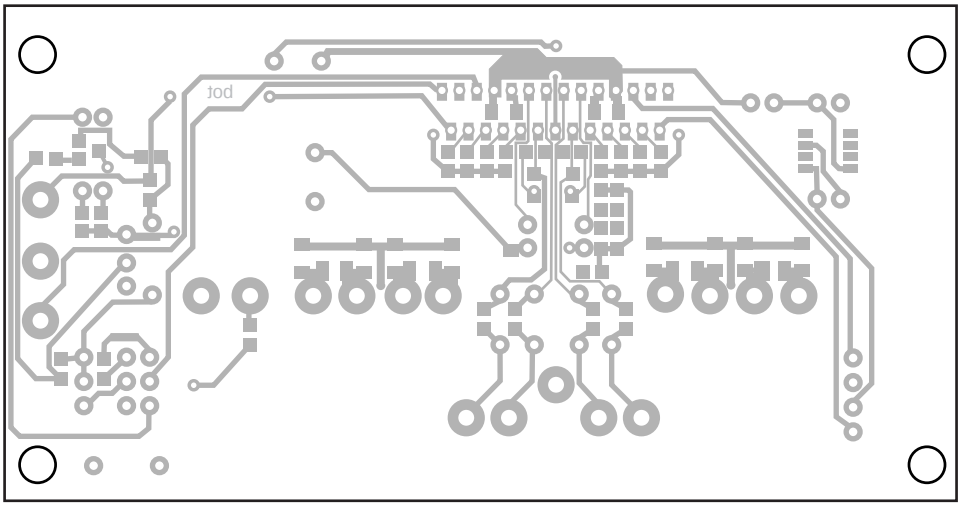

**Fig 32. Circuit for combined mode selection and clip detection functions on pin STB**

## 13.1 PCB layout



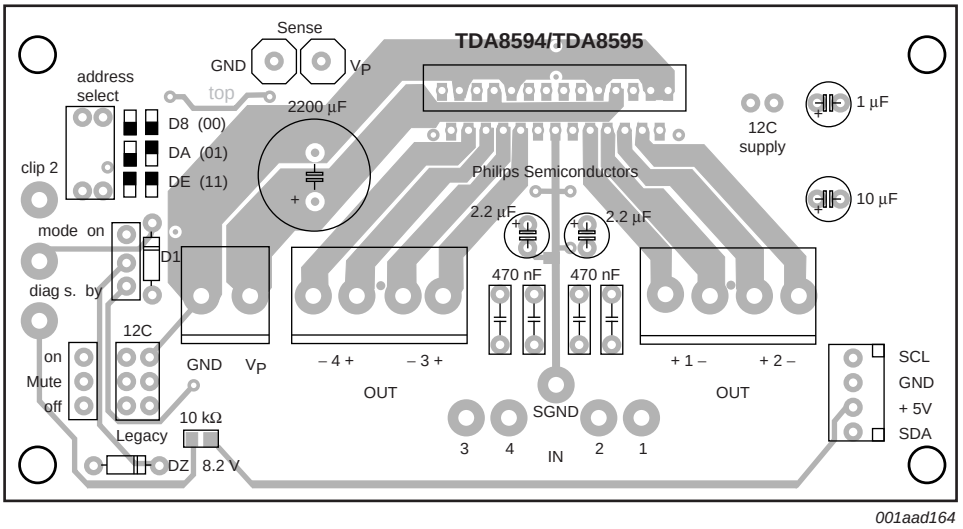

001aad162

**Fig 33. PCB layout of test and application circuit; copper layer top**



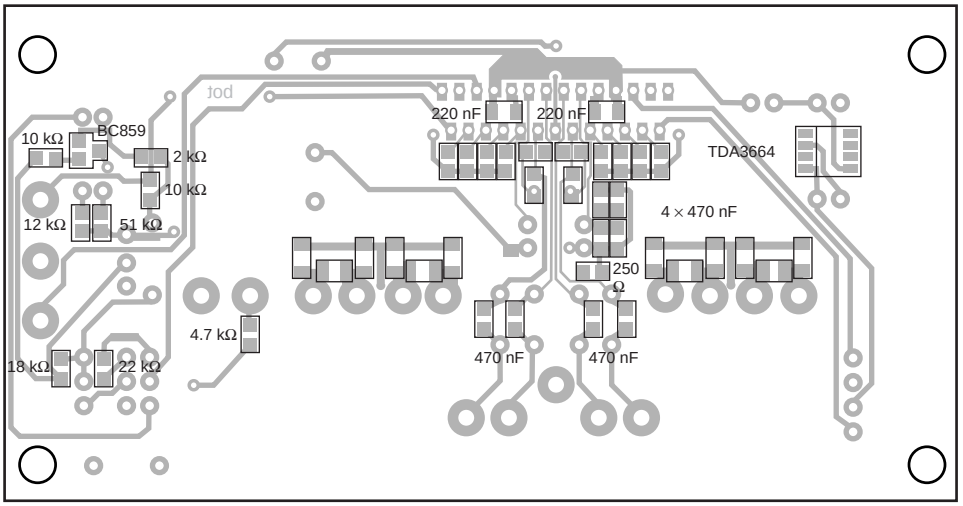
001aad163

**Fig 34. PCB layout of test and application circuit; copper layer bottom (top view)**




001aad164

**Fig 35. PCB layout of test and application circuit; components top**




001aad165

**Fig 36. PCB layout of test and application circuit; components bottom (top view)**

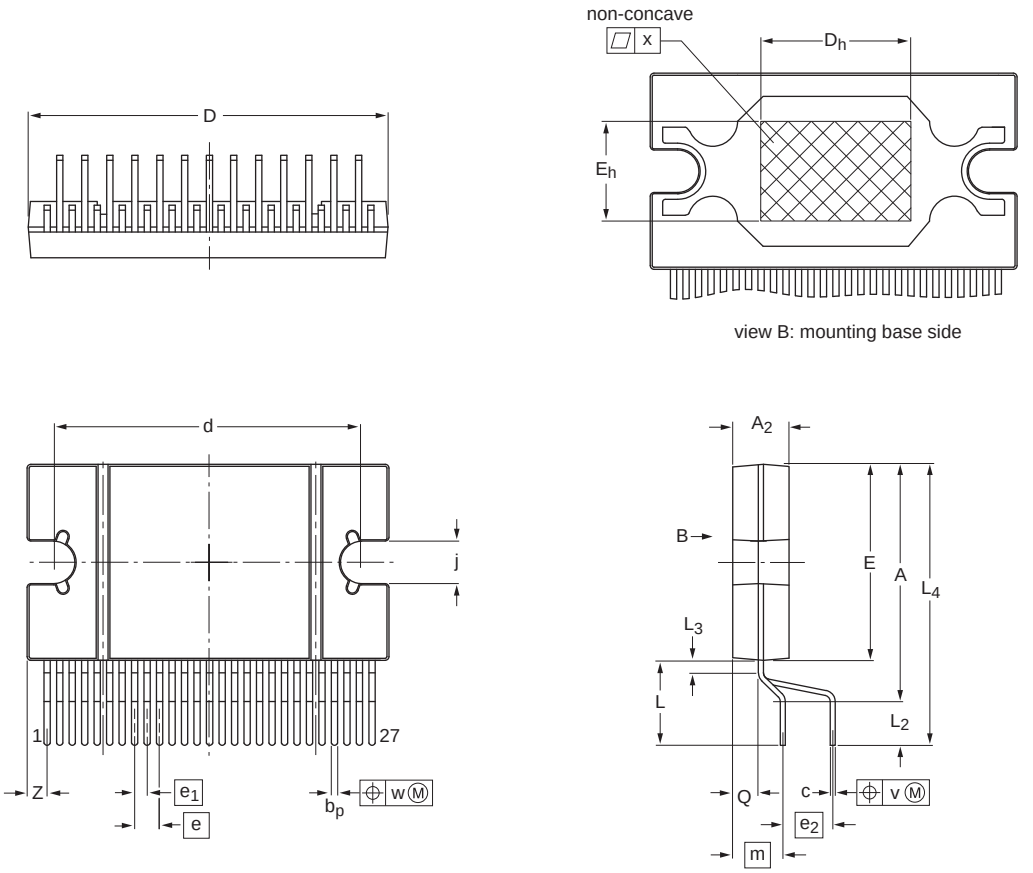
# 14. Test information

## 14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

## 15. Package outline

**DBS27P: plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)** **SOT827-1**




| x | $Z^{(1)}$ |
|---|---|
| 0.03 | 1.8 |
| | 1.2 |

Dimensions (mm are the original dimensions)

| Unit | | A | $A_2$ | $b_p$ | c | $D^{(1)}$ | d | $D_h$ | $E^{(1)}$ | e | $e_1$ | $e_2$ | $E_h$ | j | L | $L_2$ | $L_3$ | $L_4$ | m | Q | v | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 19 | 4.6 | 0.60 | 0.5 | 29.2 | 24.8 | 12 | 15.9 | 2 | 1 | 4 | 8 | 3.55 | 6.8 | 3.9 | 1.15 | 22.9 | 4 | 2.1 | 0.6 | 0.25 |
| | nom | | | | | | | | | | | | | 3.40 | | | | | | | | |
| | min | | 4.4 | 0.45 | 0.3 | 28.8 | 24.4 | | 15.5 | | | | | 3.25 | | 3.1 | 0.85 | 22.1 | | 1.8 | | |

Note

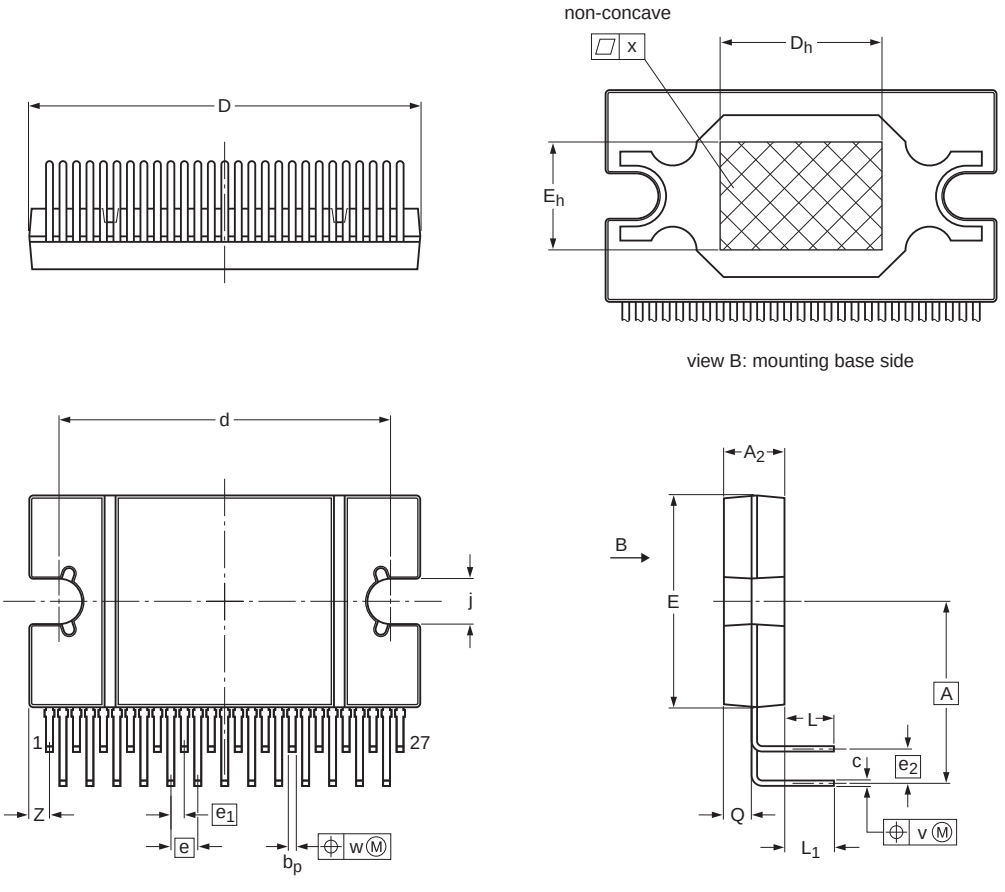
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

*sot827-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT827-1 | | | | | | ~~13-02-13~~ 13-05-30 |

**Fig 37. Package outline SOT827-1 (DBS27P)**

**RDBS27P: plastic rectangular-DIL-bent-SIL (reverse bent) power package; 27 leads (row spacing 2.54 mm)** **SOT878-1**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_2$ | $b_p$ | c | $D^{(1)}$ | d | $D_h$ | $E^{(1)}$ | e | $e_1$ | $e_2$ | $E_h$ | j | L | $L_1$ | Q | v | w | x | $Z^{(1)}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | | 4.6 | 0.60 | 0.5 | 29.2 | 24.8 | | 15.9 | | | | | 3.55 | 3.75 | 3.75 | 2.1 | | | | 1.8 |
| | nom | 13.5 | | | | | | 12 | | 2 | 1 | 2.54 | 8 | 3.40 | | | | 0.6 | 0.25 | 0.03 | |
| | min | | 4.4 | 0.45 | 0.3 | 28.8 | 24.4 | | 15.5 | | | | | 3.25 | 3.15 | 3.15 | 1.8 | | | | 1.2 |

Note

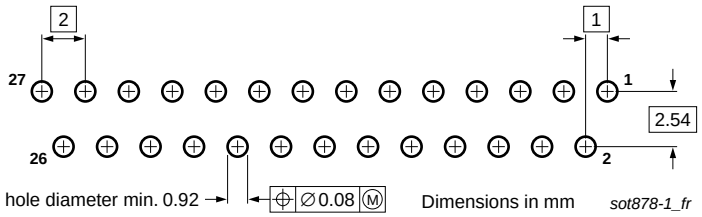
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

*sot878-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT878-1 | | | | | | ~~12-12-19~~ 13-02-13 |

**Fig 38. Package outline SOT878-1 (RDBS27P)**

# 16. Mounting




Dimensions in mm.

Reflow soldering is the recommended soldering method.

Dimension '1' relates to dimension '$e_1$' in Figure 38; dimension '2' relates to dimension '$e_2$' in Figure 38.

**Fig 39. SOT878-1 reflow soldering footprint**

# 17. Abbreviations

**Table 18. Abbreviations**

| Acronym | Description |
|---|---|
| $\overline{\text{ACK}}$ | ACKnowledge not |
| BCDMOS | Bipolar CMOS/DMOS |
| BTL | Bridge Tied Load |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DMOS | Double-diffused Metal-Oxide Semiconductor |
| DSP | Digital Signal Processor |
| EMC | ElectroMagnetic Compatibility |
| ESR | Equivalent Series Resistance |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| NMOS | Negative-channel Metal-Oxide Semiconductor |
| PMOS | Positive-channel Metal-Oxide Semiconductor |
| PCB | Printed-Circuit Board |
| POR | Power-On Reset |
| SOAR | Safe Operating ARea |
| SOI | Silicon On Insulator |

# 18. Revision history

**Table 19. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TDA8594 v.5 | 20130611 | Product data sheet | - | TDA8594_4 |
| Modifications: | • The package outline Figure 37 has been updated. | | | |
| TDA8594 v.4 | 20130226 | Product data sheet | - | TDA8594_3 |
| Modifications: | • The data sheet template has been updated to the latest version. | | | |
| TDA8594 v.3 | 20130221 | Product data sheet | - | TDA8594_2 |
| Modifications: | • The package outline figures, Figure 37 and Figure 38, have been updated. | | | |
| TDA8594_2 | 20071211 | Product data sheet | - | TDA8594_1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section 2.1 and Section 14: Added device qualification “AEC-Q100 qualification”.<br>• Figure 1 and Figure 29: Changed internal circuit on pin SVR.<br>• Figure 32: Value of base-emitter resistor changed to 5.6 kΩ.<br>• Table 17, Diagnostic:<br>– Symbols and parameters of “junction temperature” characteristics updated (4×).<br>– (Old) symbol and parameter “$I_{oM}$ = peak current output” changed to “$I_{th(o)det(load)AC}$ = AC load detection output threshold current”. | | | |
| TDA8594_1 (9397 750 15066) | 20060302 | Product data sheet | - | - |

# 19. Legal information

## 19.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 20. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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