DATA SHEET

TDA8433
Deflection processor for computer controlled TV receivers

Product specification
File under Integrated Circuits, IC02

August 1991

Philips
Semiconductors

PHILIPS

Deflection processor for computer controlled TV receivers

TDA8433

FEATURES

- I²C-bus interface
- Input for vertical sync
- Sawtooth generator with amplitude independent of frequency
- Vertical deflection output stage driver
- East-west raster correction drive output
- EHT modulation input
- Changes picture width and height without affecting geometry.

GENERAL DESCRIPTION

The TDA8433 is an I²C-bus controlled deflection processor which, together with a sync processor (e.g. TDA2579A, see Fig.6), contains the control and drive functions of the deflection part in a computer controlled TV receiver. The TDA8433 replaces all picture geometry settings which were previously set manually during manufacture.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage (pin 12)	10.8	12.0	13.2	V
I_{CC}	supply current (pin 12)	12	20	27	mA
V_2	vertical sync trigger level	–	3	–	V
V_{21}	vertical feedback (note 1)				
	DC level	–1.7	1.85	2.05	V
	AC level	1.65	1.8	1.95	V_P
V_{24}	EHT compensation operating range	1.7	–	6	V
V_{11-13}	inputs for control register data:				
	not locked to video	–	0.7	1	V
	at 50 Hz status	0.8 V_{CC}	–	–	V
	at 60 Hz status	–	–	0.7 V_{CC}	V
V_{10-13}	HCENT comparator switching level	–	V_{17}	–	V
V_{14-13}	SDA I²C-bus switching level data input	–	3.5	–	V
V_{15}	SCL I²C-bus switching level clock input	–	3.5	–	V
V_1	device selection where:				
	Ao = '1'	9.0	–	V_{CC}	V
	Ao = '0'	0	–	2.0	V

Note to quick reference data

1. VR_{in} = 0; V-S-corr = 0; V_{shift} = 20 H; V_{ampl} = 20 H.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8433	24	DIL	plastic	SOT101(1)

Note

1. SOT101-1; 1996 December 2.

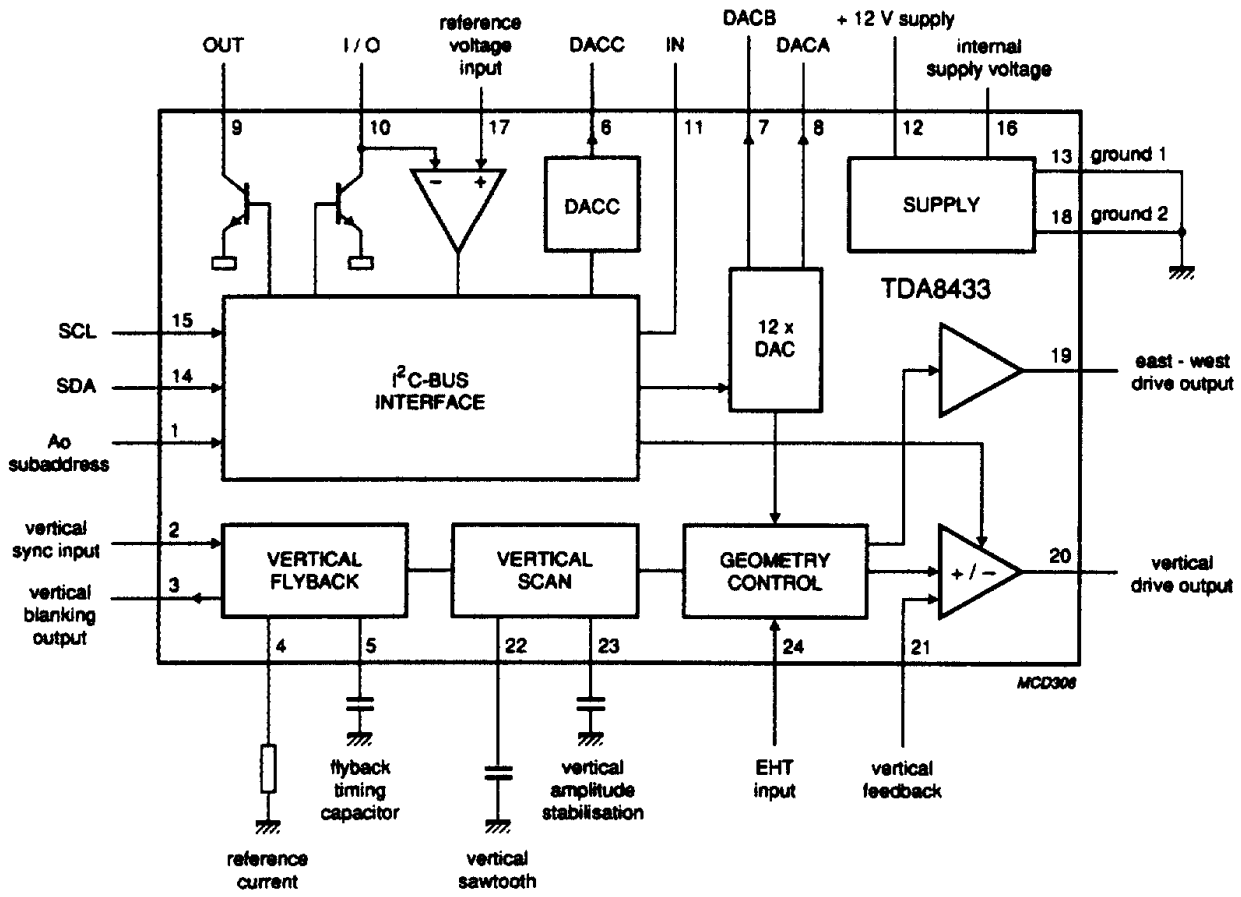


Fig.1 Block diagram.

PINNING

PIN	DESCRIPTION
1	Ao subaddress
2	vertical sync input
3	vertical blanking output
4	I_{ref} resistor
5	vertical blanking/flyback timing capacitor
6	DACC (tau switching)
7	DACB (horizontal phase)
8	DACA (horizontal frequency)
9	OUT (video switch)
10	I/O (f_o adjustment)
11	IN (HLOCKN –50/60 Hz)
12	positive supply +12 V
13	ground 1
14	serial data input
15	serial clock input
16	internal supply voltage
17	voltage reference for I/O
18	ground 2 (waveform)
19	east-west drive output
20	vertical drive output
21	vertical feedback
22	vertical sawtooth capacitor
23	vertical amplitude capacitor
24	EHT input

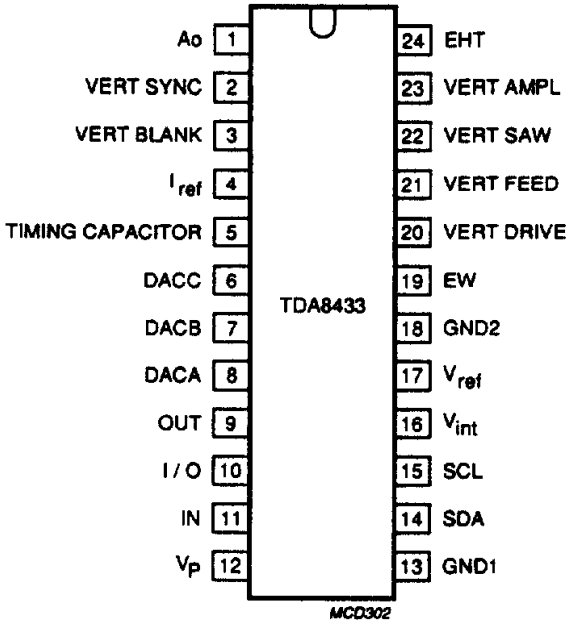


Fig.2 Pinning diagram.

PIN FUNCTIONS

Pin 1 - Ao subaddress

The Ao bit is the least significant bit of the bus-address. It enables two TDA8433s, with different addresses, to be connected to the same bus.

Pin 2 - Vertical sync input

Positive trigger pulses of > 3 V are sufficient to exceed the internal threshold of the ramp generator. Flyback and blanking will then start and, during the blanking period, the circuit will be inhibited for further input pulses (see Fig.3). It should be noted that the TDA8433 has no vertical oscillator therefore, the sync processor, which is used in this combination, has to provide trigger pulses as well when the video input is absent.

Pin 3 - Vertical blanking

The positive going blanking pulse is fed from a current source. The blanking period is fixed by the capacitor connected to pin 5 and the resistor connected to pin 4 (see Fig.3).

Pins 4 and 5 - Reference/flyback timing

The external resistor connected between pin 4 and ground provides a reference current for the triangle generator circuit. This circuit generates the triangle waveform at pin 5. The width of the blanking pulse is set by the external capacitor connected to pin 5.

Table 1 Sync processor time constants

VTRA	VTRC	OUTPUT	TIME CONSTANT
'0'	'0'	12 V	automatic operation
'0'	'1'	5.3 V	medium
'1'	'0'	1.5 V	fast (video recorder)
'1'	'1'	0.2 V	not to be used

Pin 6 - DACC (tau switching)

The output voltage, which depends on the VTRA and VTRC bits in the I^2C-bus control register, is connected to the coincidence detector of the sync processor. In this way the time constants of the horizontal PLL (in the sync processor) can be set. If the TDA2579 is used (see Fig.6) the effect will be as listed in Table 1.

Pin 7 - DACB (horizontal phase)

The voltage at pin 7 is fed to the horizontal pulse modulator in the sync processor. This voltage, together with the signal produced by the phase 2 detector during horizontal flyback, sets the phase of the horizontal output with respect to the flyback pulse in the horizontal output stage. The voltage range is variable between 0.05 V and 10 V.

Pin 8 - DACA (horizontal frequency)

The frequency of the horizontal oscillator in the external sync processor is adjusted by the voltage level at pin 8. The voltage is variable in 63 steps from 0.05 V to 10 V (i.e. 0.158 V per step).

Pin 9 - OUT (video switch)

The output at pin 9 is controlled by the CVBS bit from the control register where

CVBS = logic 0; the output is HIGH (open collector)

CVBS = logic 1; the output is LOW (saturation voltage)

An external video selector can be controlled by means of this switching function.

Pins 10 and 17 - I/O and Voltage reference

Pin 10 is connected to the output of the phase 1 detector in the sync processor. Whether the pin is used as an input or an output is dependent on the PHI1 bit of the horizontal frequency (HFREQ) register. When PHI = logic 0 (output transistor open) pin 10 is used as an input. The DC information at this pin is compared with the reference voltage at pin 17 and is reflected in the HCENT of the status register.

HCENT = logic 0; input > V_{ref} at V_{17}

HCENT = logic 1; input < V_{ref} at V_{17}

In this way the free running frequency can be adjusted by computer while the oscillator is locked. Alternatively, when PHI1 = logic 1, pin 10 is switched to ground. The free running frequency of the oscillator can the be adjusted while watching the screen provided that pin 10 is connected to the video input of the sync processor.

Pin 11 -IN (HLOCKN and 50/60 Hz)

This pin is connected to the combined MUTE and 50/60 Hz pin of the sync processor. The various DC levels define the state of the HLOCKN and 50/60 Hz bits in the status register (see Table 2.)

Table 2 Status register bits

STATE OF SYNC PROCESSOR (TDA2579)	TYPICAL VOLTAGE AT PIN 11	STATE OF	
		HLOCKN	50/60 Hz
Not locked to computer video	< 0.7 V(min.)	'1'	'0'
60 Hz transmitter found	0.7 to 0.75 V_{CC}	'0'	'0'
50 Hz transmitter found	> 0.75 V_{CC} to V_{CC}	'0'	'1'

Pin 12 - Positive supply (12 V)

The nominal supply voltage at pin 12 is 12 V which should remain within the defined limits. The nominal current consumption is 20 mA.

Pins 13 and 18 - Ground (1 and 2)

Ground 1 (pin 13) is for the bus transceiver section
Ground 2 (pin 18) is for the sawtooth and picture geometry control section.

Pins 14 and 15 - SDA and SCL (serial data and serial clock)

Input serial data is applied to pin 14. The serial clock input from the I^2C-bus is applied to pin 15.

Pin 16 - Internal supply voltage (+5 V)

In some applications it may be necessary to connect a capacitor to this pin to avoid interference.

Pin 19 - East-west drive output

The output drive for the East-west correction circuit has a nominal range from 1.6 to 11.7 V and contains 5 programmable parameters (see Fig.5). The parameters are:

- Picture width
- East-west raster correction
- East-west trapezium correction
- East-west corner correction
- Compensation for EHT variations

Pins 20 and 21 - Vertical drive output and vertical feedback input

The vertical comparator and drive output stage is designed so that the feedback signal applied to pin 21 can be inverted in the comparator by the V-out control bit. This enables the use of two different vertical output stages. One output stage is without an internal comparator (e.g. TDA3654). The feedback signal at pin 21 has a negative slope during scan. During power-up the IC is adapted (preset) for this type of output stage. The other output stage contains a comparator. The drive for this output stage is obtained by interconnecting pins 20 and 21 and switching the V-out polarity. The V-out bit will then be set to logic 1. In both cases the drive signal available at pin 20 contains 5 parameters which can be set via the I^2C-bus control;

- Picture height
- Vertical linearity
- Vertical S-correction
- Vertical shift
- Extent of compensation for EHT variations (see Fig.4.)

Pins 22 and 23 - Vertical sawtooth/vertical amplitude capacitor

The 100 nF capacitor connected to pin 22 is charged and discharged by two current sources in the vertical ramp generator. In order to obtain an equal amplitude, at different frequencies, an amplitude comparator has been incorporated. The circuit, together with the 330 nF capacitor connected to pin 23, keeps the sawtooth amplitude at reference voltage level (7.1 V). The external load of the amplitude stabilization loop of pin 23 should be as low as possible. The recommended value is ≥ 500 MΩ.

Pin 24 - EHT input (Modulation)

A voltage between 1.7 and 6 V (depending on the EHT variations) applied to pin 24 will modulate the amplitude of the vertical drive sawtooth and the East-west drive output. In this way the effect of beam current variations can be virtually eliminated.

I^2C-BUS CONTROL

The addresses for the I^2C-bus are 100011Ao0 (write) and 100011Ao1 (read). The inclusion of the Ao bit makes it possible to control two different deflection processors. After receiving the address byte the I^2C-bus transmits its status byte in which the status of the control bits is contained.

PONRES - Power-on-reset

After switch-on, or a power dip below 6.7 V, the PONRES bit is set to logic 1. After a status read operation PONRES is reset to logic 0.

HLOCKN - Horizontal lock

This bit indicates whether the horizontal oscillator in the sync processor is locked to the video signal. When the oscillator is locked HLOCKN is set to logic 0 ($V_{11} > 0.7$ V). When the oscillator is not locked HLOCKN is set to logic 1 ($V_{11} < 0.7$ V).

HCENT - Horizontal centre

This bit is set to logic 0 when the horizontal oscillator frequency is too high ($V_{10} > V_{ref}$). The bit is set to logic 1 when the frequency is too low $V_{10} < V_{ref}$).

IN - 50/60 Hz

The voltage at pin 11 also contains the 50/60 Hz information where:

logic 0 = ≤ V_{11} 0.75 V_{CC} (60 Hz or no transmitter)
logic 1 = ≥ V_{11} 0.75 V_{CC} (50 Hz)

The sequence of data in the status byte is: PONRES, HLOCKN, 50/60 Hz, 0 0 0 0.

A write operation starts with address byte 100011Ao0. The device is then ready to receive the subaddress byte e.g. trapezium (HEXOA) 00001010 followed by the data byte e.g. HEX20. The DAC will then set the trapezium correction signal into the selected position (see Fig.5). If more data bytes follow within one transmission then, by means of an auto-increment, the next highest subaddress will be selected. Wrap-around occurs after HEXOF.

Table 3 Registers

FUNCTION	SUB ADDR HEX	DATA BITS	PRESET VALUE HEX	SETT HEX	MIN.	TYP.	MAX.	UNIT
H-frequency	00	PHI-X-6	01	00 3F	– 9.5	0.05 10	0.2 11	V V
H-phase	01	6	01	00 3F	– 9.5	0.05 10	0.2 11	V V
Picture height $V_{21/20}$	02	6	01	00 3F	– +15	–19 +19	–22 –	% %
V-linearity	03	6	01	00 3F	0 13	– 17	1 21	% %
V-S correction	04	6	01	00 3F	0 15	– 19	1 –	% %
V-shift	05	6	01	00 3F	+17 –17	+19 –19	+22 +22	% %
V-compensation V_{24} = 1.7 V	06	5	01	00 1F	tbf –8	0 –10	– –12	– %
Picture width	07	6	01	00 3F	– 6.0	1.6 6.6	2.4 7.2	V V
E-W parabola (Reg: 07 = 0)	08	6	01	00 3F	– 7.0	0.07 7.5	0.1 8.5	V V
E-W corner (Reg: 08 = 3F)	09	6	01	00 3F	– 1.7	0 2.2	tbf 2.8	V V
Trapezium Reg: 07 = 00; 08 = 20H	0A	6	01	00 3F	0.75 1.0	1.25 1.9	– –	V V
H-compensation Reg. 07 = 00; 08 = 0; 09 = 00 V_{24} = 1.7 V	0B	5	01	00 1F	0 –	tbf 10	– –	% %

FUNCTION	SUB ADDR HEX	DATA BITS	PRESET VALUE HEX	SETT HEX	MIN.	TYP.	MAX.	UNIT
Not used	0C/0E	–	–		–	–	–	–
Control	0F	X-VOUT	–	40	11.5	11.9	V_{CC}	V
		VTRA–VTRC	–	50	5.0	5.3	5.6	V
		CVBS–X–X–X	–	60	1.2	1.5	1.8	V
				70	0	0.2	0.5	V
				40	5.5	7.5	9.5	kΩ
				50	2.4	3.3	4.2	kΩ
				60	0.7	1.0	1.35	kΩ
				70	–	50	–	Ω
				00	–	–	(VBS)	V
				08	–	–	0.4 (1 mA)	V
PHI1 bit	00	1	–	80	–	–	0.4 (–2 mA)	V
				00	–	–	V_{CC}	V
Not used	10–EF							
Test functions	F0–FF							

Note to Table 3

1. tbf = value to be fixed.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	10.8	13.2	V
I_{CC}	supply current	12	27	mA
P_{tot}	total power dissipation	–	360	mW
T_{amb}	operating ambient temperature range	–25	+75	°C
T_{stg}	storage temperature range	–55	+150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	–	35	K/W

CHARACTERISTICS

V_{CC} = 12 V; V_{24} = 1/2 x V_{CC}; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage (pin 12)		10.8	12.0	13.2	V
I_{CC}	supply current (pin 12)		12	20	27	mA
Ao subaddresses (pin 1)						
V_1	switching level allowed voltage for A_O = '0' for Ao = '1'	note 1	– – 9	2.3 – –	– 2 V_{CC}	V V V
I_1	input current		–	–	+10	µA
V_1	not allowed voltage range		2.0	–	8.9	V
Vertical sync input (pin 2)						
V_2	switching level		2.5	3.0	3.5	V
I_2	current during non-active state	V_2 = 0 V	–	3	10	µA
Vertical blanking output (pin 3)						
$V_{3(p-p)}$	pulse amplitude (peak-to-peak value)	1 mA load	–	–	V_{CC}–2	V
V_3	output voltage	1 mA load	10.0	10.5	–	V
I_O	output source current		1	–	–	mA
t_W	pulse width	R_4 = 75 kΩ C_5 = 8.2 nF	–	1.13	–	ms
Reference (pin 4)						
V_4	reference voltage		6.8	7.15	7.5	V
I_4	current range		90	–	150	µA
Vertical blanking timing (pin 5)						
$V_{5(p-p)}$	amplitude of triangular pulse (peak-to-peak value)	R_4 = 75 kΩ C_5 = 8.2 nF	7.5	7.9	8.3	V
t_W	width of triangular pulse		–	1.3	–	ms
I_5	sink current	V_5 = 3.5 V; I_4 = 100 µA	85	105	125	µA
I_5	source current	V_5 = 3.5 V; I_4 = 100 µA	80	100	120	µA
DACC output (pin 6)						
V_6	voltages at VTR(A) and VTR(C) where: (A) = '0'; (C) = '0' (A) = '0'; (C) = '1' (A) = '1" (C) = '0' (A) = '1'; (C) = '1'		 11.5 5.0 1.2 0	 11.9 5.3 1.5 0.2	 – 5.6 1.8 0.5	 V V V V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACC output (pin 6)						
Z_6	output impedance at VTR(A) and VTR(C) where:					
	(A) = '0'; (C) = '0'		5.5	7.5	9.5	kΩ
	(A) = '0'; (C) = '1'		2.4	3.3	4.2	kΩ
	(A) = '1'; (C) = '0'		0.7	1.0	1.35	kΩ
	(A) = '1'; (C) = '1'		–	50	–	Ω
DACB horizontal phase (pin 7)						
V_7	output voltage					
	at HEX00		–	0.05	0.2	V
	at HEX3F		9.4	10.0	11.0	V
ΔV_7	variable DC output voltage for setting horizontal frequency		0.05	–	10	V
R_7	internal resistance		–	0.3	1.0	kΩ
	step size	note 3	10	–	190	%
RR	ripple rejection		26	–	–	dB
DACA horizontal frequency (pin 8)						
V_8	output voltage					
	at HEX00		–	0.05	0.2	V
	at HEX3F		9.5	10.0	11.0	V
ΔV_8	variable DC output voltage for setting horizontal frequency		0.05	–	10	V
R_8	internal resistance		–	0.3	1.0	kΩ
	step size	note 3	10	–	190	%
RR	ripple rejection		26	–	–	dB
OUT video switch (pin 9)						
FOR EXTERNAL CVBS SWITCH WHEN CVBS BIT = 1						
V_9	saturation voltage	I_{sink} = 1 mA	–	–	0.4	V
I_L	leakage current		–	–	2	µA
I/O combined input/output (pin 10)						
V_{10}	when used as an output (open collector)					
	where PHI1 = '0'		–	–	V_{CC}	V
	where PHI1 = '1'		–	–	0.4	V
I_{sink}	sink current		–	–	2	mA
V_{10}	when used as an input (switching point HCENT is '0' to '1')	PHI1 = '0'	V_{17} – 35 mV	V_{17}	V_{17} + 35 mV	V
I_{10}	input current		–	–	2	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IN HLOCKN and 50/60 Hz (pin 11)						
V_{11}	HLOCKN switching level		–	0.7	–	V
V_{11}	switching level where:					
	LOCKN = '0'		1.0	–	–	V
	LOCKN = '1'		–	–	0.4	V
V_{11}	switching level where:					
	50/60 Hz = '0'		–	–	0.7 V_{CC}	V
	50/60 Hz = '1'	state 50 Hz	0.8 V_{CC}	–	–	V
I_{11}	source current		10	25	35	µA
SDA serial data input (pin 14)						
V_{14}	switching level where:					
	SDA = ‘0’		–	–	1.5	V
	SDA = ‘1’		3.0	–	–	V
I_{14}	sink current		–	0.5	10	µA
SCL serial clock input (pin 15)						
V_{15}	switching level where:					
	SDA = ‘0’		–	–	1.5	V
	SDA = ‘1’		3.0	–	–	V
I_{15}	sink current		–	0.5	10	µA
Internal supply voltage						
V_{16}	maximum allowed load	1 mA load	4.5	5.0	5.5	V
V_{17}	voltage reference for pin 10 (pin 17)		1.0	–	V_{cc} – 1.5	V
I_{17}	input load current		–	–	2.0	µA
E-W drive output (pin 19; see application information)						
V_{19}	output voltage	1 mA load	0.5	–	11.5	V
I_{19}	output current		±1.0	–	±2.0	mA
RR	ripple rejection		24	30	–	dB
R_I	internal resistance		–	1	2	kΩ
t_R	response time		–	2	–	µs
Vertical drive output (pin 20; see application information)						
V_{20}	output voltage	1 mA load	0.5	–	10.5	V
I_{20}	output current		±1.5	±2.0	–	mA
RR	ripple rejection	note 2	35	40	–	dB
	DAC stepsize	note 3	10	–	190	%
Vertical feedback (pin 21; see application information: Register 02 = 20H, 03 = 0, 04 = 0, 05 = 20H, 06 = 0)						
V_{21}	DC input voltage		1.7	1.85	2.05	V
$V_{21(p-p)}$	AC output voltage (peak-to-peak value)	note 2	1.65	1.8	1.95	V
I_{21}	input current		–	–	–3	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical sawtooth voltage (pin 22; see application information)						
V_{22}	top level of sawtooth		6.7	7.1	7.4	V
V_{22}	minimum level of sawtooth	I_{sink} = 0.5 mA	–	–	50	mV
I_{22}	discharge sink current	V_{22} = 3.5 V	6.5	9.5	15	mA
I_{22}	charge source current	V_{23} = 5 V; V_{22} = 3.5 V	1	20	35	µA
I_{22}	control range	5 V to 1 V	80	135	190	µA
$\lvert Z_{22} \rvert$	AC impedance		–	3	–	MΩ
C_{EXT}	external capacitance		–	100	–	nF
Vertical sawtooth stabilizer (pin 23; see application information)						
I_{23}	discharge sink current	V_{22} = 2 V	200	250	300	µA
I_{23}	charge source current	V_{22} = 9.75 V	185	235	285	µA
C_{EXT}	external capacitance		–	390	–	nF
I_L	leakage current	note 5	–	–	0.015	µA
EHT modulation input (pin 24; see application information)						
V_{24}	voltage operating range		1/7 V_{CC}	–	1/2 V_{CC}	V
I_{24}	input current		–	0.5	2.0	µA

Notes to the characteristics

1. Outside the test mode.
2. Test condition (hex values): register 02 = 3F; 03 = 00; 04 = 00; 05 = 20; 06 = 00; V_{22} = 1/2 V_4; f = 50 Hz to 30 kHz.
3. $\frac{\text{Value StepN} - \text{Value StepN} - 1}{\text{average step size}} \times 100\% \; (63>N>1)$.
4. Applies to both modes.
5. External load of this pin (leakage current capacitor etc.) should be ≥ 500 MΩ.

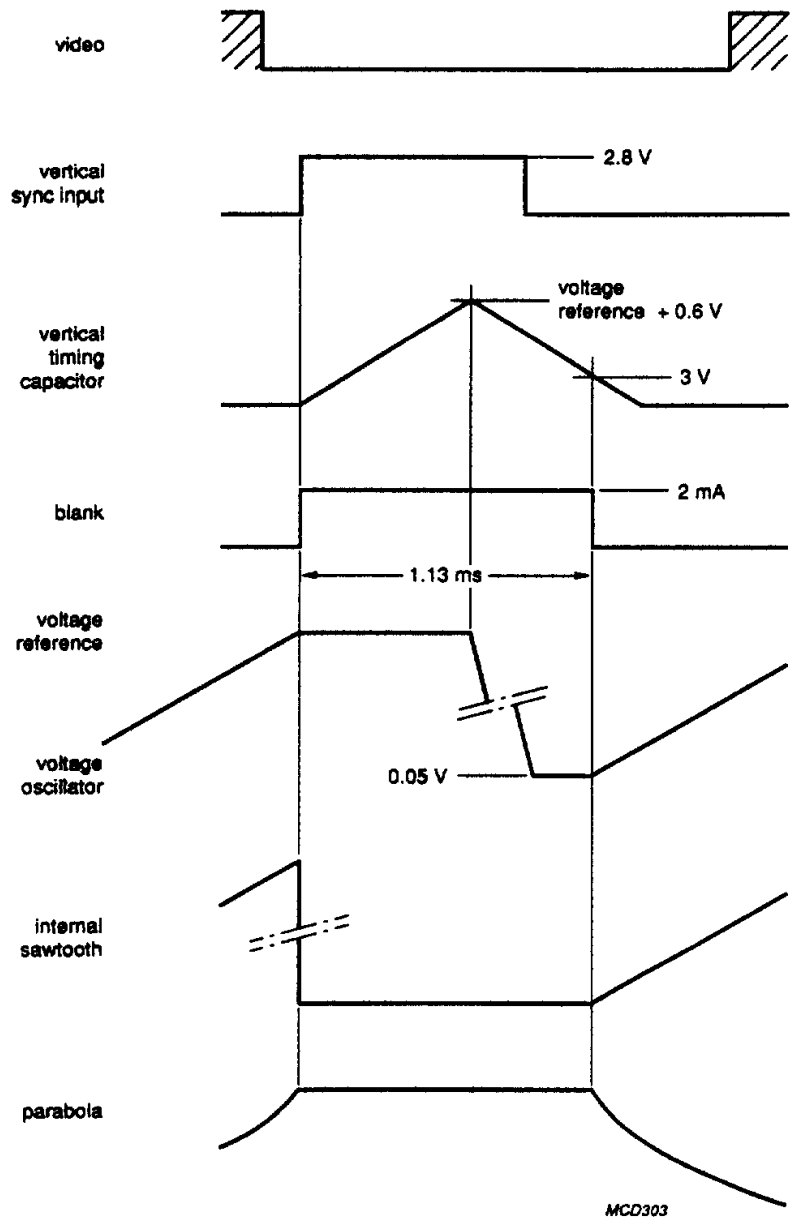


Fig.3 Vertical sawtooth timing.

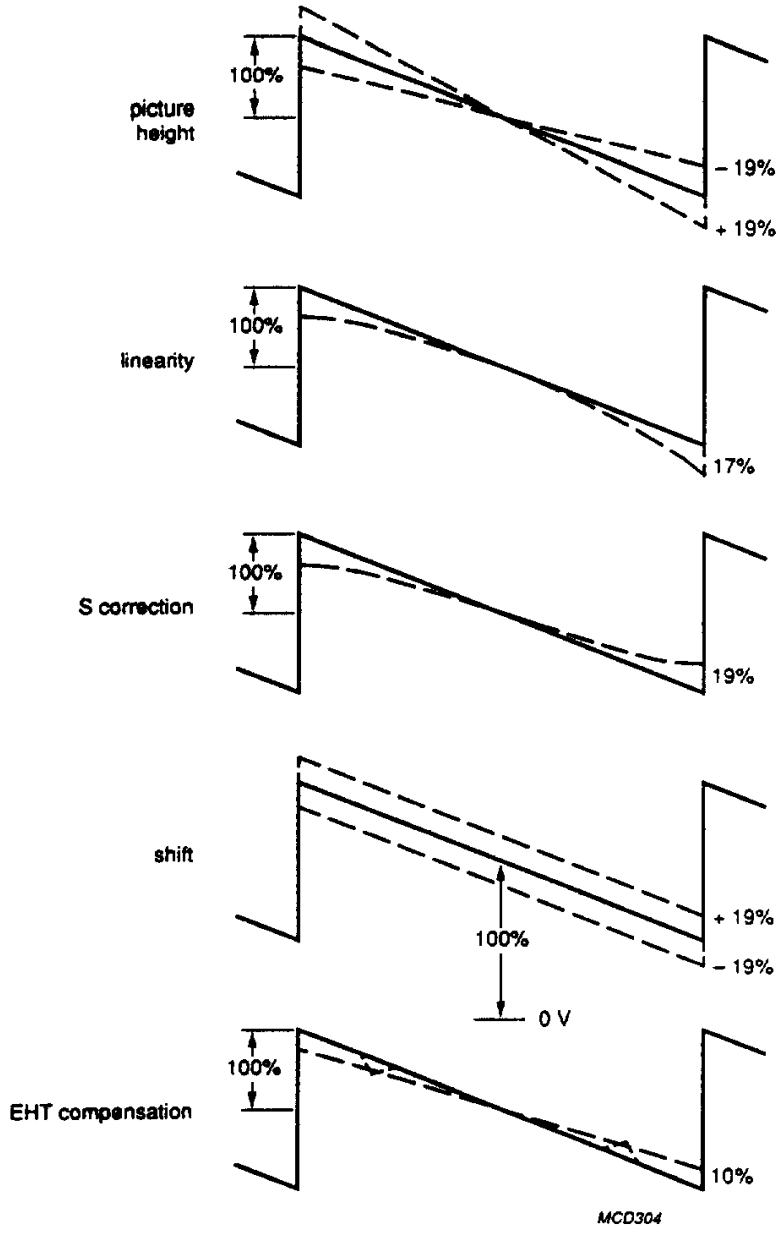


Fig.4 Vertical raster-corrections.

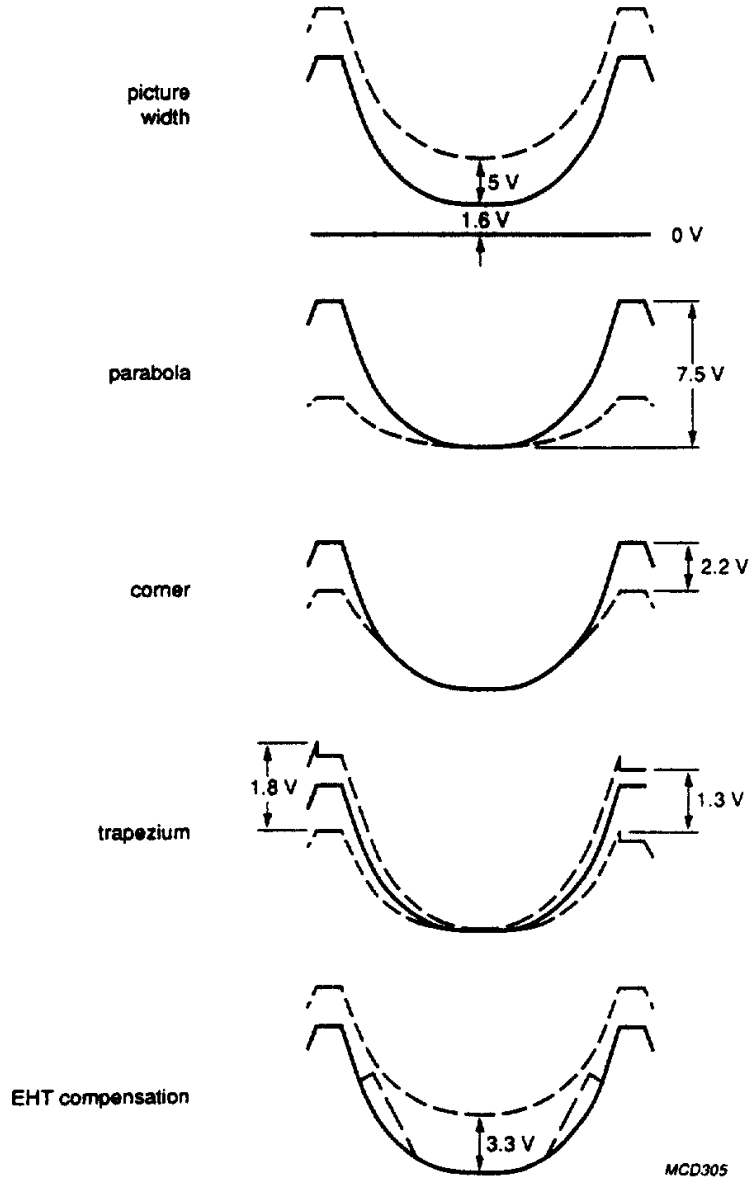


Fig.5 East-west raster-corrections.

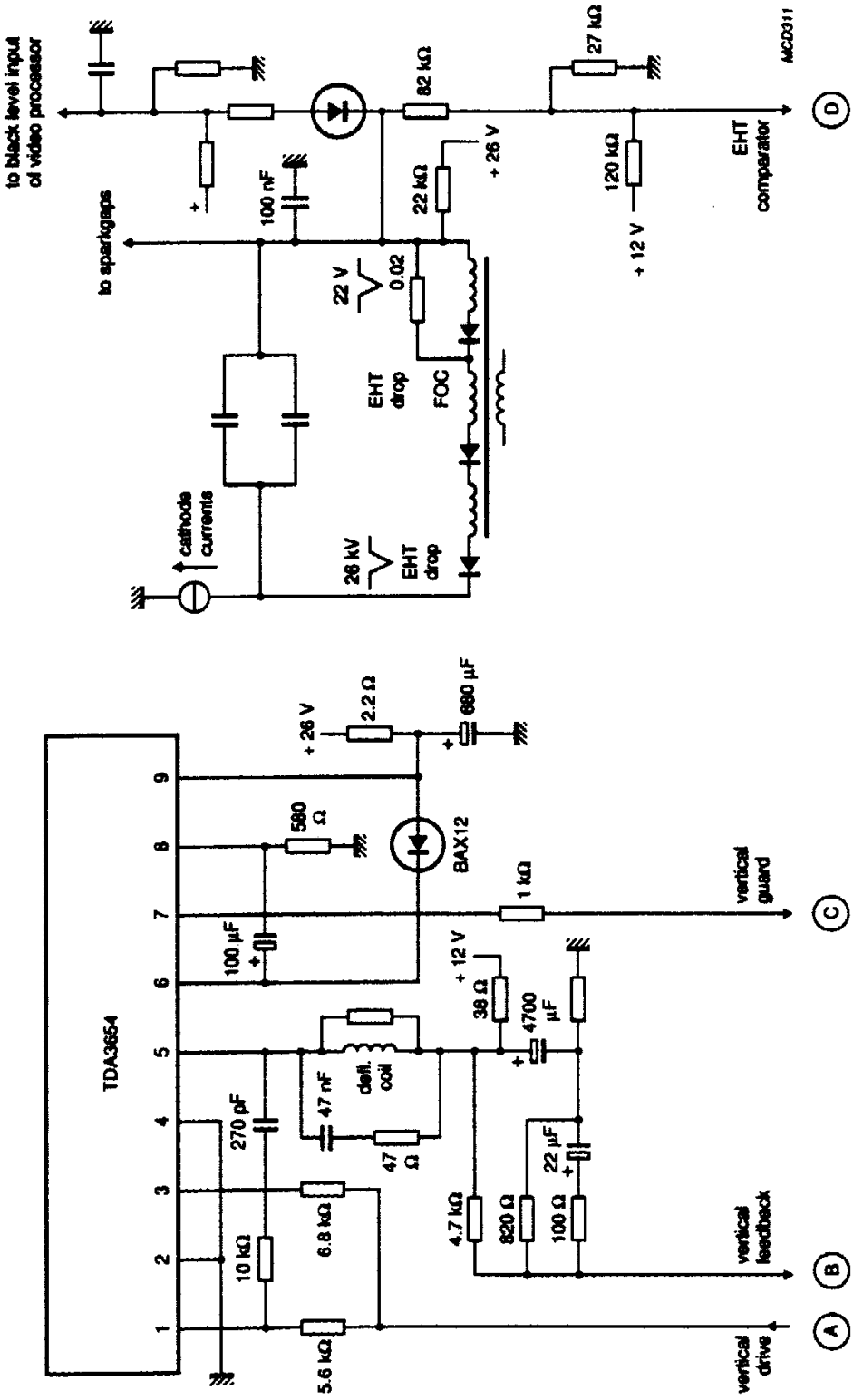


Fig.6 Application diagram (continued in Fig.7).

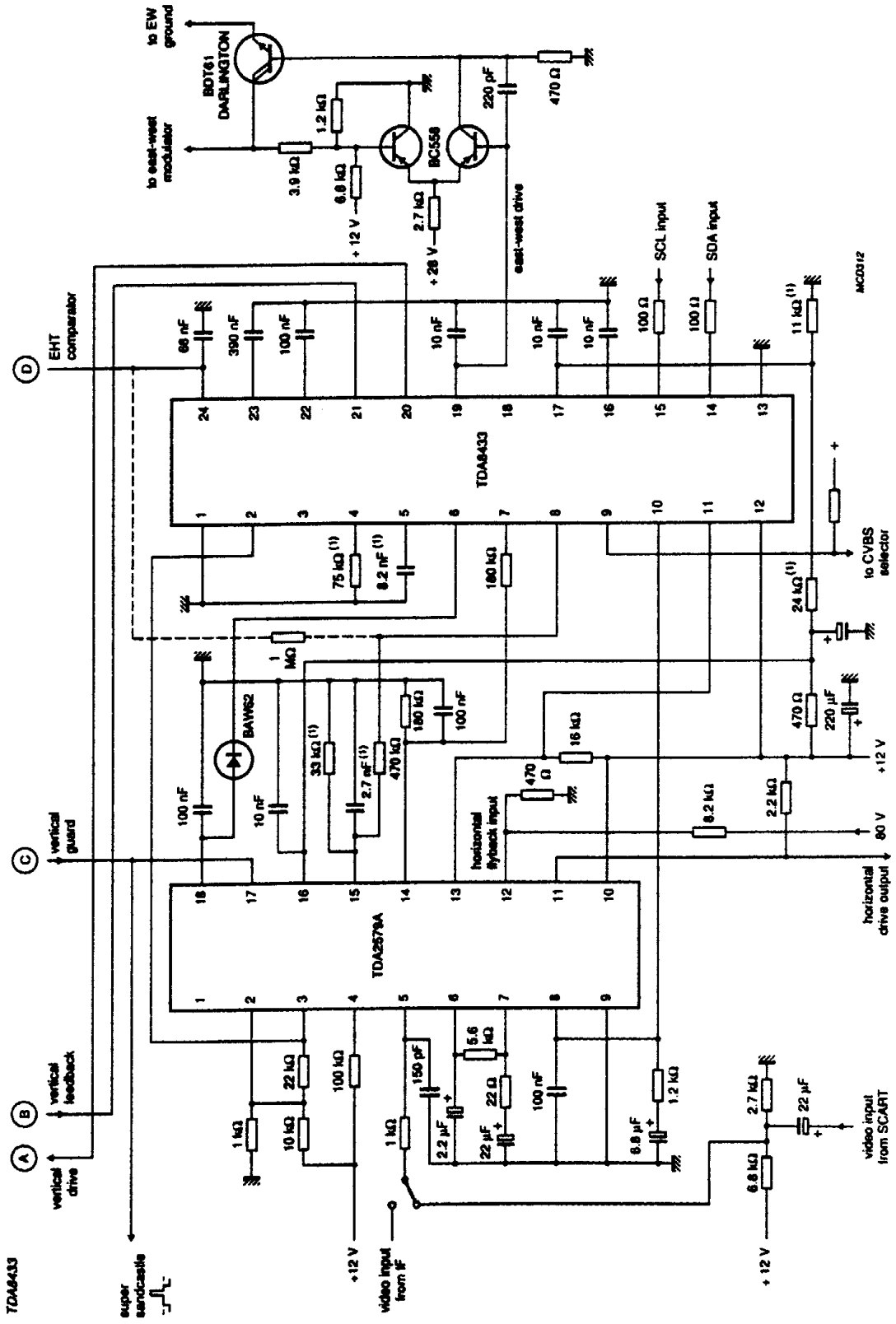


Fig.7 Application diagram (continued from Fig.6).

APPLICATION INFORMATION

The formulae from which the typical vertical drive and typical E-W drive waveforms are generated are given in the following sub-paragraphs. For this purpose a typical application diagram for the vertical drive stage is assumed to be as illustrated in Fig.7. Pin 20 is the vertical drive output which drives an inverting power amplifier. The feedback network, R1 to R4 and C1 and C2, has two functions;

- To transfer the voltage on the feedback pin (pin 21) to a voltage across the feedback resistor R1
- To stabilize the voltage across C1 at a fixed value.

For this typical application the formula for the vertical scan waveform refers to the voltage at pin 21. The formula for the E-W drive waveform refers to the voltage at pin 19.

All DAC variables that control the vertical and E-W drive waveforms are normalized. Each DAC is defined as having a control range between 0 and 1. The 0 corresponds to a register value of HEX00 and the 1 to a maximum value of HEX1F (for a 5-bit DAC) or HEX3F (for a 6-bit DAC).

Table 4 DAC variables

a: Picture height	$0 < a < 1$	64 steps (6 bits)
y: V-linearity	$0 < y < 1$	64 steps (6 bits)
s: V-S correction	$0 < s < 1$	64 steps (6 bits)
d: V-shift	$0 < d < 1$	64 steps (6 bits)
v: V-compensation	$0 < v < 1$	32 steps (5 bits)
w: Picture width	$0 < w < 1$	64 steps (6 bits)
p: E-W parabola	$0 < p < 1$	64 steps (6 bits)
c: E-W corner	$0 < c < 1$	64 steps (6 bits)
t: Trapezium	$0 < t < 1$	64 steps (6 bits)
h: H-compensation	$0 < h < 1$	32 steps (5 bits)

Further definitions

V_{SAW} = Instantaneous sawtooth voltage (pin 22) normally; $0 < V_{saw} < 7.1$ V;
V_{CC} = supply voltage applied to pin 12.

V_{EHT} = EHT compensation voltage applied to pin 1, normally between 1/2 V_{CC} and 1/7 V_{CC}.

V_{OFF} = Internal offset voltage.

V_{int} = Internal reference voltage of 7.1 V (also on pin 4)

$A = 0.80\ (a + 2)/3$	$P = 0.55\ p$
$Y = 0.17\ y$	$C = 0.38\ c$
$S = 0.42\ s$	$T = 0.32\ (1 + 2t)$ volts
$D = 2.4 - 0.7\ d$ volts	$E = (V_{CC} / 2 - V_{EHT}) / 42$
$W = 0.16\ w$	$Z = -1 + 2 \times (V_{saw} - T)\ V_{int}$

If the Trapezium function (T) compensates for the internal offset voltage then the actual formula for Z will simplify to:

$Z = -1 + 2V_{saw}/V_{int}$

Since $0\ V < V_{SAW} < 7.1$ V, this is simply a negative going sawtooth and it follows that: $-1 < Z < 1$.

Vertical drive waveform

The vertical drive waveform has certain interactions between the parameters whereby:

- The S-correction influences the picture height
- The linearity correction can influence the picture shift.

The alignment can be made non-repetitive. Once correct values for the V-S correction and V-linearity are set, the picture height may be changed without affecting the V-S correction and V-linearity on the screen.

The formula for the vertical drive waveform at pin 21 is:

$V_{vert} = D + 1.32\ A\ \{(Z - SA^2\ Z^3)\ (1 - VE) + YZ^2\}$ volts.

Picture height

The amplitude of the sawtooth waveform is controlled by 'A'. It follows therefore that:

$0.53 < A < 0.8$

The nominal value for 'A' is found for a = 0.5, therefore A = 0.67. By programming the picture height, the sawtooth amplitude can be adjusted from −19% to +19%. Without S-correction (S = O) and linearity correction (Y = O), the nominal sawtooth amplitude is (with A = 0.67);

$1.32 \times 0.67 \times 2 = 1.77\ V_{(p\text{-}p)}$

V-linearity

This function is meant to compensate for non-linearity of AC coupled vertical output stages. The linearity correction changes proportionally to the picture height setting. The range for linearity control is typically 17% of the peak-to-peak value of the linear sawtooth (see Fig.7).

V-S correction

The range for the V-S correction (SA^2) is defined as a percentage of the undistorted peak-to-peak sawtooth voltage (see Fig.7). The actual S-correction component (SA^2) is dependent on the picture height setting where:

At maximum picture height (A = 0.80) : $SA^2 = 0.282$
At nominal picture height (A = 0.62) : $SA^2 = 0.197$
At minimum picture height (A = 0.53) : $SA^2 = 0.125$

Picture shift

The DC level of the output is fixed by 'D'. It can be adjusted within a range of −19% to +19%. In actual application this will be used for shifting the picture vertically.

V-compensation

The vertical deflection can be modulated by the instantaneous value of the signal applied to the EHT compensation input. This external signal should reflect the EHT variations. The amount of deflection reduction is in the range 0 to 10%, if pin 24 is at (V_{CC} / 2) − 4.3 V (maximum modulation i.e. 1.7 V typical). Thus for maximum modulation, the V-drive waveform can be reduced to 90% of its value. There is no reduction when the EHT-compensation input is at V_{CC} / 2 V (i.e. 6 V typical).

Trapezium

The trapezium function is the only IC-confined adjustment and is intended to compensate for any internal offsets. The function is called Trapezium because of its effect on the picture if an AC-coupled vertical deflection stage is used. The trapezium function can alter the picture shift range by a maximum of 190 mV. If the trapezium function is used for purposes other than eliminating the internal offsets, then the V-linearity can affect the actual picture height. This can affect the symmetry of the S-correction which, in turn, can affect the V-linearity.

E-W drive waveform

In order to obtain independent control of the picture width, parabola function and the H-compensation on a screen each function has been designed to be dependent on the other two. With reference to Fig.8, the voltage across the H-deflection stage is:

$V_{def1} = V_{supply}\ (1 - W)\ (1 - P)\ (1 - E)$

Where:

V_{supply}	= supply voltage for H-deflection stage
W	= picture width alignment
P	= parabola function
E	= H-compensation

This shows for instance, that the H-compensation is made dependent on the actual value of the parabola function. For a TV set which needs a large parabola compensation and, also, a large EHT-compensation, this function allows an optimal EHT-compensation independent of the parabola function.

All correction voltages are related to the supply voltage. The TDA8433 is designed to accept a supply voltage of 30 V. Normally higher voltages are employed therefore a voltage amplifier, with a gain of $V_{supply}/30$, is used between the TDA8433 and the diode modulator.

The formula for the E-W drive output voltage at pin 19 is:

$V_{E-W} = 30 \times \{1 - (1 - W)(1 - PA^2 Z^2 + CA^4 Z^4)(1 - 1.1 \times hE)\} + 1.8$ V

As can be seen from the formula, the picture width, parabola function and H-compensation are influenced by each other. The functions are discussed separately with the other compensations set to zero.

Picture width control (P-C-h-O)

It is possible to change the picture width by adjusting 'W' from 0 to 0.16. Thus the complete range for the picture control width is –10 to +10%. By only changing the picture width control the output voltage at pin 19 can vary between 1.8 and 6.6 V typical.

Parabola function

The parabola function is also dependent on the picture height function. The values given are valid for a nominal height setting (A = 0.67 V). The parabola function consists of two parts:

- A parabola part - E-W parabola is created by squaring a linear sawtooth. The range of this pure parabola varies from 0 to 25% typical i.e. the amplitude of the parabola waveform is programmable from 0 to 7.5 V (typical).
- A fourth order part - E-W corner is created by squaring the parabola. The range of this corner correction varies from 0 to 7% (typical) i.e. the amplitude of the corner correction waveform is programmable from 0 to –2.2 V (typical). A negative output voltage is not possible. The E-W corner correction waveform has to be subtracted from one of the other alignment functions.

The split-up into the E-W parabola and the E-W corner enables each television set to be aligned with straight vertical lines. The trapezium is also related to the parabola function. The main reason for the trapezium correction is to compensate for internal offsets in the geometry control part. Therefore:

- The amount of trapezium correction is fully dependent on the amount of parabola correction and corner correction that is needed. With no parabola and corner correction the trapezium output will be zero.
- The maximum possible trapezium output is 1.6 V (typical - see Fig.7). This is the case where: a = 0.5, c = 0 and p = 1 i.e. no corner correction and the maximum parabola correction at nominal picture height settings.

H-compensation control

The horizontal deflection can be modulated by the instantaneous value of the signal applied to the EHT compensation input. This external signal should reflect the EHT variations. The amount of deflection reduction is in the range 0 to 10% if the input at pin 7 is at $(V_{supply}/2)$ –4.3 V (maximum modulation is 1.7 V typical). With maximum modulation this range corresponds to an output voltage of 0 to 3.3 V. There is no reduction when the EHT-compensation input is at $V_{supply}/2$ V (typical 6 V).

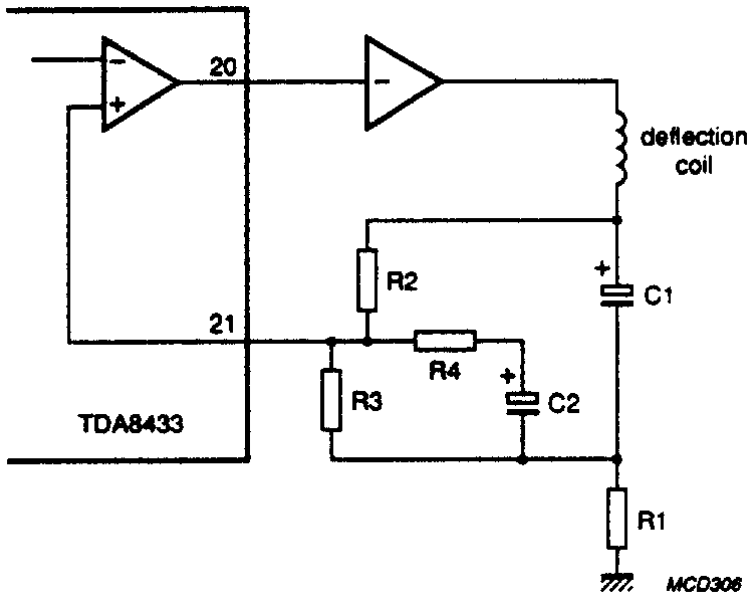


Fig.8 Application diagram of an AC coupled amplifier stage.

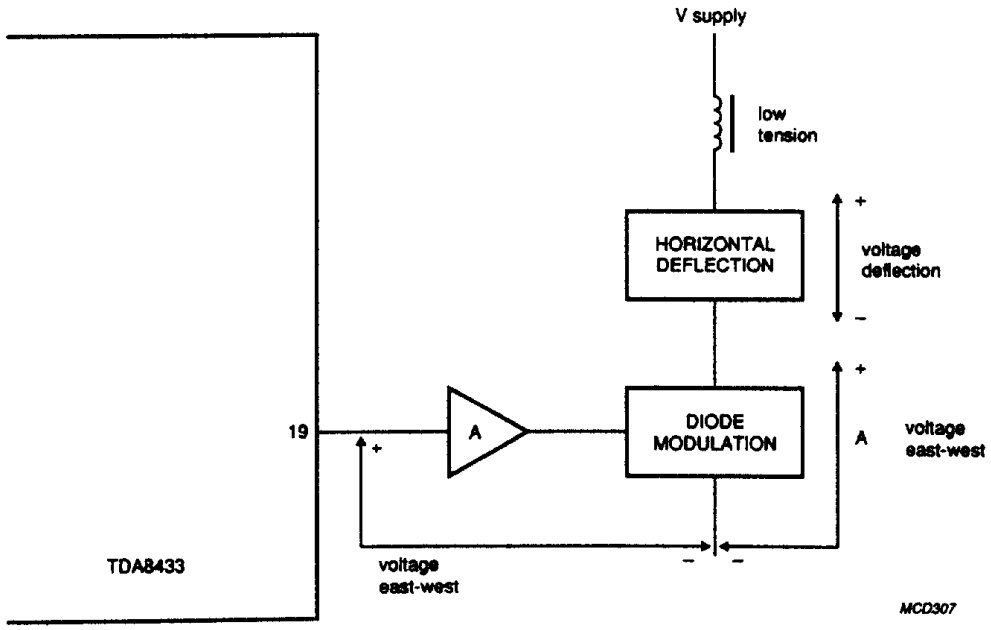


Fig.9 Application diagram for driving the diode modulator.

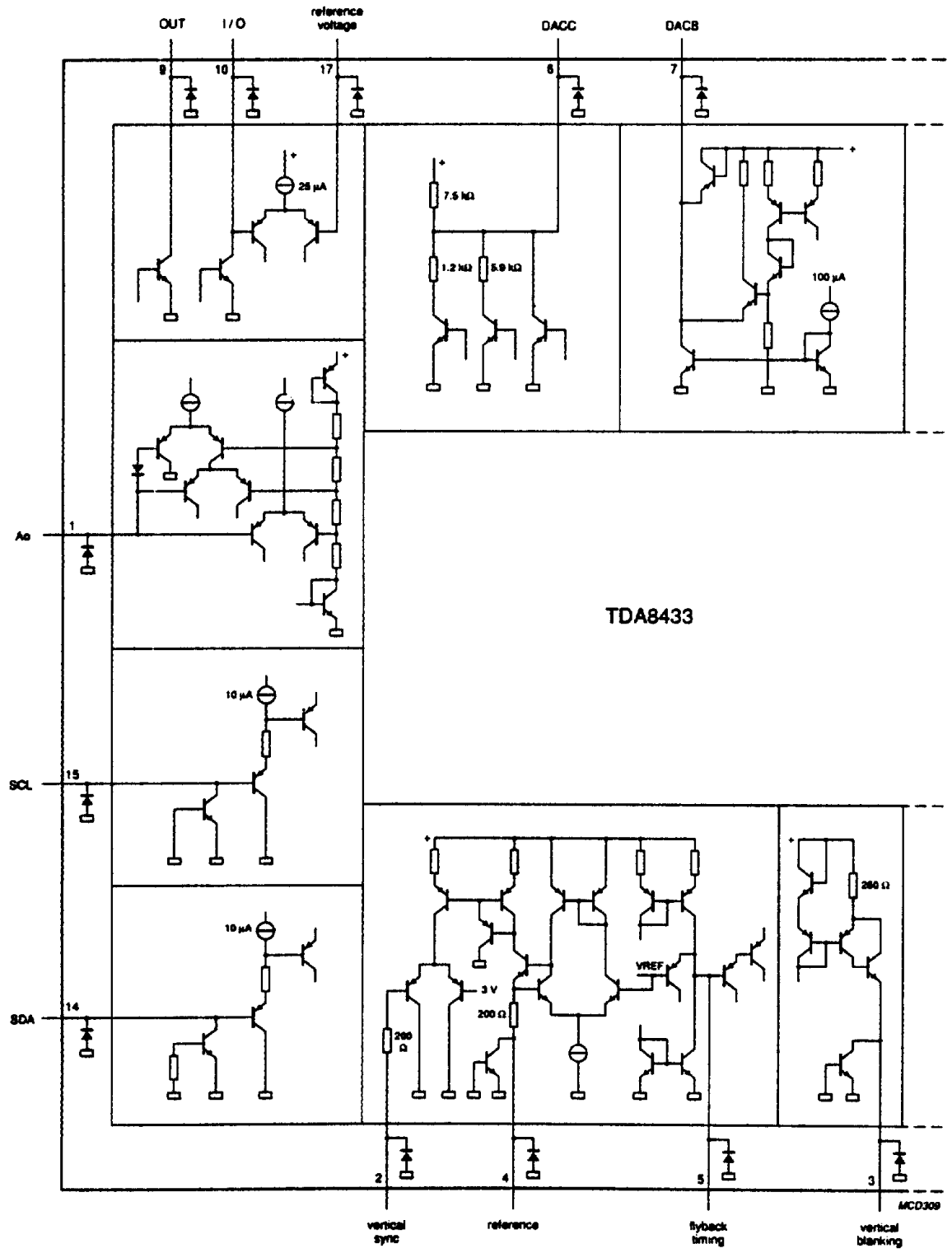


Fig.10 Input/output pin-configuration of TDA8433 (continued in Fig.11).

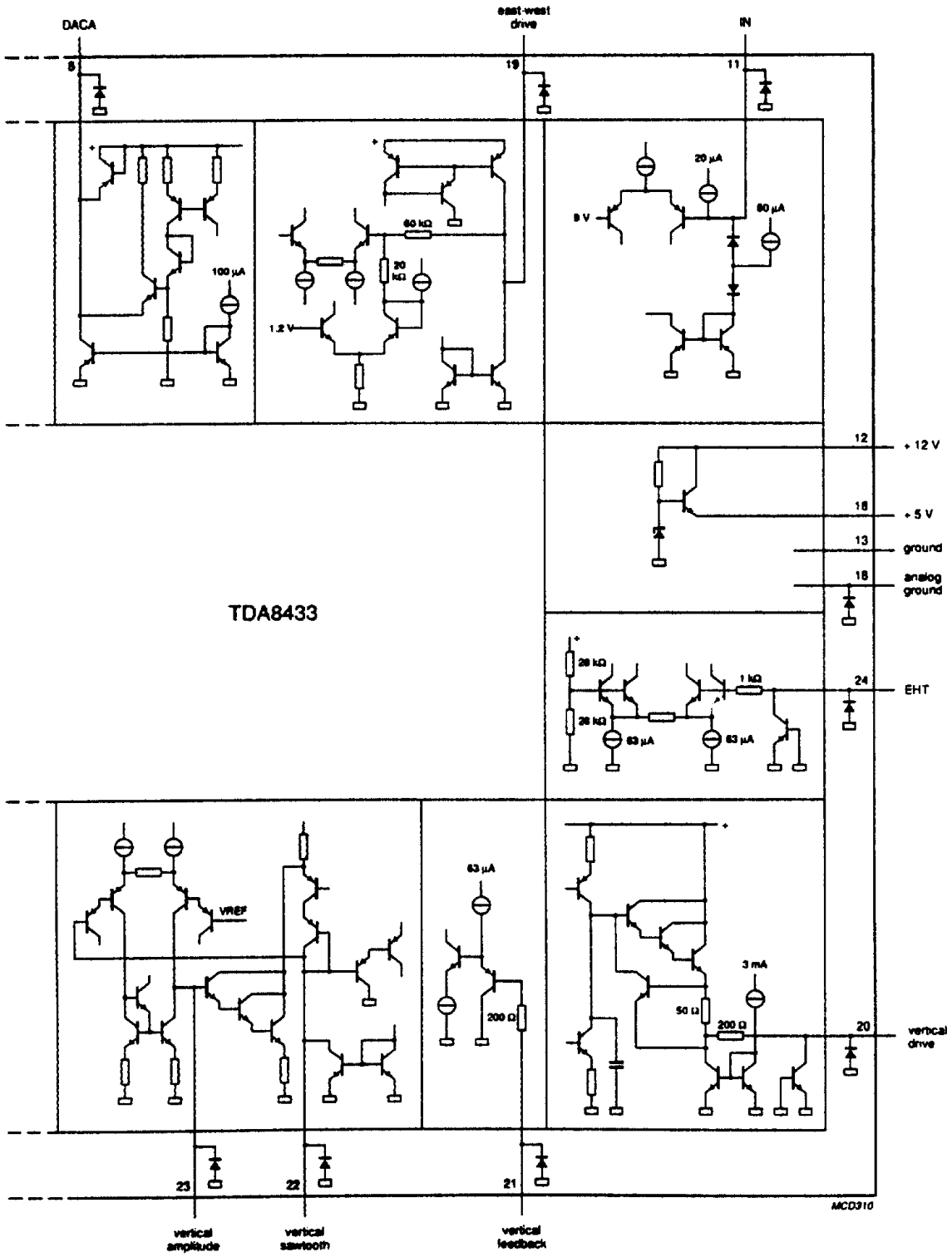
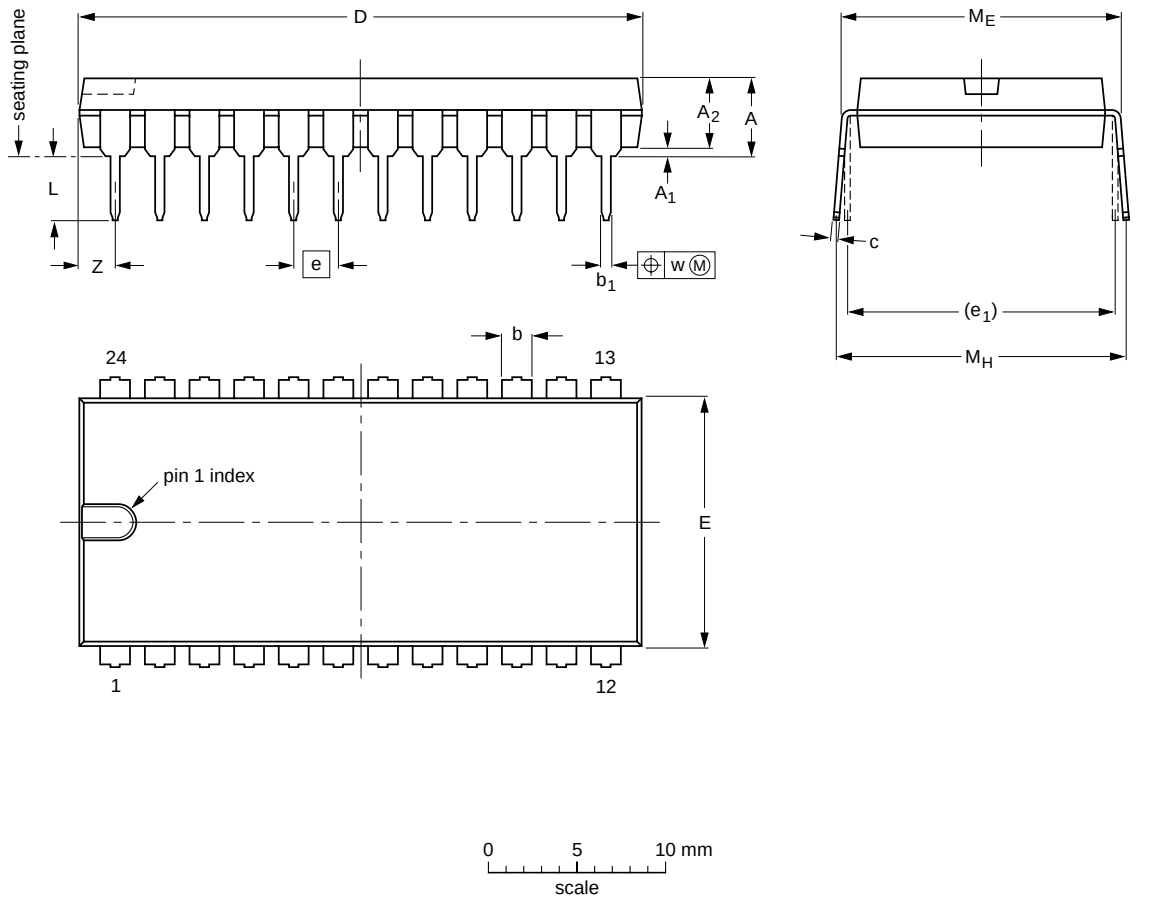


Fig.11 Input/output pin-configuration of TDA8433 (continued from Fig.10).

PACKAGE OUTLINE

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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